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United States Patent [19]

Choi

[11] **Patent Number: Des. 420,983**

[45] **Date of Patent: ** Feb. 22, 2000**

[54] **SEMICONDUCTOR POWER PACKAGE WITH THREE LEADS**

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[73] Assignee: **IXYS Corporation**, Santa Clara, Calif.

[**] Term: **14 Years**

[21] Appl. No.: **29/095,110**

[22] Filed: **Oct. 16, 1998**

[51] **LOC (7) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182, 199; 257/690, 692, 693, 694, 697; 315/291; 361/744

[56] **References Cited**

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[57] **CLAIM**

The ornamental design for a semiconductor power package with three leads, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a semiconductor power package with three leads showing my new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a right side elevational view thereof, the left side elevational view being a mirror image;
FIG. **4** is a bottom plan view thereof;
FIG. **5** is a rear elevational view thereof; and,
FIG. **6** is a front elevational view thereof.

1 Claim, 2 Drawing Sheets

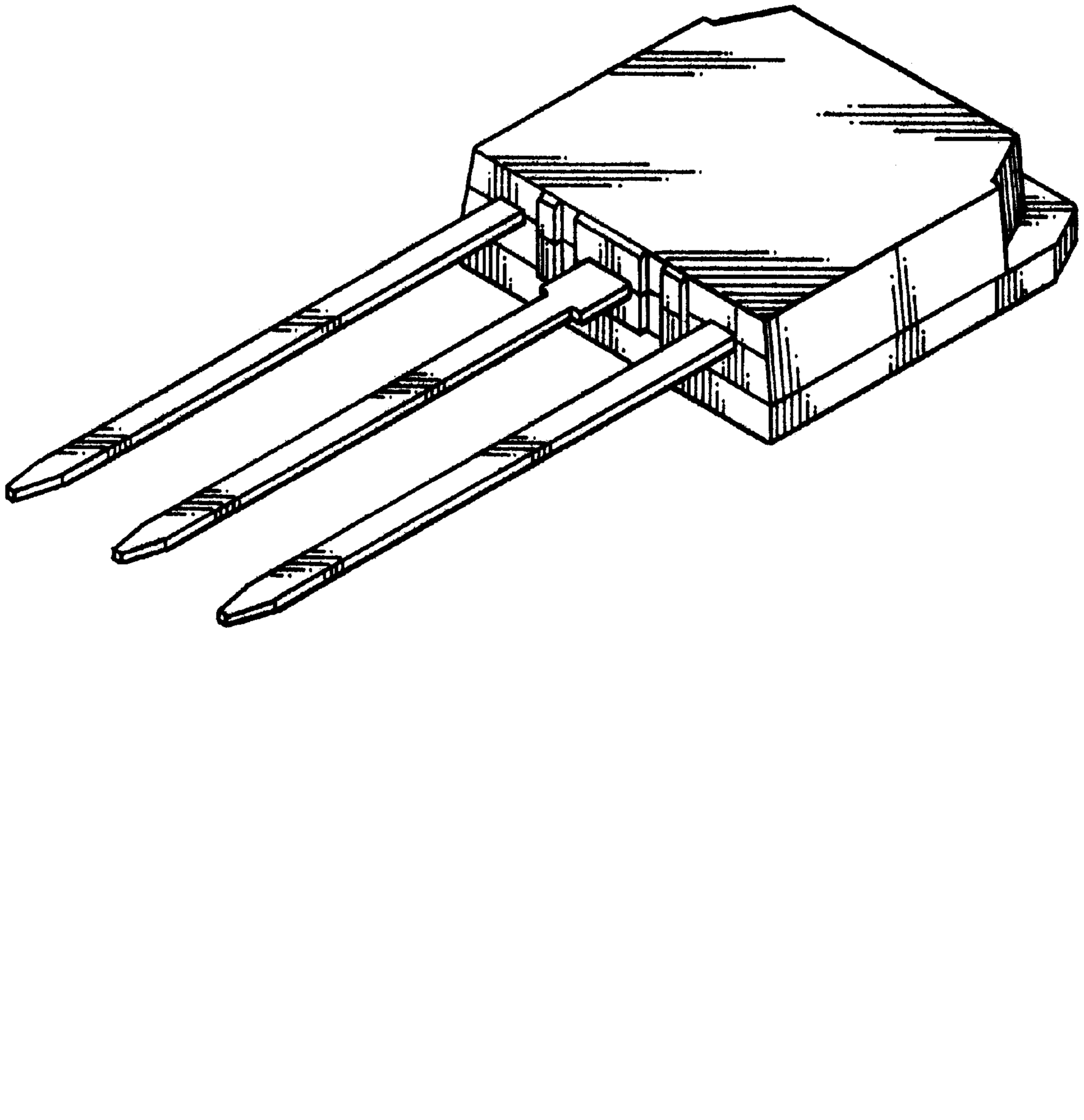

Fig. 1

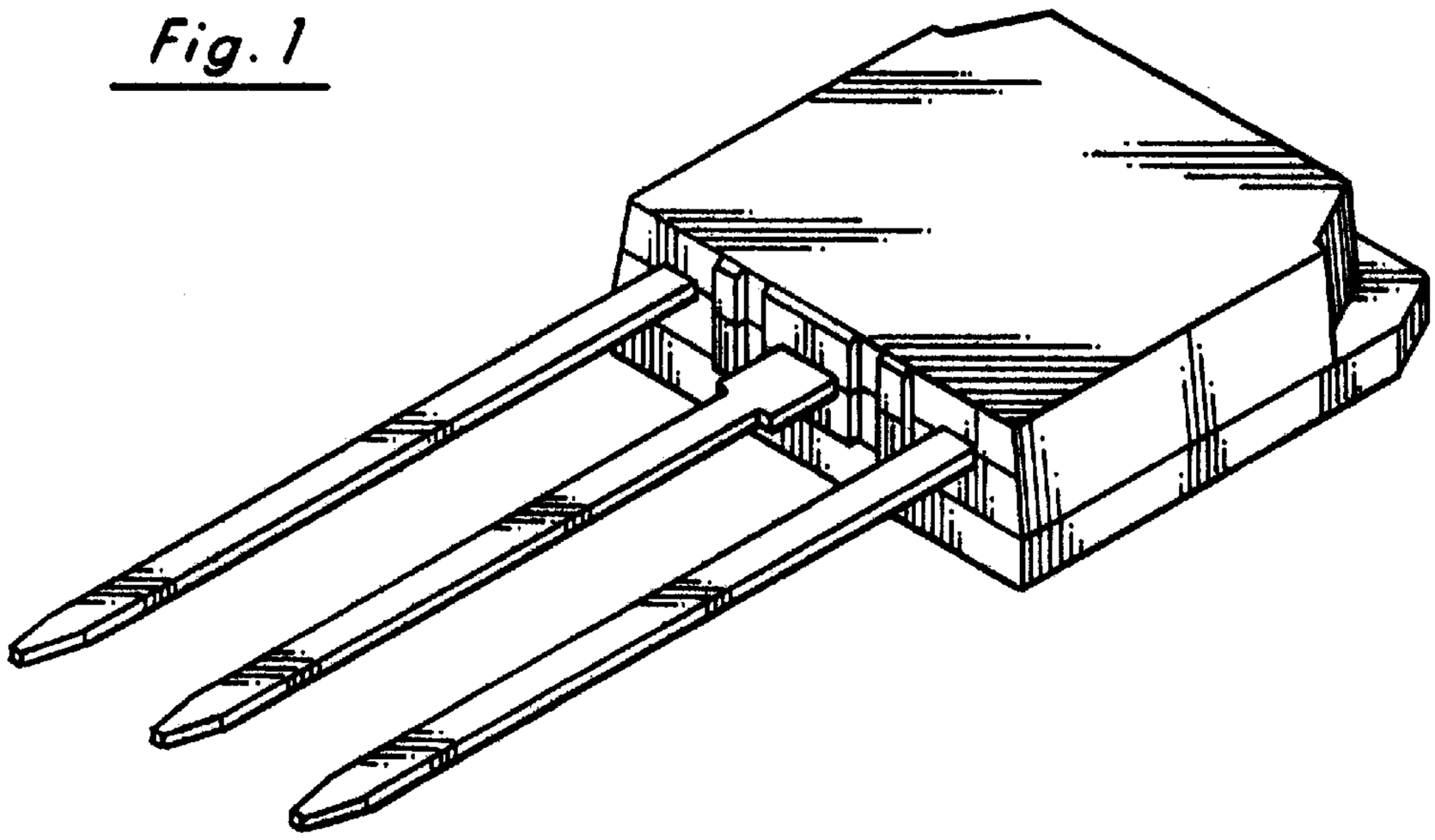

Fig. 3

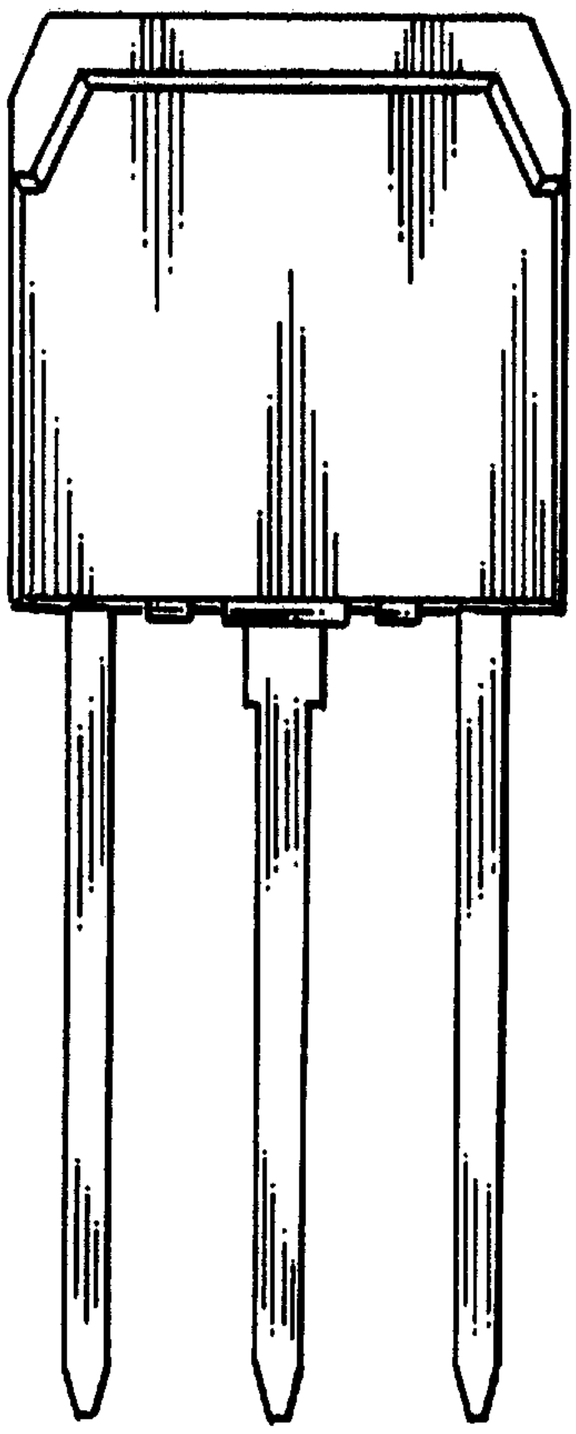

Fig. 2

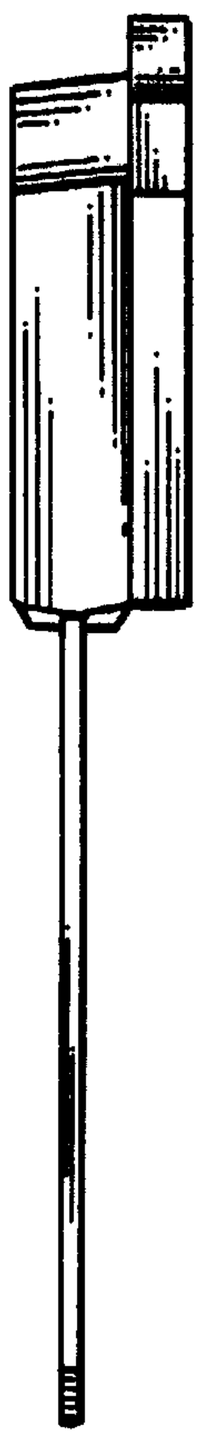

Fig. 5

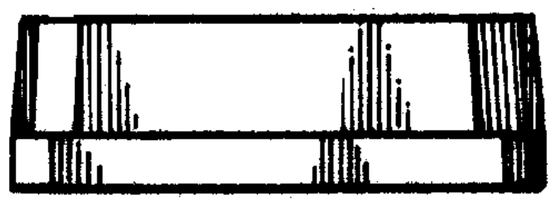

Fig. 4

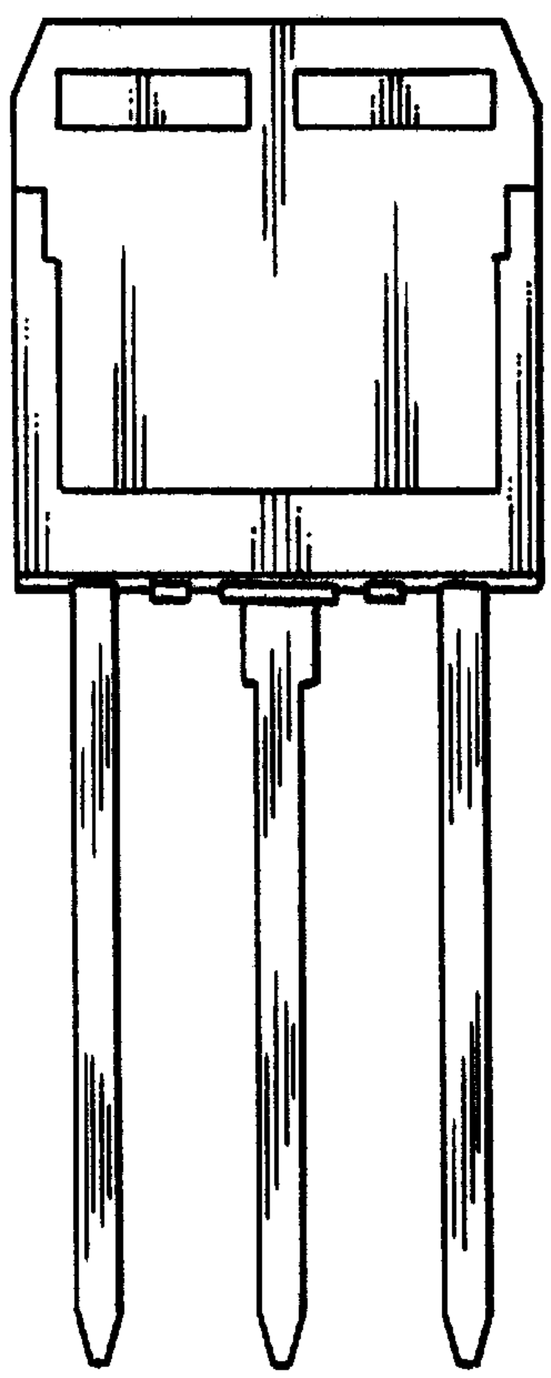

Fig. 6