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**United States Patent** [19]  
**Klinker**

[11] **Patent Number: Des. 413,316**

[45] **Date of Patent: \*\* \*Aug. 31, 1999**

[54] **PROCESSOR PACKAGE COVER PLATE  
FOR AN INTEGRATED CIRCUIT  
PROCESSOR PACKAGE CHIPSET**

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[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[\*] Notice: This patent is subject to a terminal dis-  
claimer.

[\*\*] Term: **14 Years**

[21] Appl. No.: **29/081,116**

[22] Filed: **Dec. 22, 1997**

[51] **LOC (6) Cl.** ..... **14-02**

[52] **U.S. Cl.** ..... **D14/114**

[58] **Field of Search** ..... D14/114, 121;  
D13/156; D8/353; D21/324-33; 242/348,  
348.4, 341, 343, 344-45, 345.1, 346, 343.3,  
346.2; 273/148 R, 148 B

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Zafman

[57] **CLAIM**

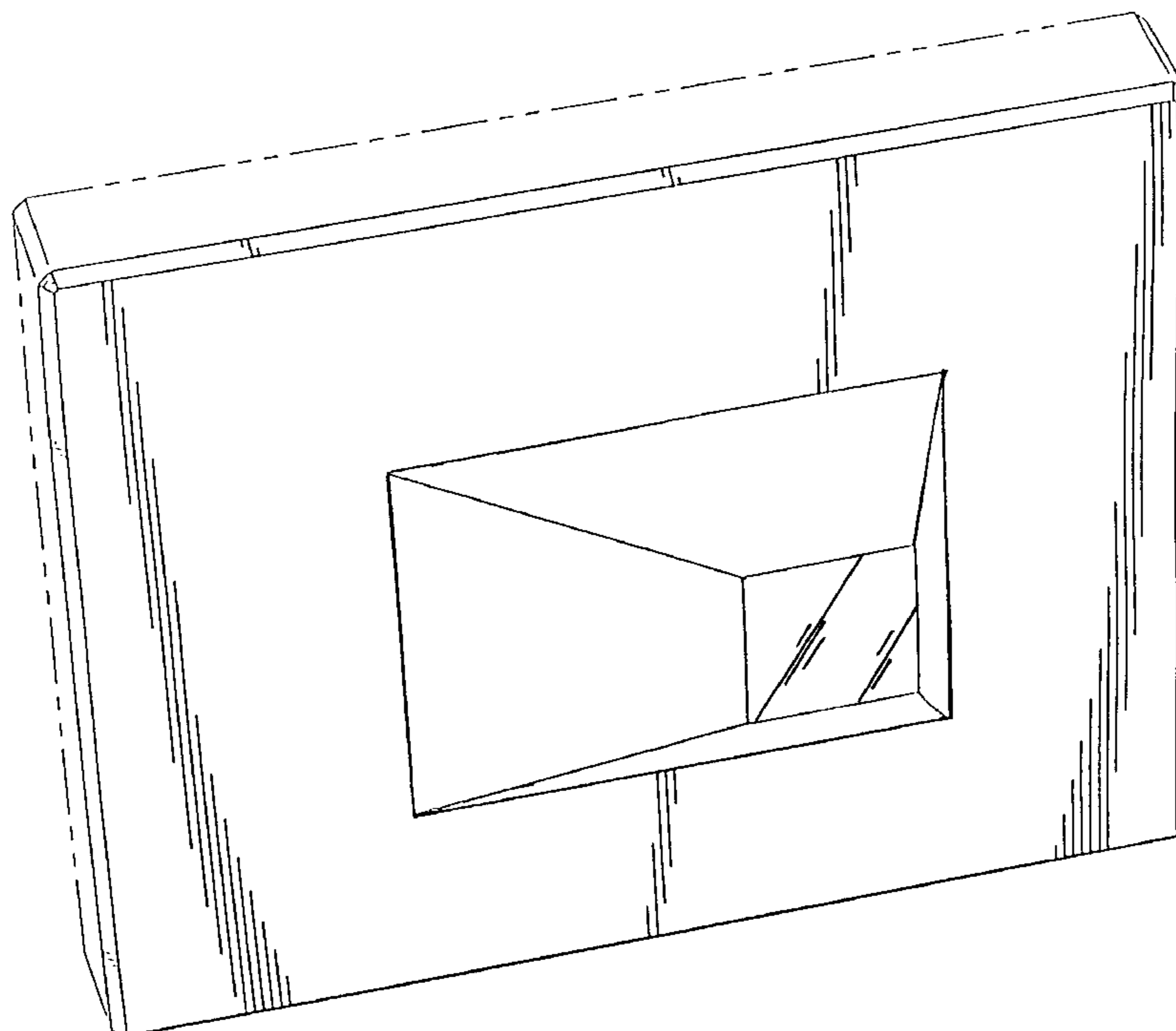
The ornamental design for a processor package cover plate for an integrated circuit processor package chipset, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view of a processor package cover plate for an integrated circuit processor package chipset; FIG. 2 is a front view thereof; FIG. 3 is a top view thereof; FIG. 4 is a back view thereof; FIG. 5 is a right side view thereof; FIG. 6 is a left side view thereof; FIG. 7 is a bottom view thereof; and, FIG. 8 is a cross-sectional view thereof, taken on line 8—8 of FIG. 2.

The broken line drawing in FIGS. 1, 3, and 5-8 of the processor package is for illustrative purposes only and forms no part of the claimed design.

**1 Claim, 4 Drawing Sheets**



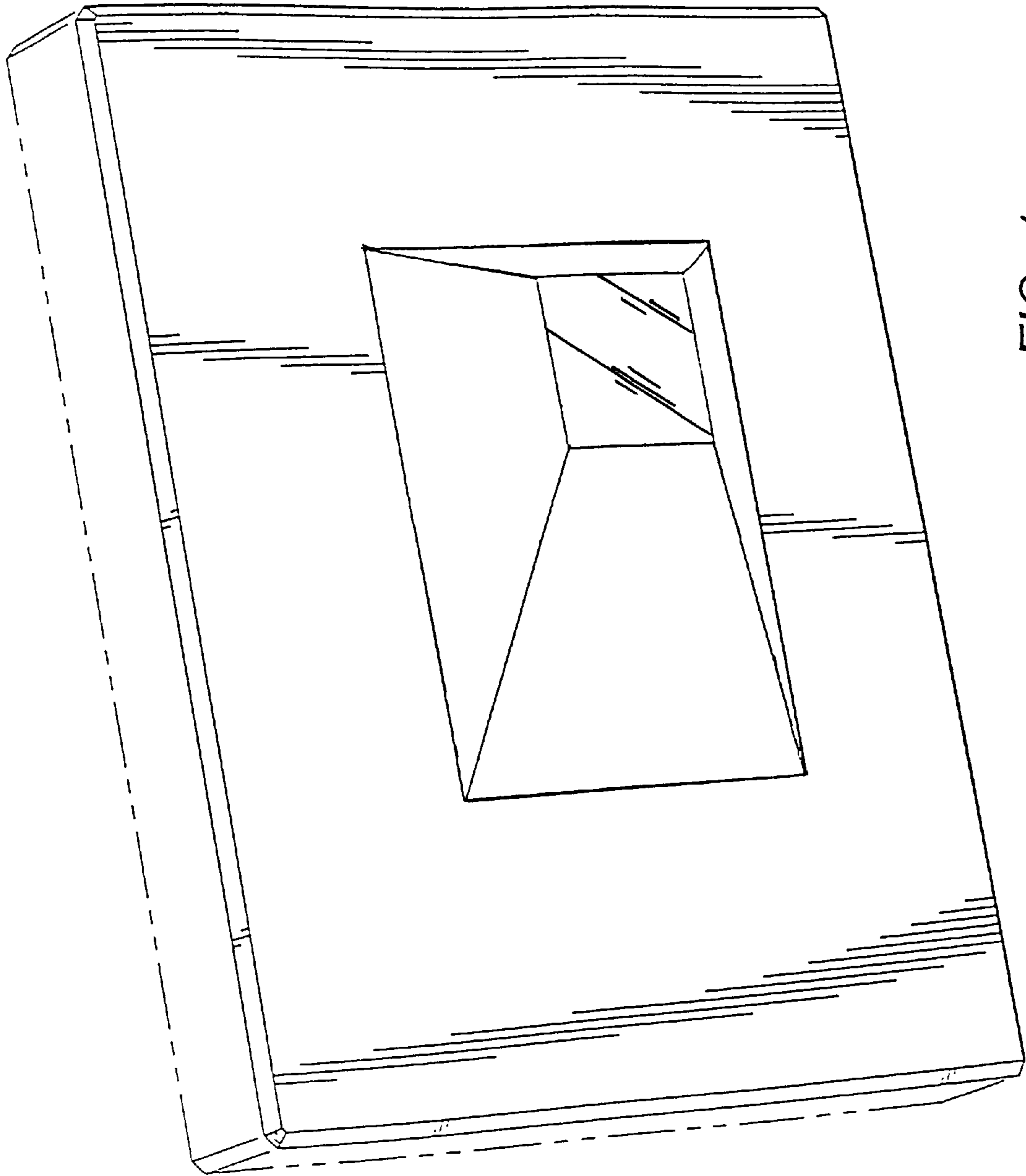


FIG. 1

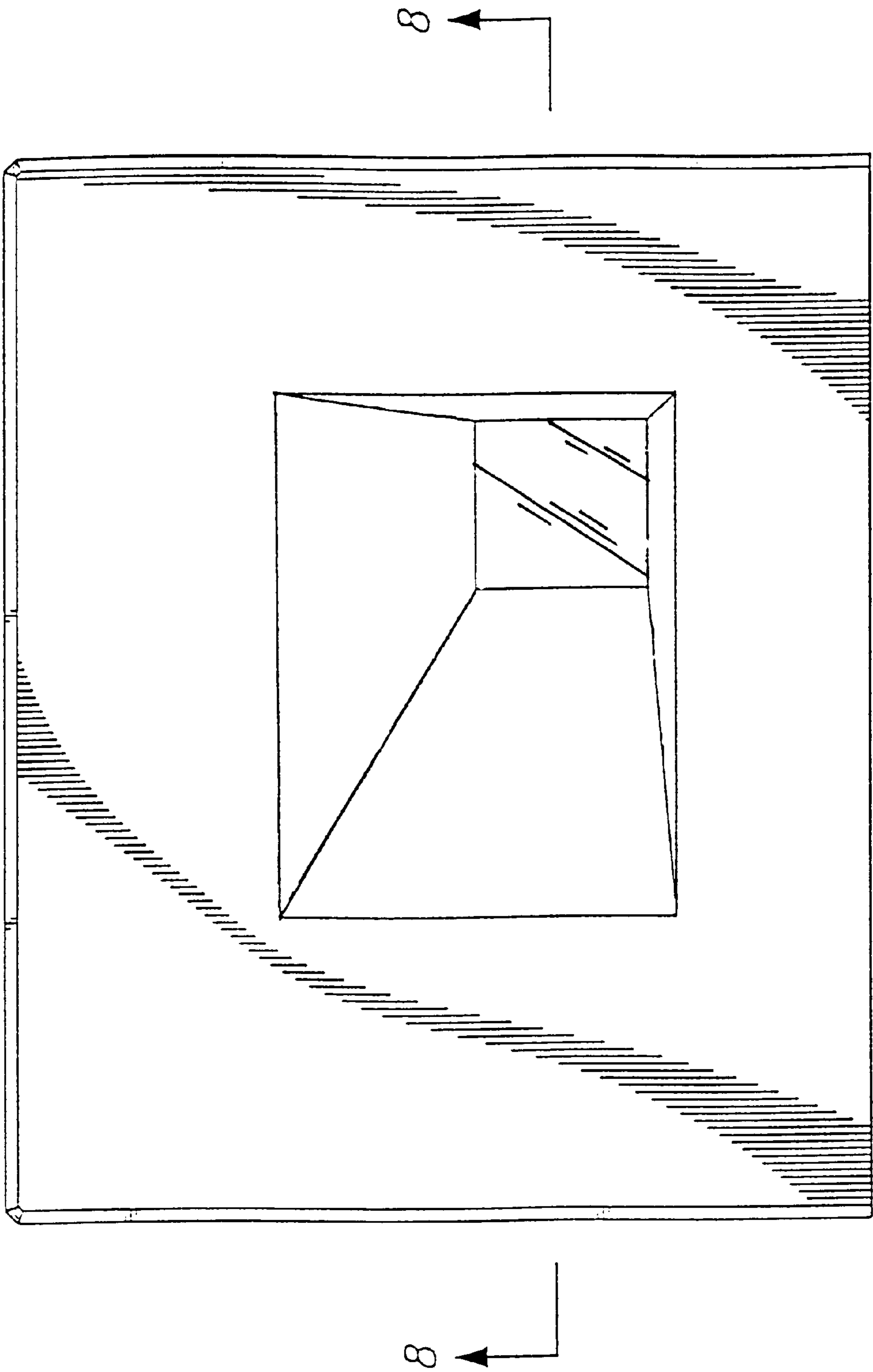


FIG. 2

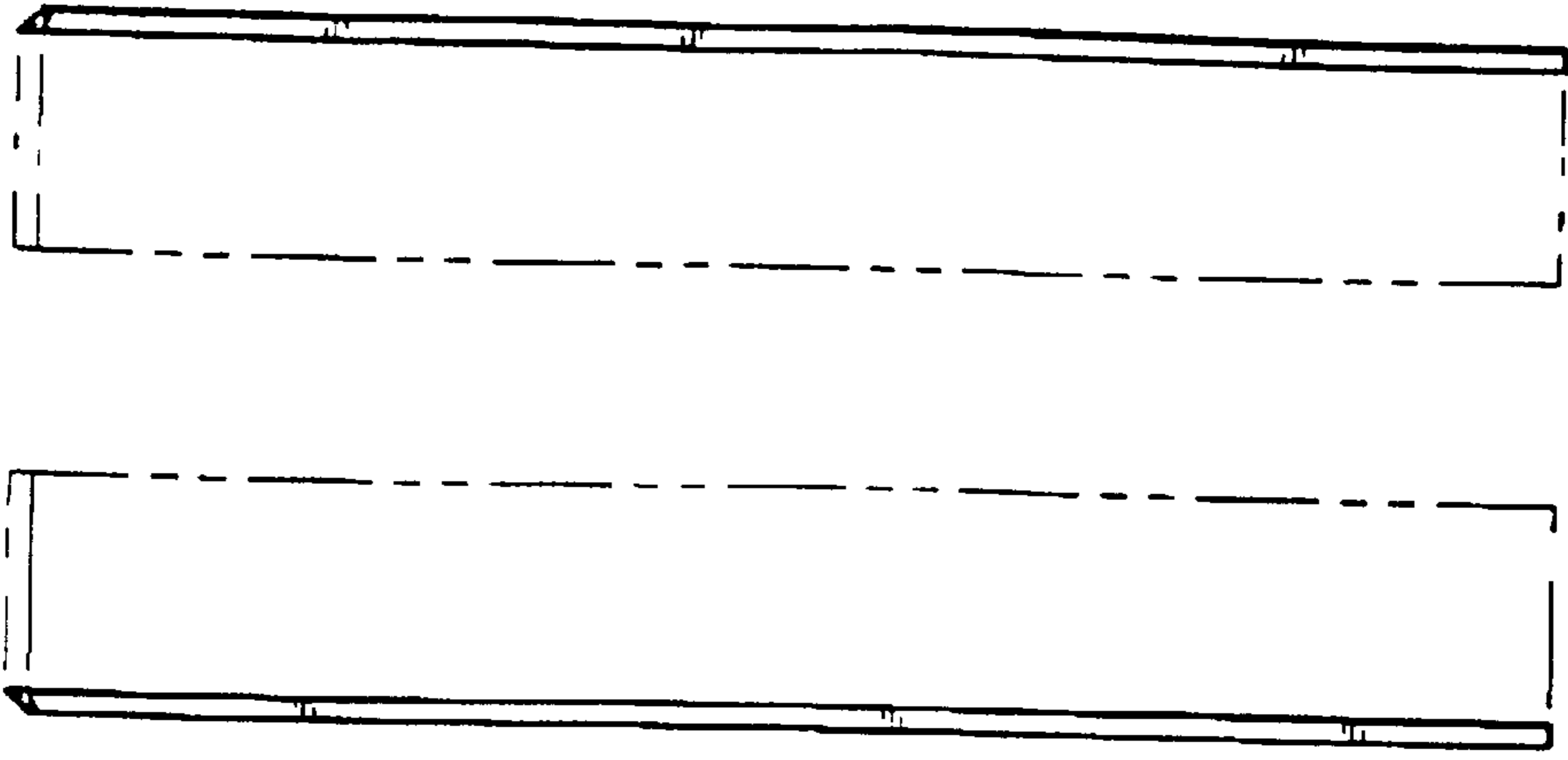


FIG. 5 FIG. 6

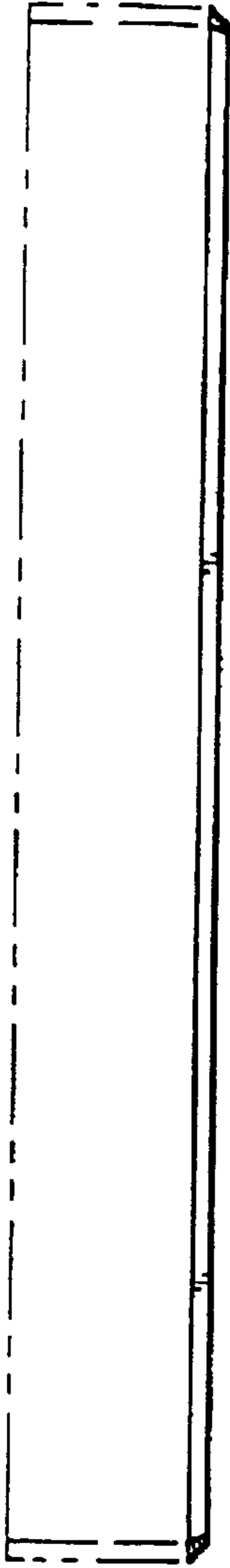


FIG. 3

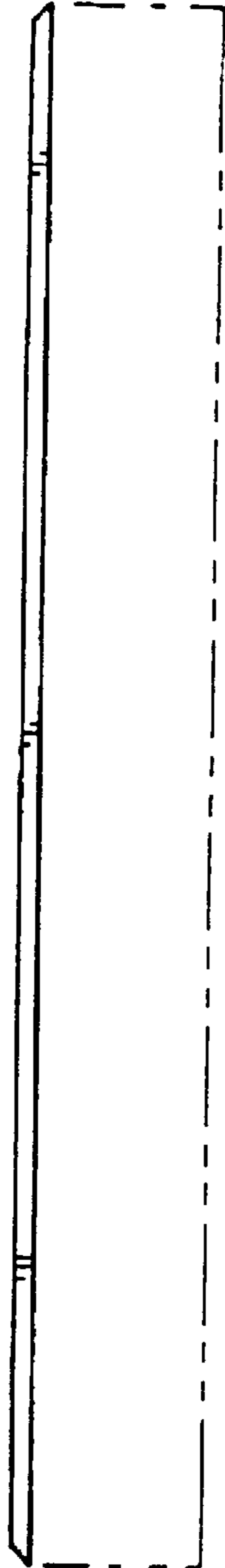


FIG. 7

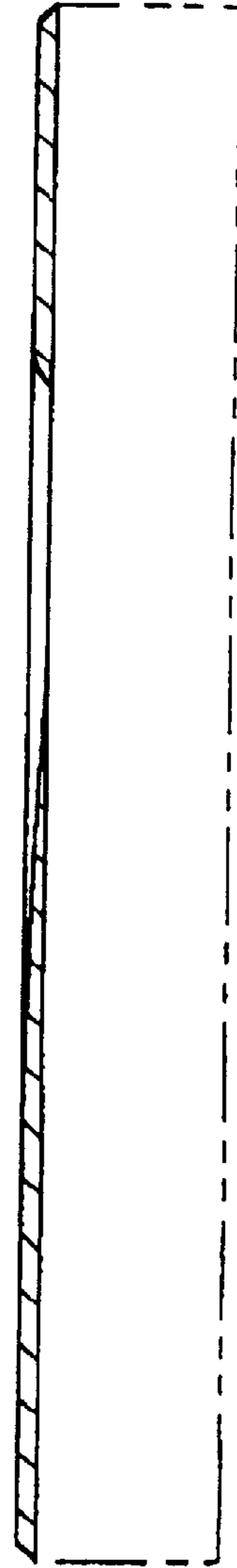
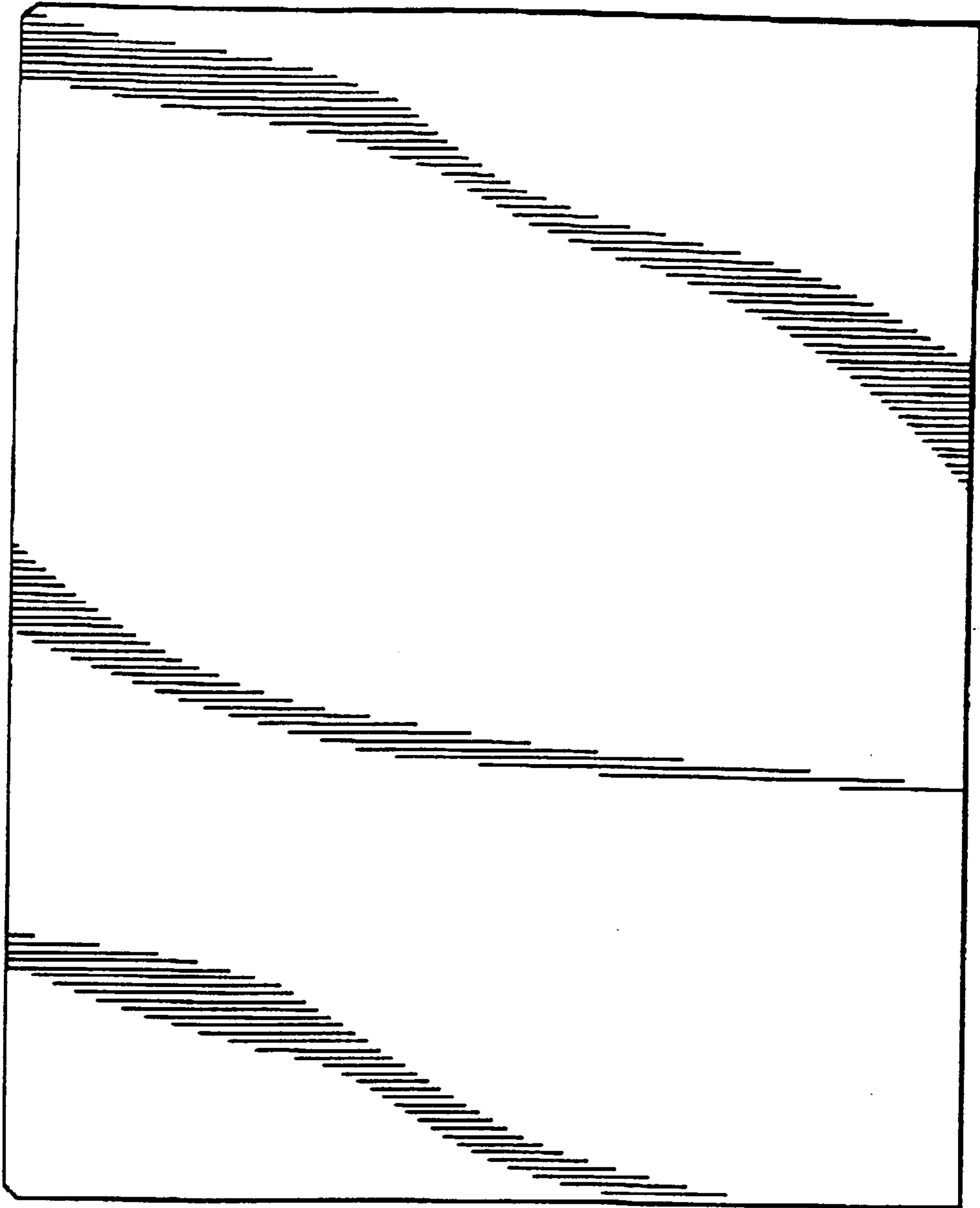


FIG. 8



**FIG. 4**