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United States Patent [19]

Klinker

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[54] **PROCESSOR PACKAGE COVER PLATE**

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[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[*] Notice: This patent is subject to a terminal disclaimer.

[**] Term: **14 Years**

[21] Appl. No.: **29/062,471**

[22] Filed: **Nov. 15, 1996**

[51] **LOC (6) Cl.** **14-02**

[52] **U.S. Cl.** **D14/114**; D14/107; D14/117

[58] **Field of Search** D14/114, 115, D14/117, 120; D13/182; D18/12; 206/706, 709; 340/825.22; 235/492; 361/816, 753, 737, 424; 257/678; 364/200, 239.3, 401.479, 578; 370/364; 379/269, 279, 399; 380/23, 24; 395/310, 376, 393, 325, 652, 670, 672, 675, 568, 800; 455/3.1

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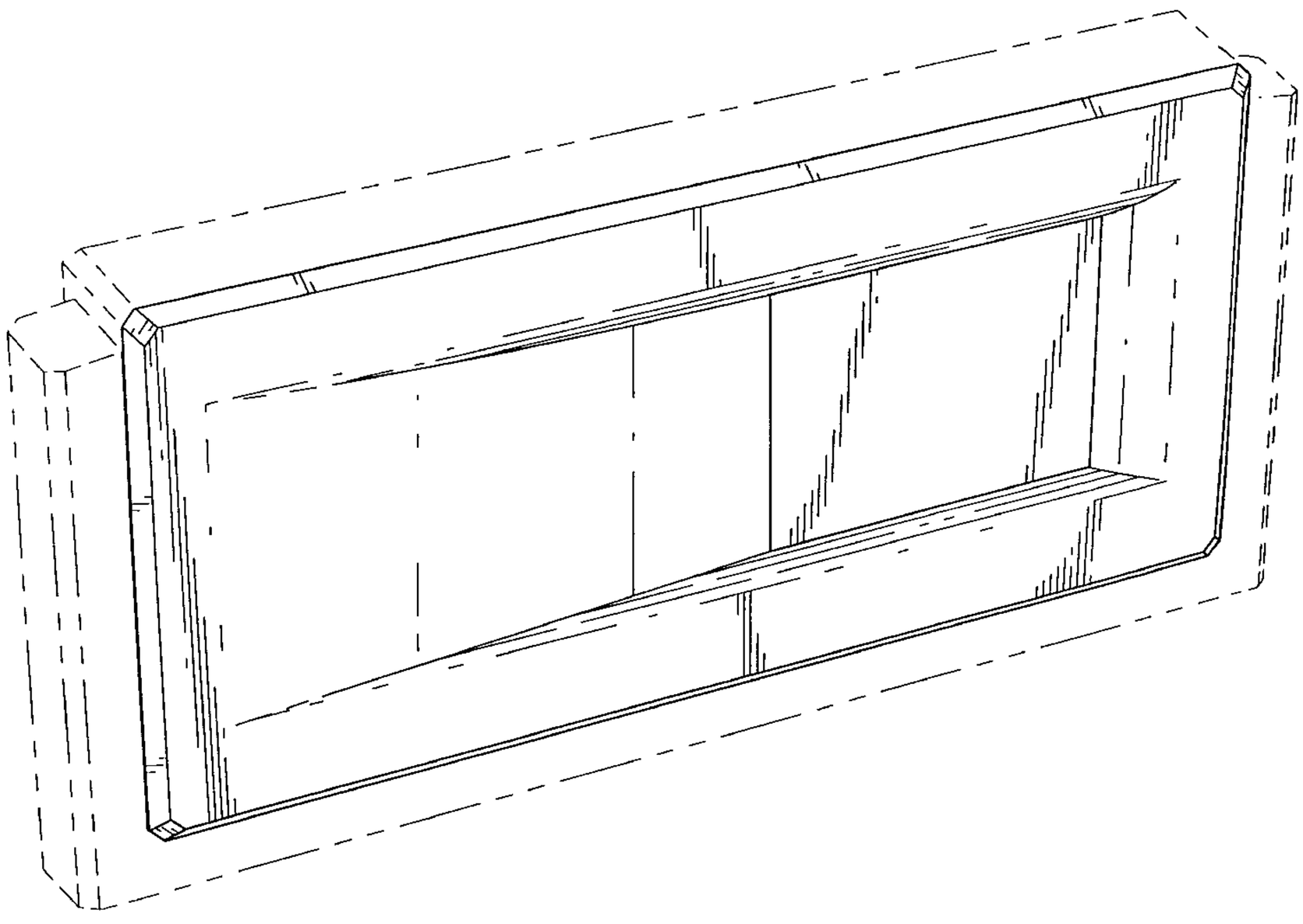
[57] **CLAIM**

The ornamental design for a processor package cover plate, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a processor package cover plate on a processor package including an indented area on the surface of the processor package cover plate;
FIG. **2–4** are front, top, and back views, respectively, of the processor package cover plate on the processor package;
FIG. **5–7** are right, left, and bottom views, respectively, of the processor package cover plate on the processor package; and,
FIG. **8** is a cross sectional view of the processor package cover plate on the processor package taken along line **8—8** of FIG. **2.**
The processor package is shown in broken lines in the views for illustrative purposes only and forms no part of the claimed design.

1 Claim, 3 Drawing Sheets



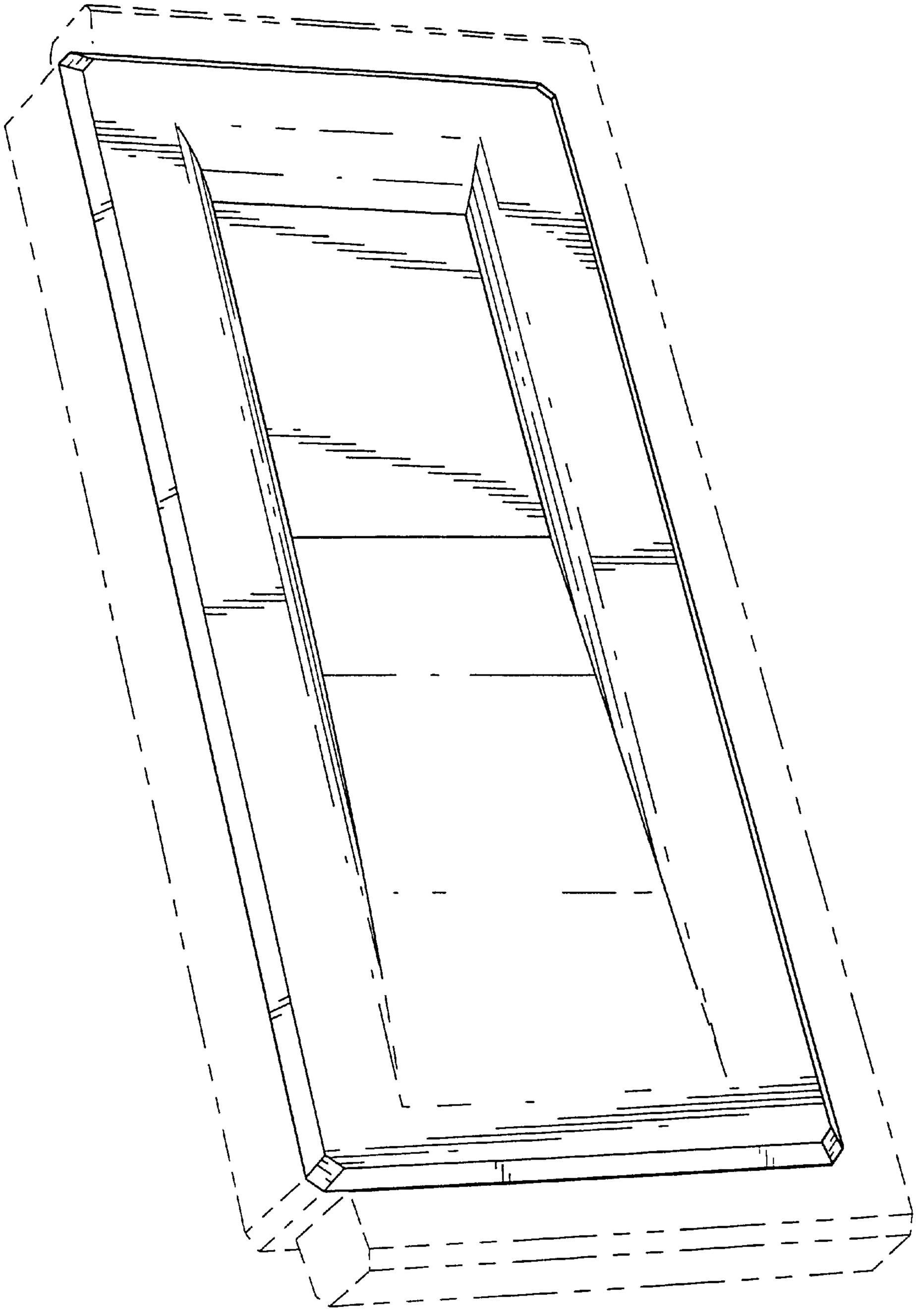


FIG. 1

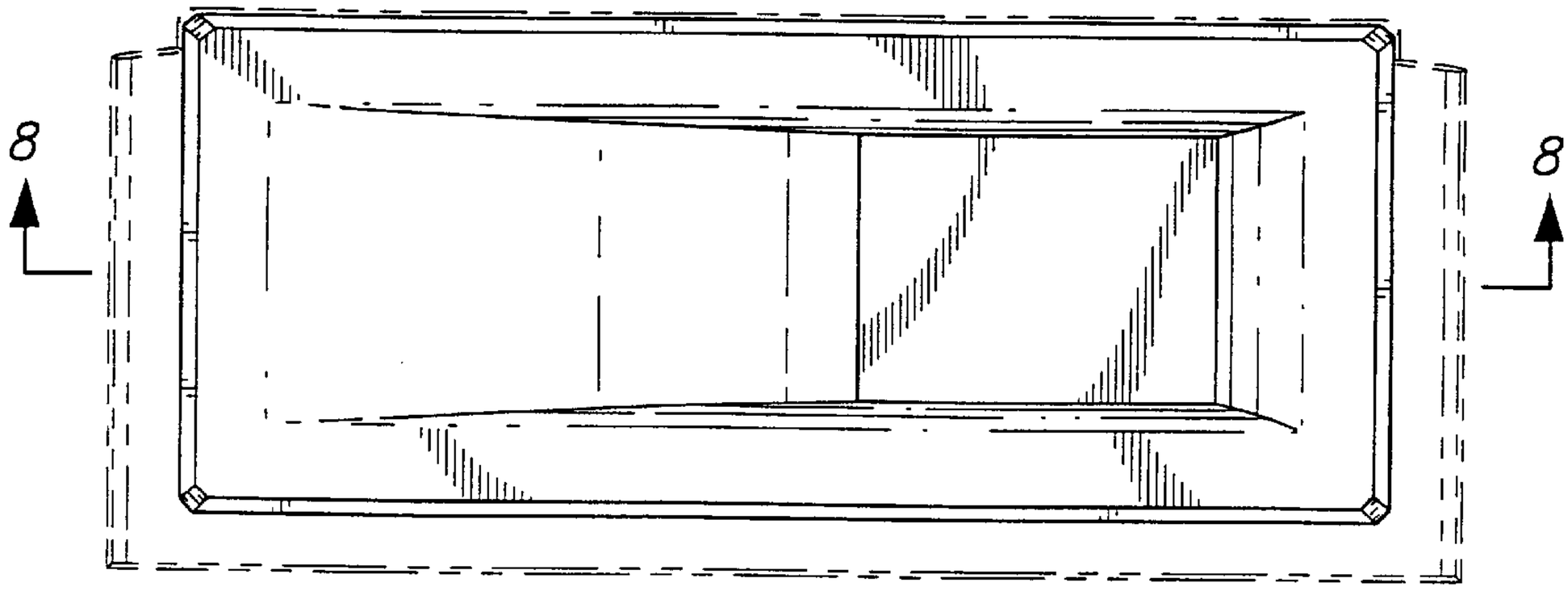


FIG. 2

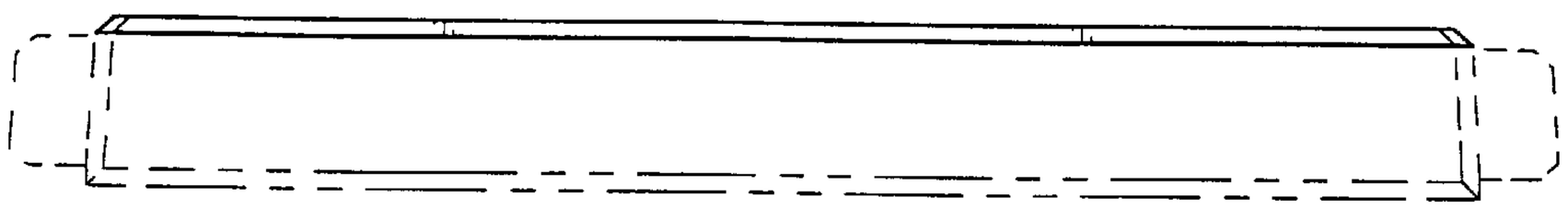


FIG. 3

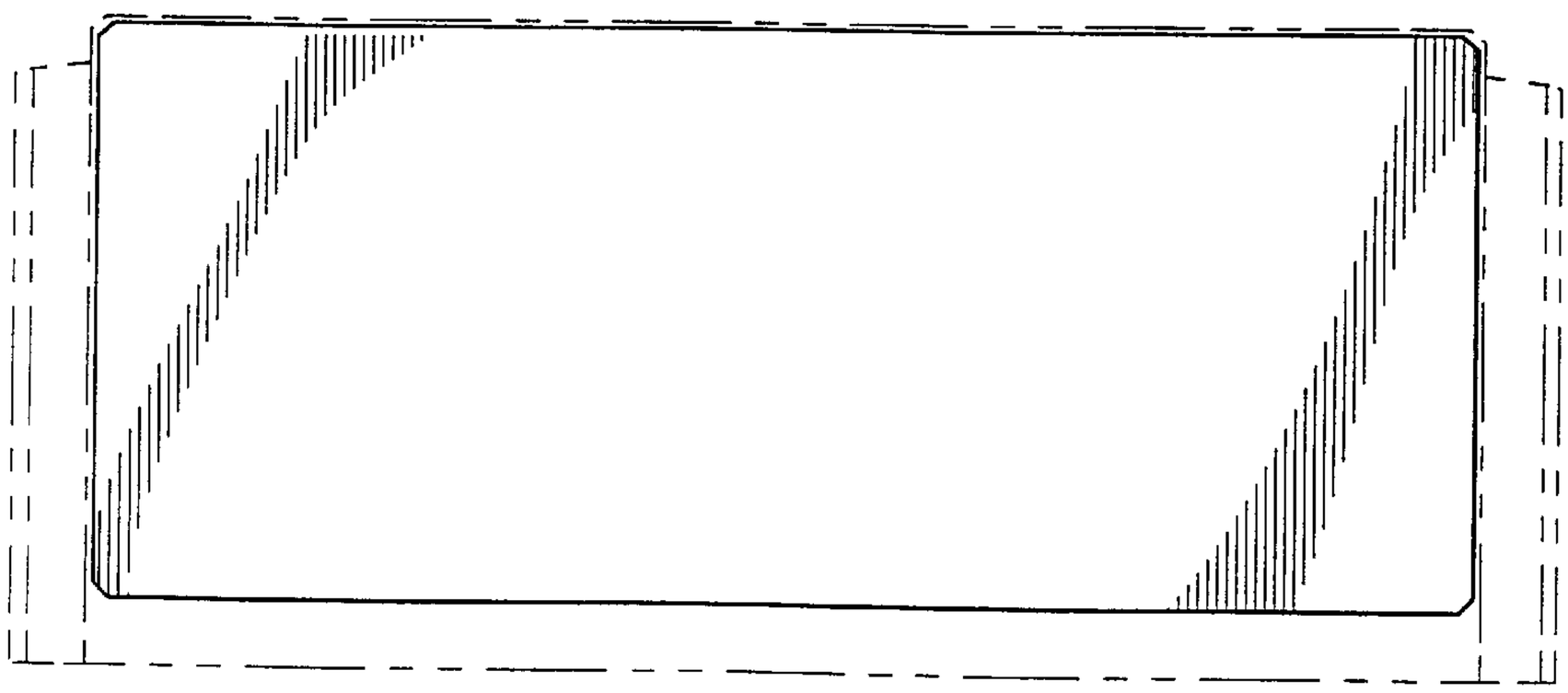


FIG. 4

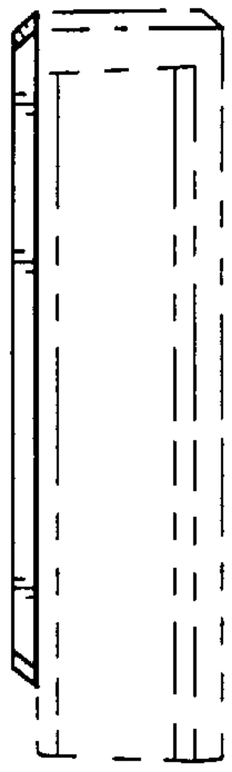


FIG. 5

FIG. 6

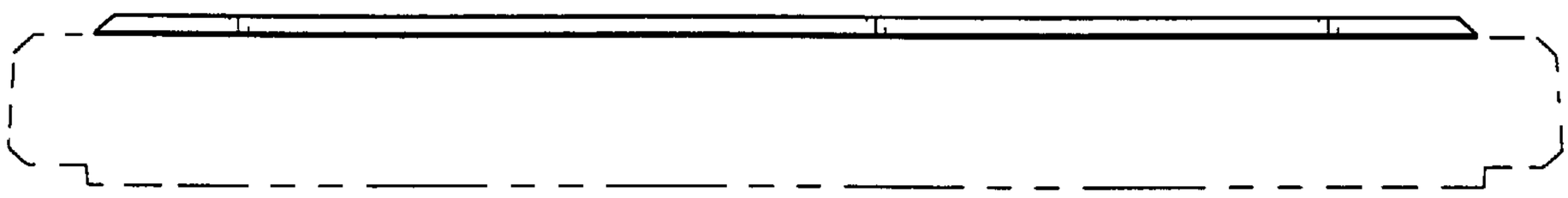


FIG. 7

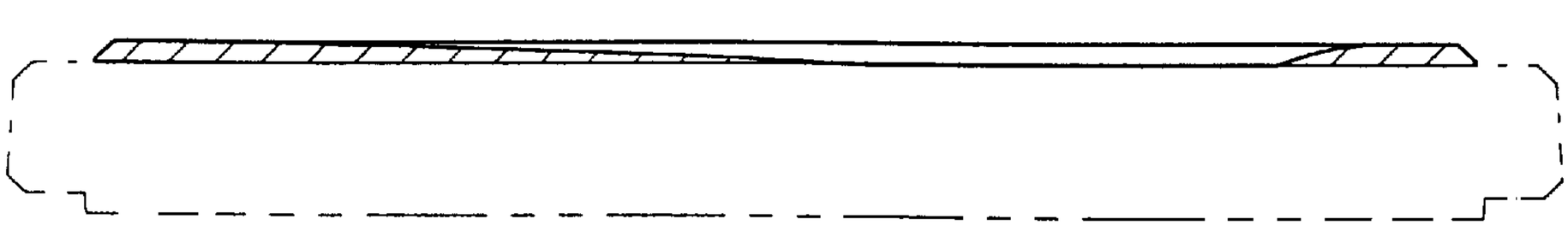


FIG. 8