



US00D411516S

United States Patent [19]

Imafuku et al.

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[45] **Date of Patent: ** Jun. 29, 1999**

[54] **GAS DIFFUSION PLATE FOR ELECTRODE OF SEMICONDUCTOR WAFER PROCESSING APPARATUS**

FOREIGN PATENT DOCUMENTS

952210 4/1996 Japan .
952210 5/1996 Japan .

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[57] CLAIM

We claim the ornamental design for gas diffusion plate for electrode of semiconductor wafer processing apparatus, as shown and described.

[*] Notice: This patent is subject to a terminal disclaimer.

DESCRIPTION

[**] Term: **14 Years**

FIG. 1 is a bottom view of a gas diffusion plate for electrode of semiconductor wafer processing apparatus showing our new design;

[21] Appl. No.: **29/059,398**

FIG. 2 is a top view thereof;

[22] Filed: **Sep. 10, 1996**

FIG. 3 is a right elevational view thereof, the left elevational view thereof being a mirror image and, therefore, not shown;

[30] Foreign Application Priority Data

Mar. 15, 1996 [JP] Japan 8-7276

FIG. 4 is a front elevational thereof, the rear elevational view thereof being a mirror image and, therefore, not shown;

[51] **LOC (6) Cl. 13-03**

FIG. 5 an enlarged sectional view of on section 5—5 in FIG. 1;

[52] **U.S. Cl. D13/182**

FIG. 6 an enlarged sectional view of on section 6—6 in FIG. 1; and,

[58] **Field of Search D13/182; 156/345, 156/643, 646; 437/228**

FIG. 7 is a bottom/rear perspective view thereof.

[56] References Cited

U.S. PATENT DOCUMENTS

D. 363,464 10/1995 Fukasawa D13/182

1 Claim, 4 Drawing Sheets

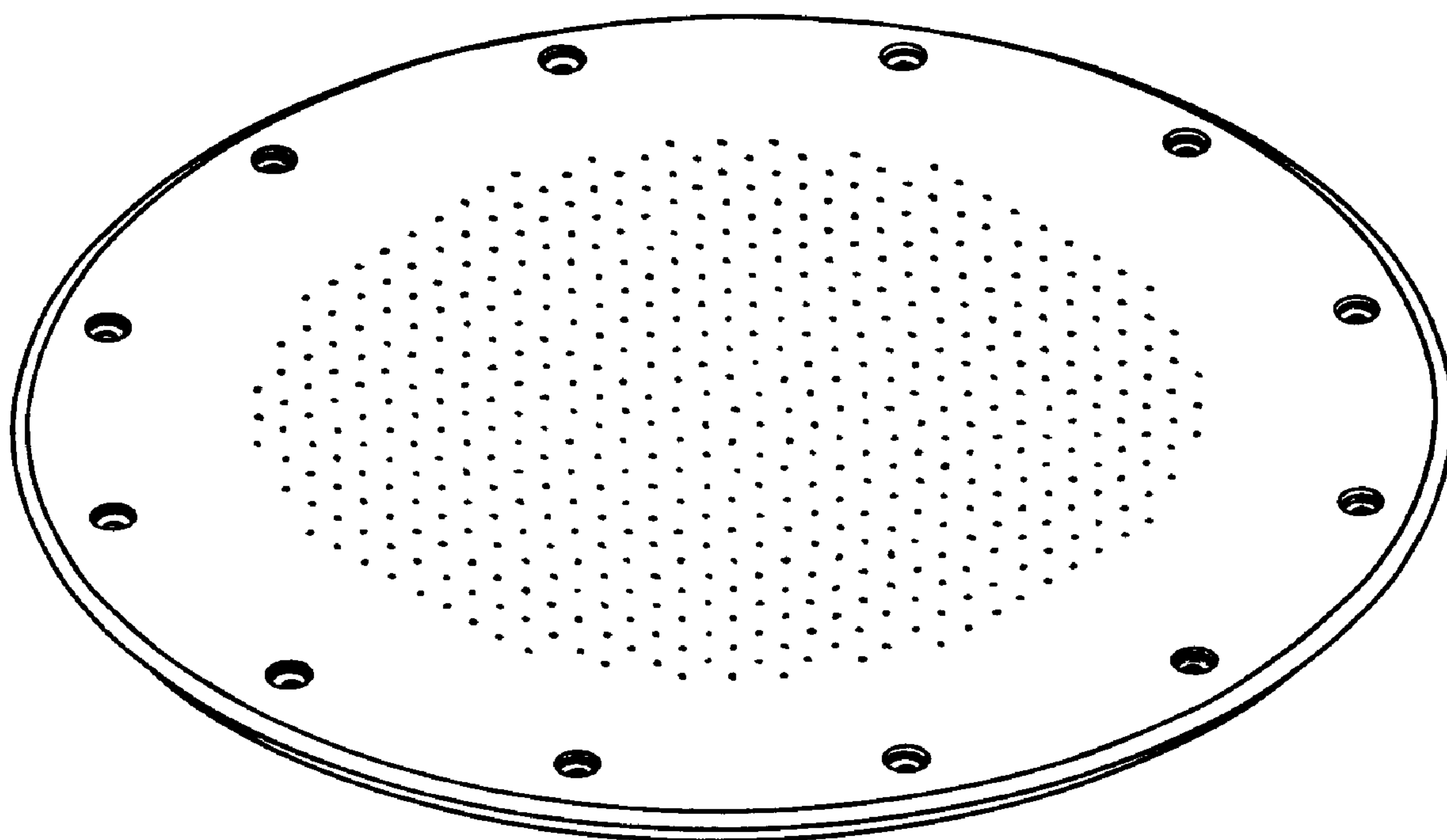


FIG. 1

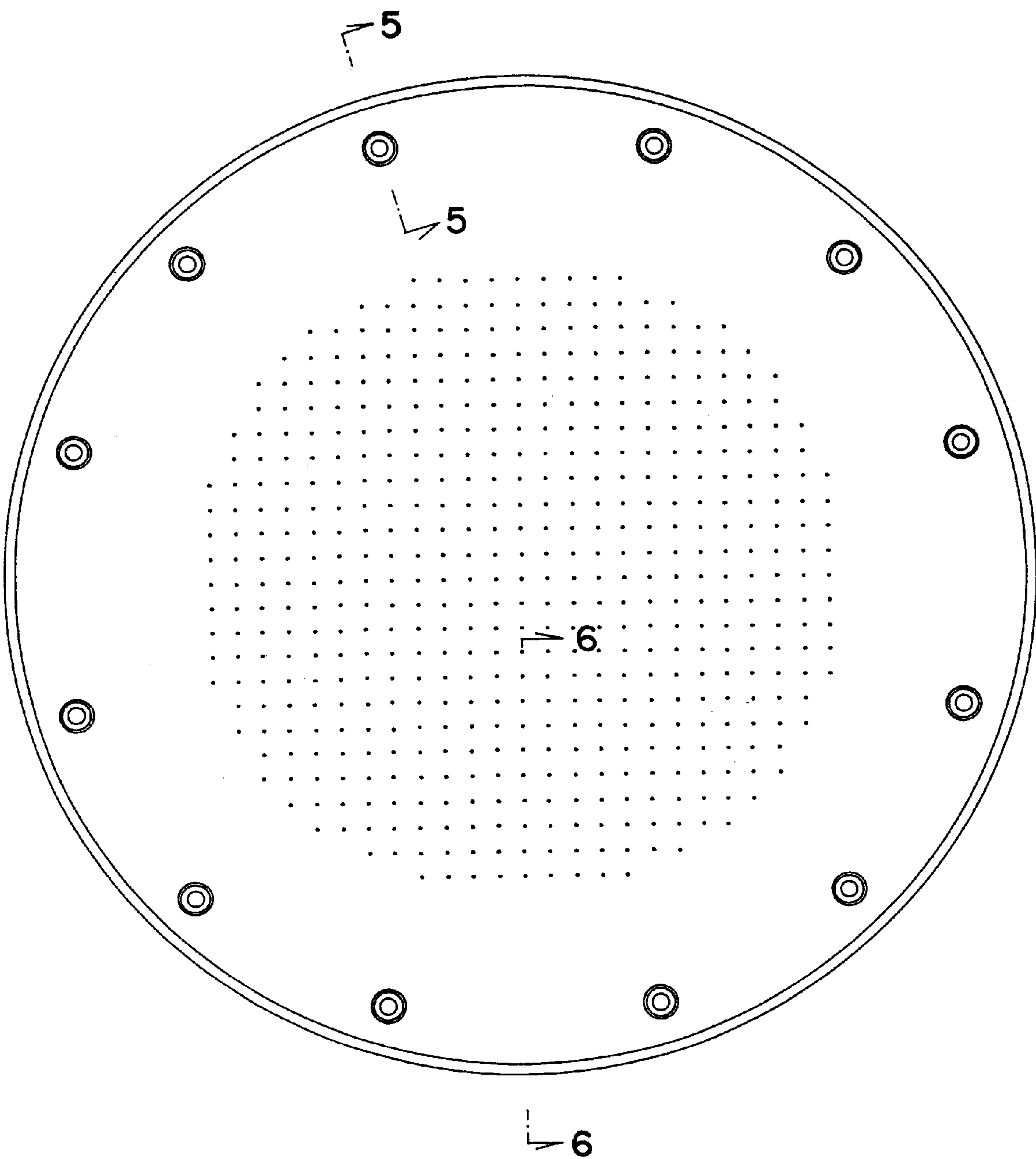


FIG. 2

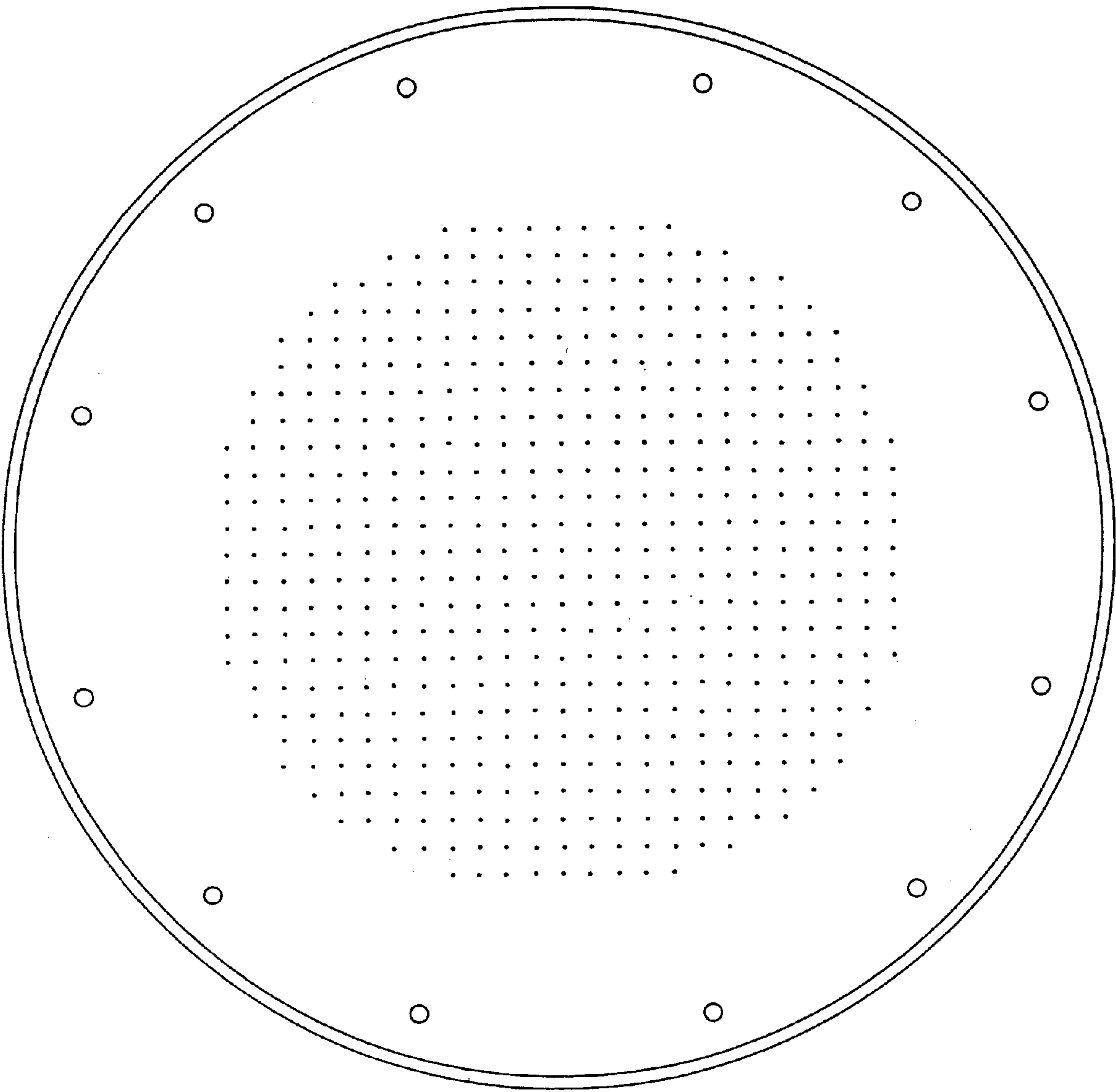


FIG. 3



FIG. 5

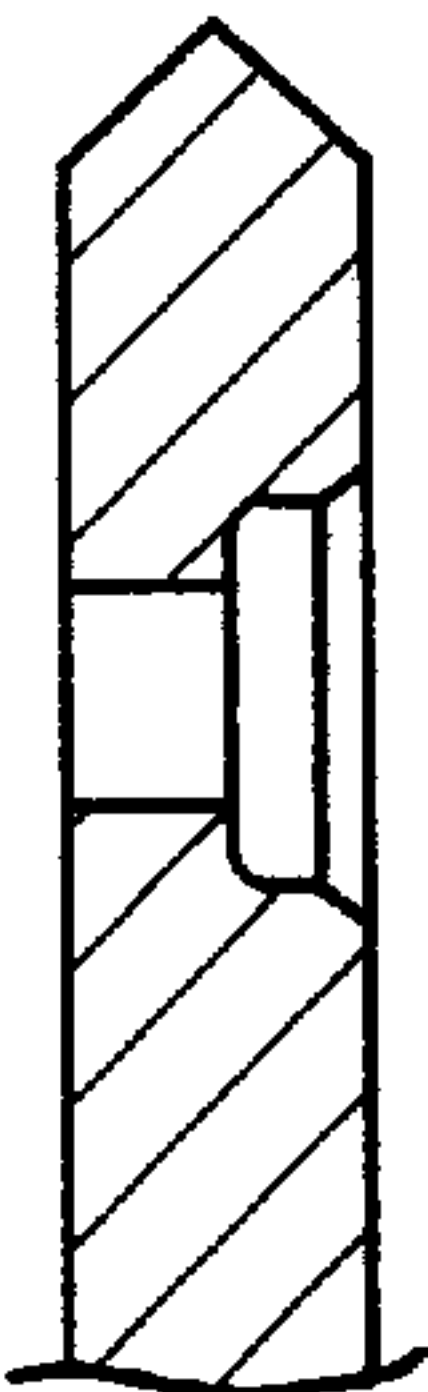


FIG. 6

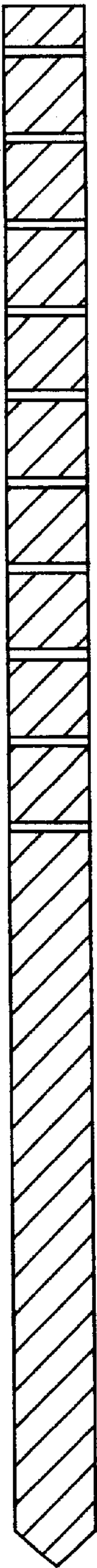


FIG. 4

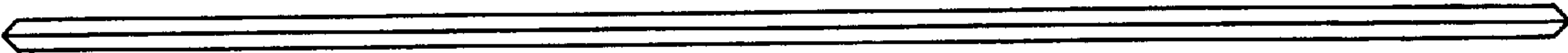


FIG. 7

