US00D411512S

United States Patent [19]

Kataoka et al.

[11] **Patent Number: Des. 411,512**

[45] **Date of Patent: ** Jun. 29, 1999**

[54] **CONNECTOR FOR PRINTED CIRCUIT BOARDS**

[75] Inventors: **Yasuhiro Kataoka**, Yokohama; **Terumi Nakashima**, Takatsuki; **Narihiko Hashimoto**, Nagoya, all of Japan

[73] Assignees: **Sony Corporation**, Tokyo; **Solderless Terminal Mfg. Co., Ltd.**, Osaka, both of Japan

[**] Term: **14 Years**

[21] Appl. No.: **29/090,451**

[22] Filed: **Jul. 9, 1998**

Related U.S. Application Data

[62] Division of application No. 29/071,612, Jun. 3, 1997, Pat. No. Des. 402,274.

[30] **Foreign Application Priority Data**

Dec. 11, 1996 [JP] Japan 8-37848
Dec. 26, 1996 [JP] Japan 8-39611
Apr. 1, 1997 [JP] Japan 9-50067

[51] **LOC (6) Cl.** **13-03**
[52] **U.S. Cl.** **D13/147**
[58] **Field of Search** D13/133, 147; 439/344, 353, 357, 660, 682, 685, 686, 687, 695, 696, 712, 713

[56] **References Cited**

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Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—W. F. Fasse; W. G. Fasse

[57] **CLAIM**

We claim the ornamental design for a connector for printed circuit boards, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a connector for printed circuit boards showing our new design in a first embodiment, while the rear view corresponds to the front view.

FIG. **2** is a top view of said connector for printed circuit boards of the first embodiment.

FIG. **3** is a bottom view of said connector for printed circuit boards of the first embodiment.

FIG. **4** is a left side view of said connector for printed circuit boards of the first embodiment, while the right side view corresponds to the left side view.

FIG. **5** is a sectional view along the line V—V in FIG. **2**.

FIG. **6** is a sectional view along the line VI—VI in FIG. **1**.

FIG. **7** is a sectional view along the line VI—VI in FIG. **1**, wherein said connector for printed circuit boards is shown in a condition connecting two circuit boards, which are drawn in broken lines for illustrative purposes only. The circuit boards drawn in broken lines form no part of the claimed design.

FIG. **8** is a front view of a connector for printed circuit boards showing our new design in a second embodiment, while the rear view corresponds to the front view.

FIG. **9** is a top view of said connector for printed circuit boards of the second embodiment.

FIG. **10** is a bottom view of said connector for printed circuit boards of the second embodiment.

FIG. **11** is a left side view of said connector for printed circuit boards of the second embodiment, while the right side view corresponds to the left side view.

FIG. **12** is a sectional view along the line XII—XII in FIG. **9**.

FIG. **13** is a sectional view along the line XIII—XIII in FIG. **8**; and,

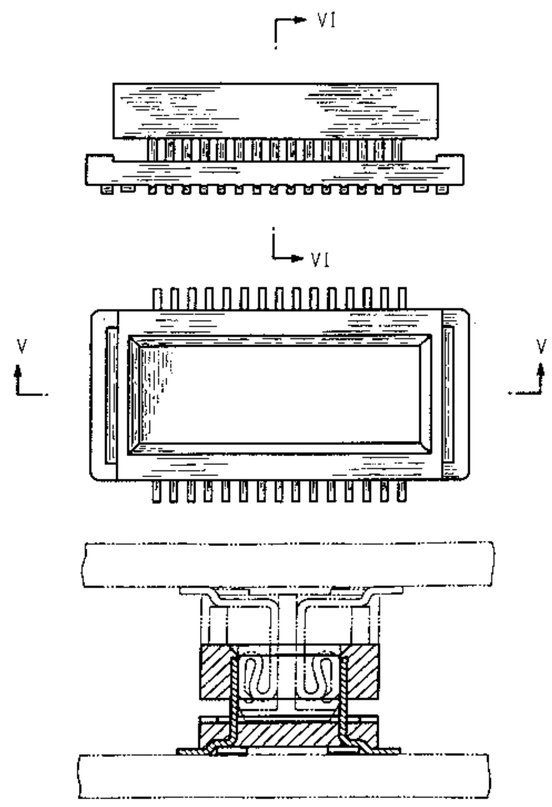


FIG. **14** is a sectional view along the line XIII—XIII in FIG. **8**, wherein said connector for printed circuit boards is shown in a condition connecting two circuit boards, which are drawn in broken lines for illustrative purposes only. The circuit boards drawn in broken lines form no part of the claimed design.

1 Claim, 8 Drawing Sheets

FIG. 1

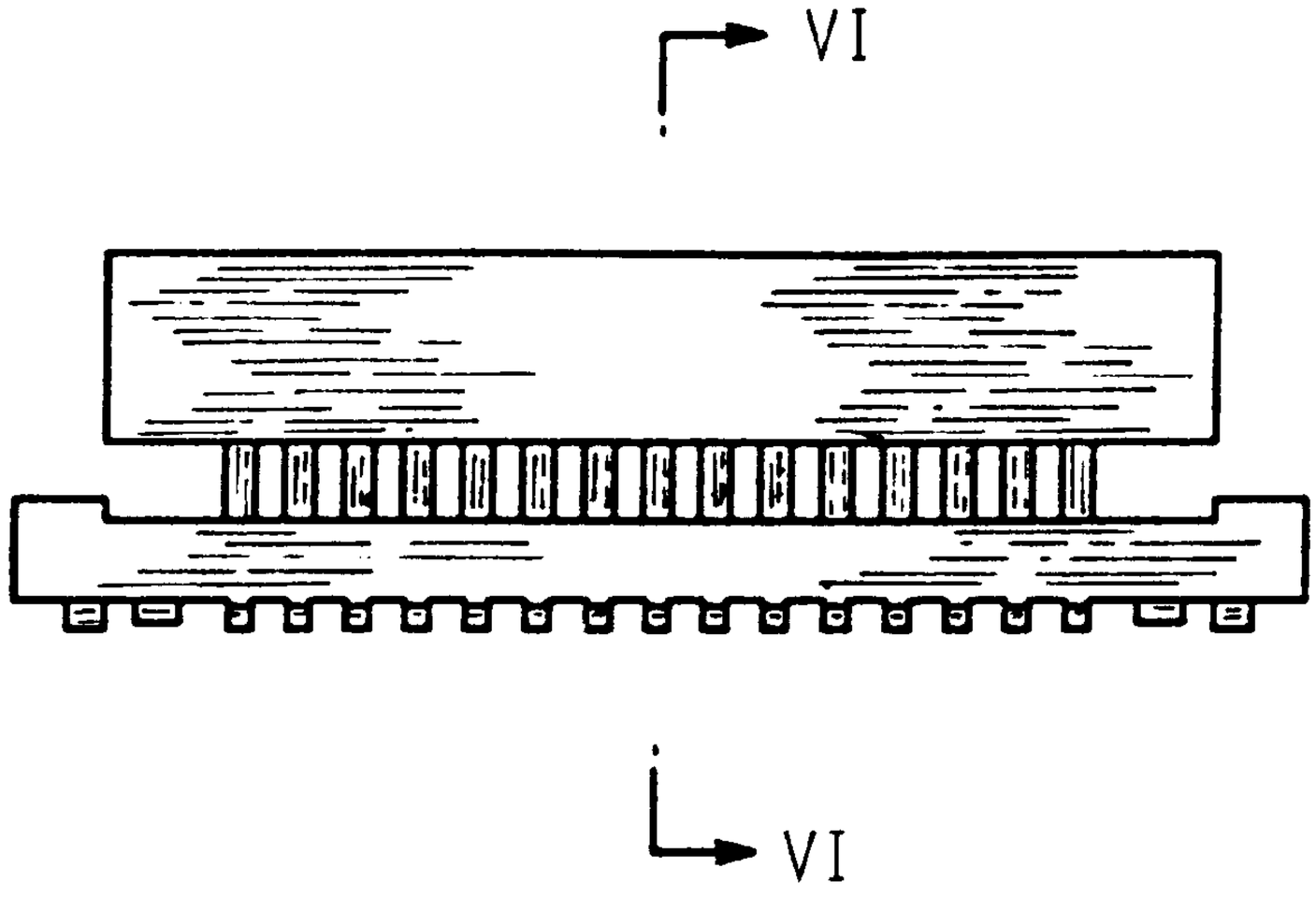


FIG. 2

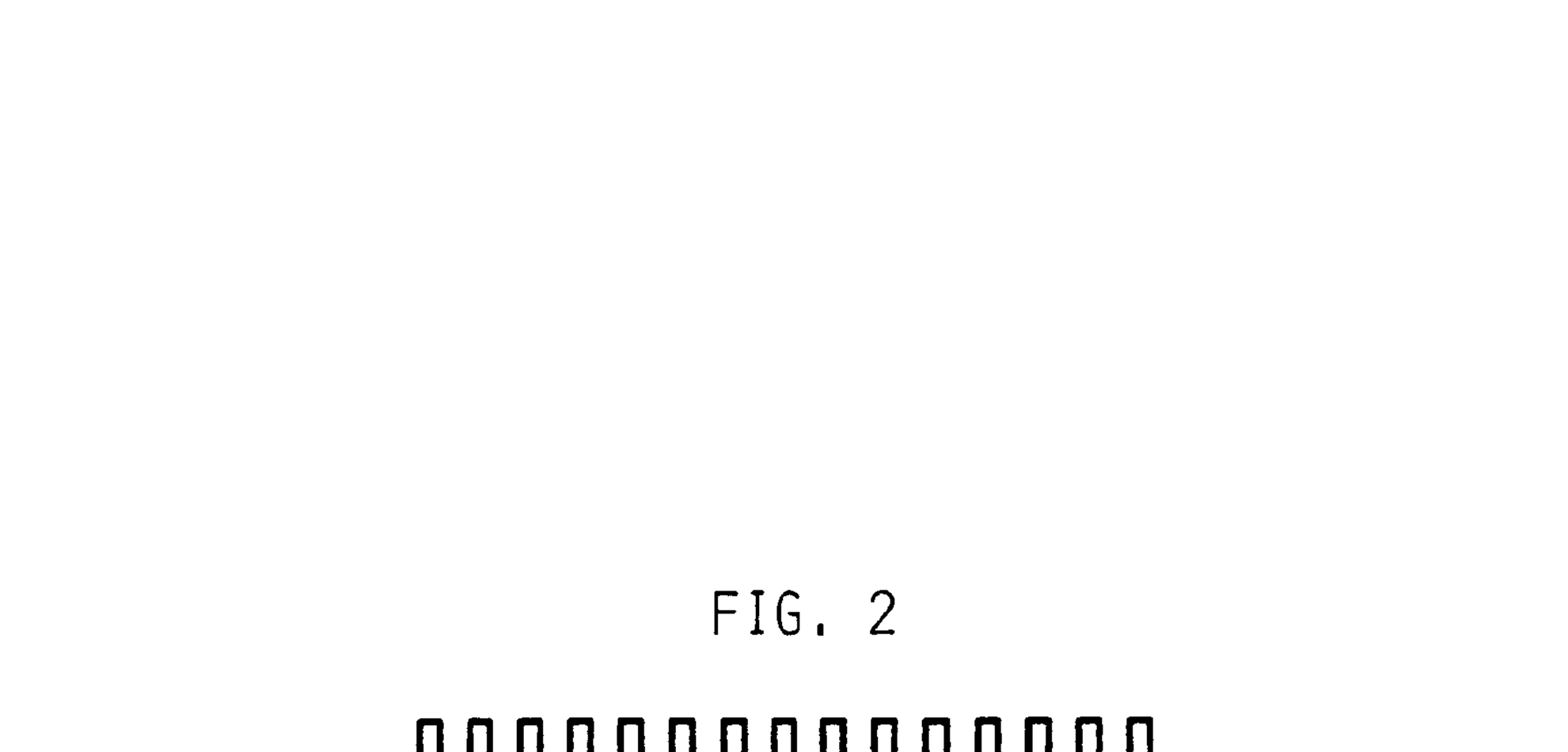


FIG. 3

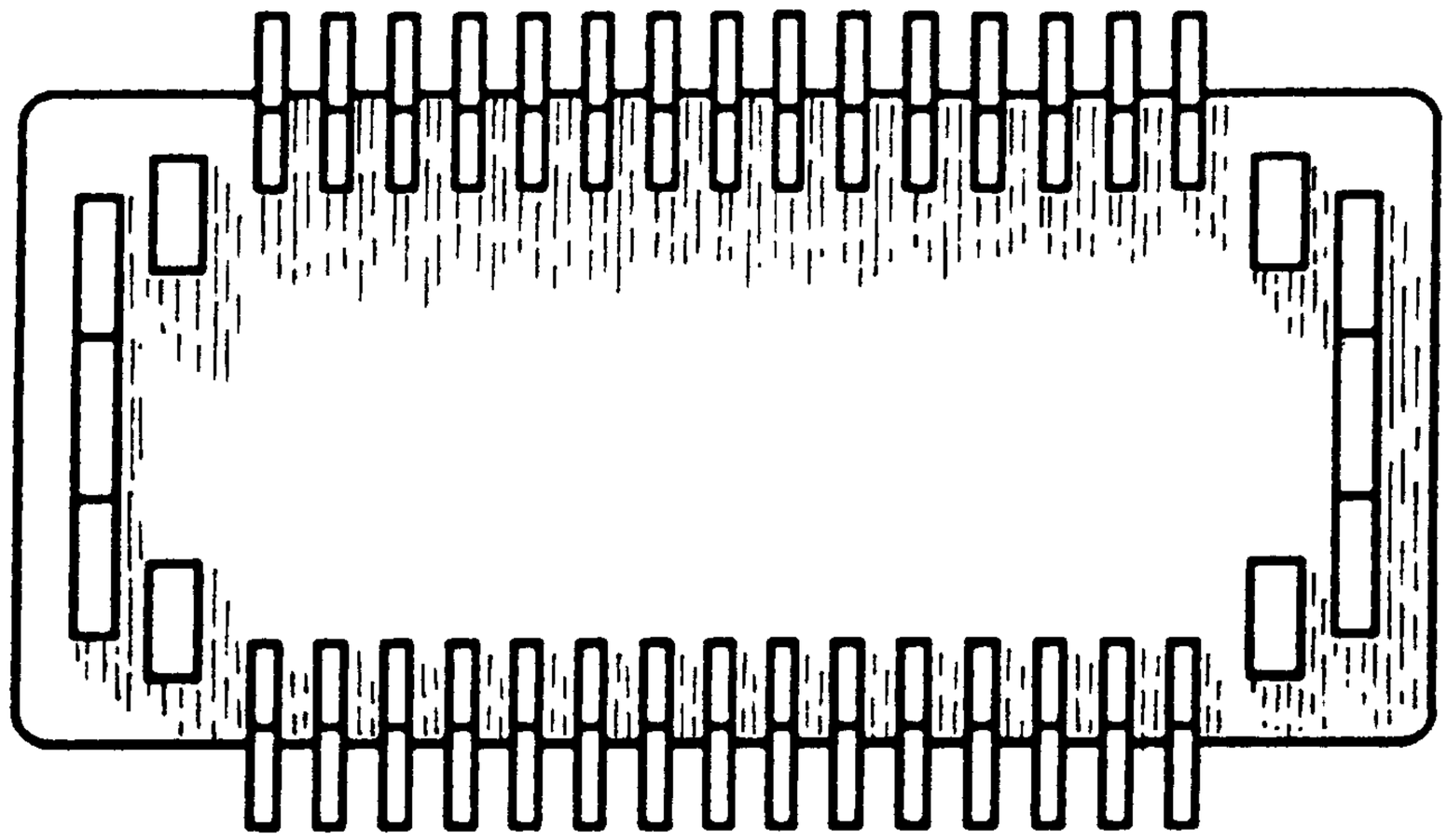


FIG. 4

FIG. 5

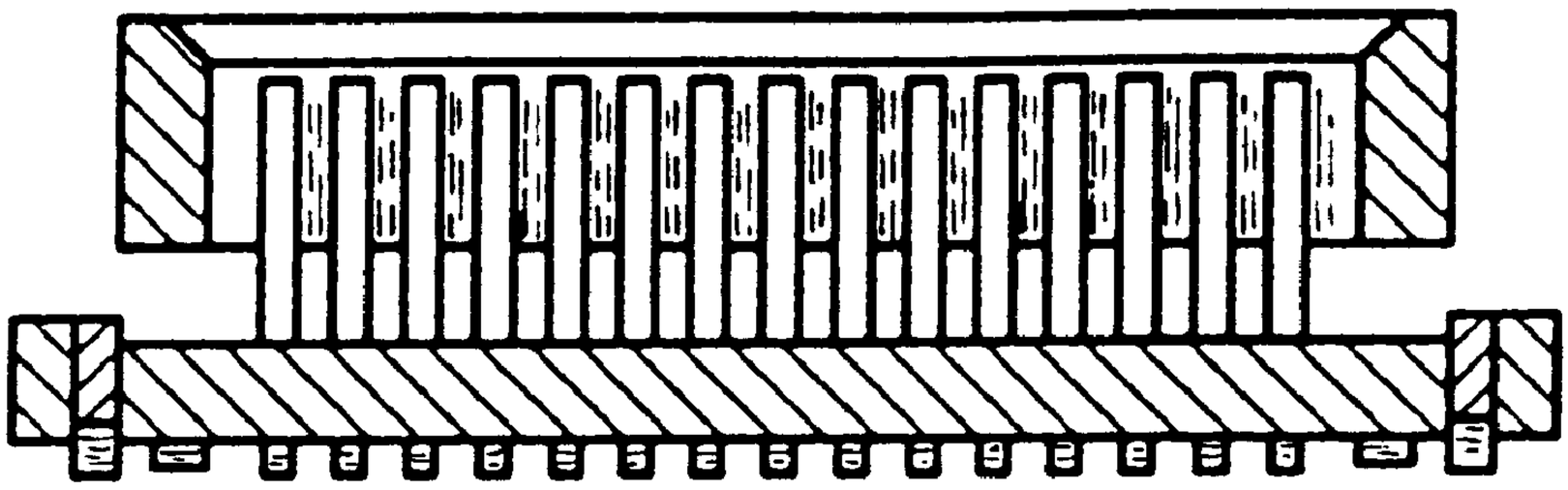


FIG. 6

FIG. 7

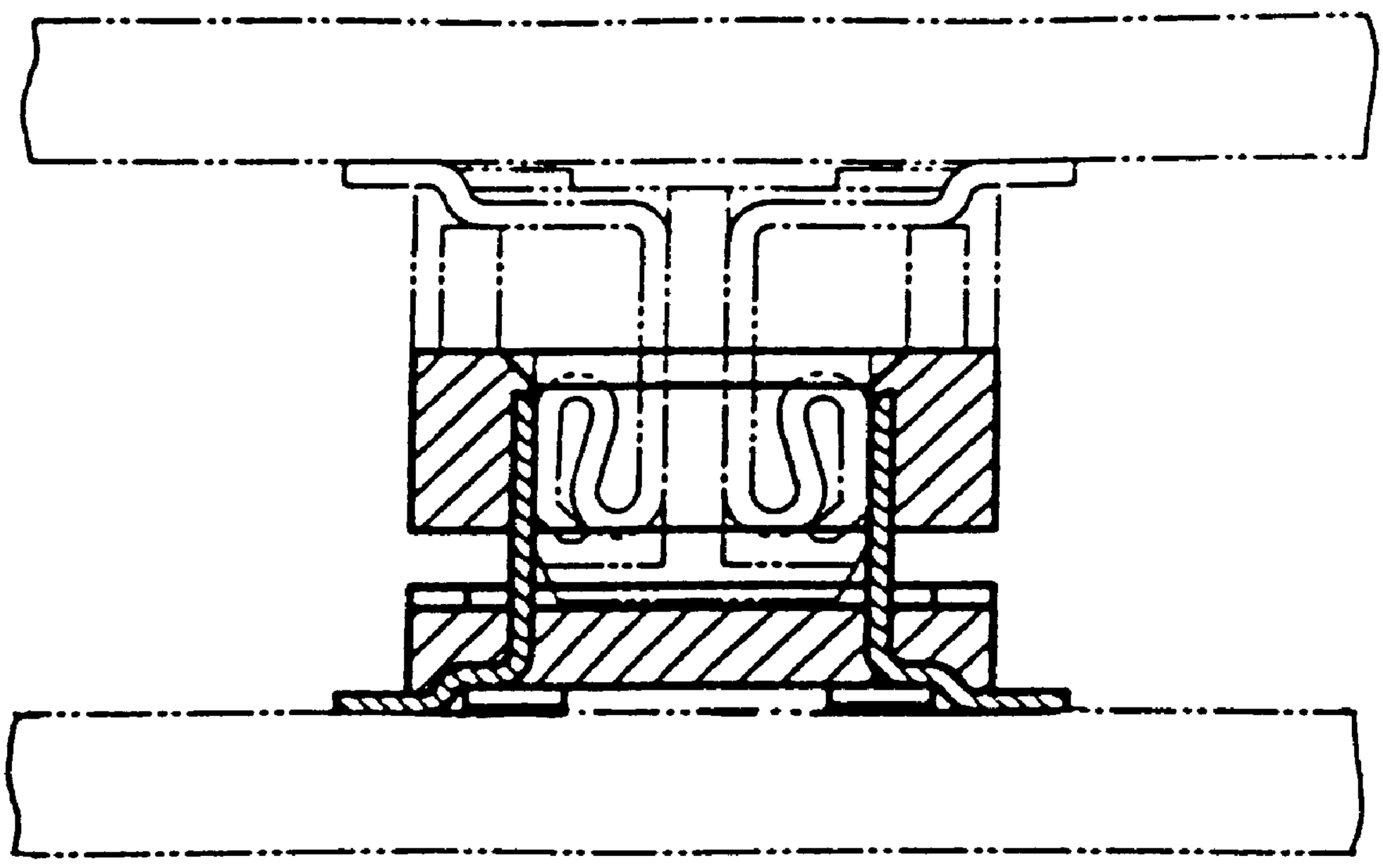


FIG. 8

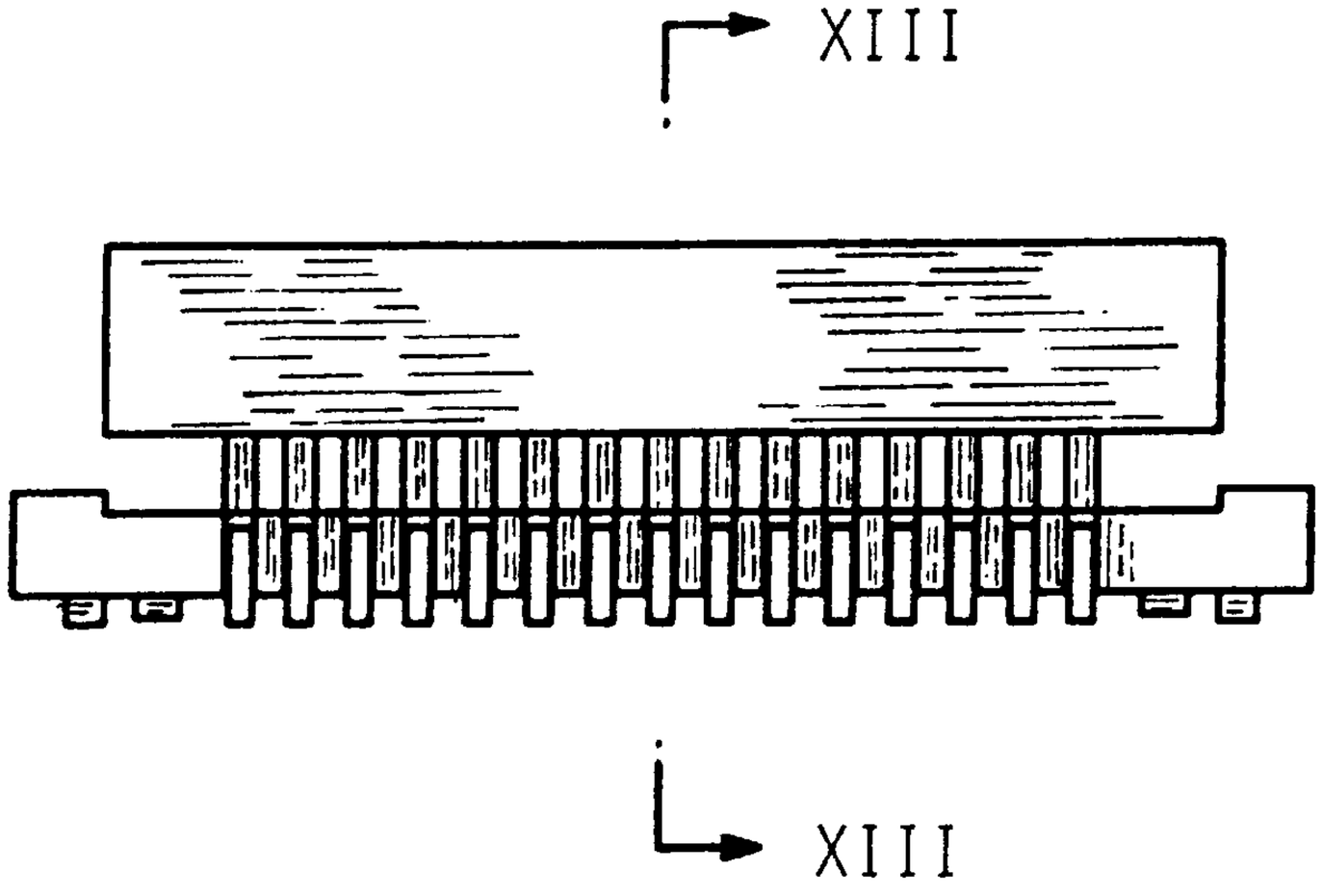


FIG. 9

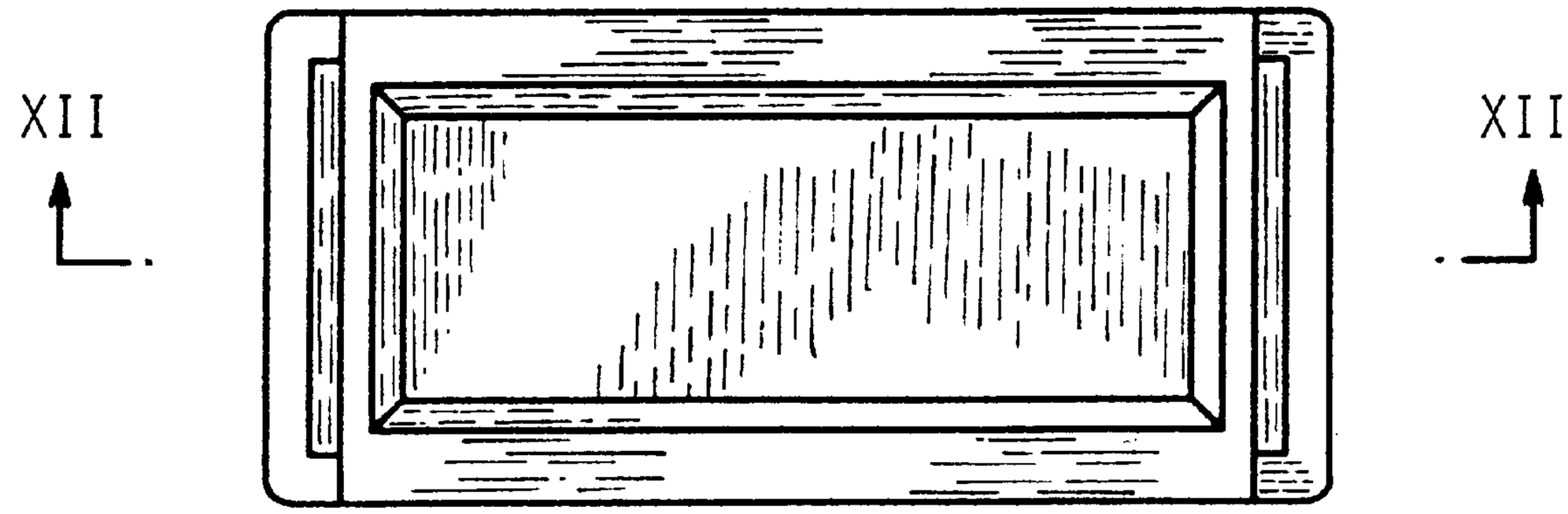


FIG. 10

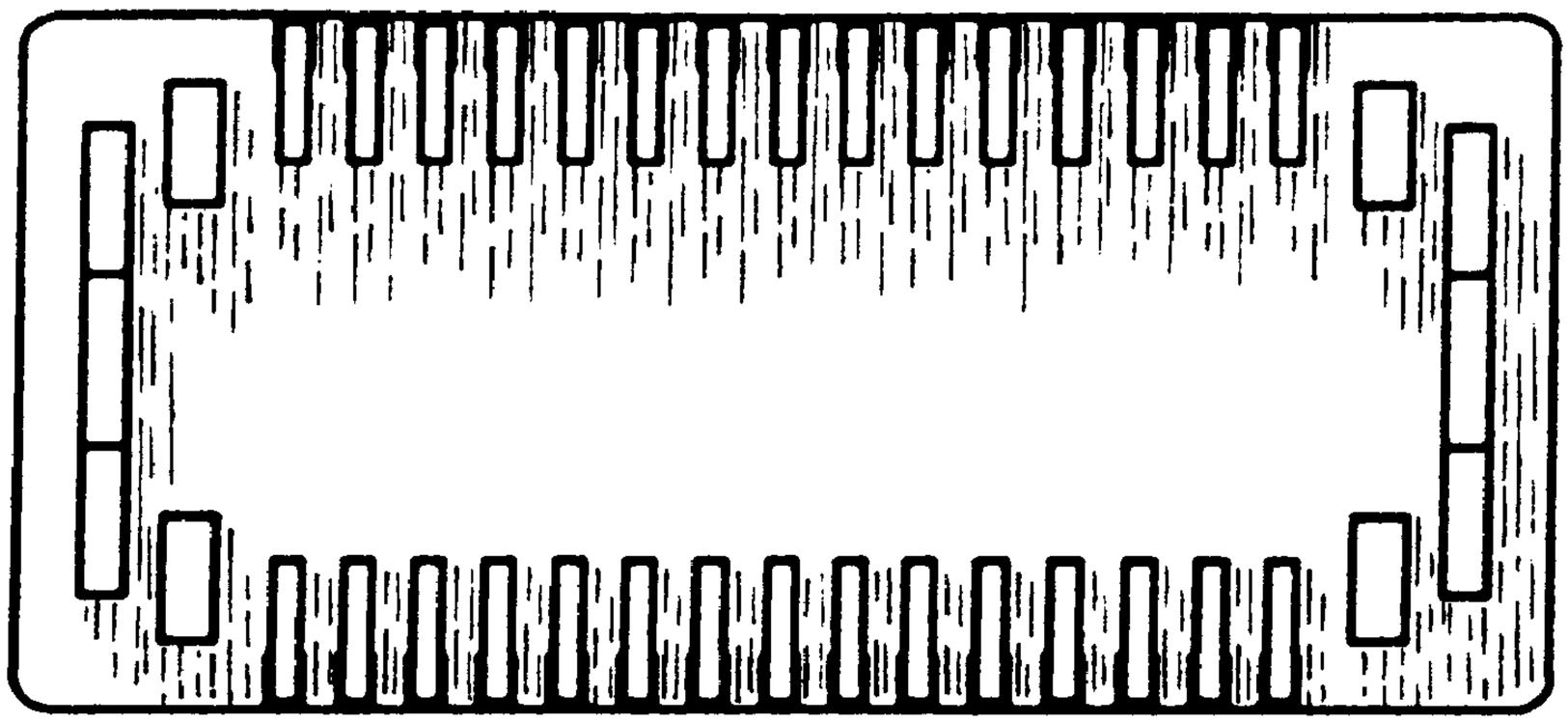


FIG. 11

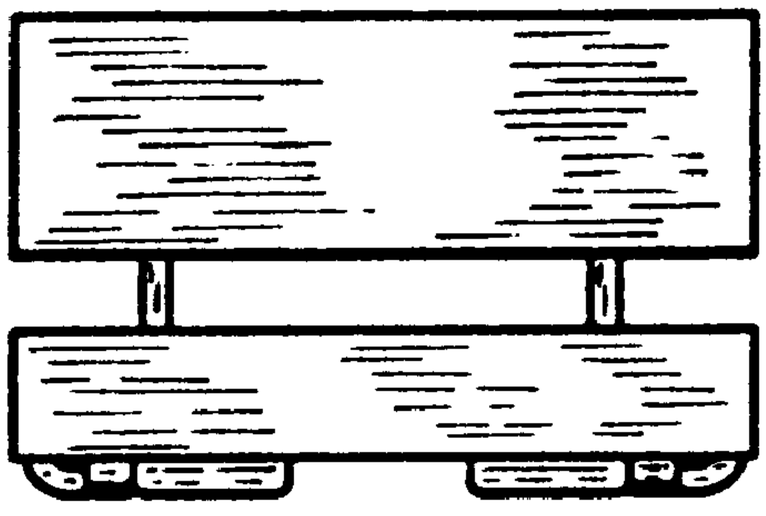


FIG. 12

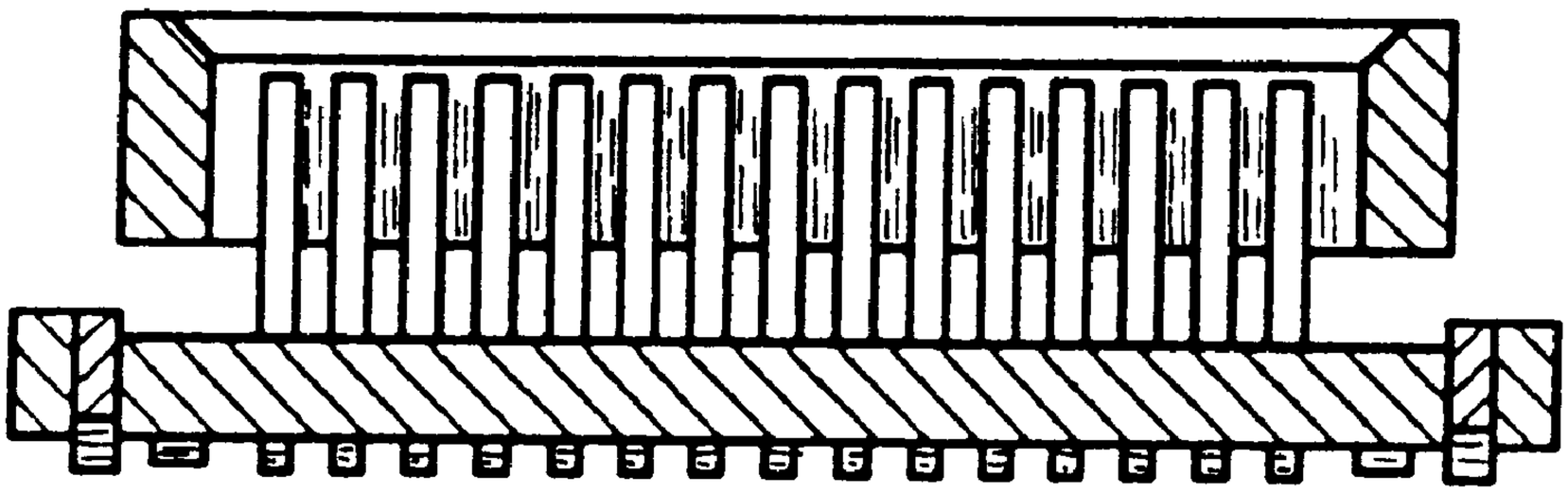


FIG. 13

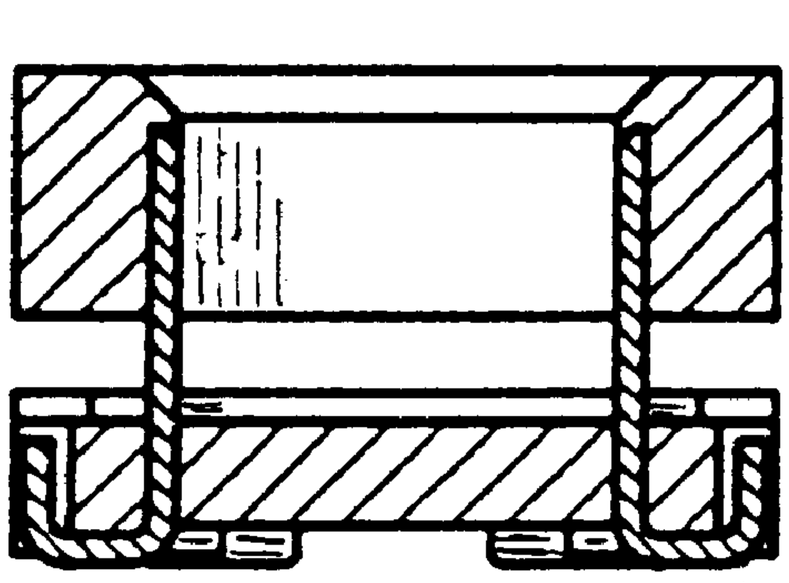
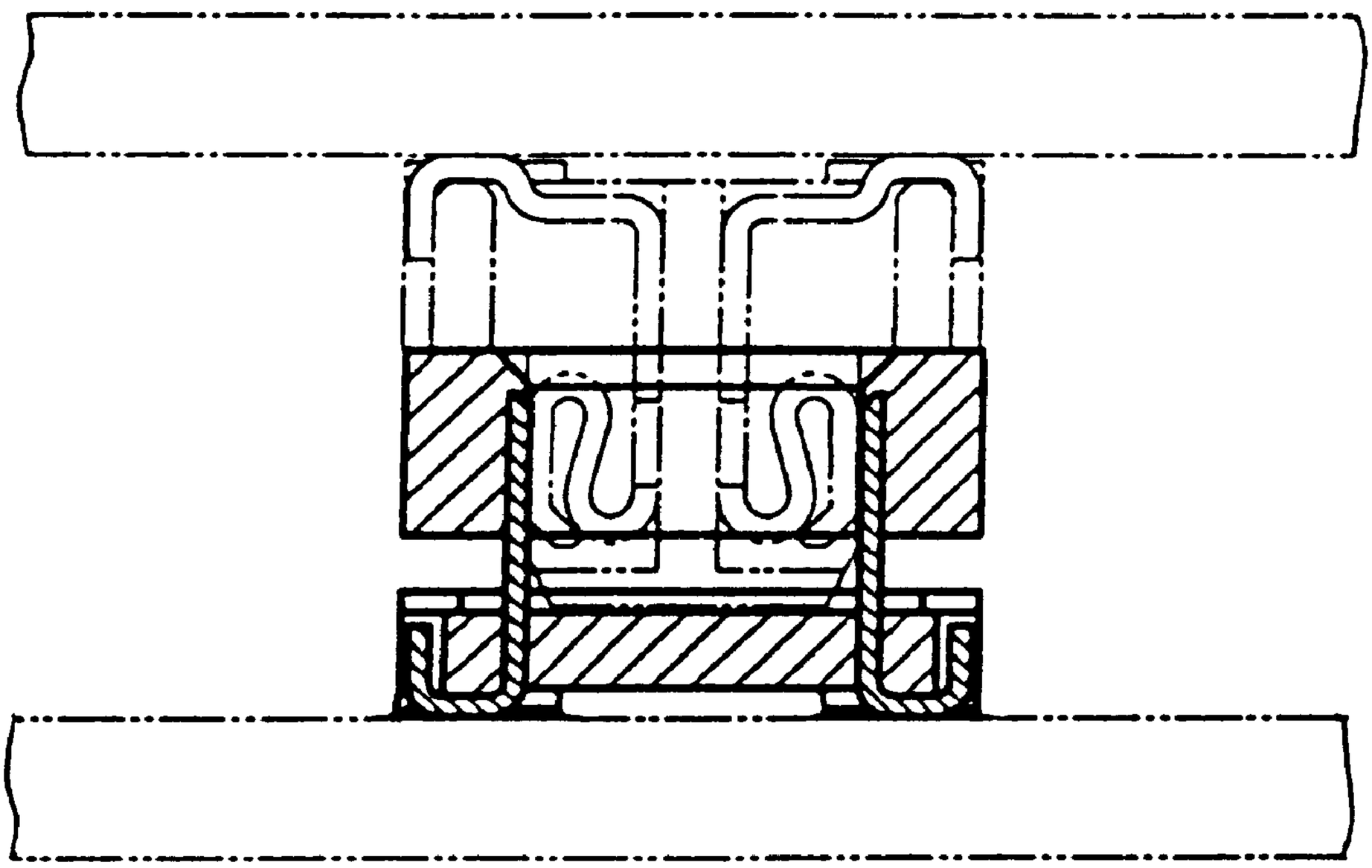


FIG. 14



UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : Des. 411,512
DATED : June 29, 1999
INVENTOR(S) : Yasuhiro Kataoka, et. al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, item [73] the second Assignee should read – Japan Solderless Terminal Mfg. Co., Ltd.

Signed and Sealed this

Fourteenth Day of March, 2000

Attest:

Q. TODD DICKINSON

Attesting Officer

Commissioner of Patents and Trademarks