US00D411176S

# United States Patent [19]

**Shimazu**

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[45] **Date of Patent: ** *Jun. 22, 1999**

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[54] **WAFER BOAT FOR USE IN A SEMICONDUCTOR WAFER HEAT PROCESSING APPARATUS**

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[73] Assignee: **Tokyo Electron Limited**, Tokyo-To, Japan

[ * ] Notice: This patent is subject to a terminal disclaimer.

[**] Term: **14 Years**

[21] Appl. No.: **29/083,421**

[22] Filed: **Feb. 5, 1998**

[30] **Foreign Application Priority Data**

Aug. 20, 1997 [JP] Japan .................................... 9-65098

[51] **LOC (6) Cl.** ........................................................ **13-03**

[52] **U.S. Cl.** ............................................................ **D13/182**

[58] **Field of Search** .......................... D13/182; D15/144, D15/144.1, 119; 414/935–941, 217, 147; 437/247, 946; D6/407, 629

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[57] **CLAIM**

I claim the ornamental design for wafer boat for use in a semiconductor wafer heat processing apparatus, as shown and described.

**DESCRIPTION**

FIG. **1** a perspective view of a wafer boat for use in a semiconductor wafer heat processing apparatus.

FIG. **2** a front elevational view thereof.

FIG. **3** a cross-sectional view taken along line III—III in FIG. **2**.

FIG. **4** a cross-sectional view taken along line IV—IV in FIG. **2**.

FIG. **5** a rear elevational view thereof.

FIG. **6** a right side view thereof.

FIG. **7** a top plan view thereof; and,

FIG. **8** a bottom plan view thereof.

**1 Claim, 3 Drawing Sheets**

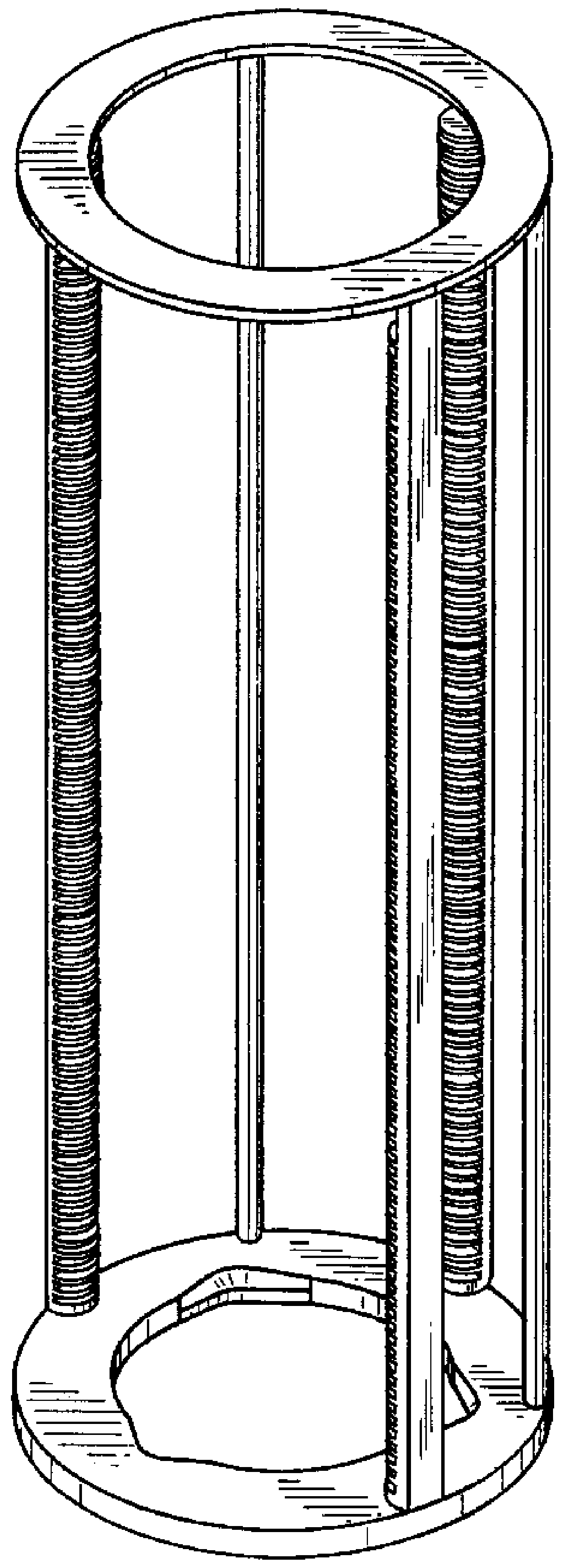

FIG. 1

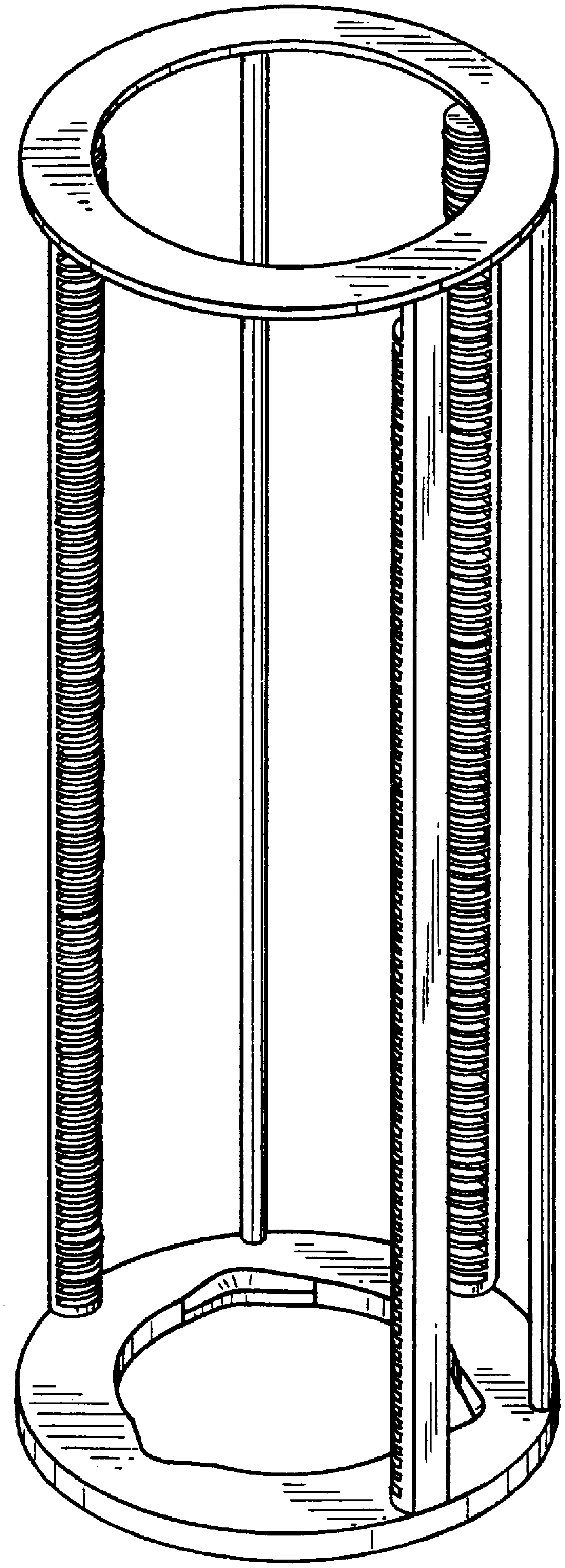

FIG. 2

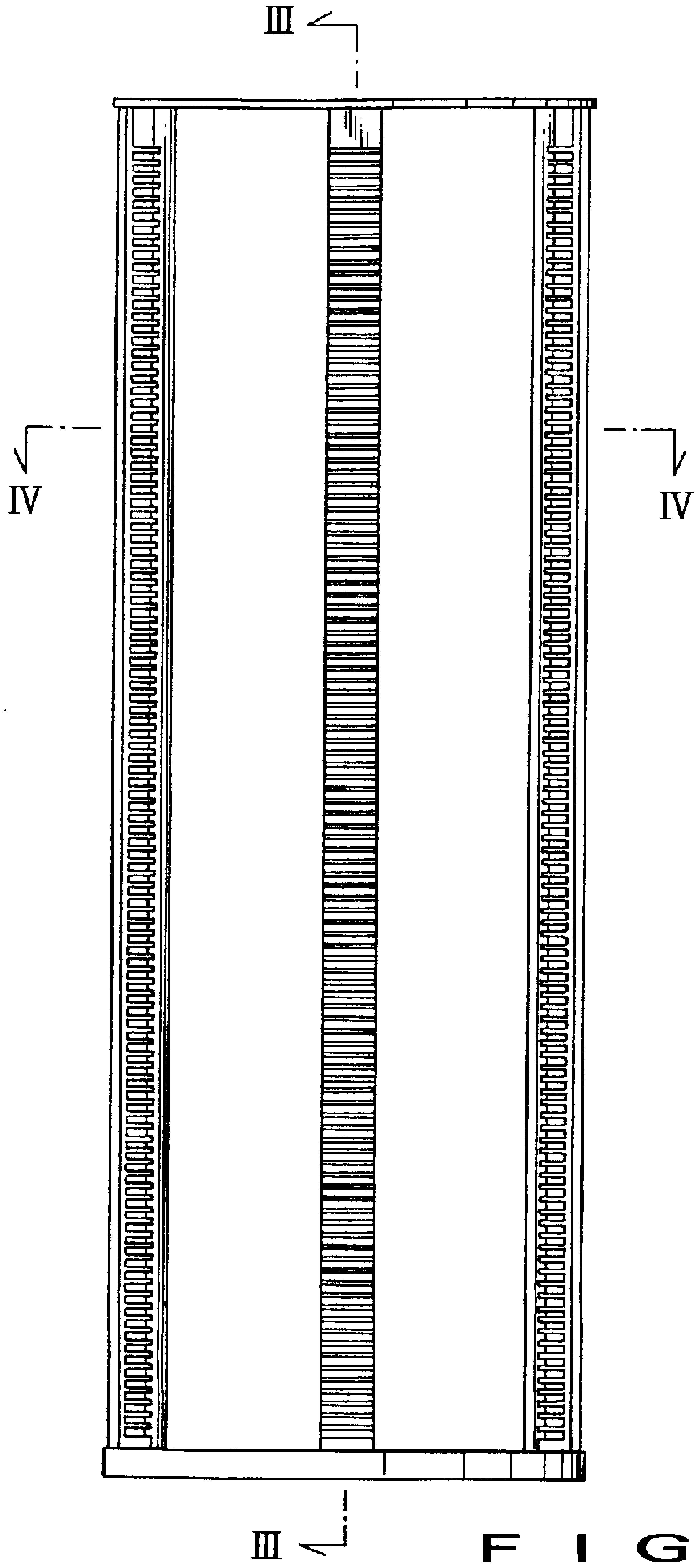

FIG. 3

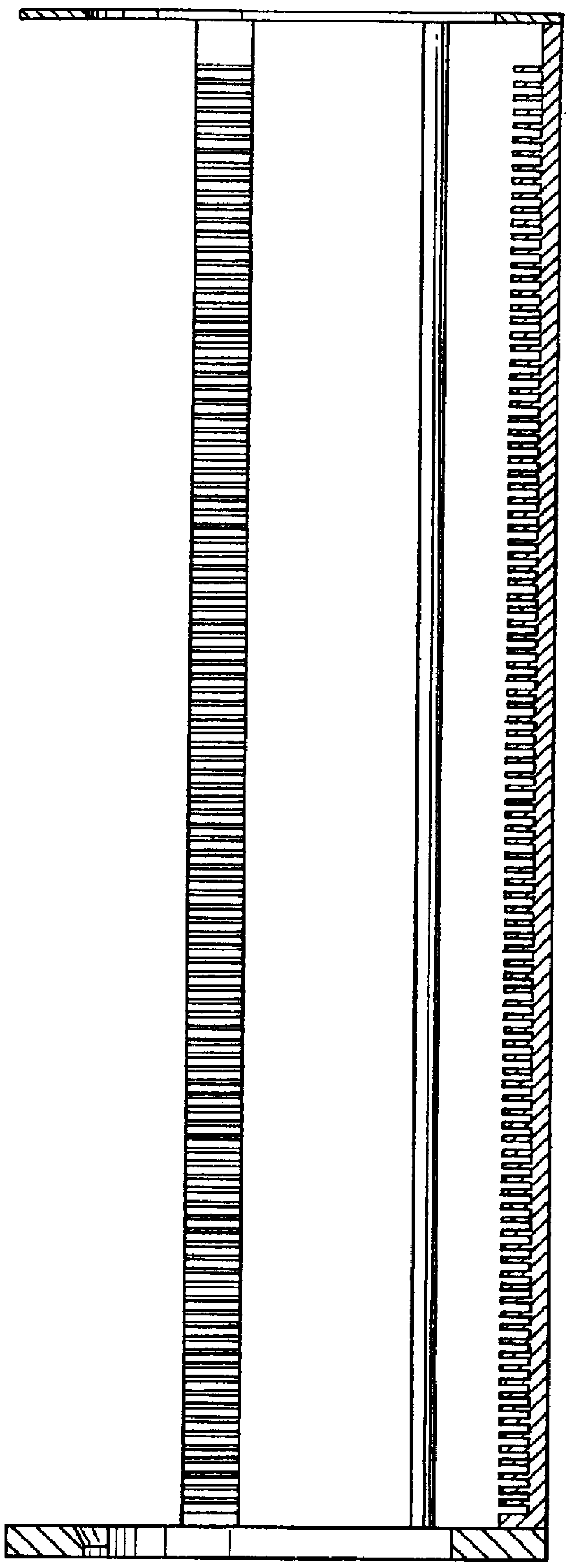

FIG. 4

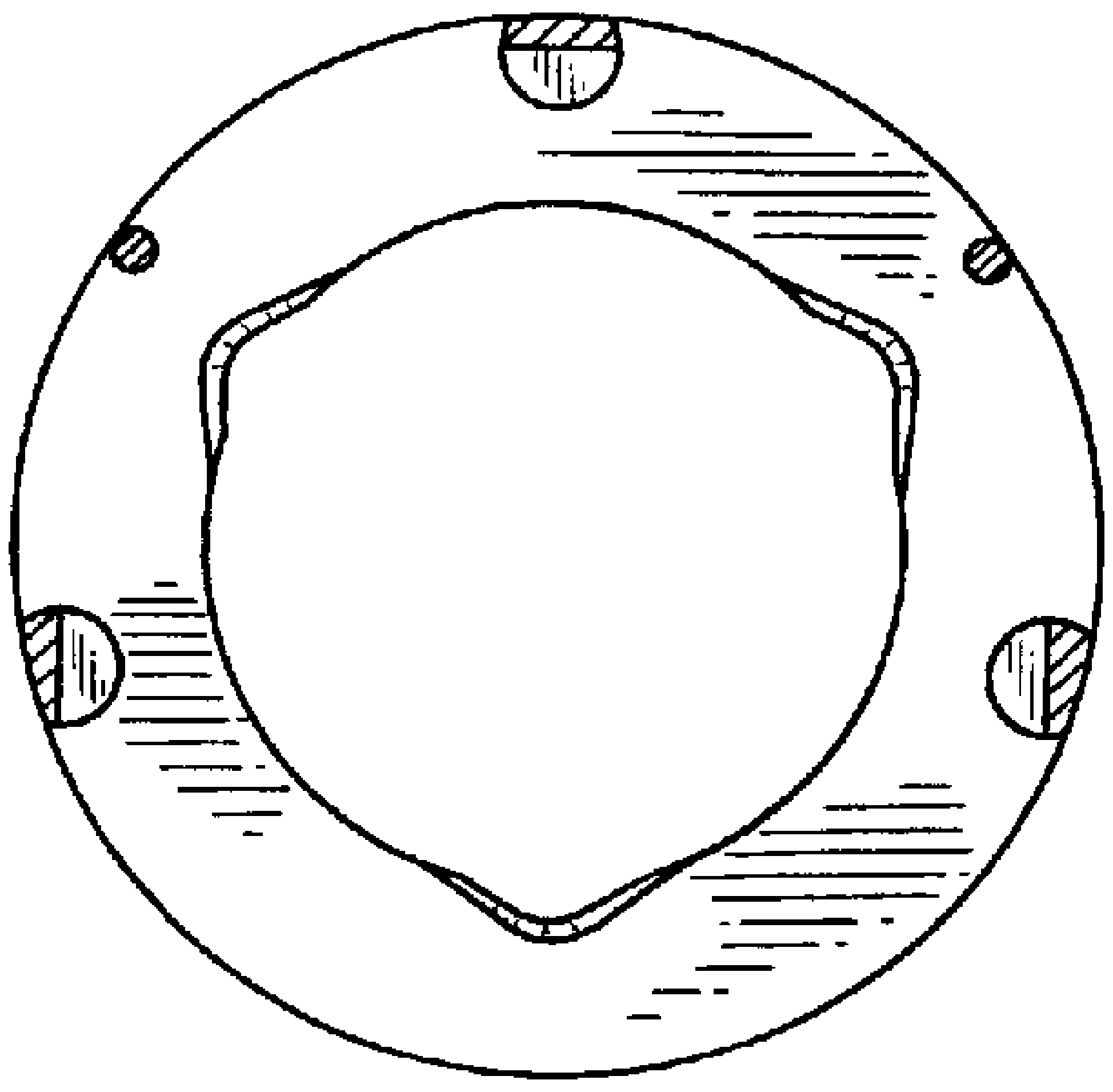

FIG. 5

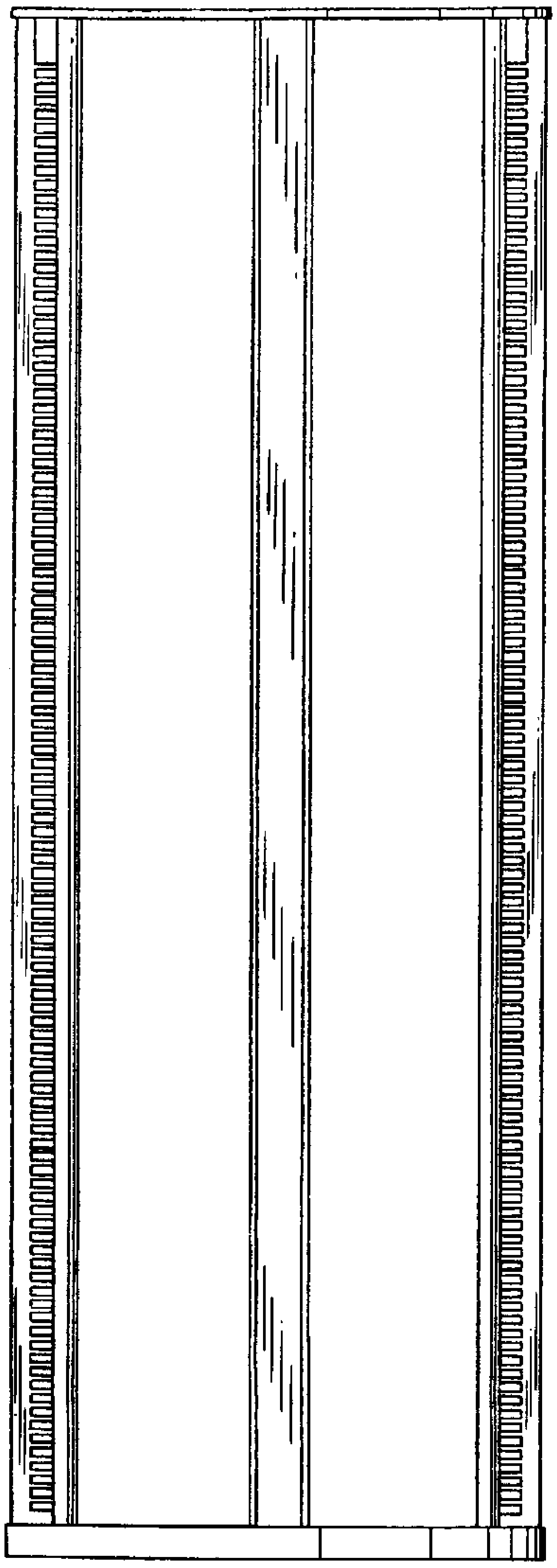

FIG. 6

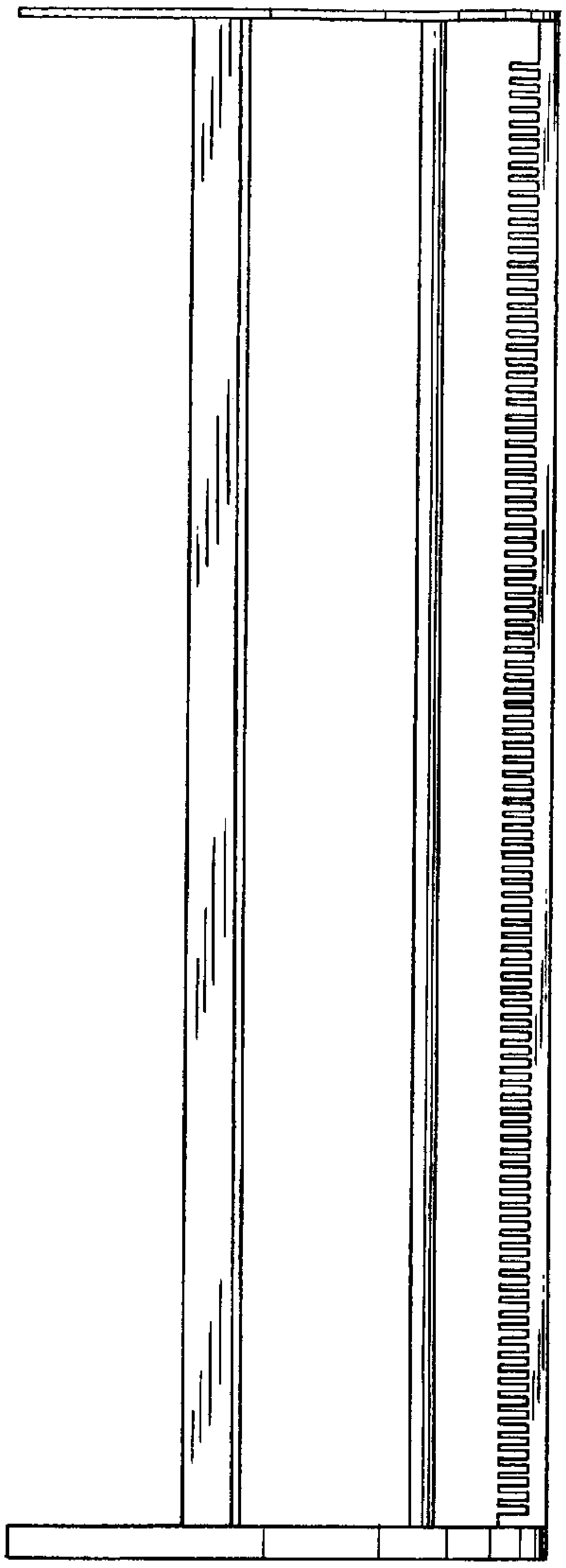

FIG. 7

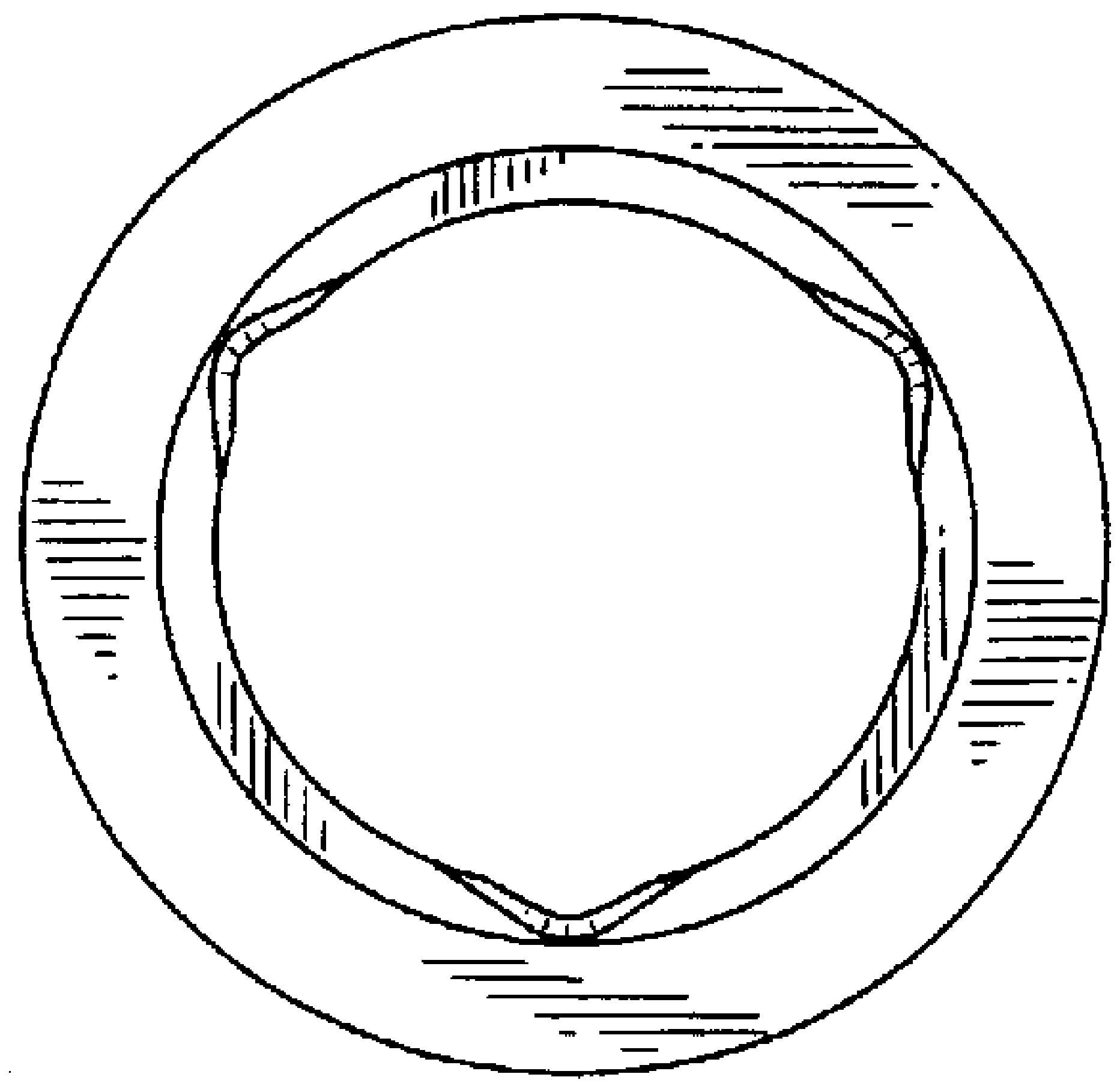

FIG. 8