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United States Patent [19]

Shimazu

[11] **Patent Number: Des. 407,696**

[45] **Date of Patent: **Apr. 6, 1999**

[54] **INNER TUBE FOR USE IN A SEMICONDUCTOR WAFER HEAT PROCESSING APPARATUS**

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[73] Assignee: **Tokyo Electron Limited**, Tokyo-to, Japan

[**] Term: **14 Years**

[21] Appl. No.: **82,977**

[22] Filed: **Feb. 2, 1998**

[30] **Foreign Application Priority Data**

Aug. 20, 1997 [JP] Japan 9-65096

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; D15/144, D15/144.1, 199; 414/935–941, 217, 147; 437/247, 946; D23/259, 262, 266

[56] **References Cited**

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[57] **CLAIM**

I claim the ornamental design for inner tube for use in a semiconductor wafer heat processing apparatus, as shown and described.

DESCRIPTION

FIG. **1** a perspective view of an inner tube for use in a semiconductor wafer heat processing apparatus;

FIG. **2** a front elevational view thereof;

FIG. **3** a top plan view thereof; and,

FIG. **4** a cross-sectional view taken along line **IV—IV** in FIG. **3**.

1 Claim, 2 Drawing Sheets

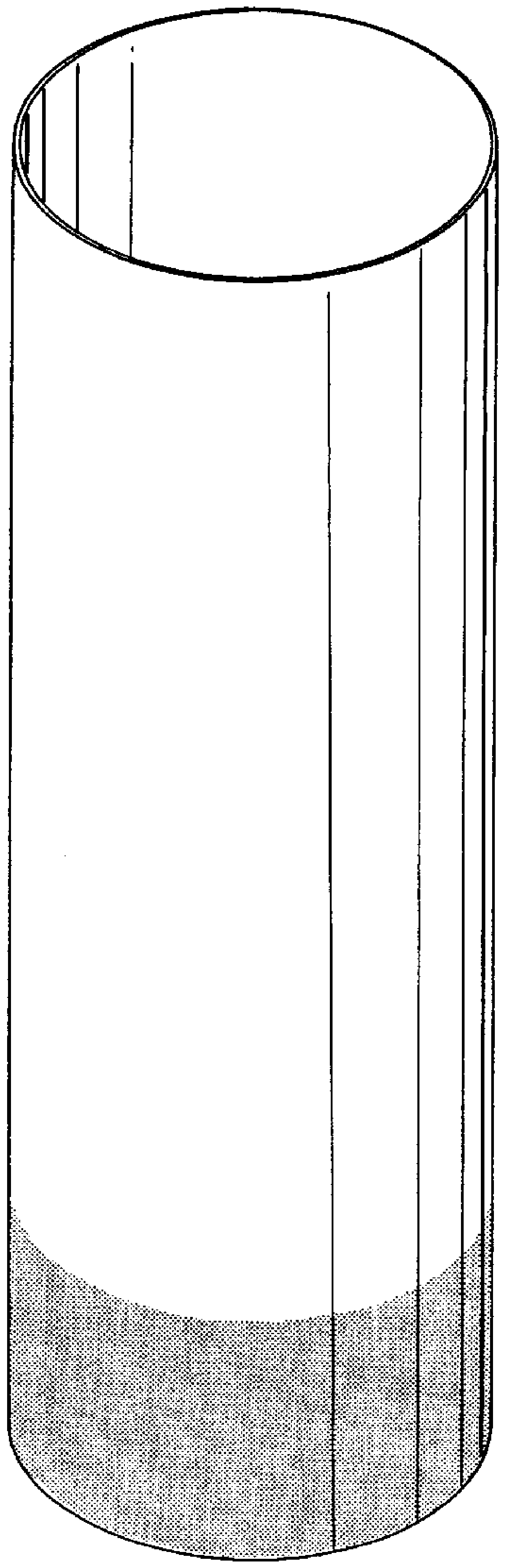

FIG. 1

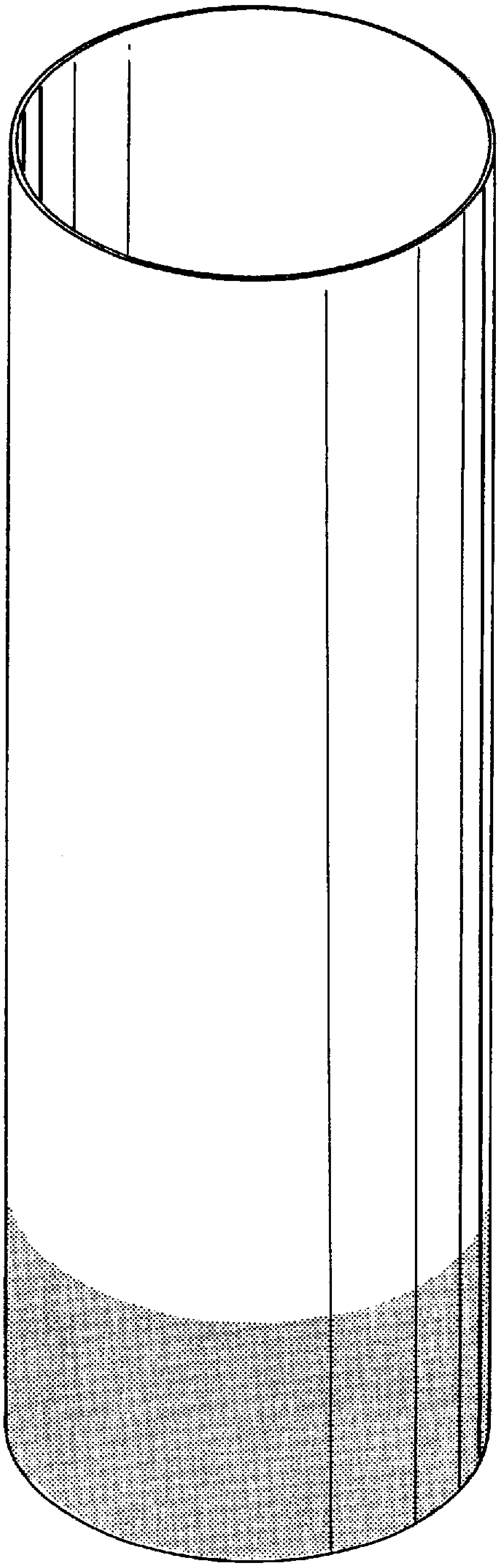

FIG. 2

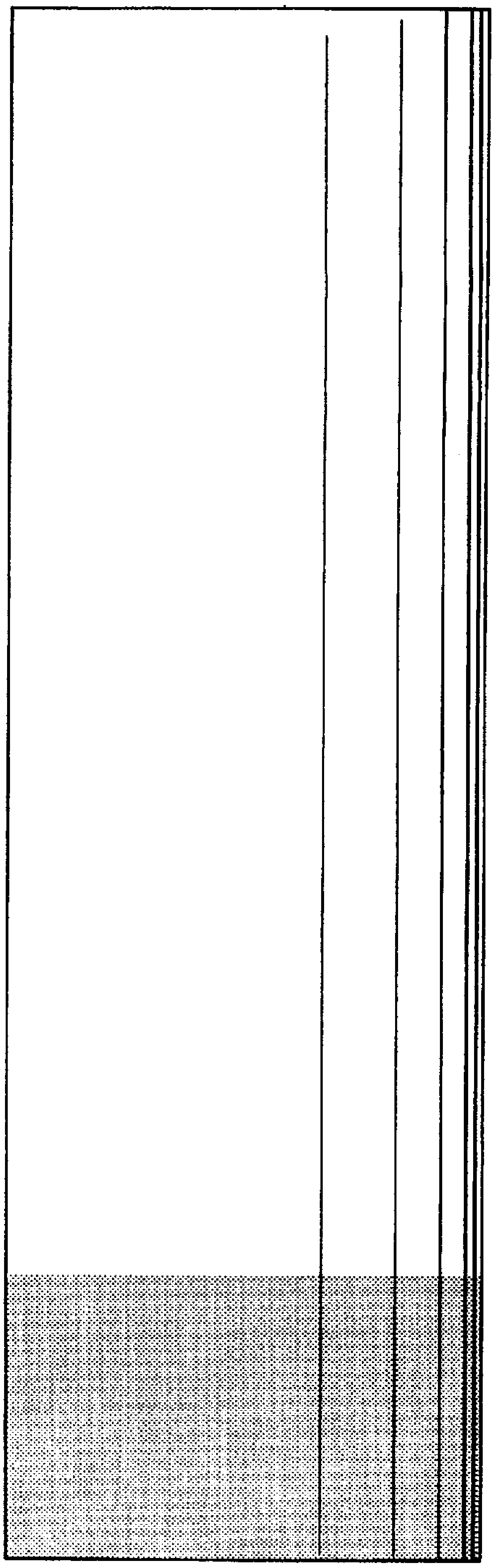

FIG. 3

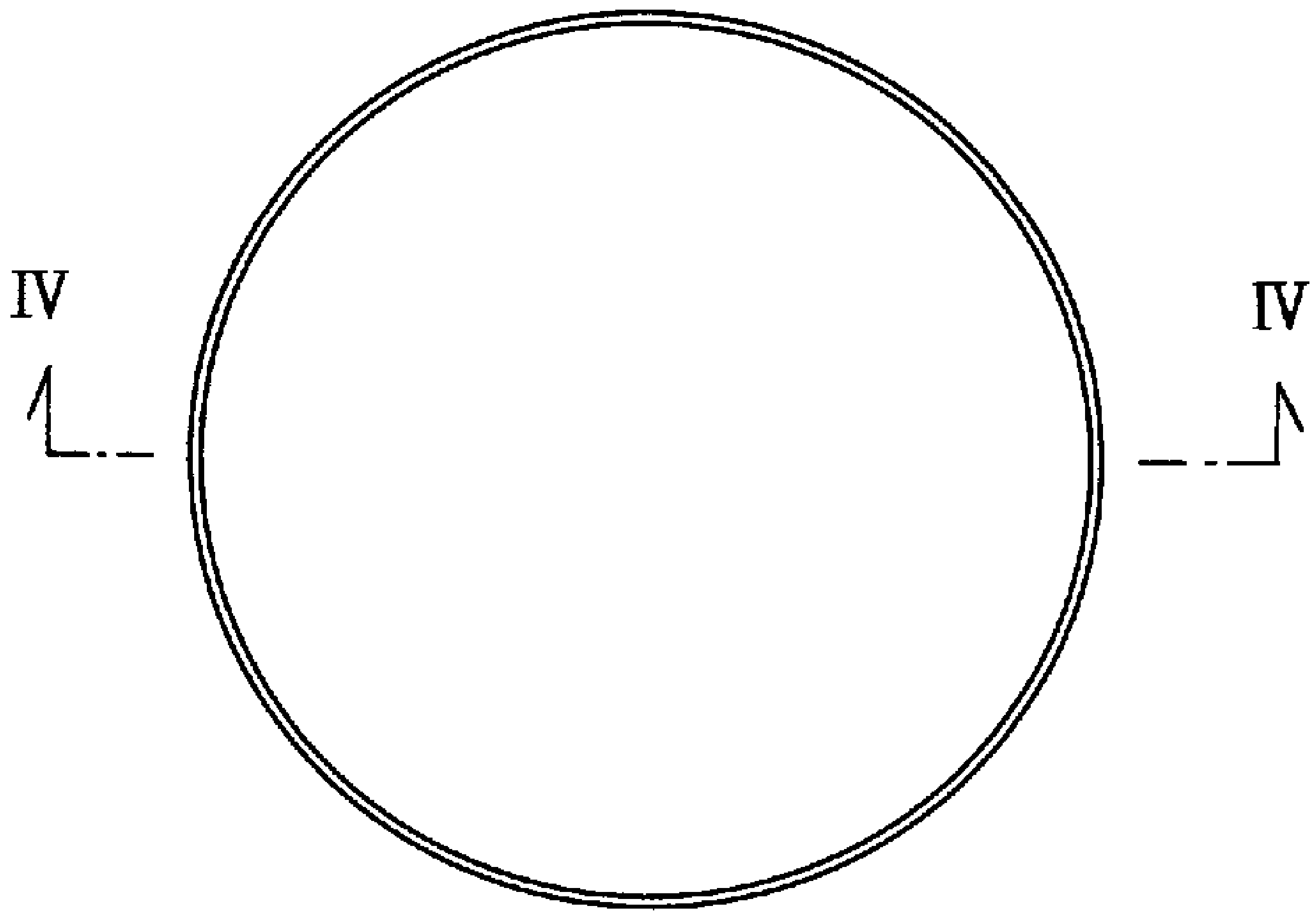

FIG. 4