US00D407383S

United States Patent [19]

Kataoka et al.

[11] **Patent Number: Des. 407,383**

[45] **Date of Patent: **Mar. 30, 1999**

[54] **CONNECTOR FOR PRINTED CIRCUIT BOARDS**

[75] Inventors: **Yasuhiro Kataoka**, Yokohama; **Terumi Nakashima**, Takatsuki; **Narihiko Hashimoto**, Nagoya, all of Japan

[73] Assignees: **Sony Corporation**, Tokyo; **Japan Solderless Terminal Mfg. Co., Ltd.**, Osaka, both of Japan

[**] Term: **14 Years**

[21] Appl. No.: **90,452**

[22] Filed: **Jul. 9, 1998**

Related U.S. Application Data

[62] Division of Ser. No. 71,611, Jun. 3, 1997.

[30] **Foreign Application Priority Data**

Dec. 11, 1996 [JP] Japan 8-37849
Dec. 26, 1996 [JP] Japan 8-36612
Apr. 1, 1997 [JP] Japan 9-50068

[51] **LOC (6) Cl.** **13-03**
[52] **U.S. Cl.** **D13/182**
[58] **Field of Search** D13/125, 182; 174/52.1, 52.4; 439/55, 70; 361/718, 820

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 317,592 6/1991 Yoshizawa .
D. 357,901 5/1995 Horman .
D. 359,028 6/1995 Siegel et al. .
5,089,929 2/1992 Hilland .

FOREIGN PATENT DOCUMENTS

898318 5/1994 Japan .
898319 5/1994 Japan .
908880 10/1994 Japan .
908881 10/1994 Japan .

OTHER PUBLICATIONS

"Electronic Parts Catalog", Electronic Industries Association of Japan, No. 58, pp. 88–13, Oct. 4, 1994 (1995 Edition).

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[57] **CLAIM**

We claim the ornamental design for a connector for printed circuit boards, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a connector for printed circuit boards showing our new design, while the rear view corresponds to the front view;

FIG. **2** is a top view of said connector for printed circuit boards;

FIG. **3** is a bottom view of said connector for printed circuit boards;

FIG. **4** is a left side view of said connector for printed circuit boards, while the right side view corresponds to the left side view;

FIG. **5** is a sectional view along the line V—V in FIG. **1**; and,

FIG. **6** is a sectional view along the line V—V in FIG. **1**, wherein said connector for printed circuit boards is shown in a condition connecting two circuit boards, which are drawn in broken lines for illustrative purposes only. The circuit boards drawn in broken lines form no part of the claimed design.

1 Claim, 3 Drawing Sheets

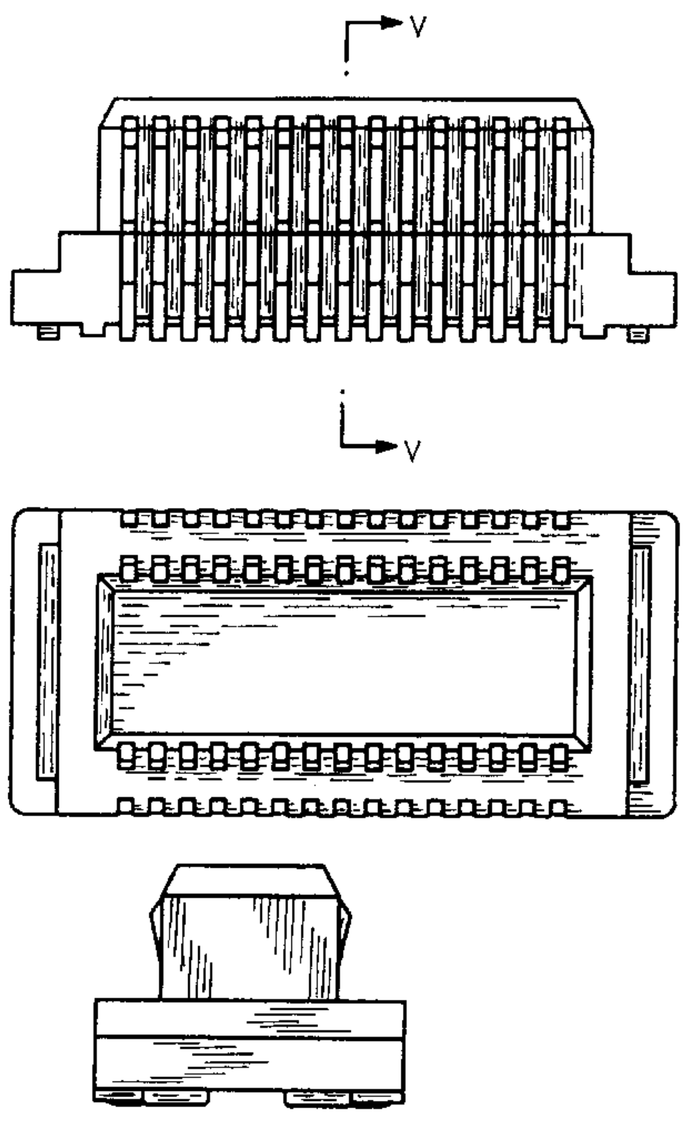


FIG. 1

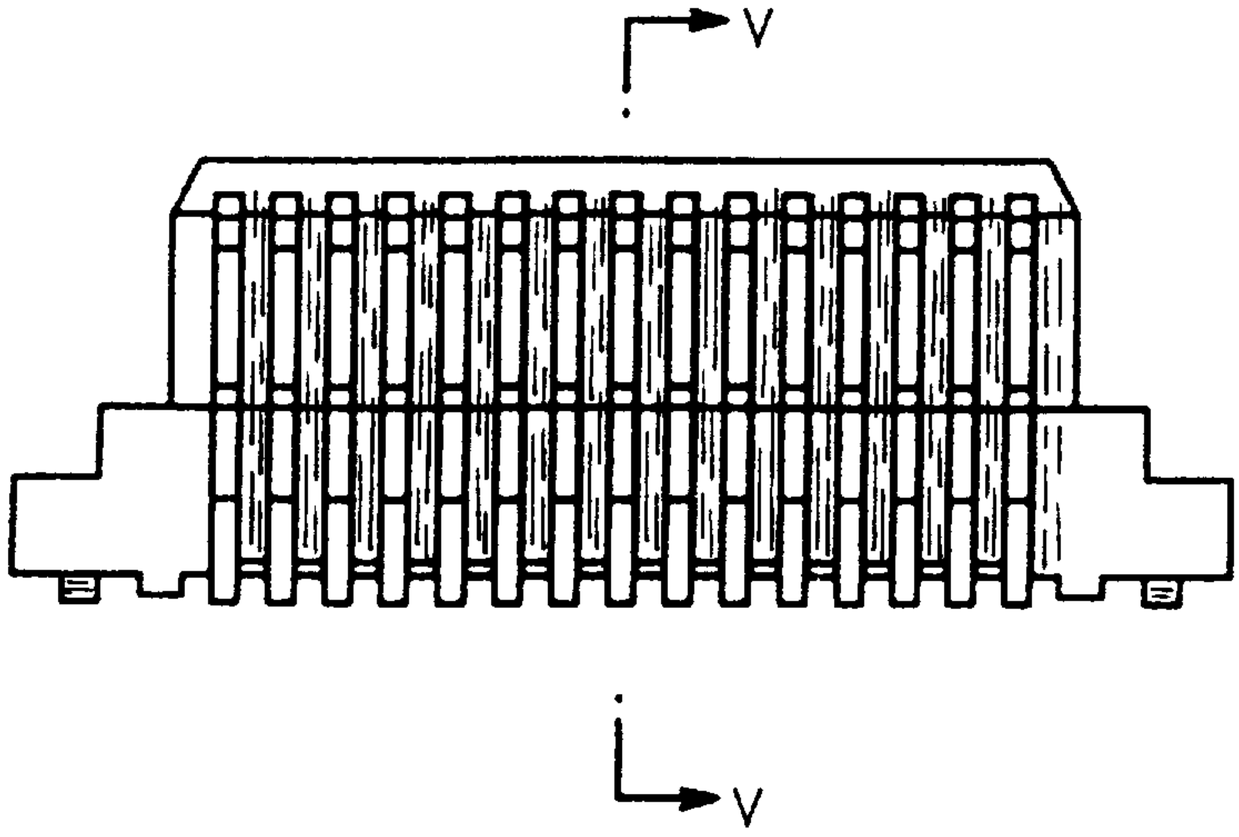


FIG. 2

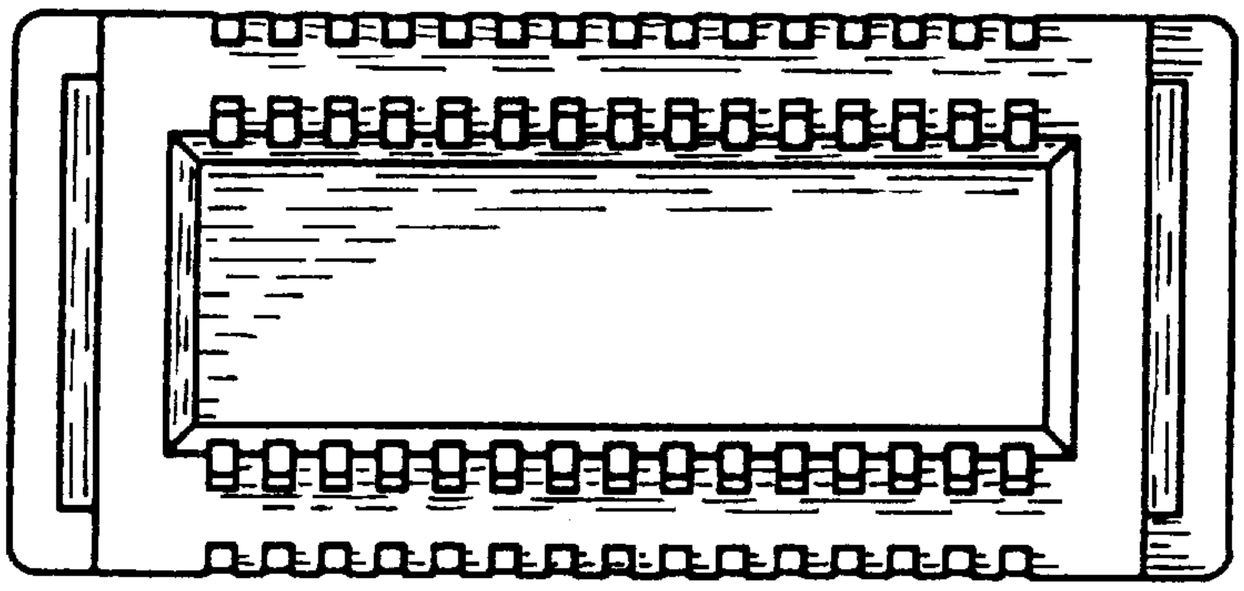


FIG. 3

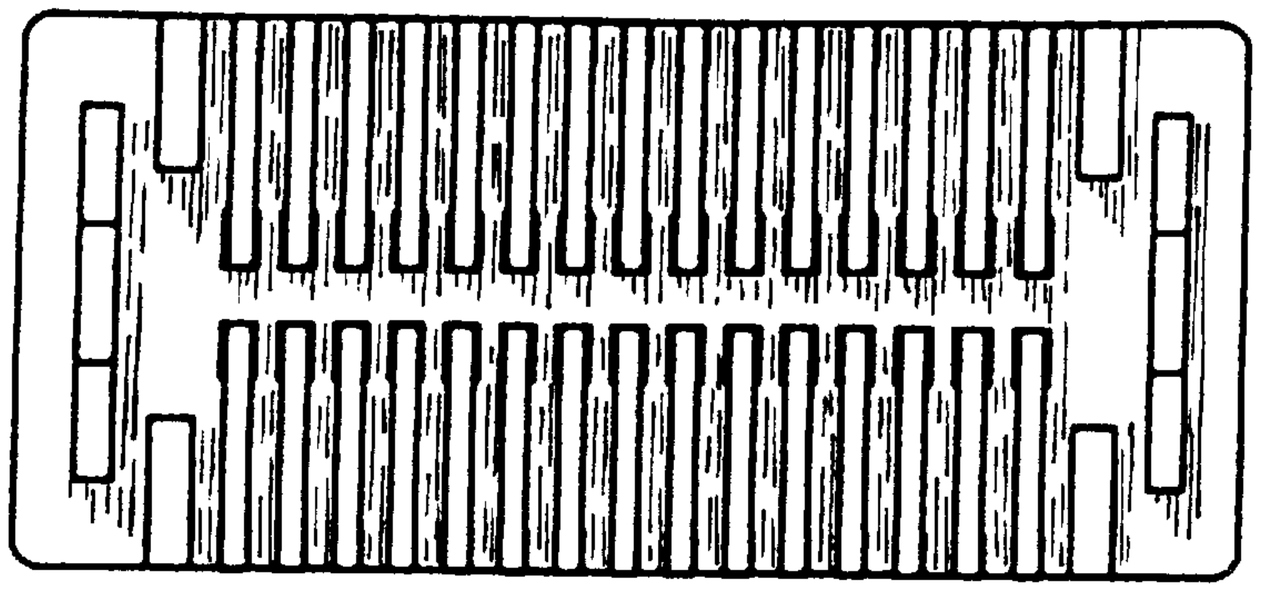


FIG. 4

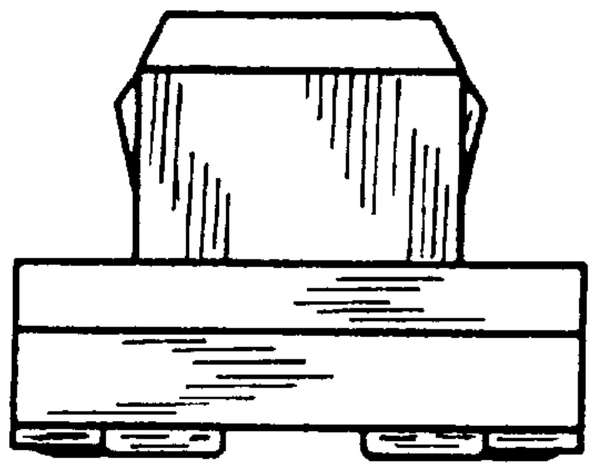


FIG. 5

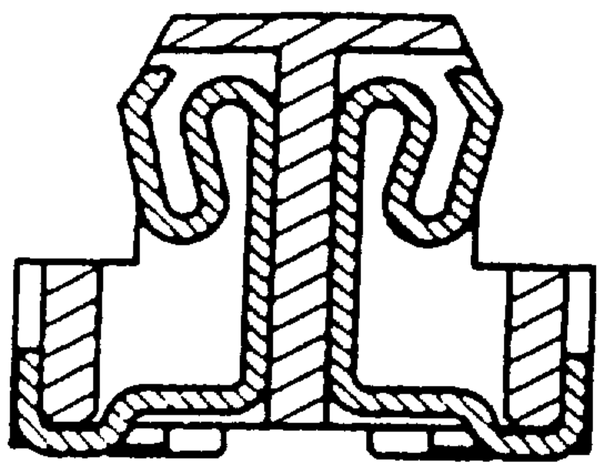
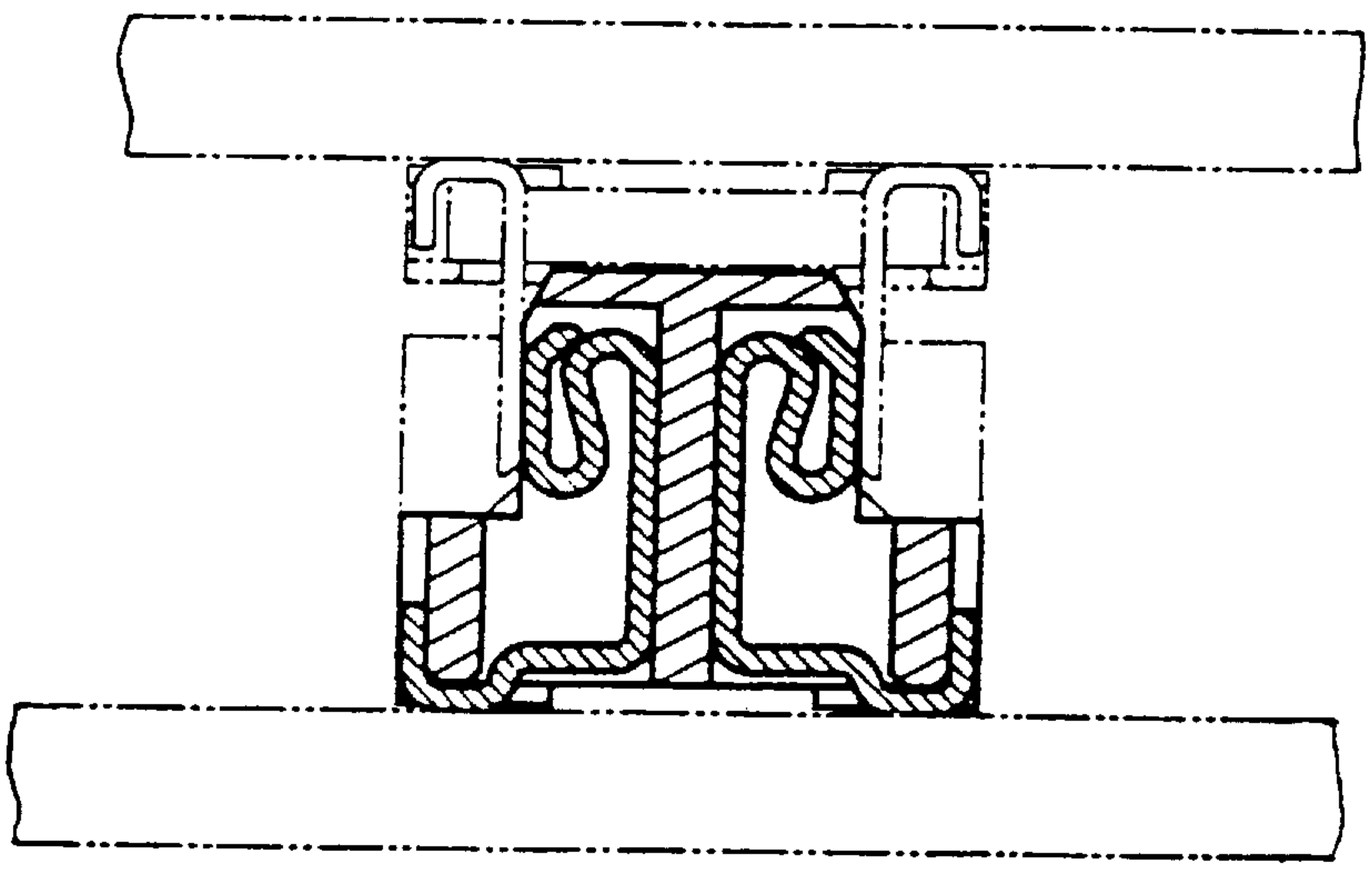


FIG. 6



UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : **Des. 407,383**

DATED : **Mar. 30, 1999**

INVENTOR(S) : **Kataoka et al.**

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item [30]:

Foreign Application Priority Data, please replace the second line to read:

--Dec. 26, 1996 [JP] .....8-39612--.

Signed and Sealed this

Twentieth Day of July, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks