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United States Patent [19]

Ishii

[11] **Patent Number: Des. 404,372**

[45] **Date of Patent: **Jan. 19, 1999**

[54] **RING FOR USE IN A SEMICONDUCTOR WAFER HEAT PROCESSING APPARATUS**

[75] Inventor: **Katsutoshi Ishii**, Shiroyama-machi, Japan

[73] Assignee: **Tokyo Electron Limited**, Tokyo-To, Japan

[**] Term: **14 Years**

[21] Appl. No.: **83,715**

[22] Filed: **Feb. 12, 1998**

[30] **Foreign Application Priority Data**

Aug. 20, 1997 [JP] Japan 9-65106

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; D15/144, D15/144.1, 199; 414/935–941, 217, 147; 437/247, 946

[56] **References Cited**

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Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—Ladas & Parry

[57] **CLAIM**

I claim the ornamental design for a ring for use in a semiconductor wafer heat processing apparatus, as shown and described.

DESCRIPTION

FIG. **1** a perspective view of a ring for use in a semiconductor wafer heat processing apparatus;

FIG. **2** a top plan view thereof;

FIG. **3** a front elevational view thereof;

FIG. **4** a bottom plan view thereof;

FIG. **5** a right side view thereof;

FIG. **6** a rear elevational view thereof; and,

FIG. **7** a cross-sectional view taken along line VII—VII in FIG. **3**.

1 Claim, 2 Drawing Sheets

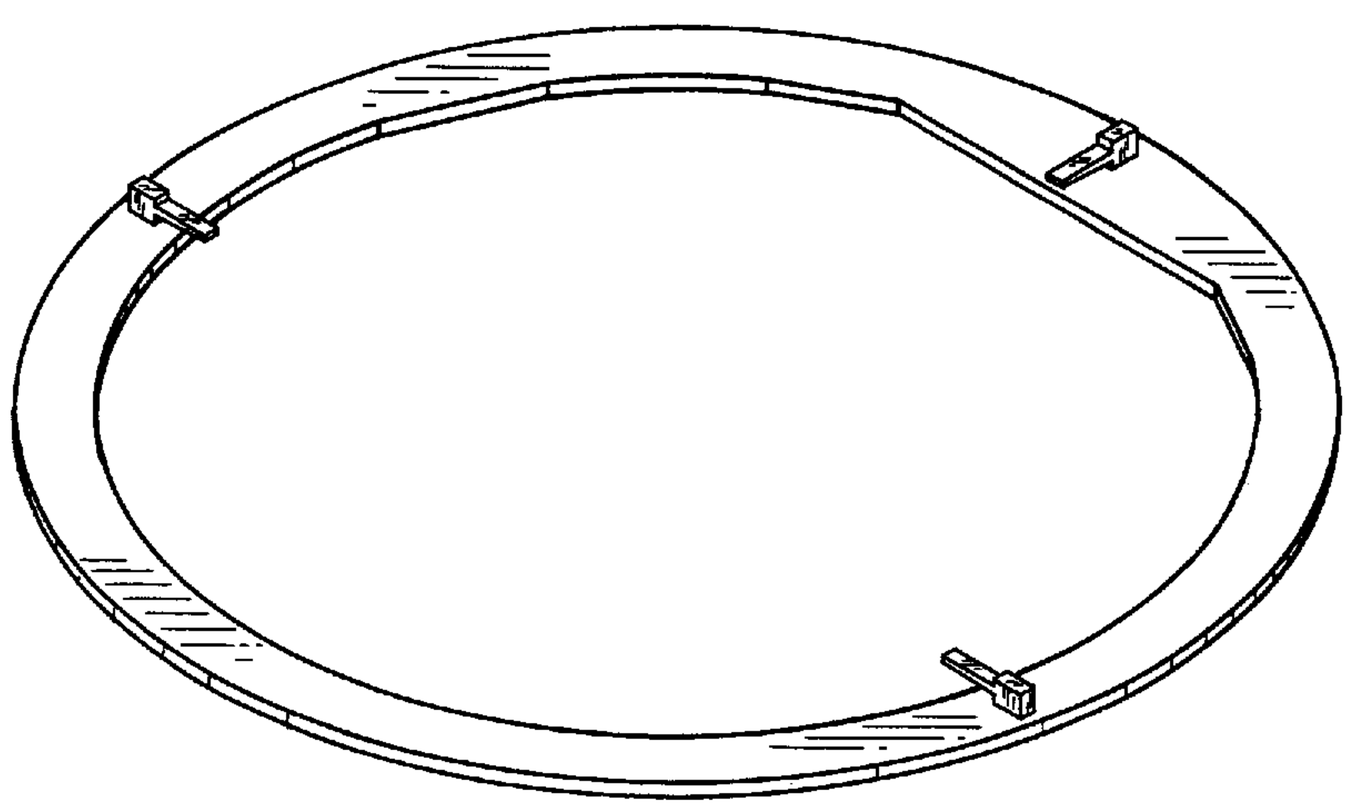

FIG. 1

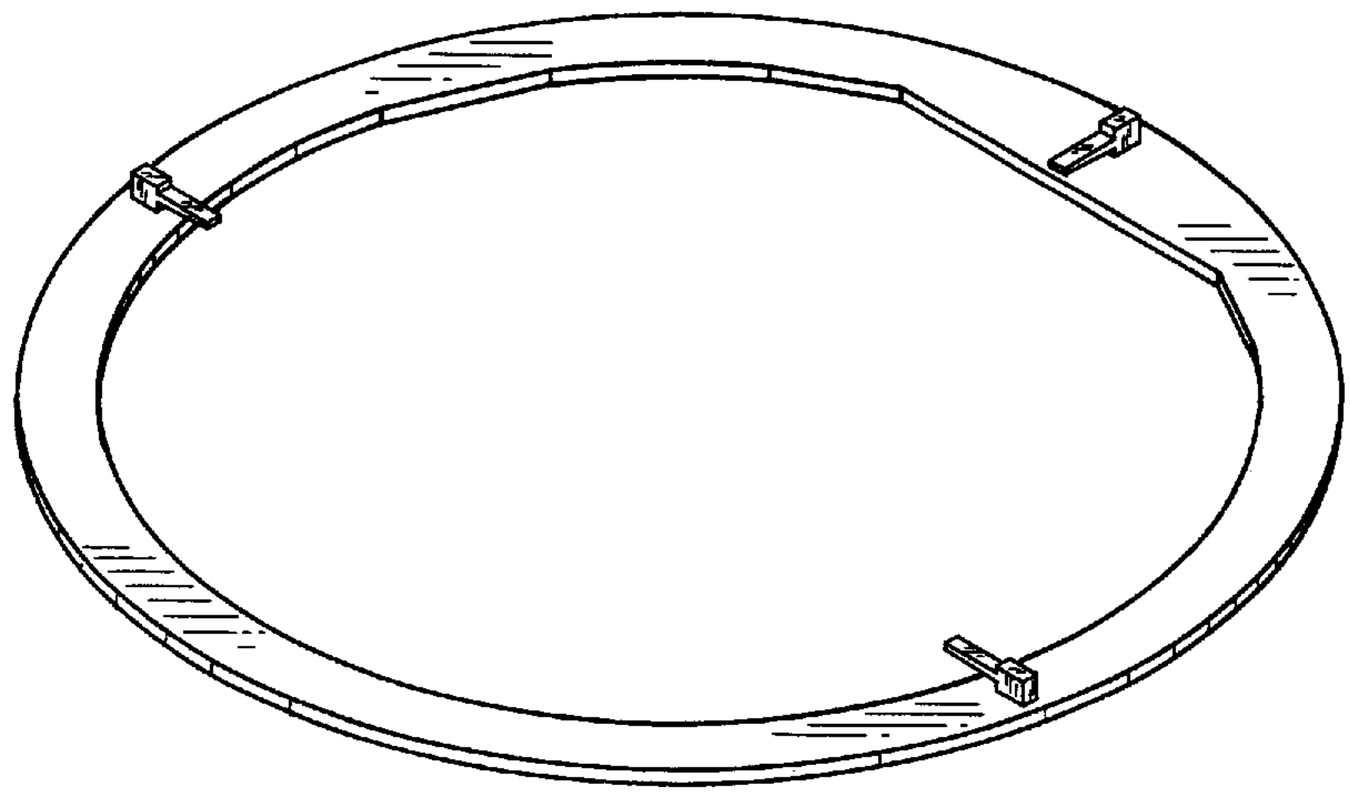

FIG. 2

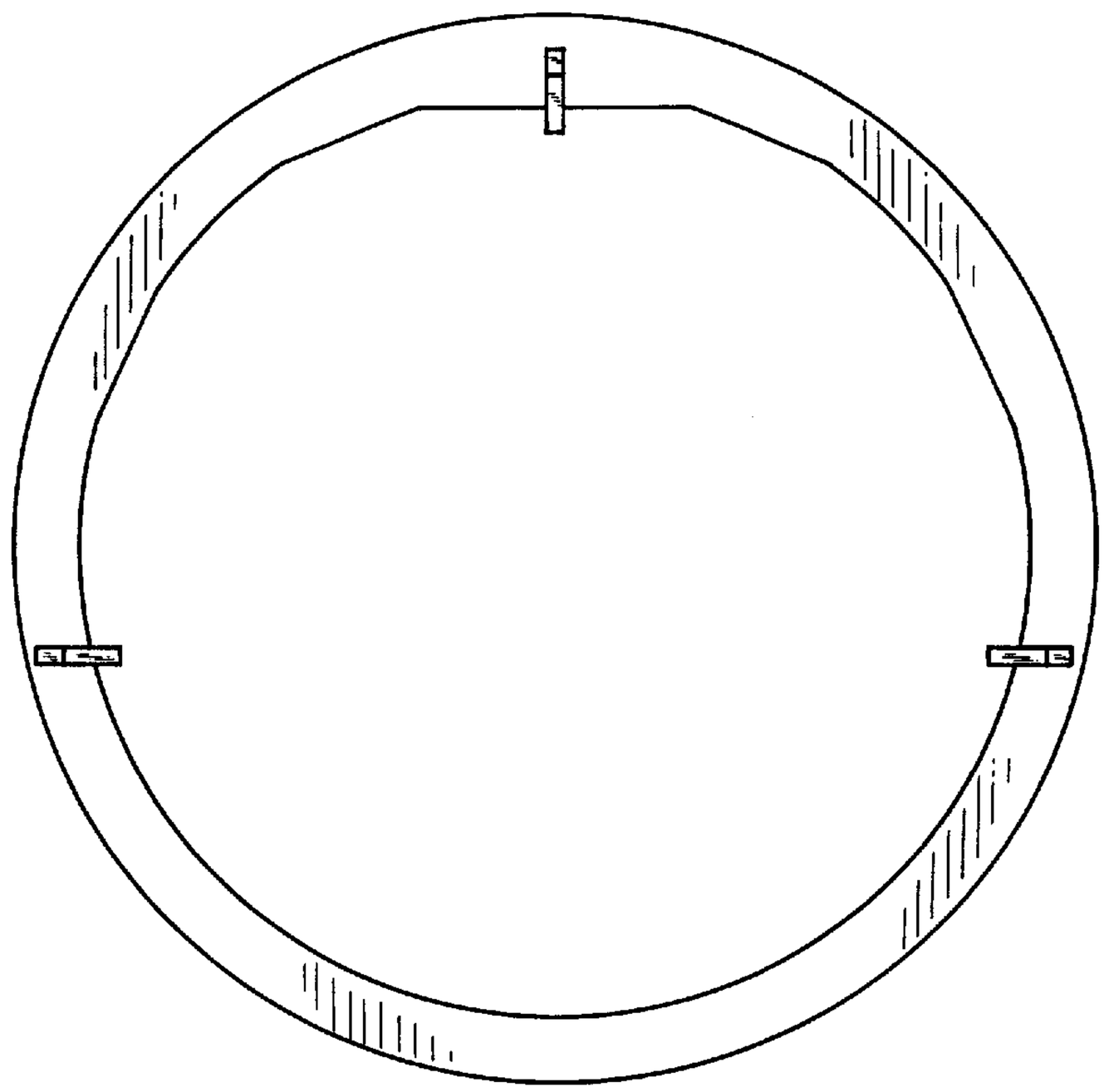

FIG. 3

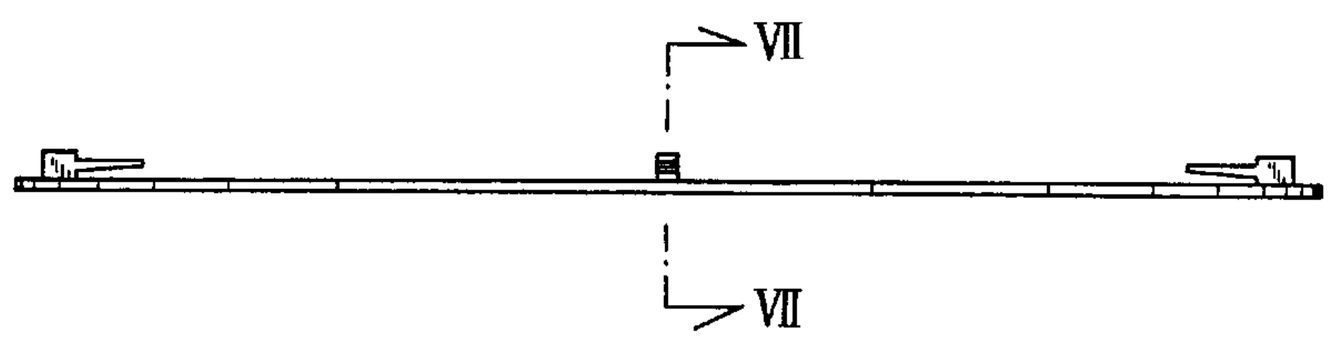

FIG. 4

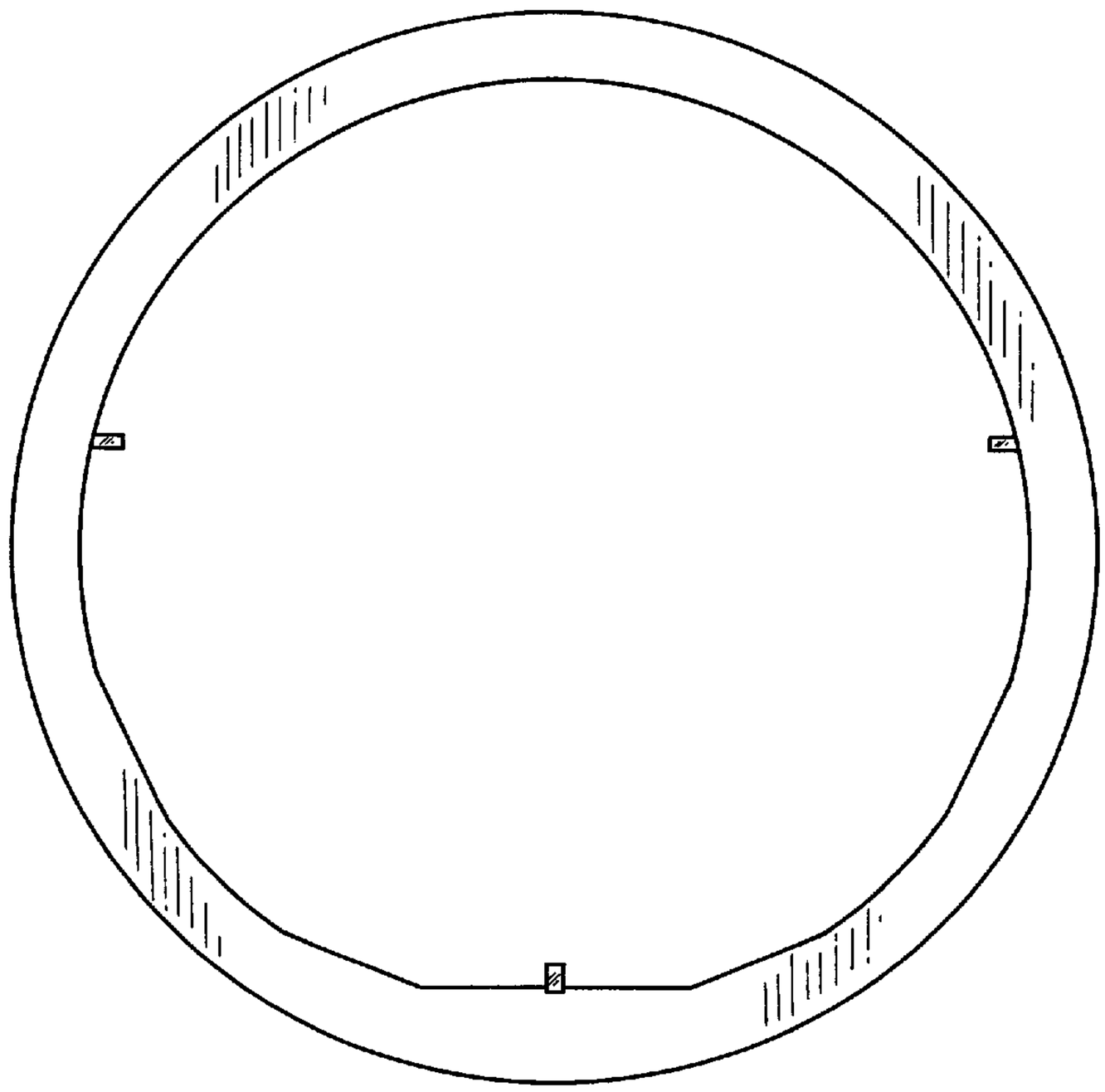

FIG. 5

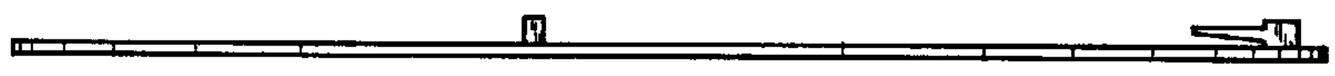

FIG. 6
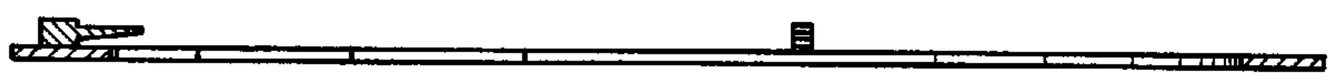
FIG. 7