



US00D404369S

United States Patent [19]

Kawachi

[11] **Patent Number: Des. 404,369**

[45] **Date of Patent: **Jan. 19, 1999**

[54] **MANIFOLD COVER FOR USE IN A SEMICONDUCTOR WAFER HEAT PROCESSING APPARATUS**

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5,320,218 6/1994 Yamashita et al. 414/935 X
5,752,796 5/1998 Muka 414/935 X

[75] Inventor: **Satoshi Kawachi**, Shiroyama-machi, Japan

Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—Ladas & Parry

[73] Assignee: **Tokyo Electron Limited**, Tokyo-to, Japan

[57] **CLAIM**

[**] Term: **14 Years**

I claim the ornamental design for a manifold cover for use in a semiconductor wafer heat processing apparatus, as shown and described.

[21] Appl. No.: **82,981**

DESCRIPTION

[22] Filed: **Feb. 2, 1998**

[30] **Foreign Application Priority Data**

Aug. 20, 1997 [JP] Japan 9-65097

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; D15/144,
D15/144.1, 199; 414/935-941, 217, 147;
437/247, 946

FIG. 1 a perspective view of a cover manifold cover for use in a semiconductor wafer heat processing apparatus;
FIG. 2 a front elevational view thereof;
FIG. 3 a rear elevational view thereof;
FIG. 4 a top plan view thereof;
FIG. 5 a bottom plan view thereof;
FIG. 6 a right side view thereof;
FIG. 7 a left side view thereof; and,
FIG. 8 a cross-sectional view taken along line VIII-VIII in FIG. 2.

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,857,689 8/1989 Lee 414/935 X

1 Claim, 2 Drawing Sheets

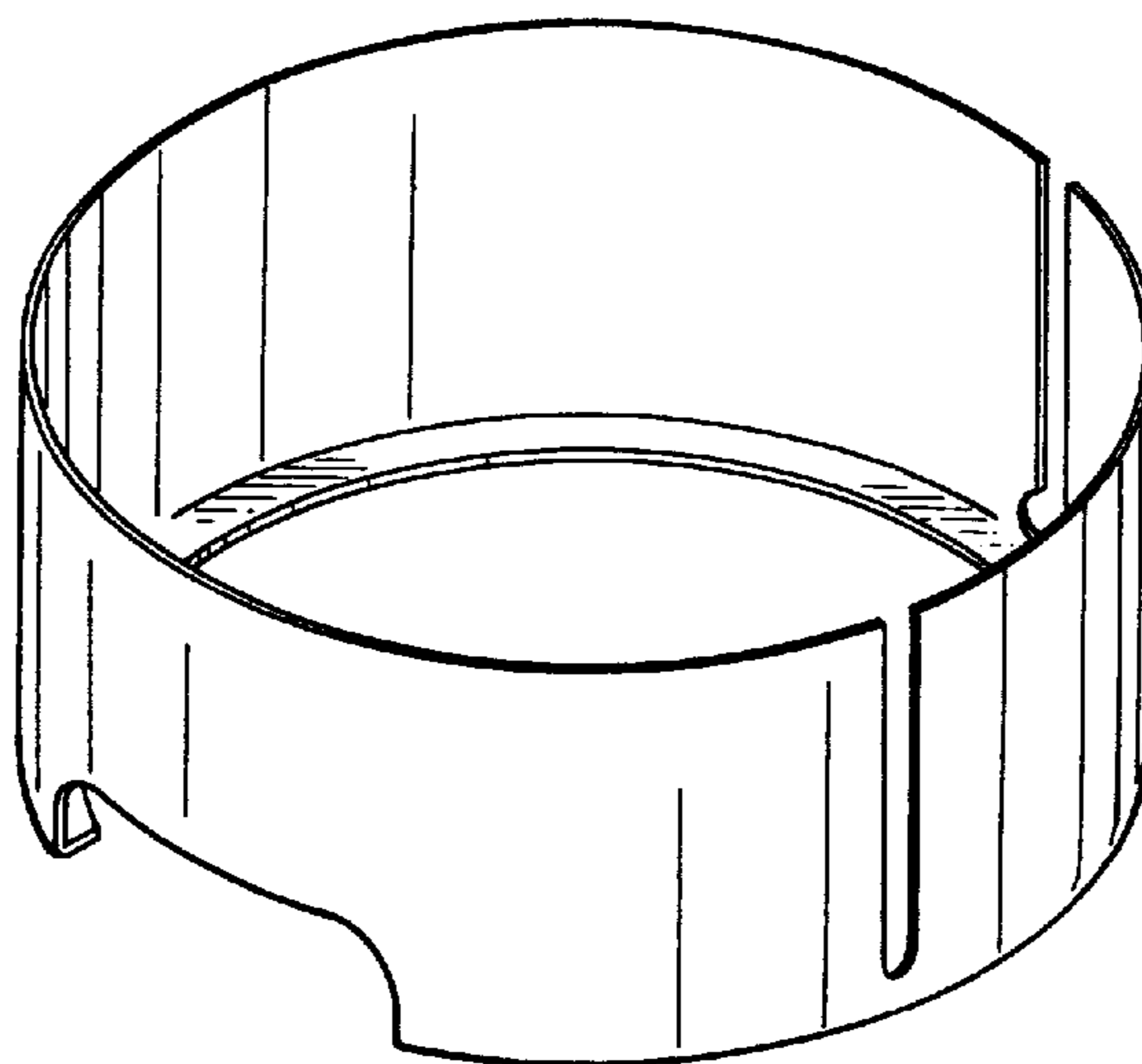


FIG. 1

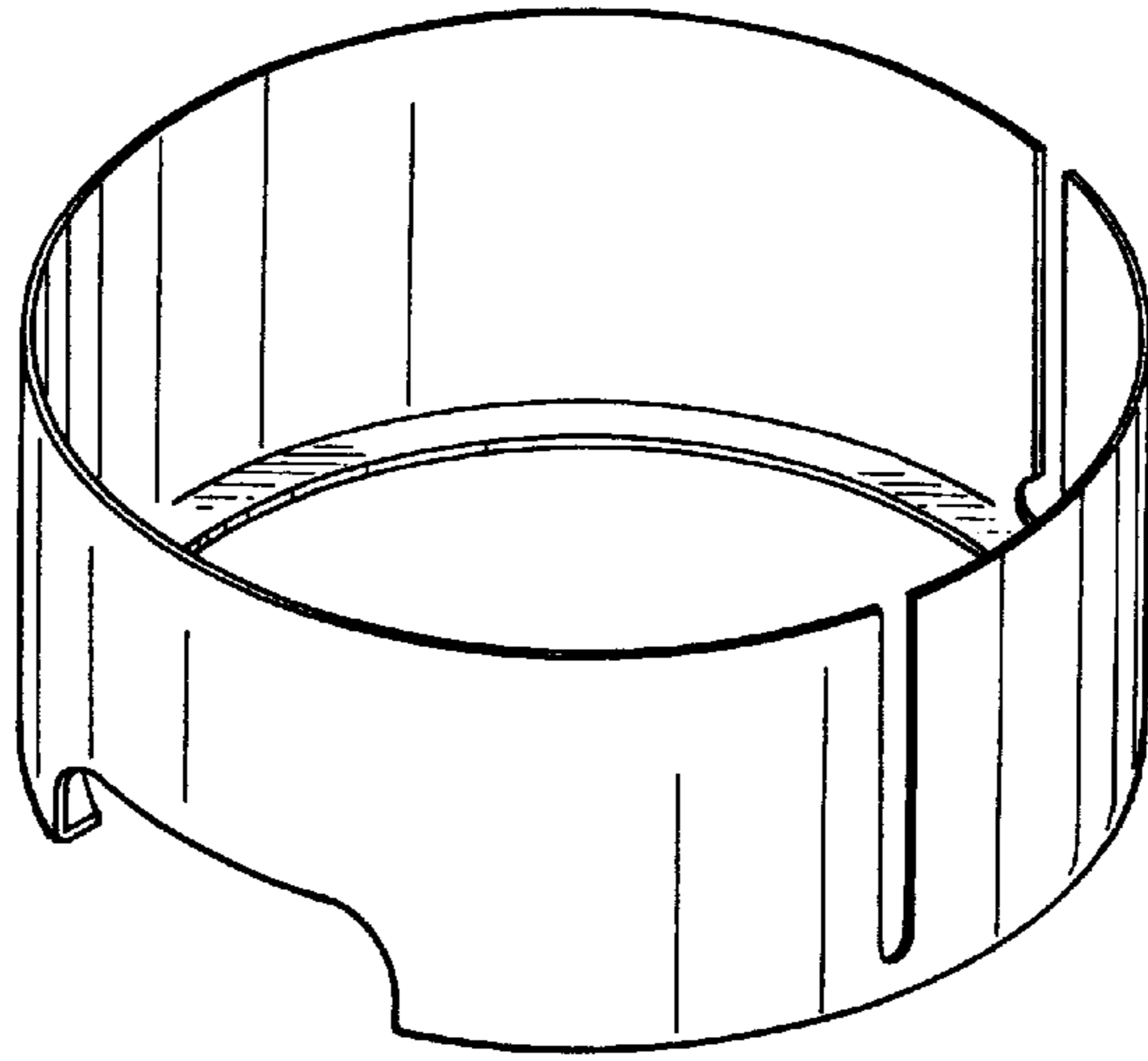


FIG. 2

VIII ←

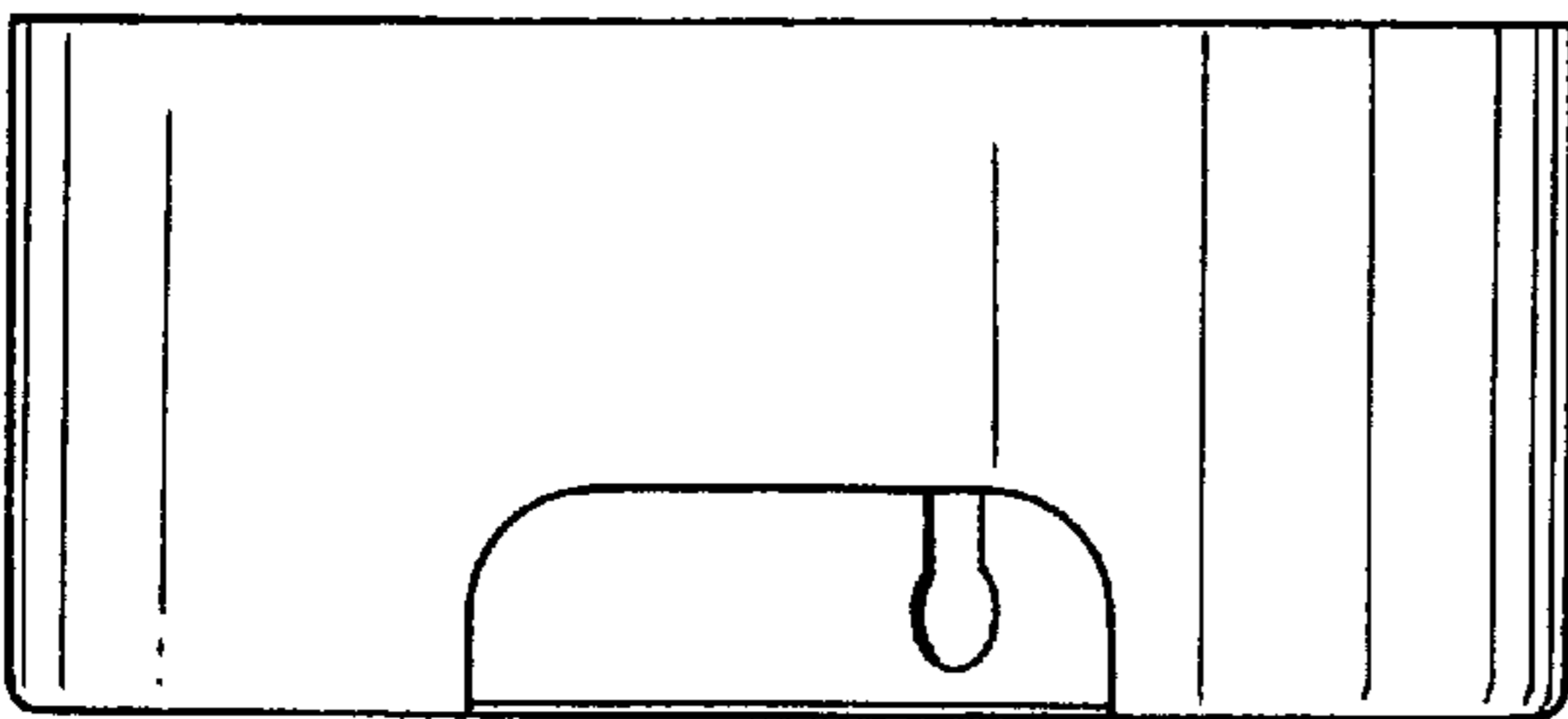
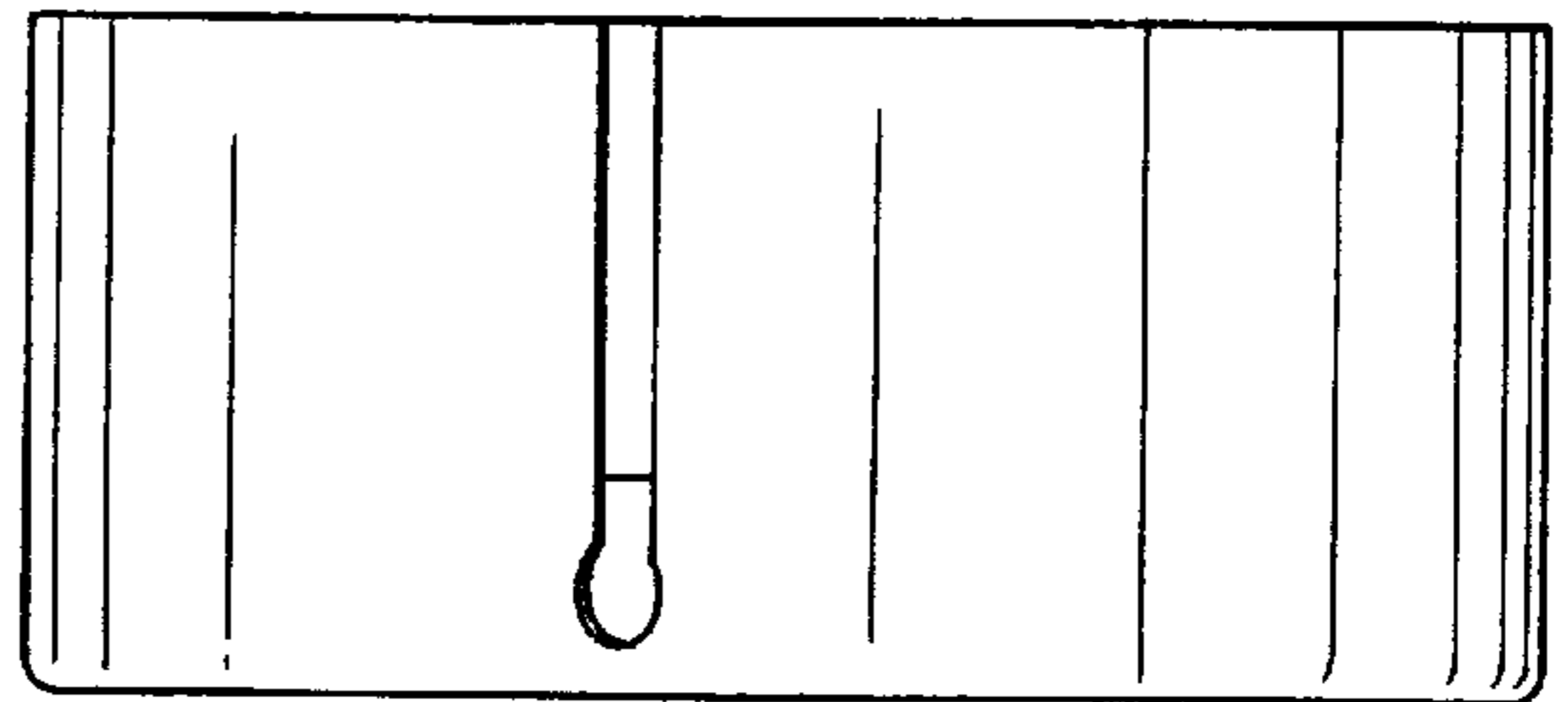


FIG. 3



VIII ←

FIG. 4

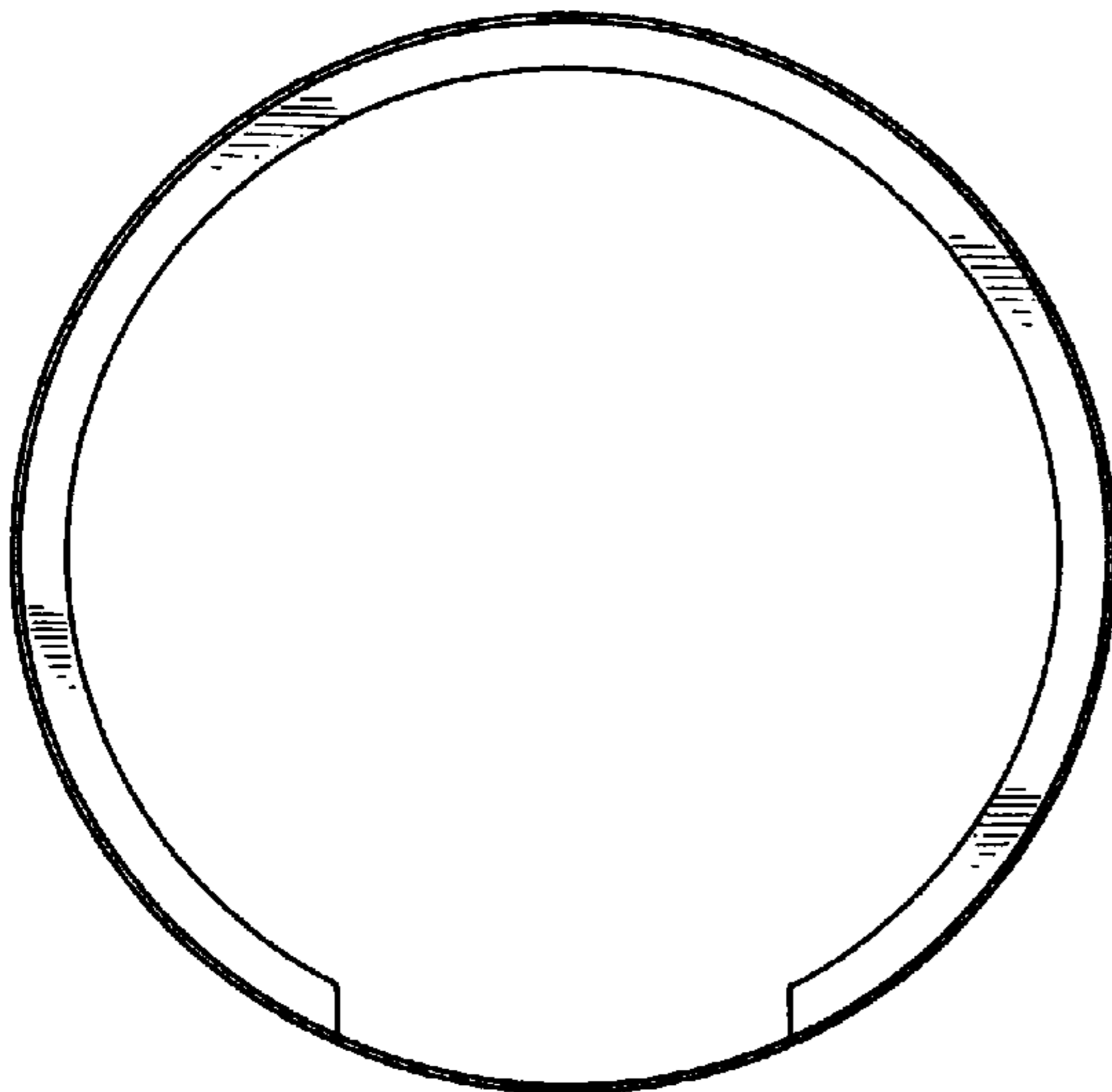


FIG. 5

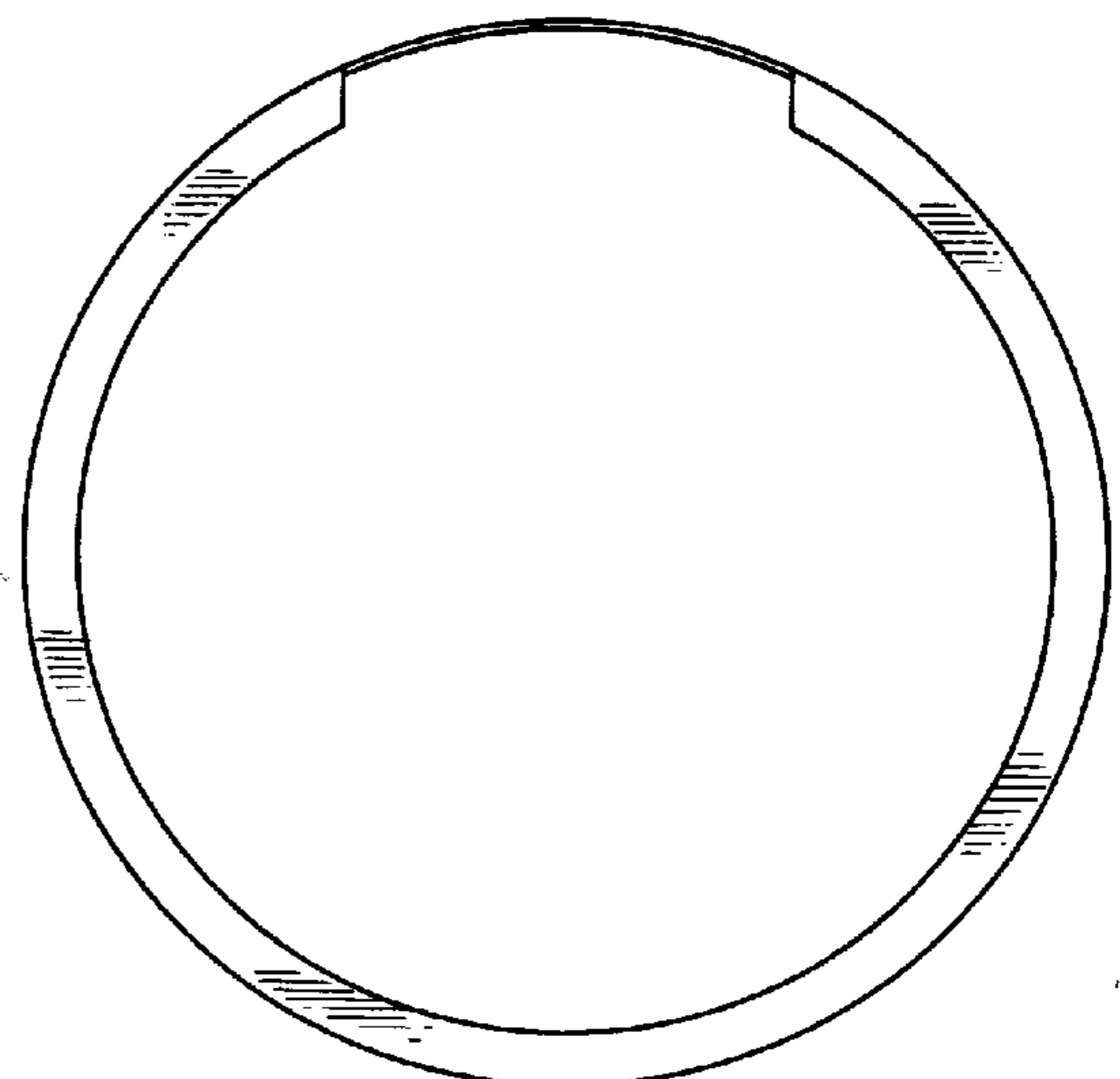


FIG. 6

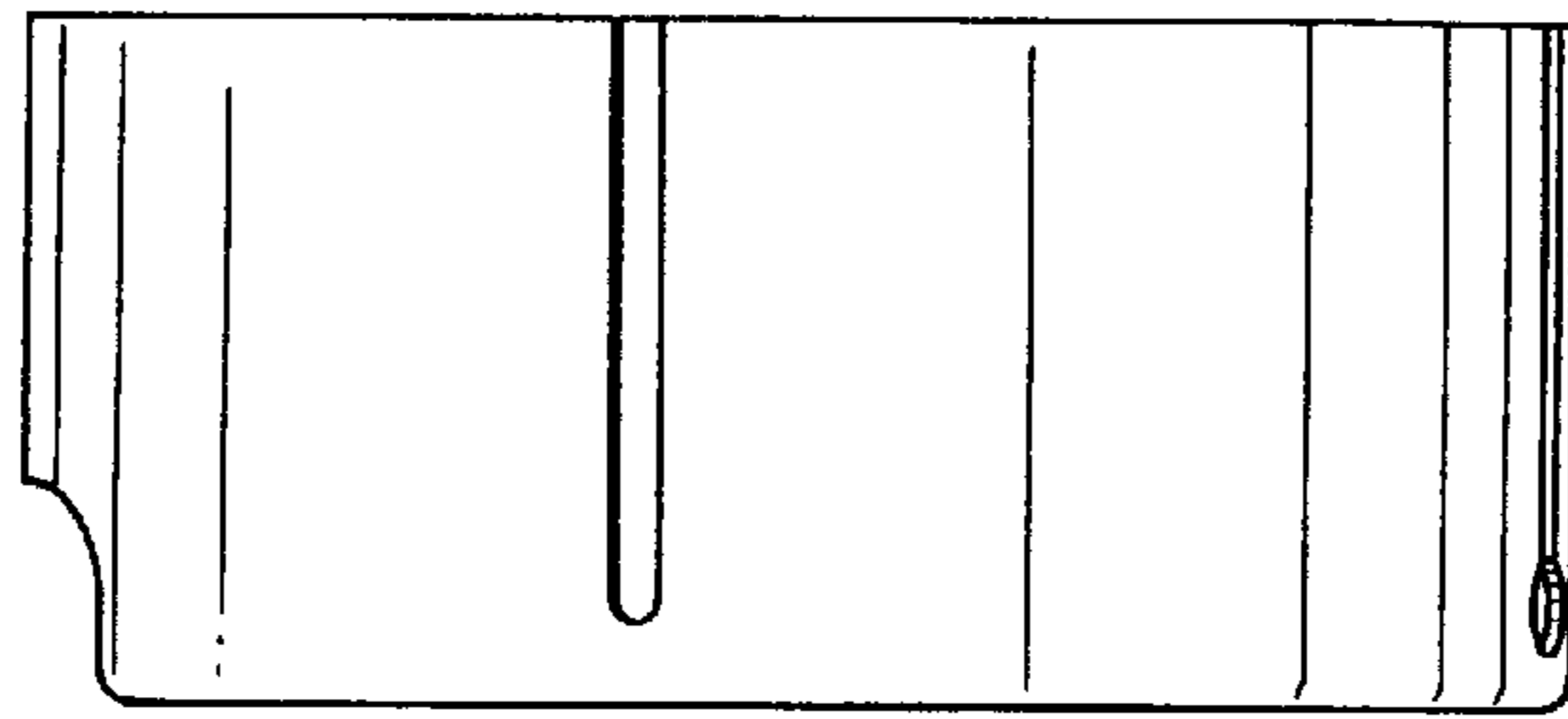


FIG. 7

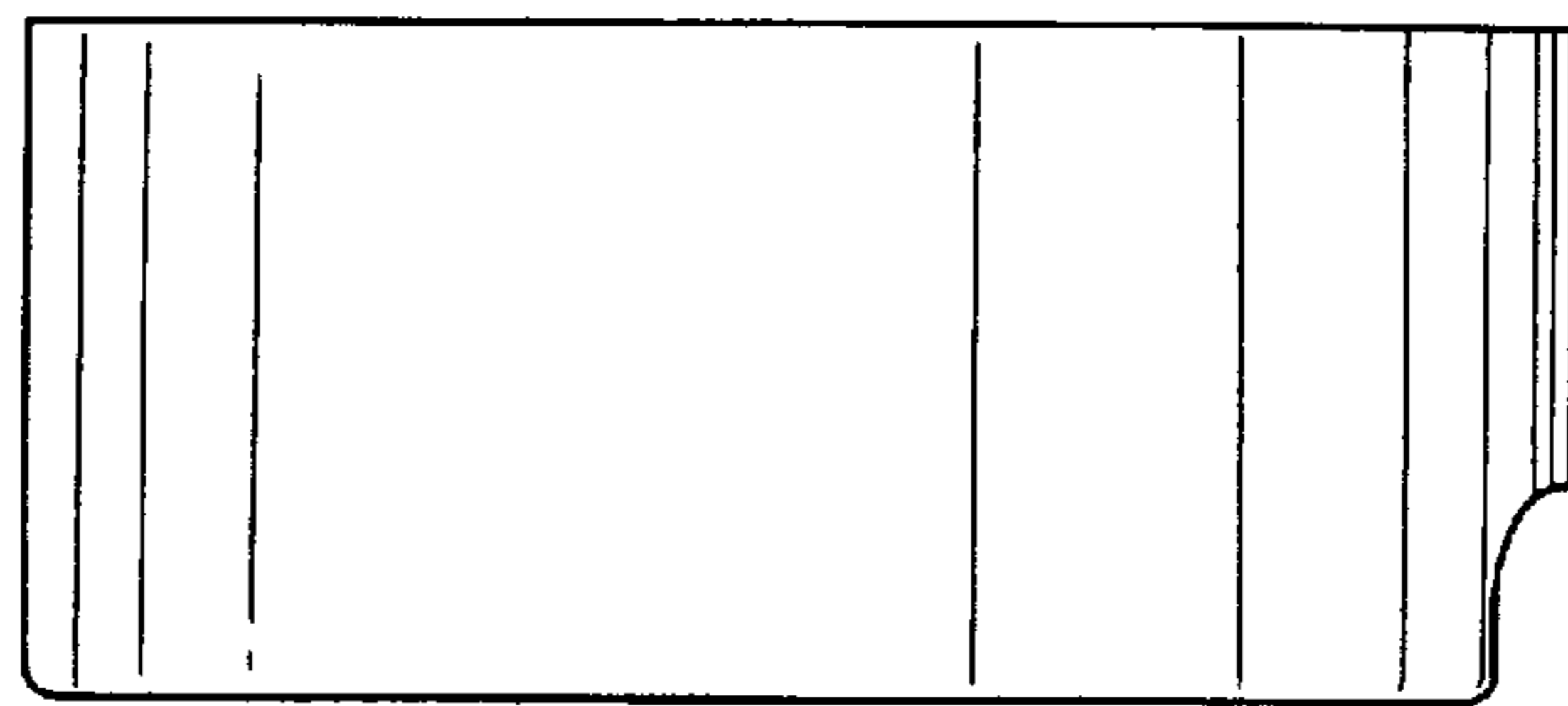


FIG. 8

