US00D402274S

United States Patent [19]

Kataoka et al.

[11] **Patent Number: Des. 402,274**

[45] **Date of Patent: **Dec. 8, 1998**

[54] **CONNECTOR FOR PRINTED CIRCUIT BOARDS**

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[73] Assignees: **Sony Corporation**, Tokyo; **Japan Solderless Terminal Mfg. Co., Ltd.**, Osaka, both of Japan

[**] Term: **14 Years**

[21] Appl. No.: **71,612**

[22] Filed: **Jun. 3, 1997**

[30] **Foreign Application Priority Data**

Apr. 1, 1997 [JP] Japan 9-50067

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; 174/52.3, 174/52.4; 361/760, 761, 764, 785

[56] **References Cited**

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Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—W. F. Fasse; W. G. Fasse

[57] **CLAIM**

We claim the ornamental design for a connector for printed circuit boards, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a connector for printed circuit boards showing our new design in a first embodiment, while the rear view corresponds to the front view;

FIG. **2** is a top view of the connector for printed circuit boards;

FIG. **3** is a bottom view of the connector for printed circuit boards;

FIG. **4** is a left side view of the connector for printed circuit boards, while the right side view corresponds to the left side view;

FIG. **5** is a sectional view along the line V—V in FIG. **2**;

FIG. **6** is a sectional view along the line VI—VI in FIG. **1**;

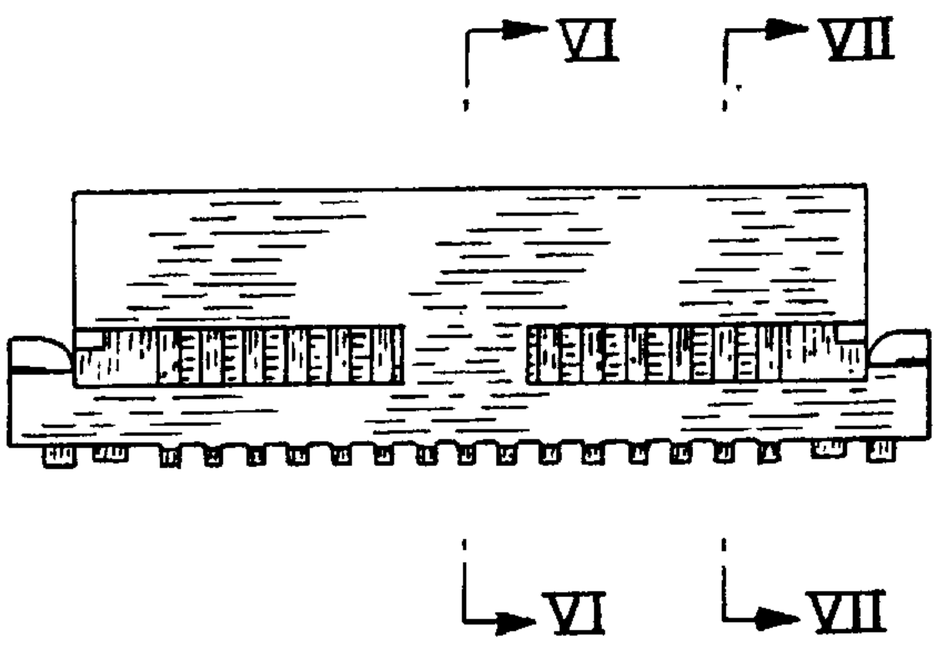
FIG. **7** is a sectional view along the line VII—VII in FIG. **1**;

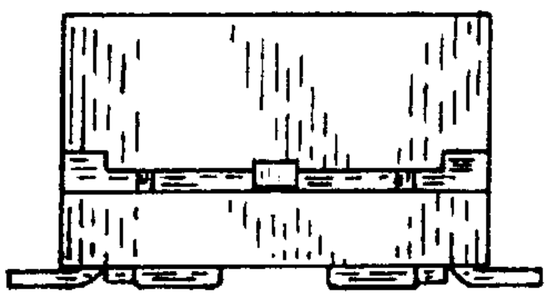
FIG. **8** is a sectional view along the line VI—VI in FIG. **1** in a connecting condition of printed circuit boards; and,

FIG. **9** is a sectional view along the line VII—VII in FIG. **1** in a connecting condition of printed circuit boards.

The broken-line disclosure of a portion of a circuit board in the views is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 3 Drawing Sheets





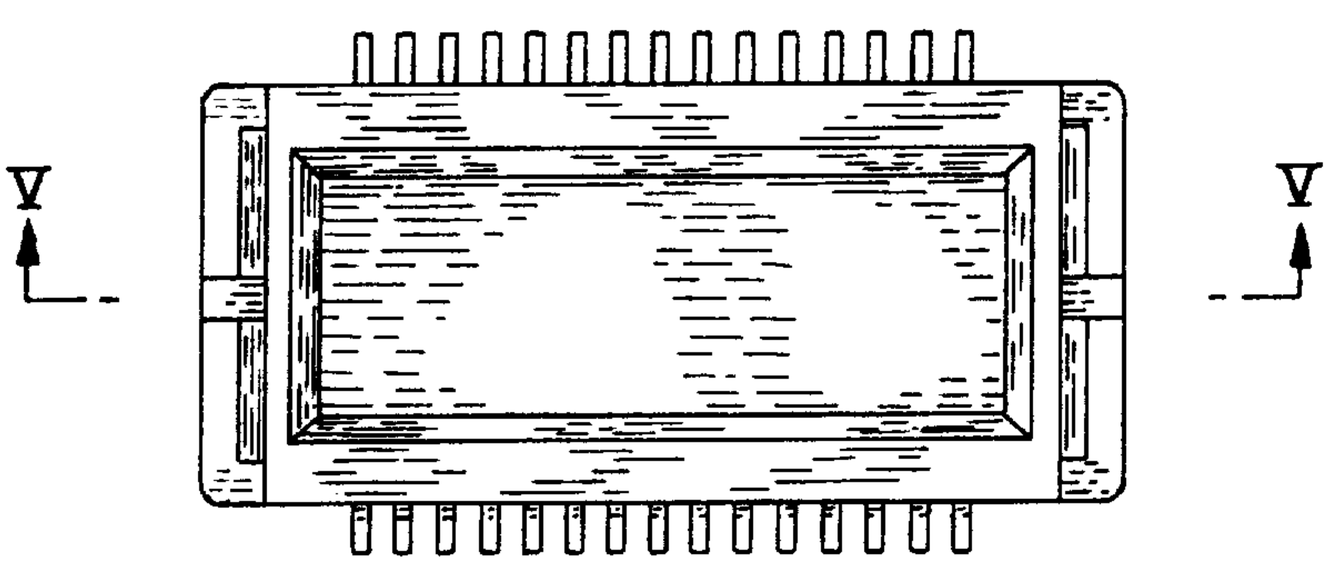


FIG.1

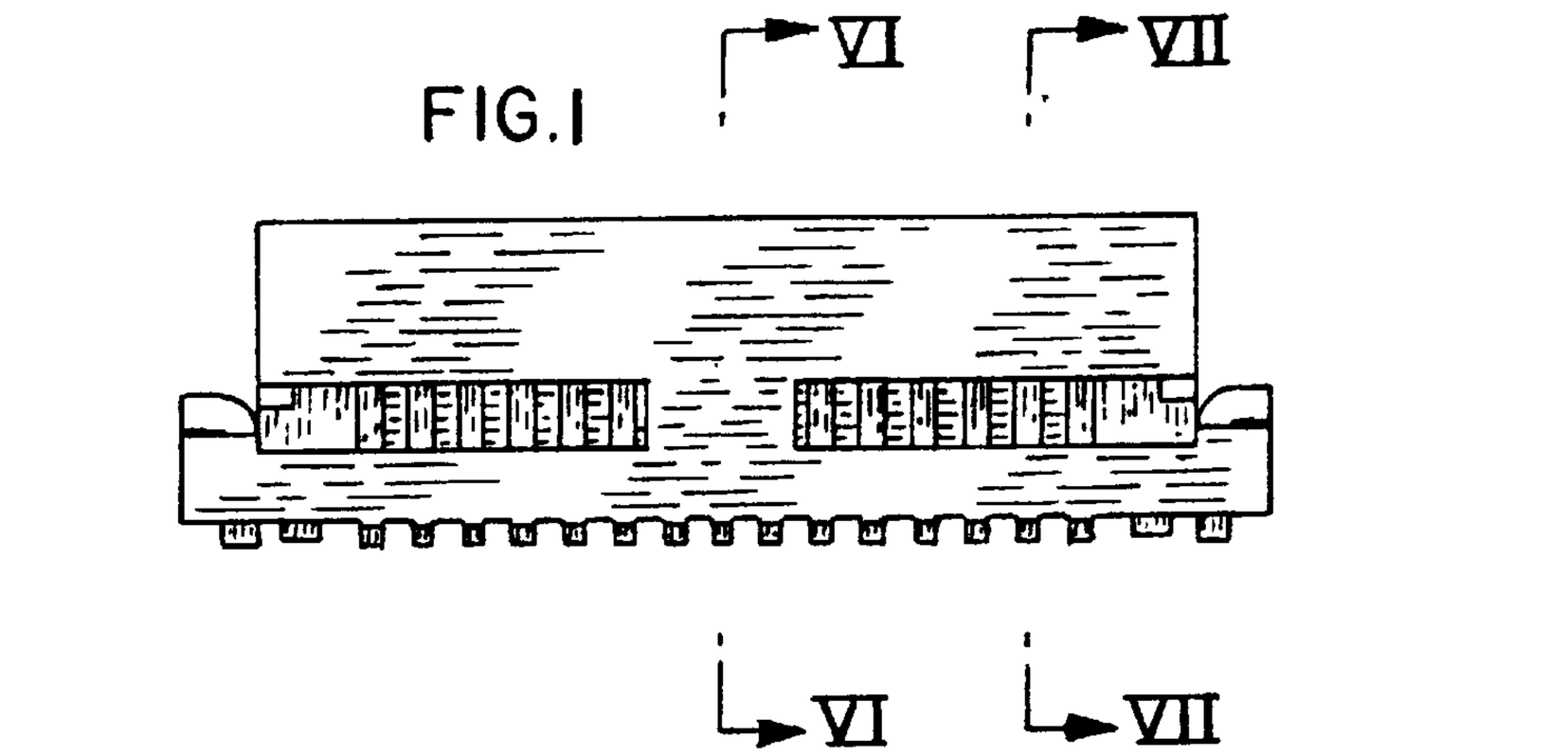


FIG.2

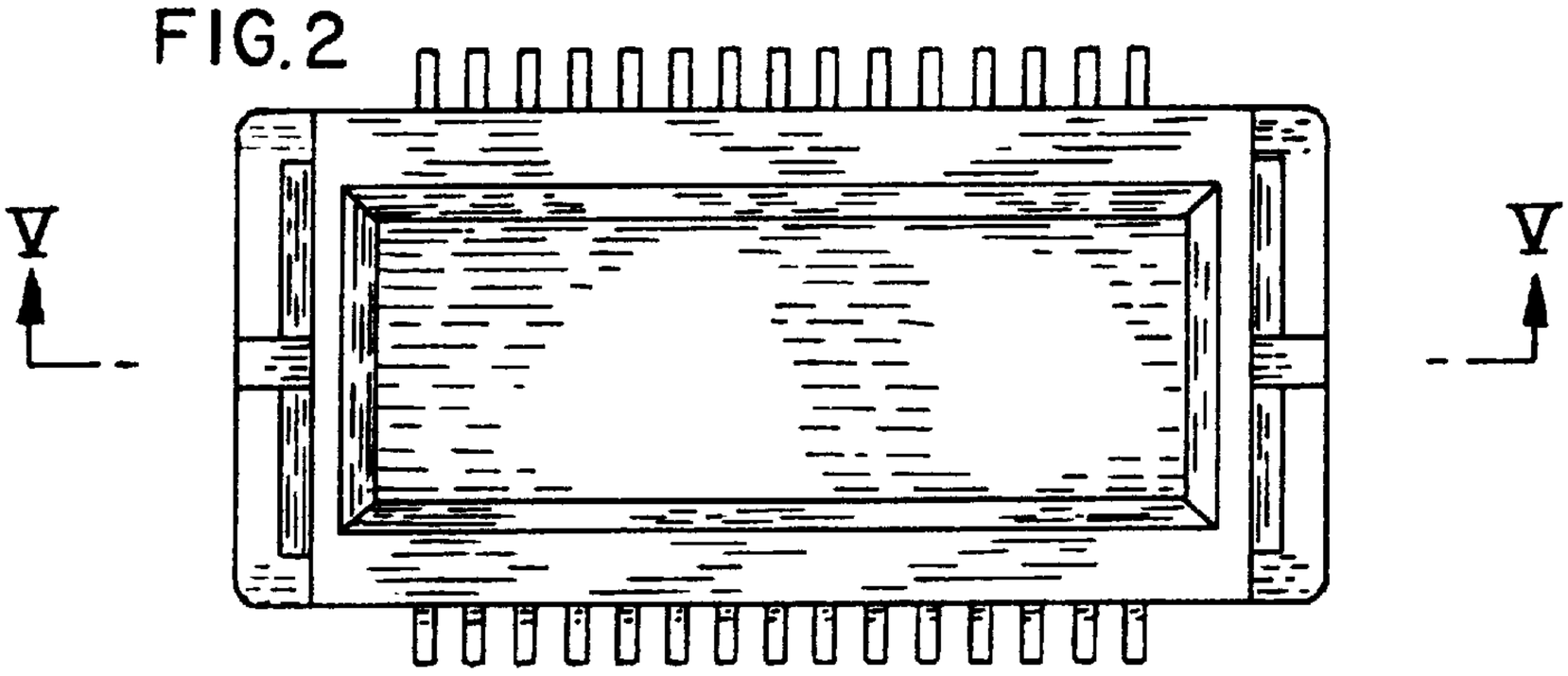


FIG.3

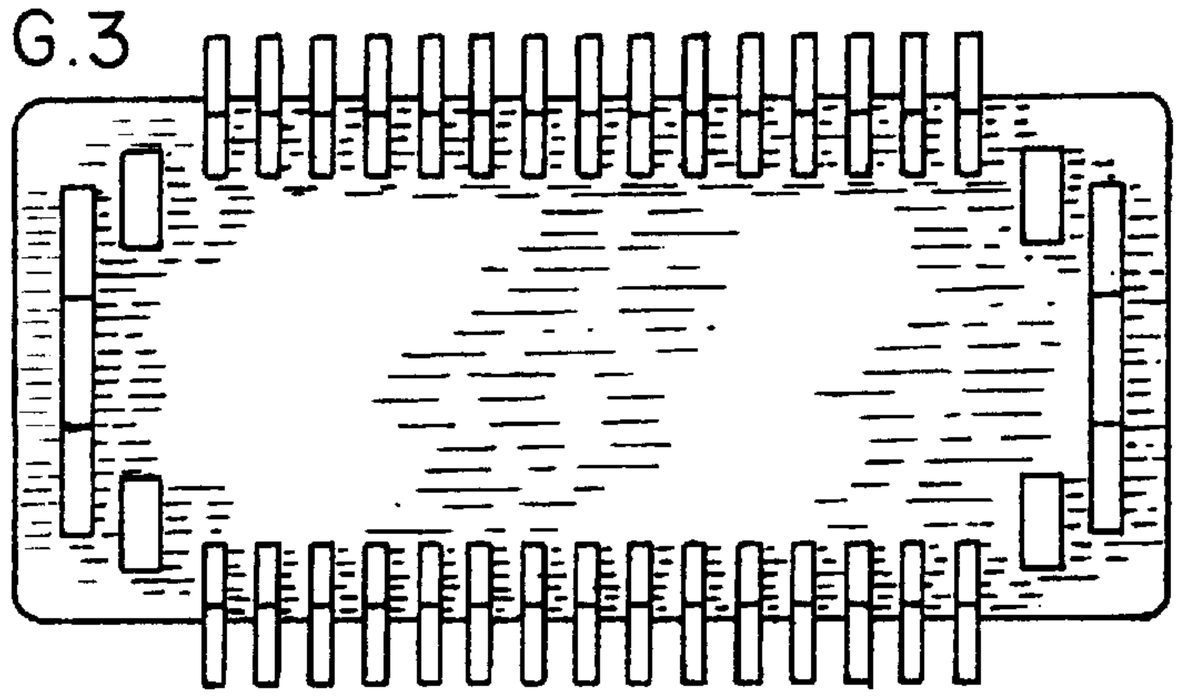


FIG. 4

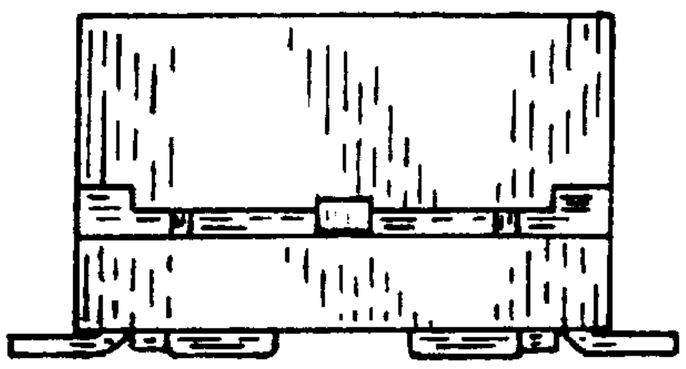


FIG. 6

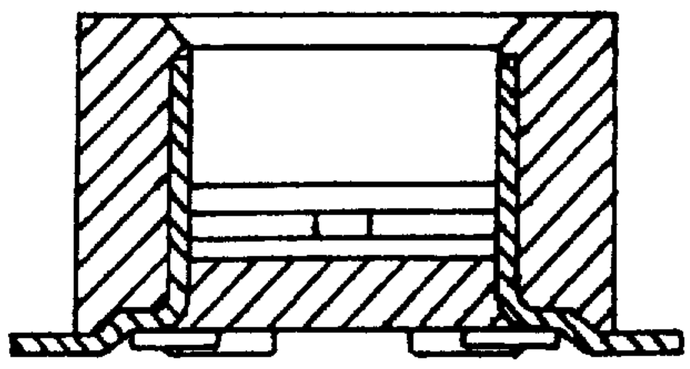


FIG. 5

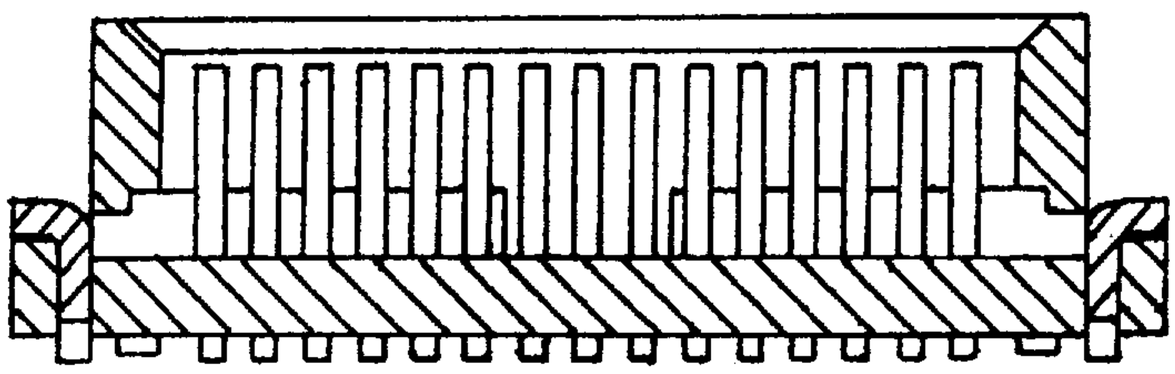


FIG. 7

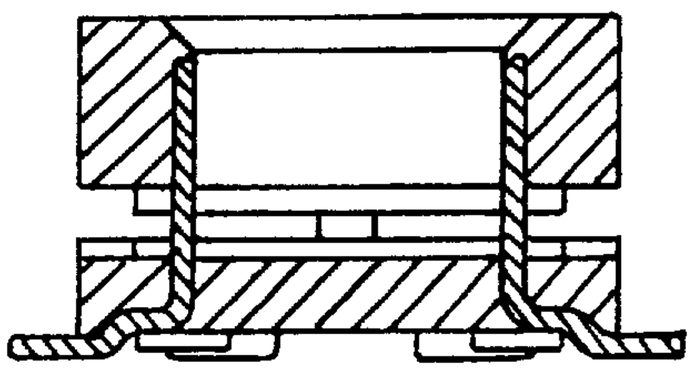


FIG.8

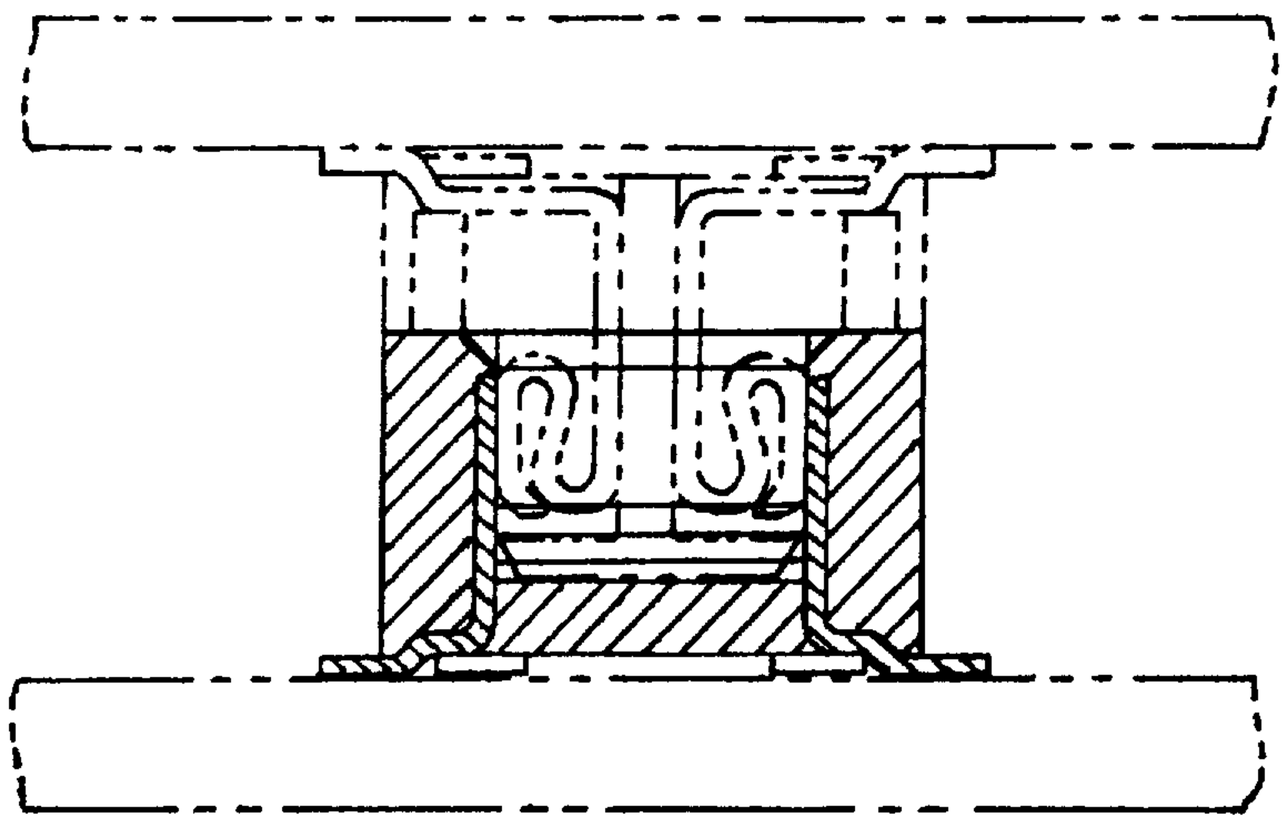
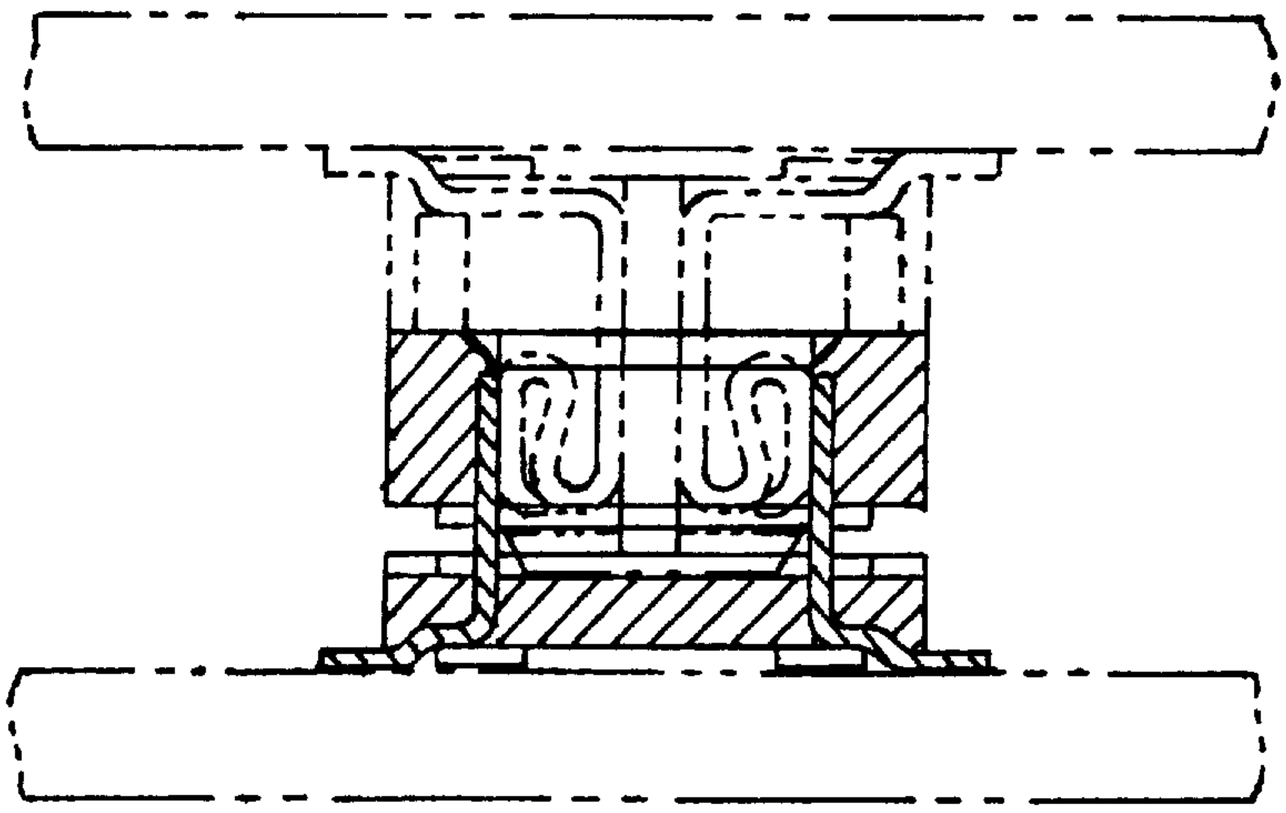


FIG.9



UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT : Des. 402,274

DATED : December 8, 1998

INVENTOR(S) : Kataoka et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in item [75] Inventors: lines 2 and 3, delete "Narihiko Hashimoto, Nagoya, all of Japan"; and line 3, should should read --both of Japan--.

In item [30] Foreign Application Priority Data, please add the following:

--Dec. 11, 1996 [JP] Japan.....8-37848
Dec. 26, 1996 [JP] Japan.....8-39611--.

Signed and Sealed this

Fifteenth Day of June, 1999

Attest:

Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks