



US00D402273S

United States Patent [19]

Kataoka et al.

[11] Patent Number: Des. 402,273

[45] Date of Patent: **Dec. 8, 1998

[54] **CONNECTOR FOR PRINTED CIRCUIT BOARDS**

[75] Inventors: **Yasuhiro Kataoka**, Yokohama; **Terumi Nakashima**, Takatsuki; **Narihiko Hashimoto**, Nagoya, all of Japan

[73] Assignees: **Sony Corporation**, Tokyo; **Japan Solderless Terminal Mfg. Co., Ltd.**, Osaka, both of Japan

[**] Term: **14 Years**

[21] Appl. No.: **71,611**

[22] Filed: **Jun. 3, 1997**

[30] **Foreign Application Priority Data**

Dec. 26, 1996	[JP]	Japan	8-39612
Apr. 1, 1997	[JP]	Japan	9-50068

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; 174/52.3, 174/52.4; 361/760, 761, 764, 783

[56] **References Cited**

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Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—W. F. Fasse; W. G. Fasse

[57] **CLAIM**

We claim the ornamental design for a connector for printed circuit boards, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a connector for printed circuit boards showing our new design in a first embodiment, while the rear view corresponds to the front view;

FIG. 2 is a top view of the connector for printed circuit boards;

FIG. 3 is a bottom view of the connector for printed circuit boards;

FIG. 4 is a left side view of the connector for printed circuit boards, while the right side view corresponds to the left side view;

FIG. 5 is a sectional view along the line V—V in FIG. 1;

FIG. 6 is a sectional view along the line V—V in FIG. 1 in a connecting condition of printed circuit boards;

FIG. 7 is a front view of a connector for printed circuit boards showing our new design in a second embodiment, while the rear view corresponds to the front view;

FIG. 8 is a top view of the connector for printed circuit boards of the second embodiment;

FIG. 9 is a bottom view of the connector for printed circuit boards of the second embodiment;

FIG. 10 is a left side view of the connector for printed circuit boards of the second embodiment, while the right side view corresponds to the left side view;

FIG. 11 is a sectional view along the line XI—XI in FIG. 7; and,

FIG. 12 is a sectional view along the line XI—XI in FIG. 7 in a connecting condition of printed circuit boards.

The broken-line disclosure of a portion of a circuit board in the views is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 3 Drawing Sheets

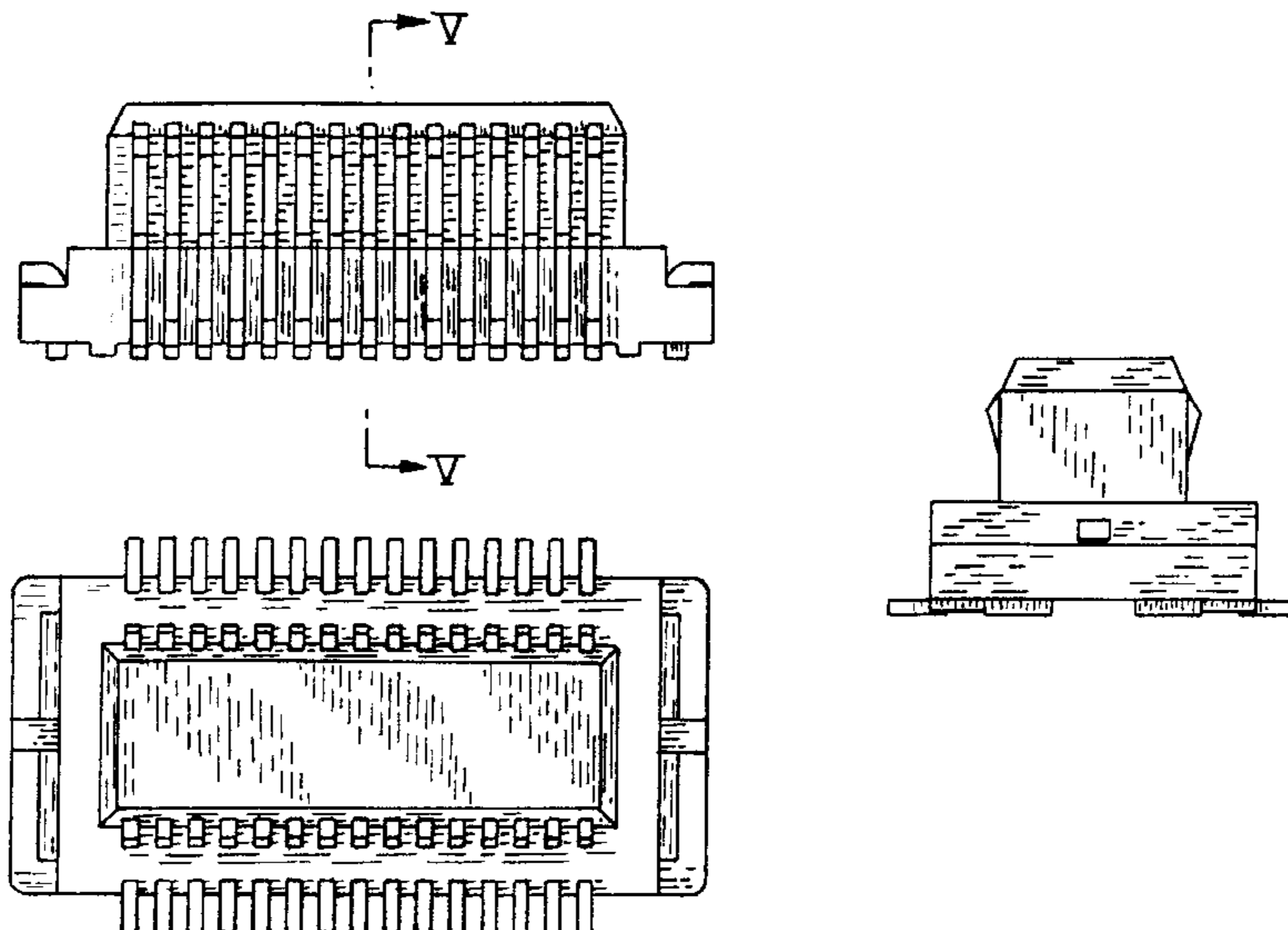


FIG. 1

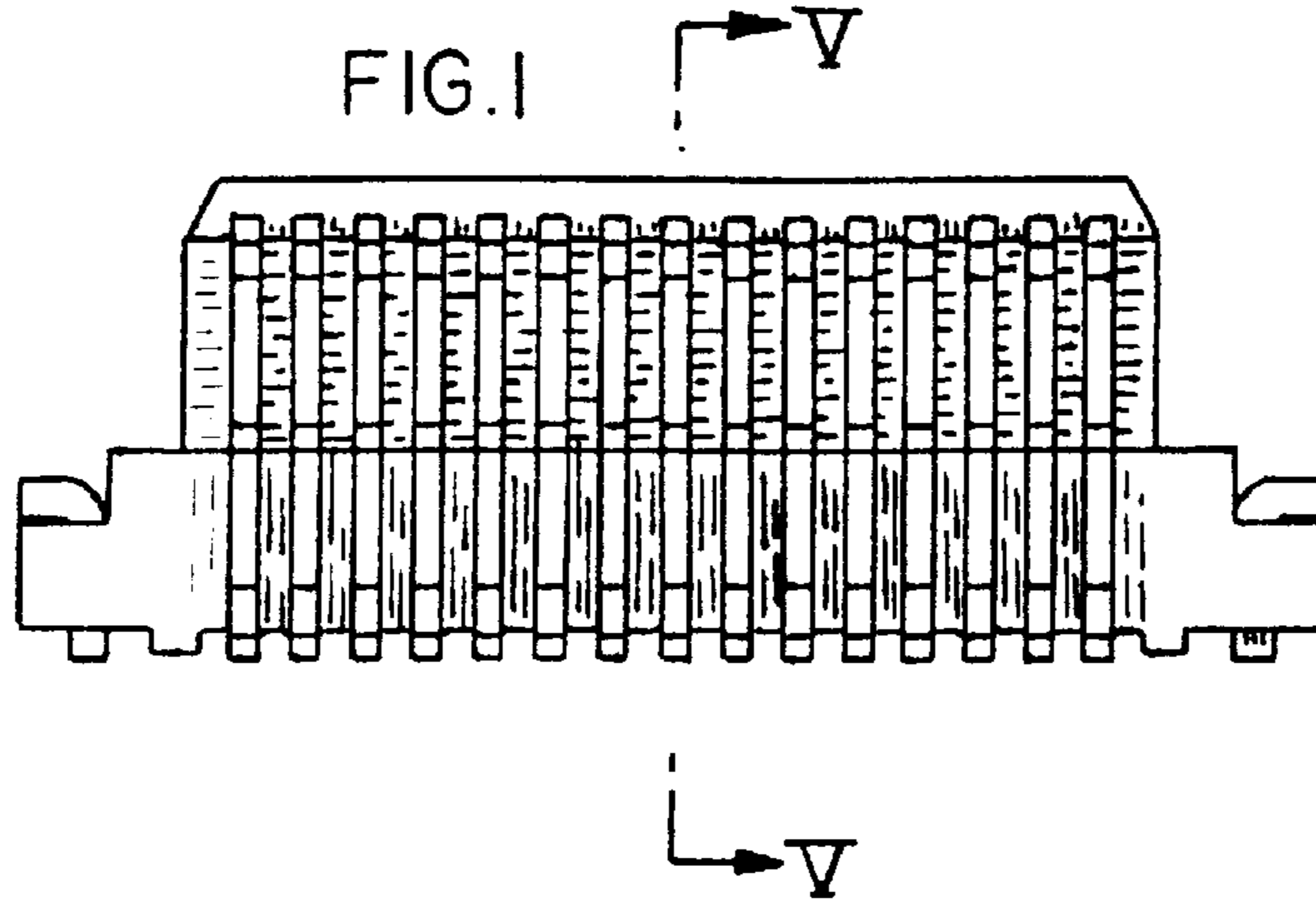


FIG. 2

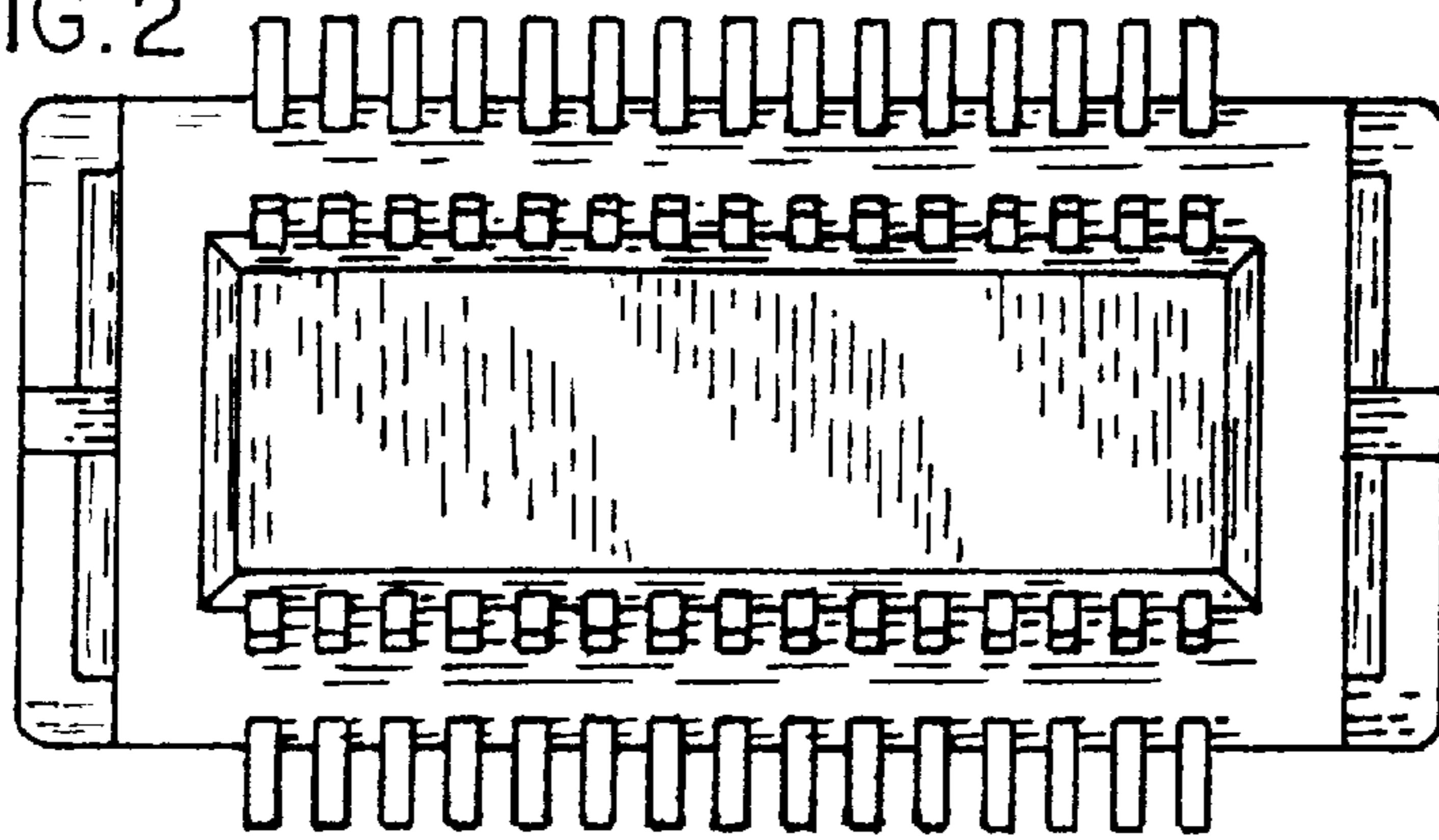


FIG. 3

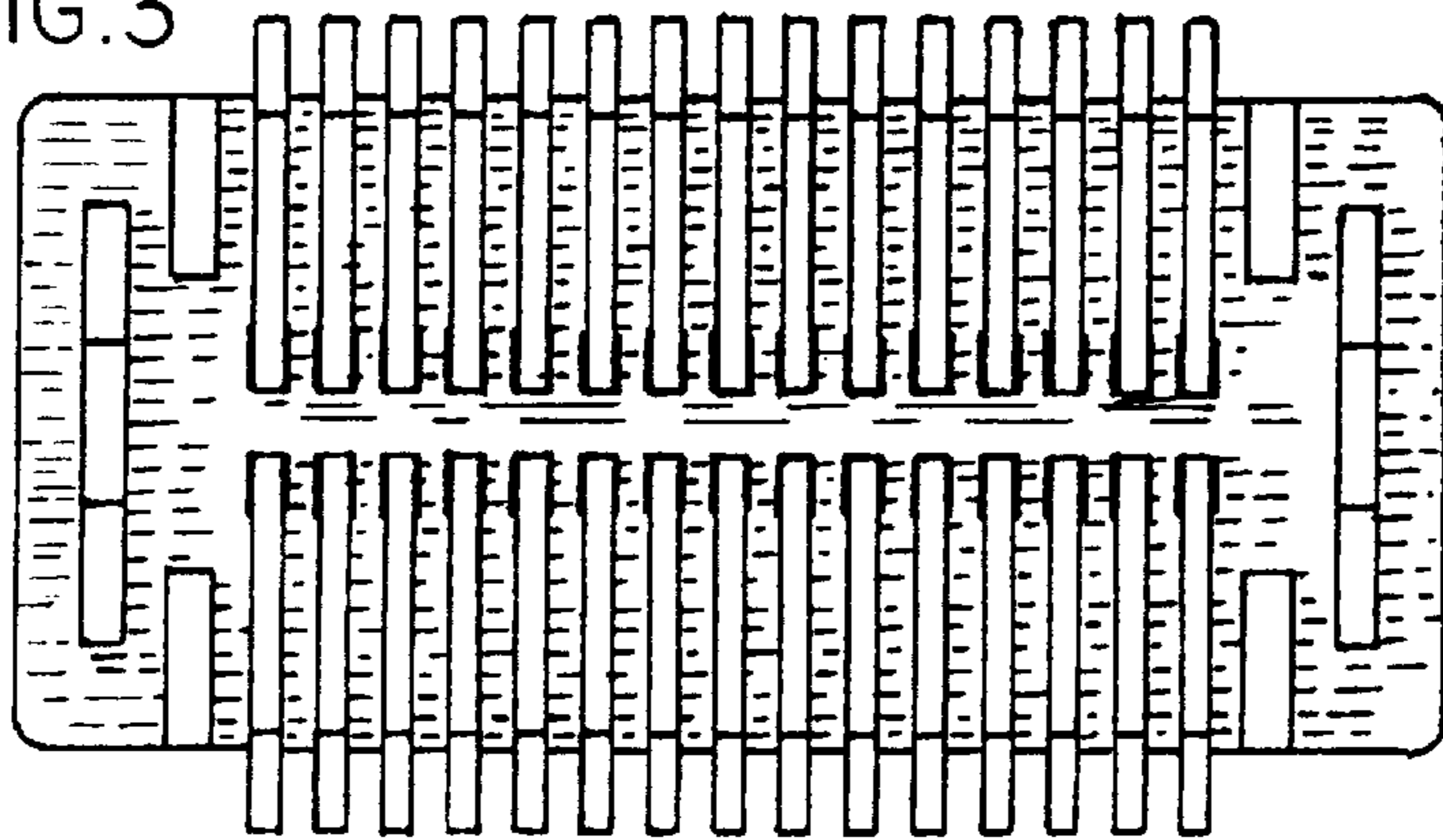


FIG. 4

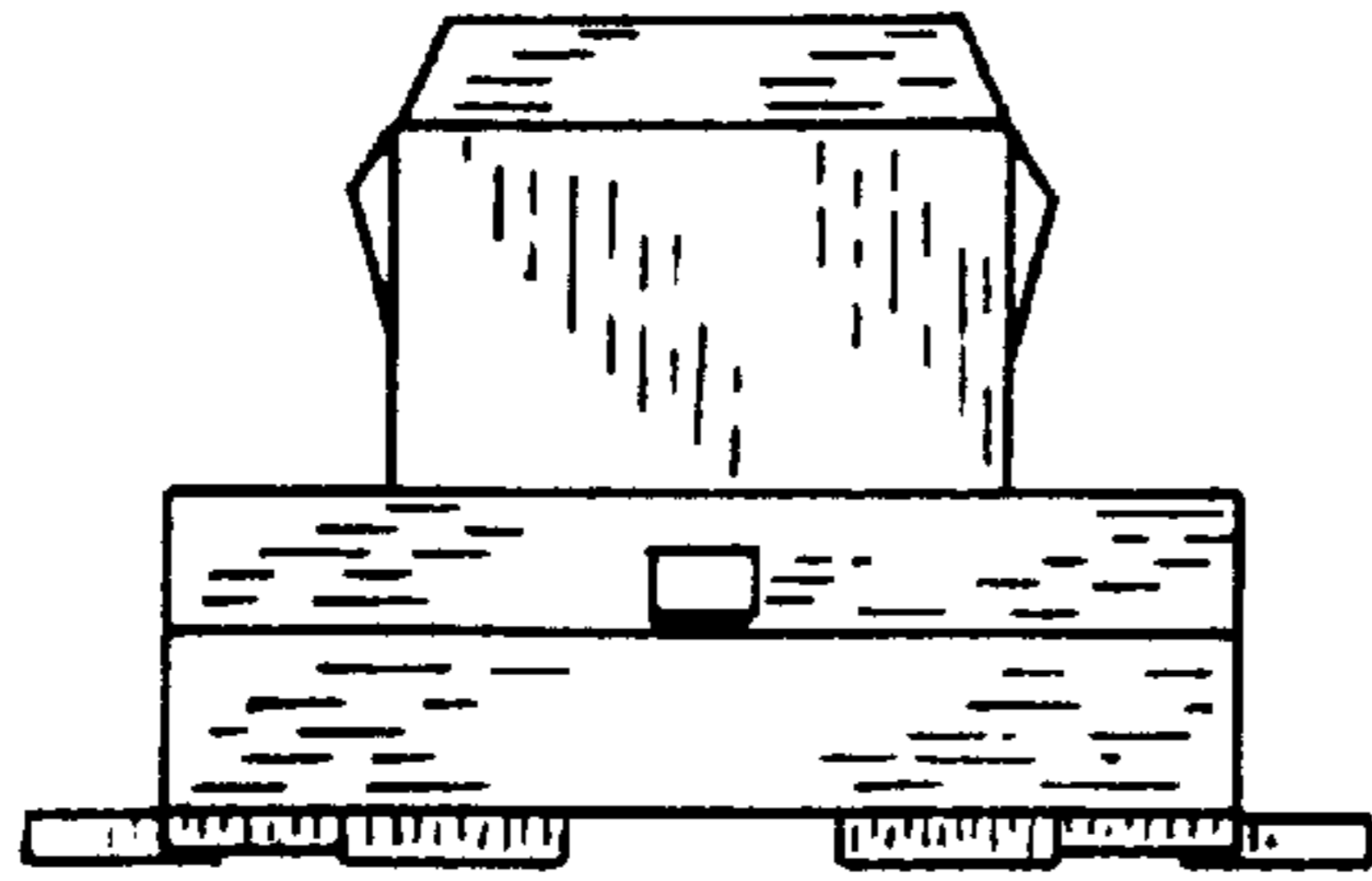


FIG. 5

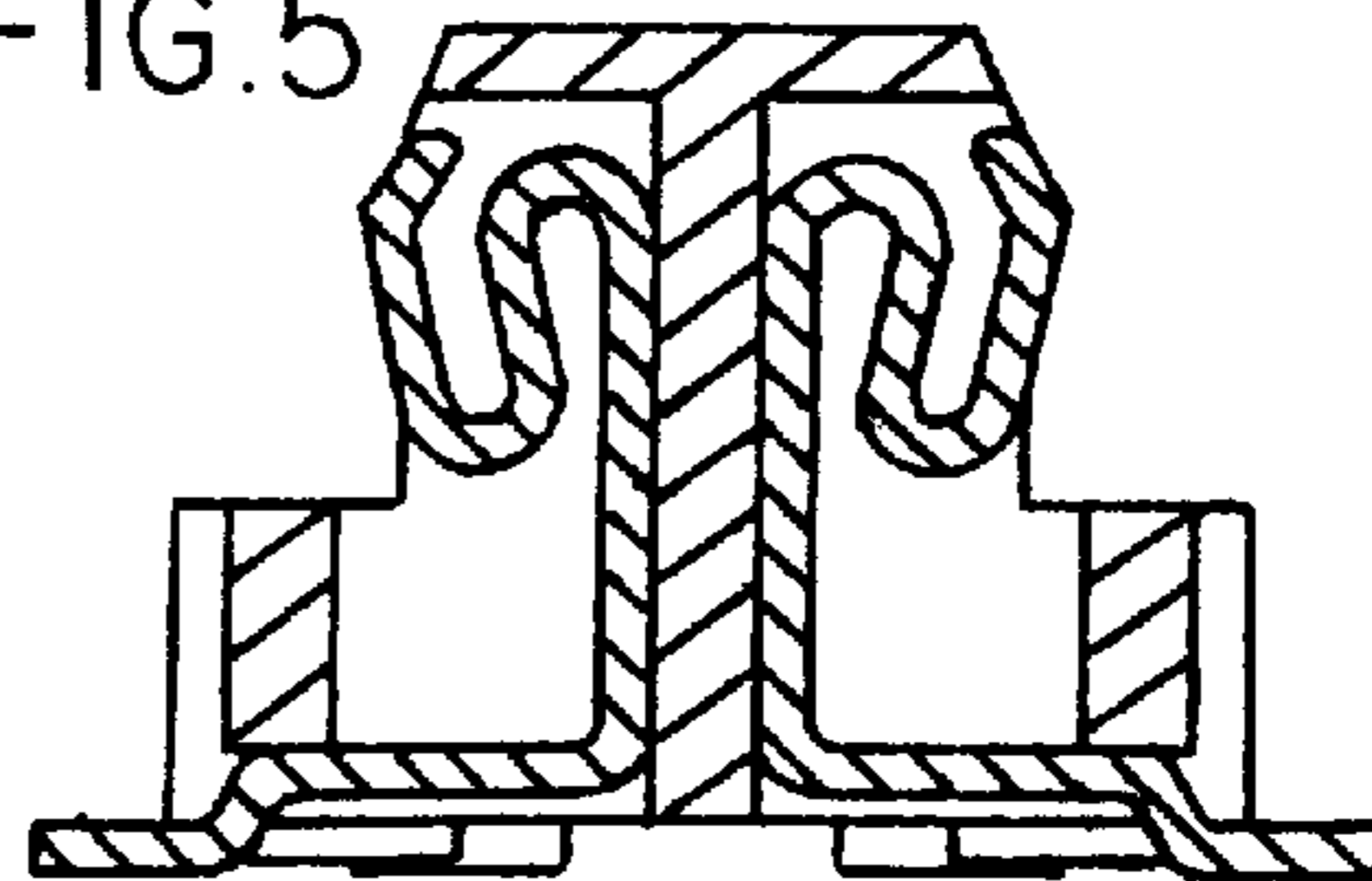


FIG. 6

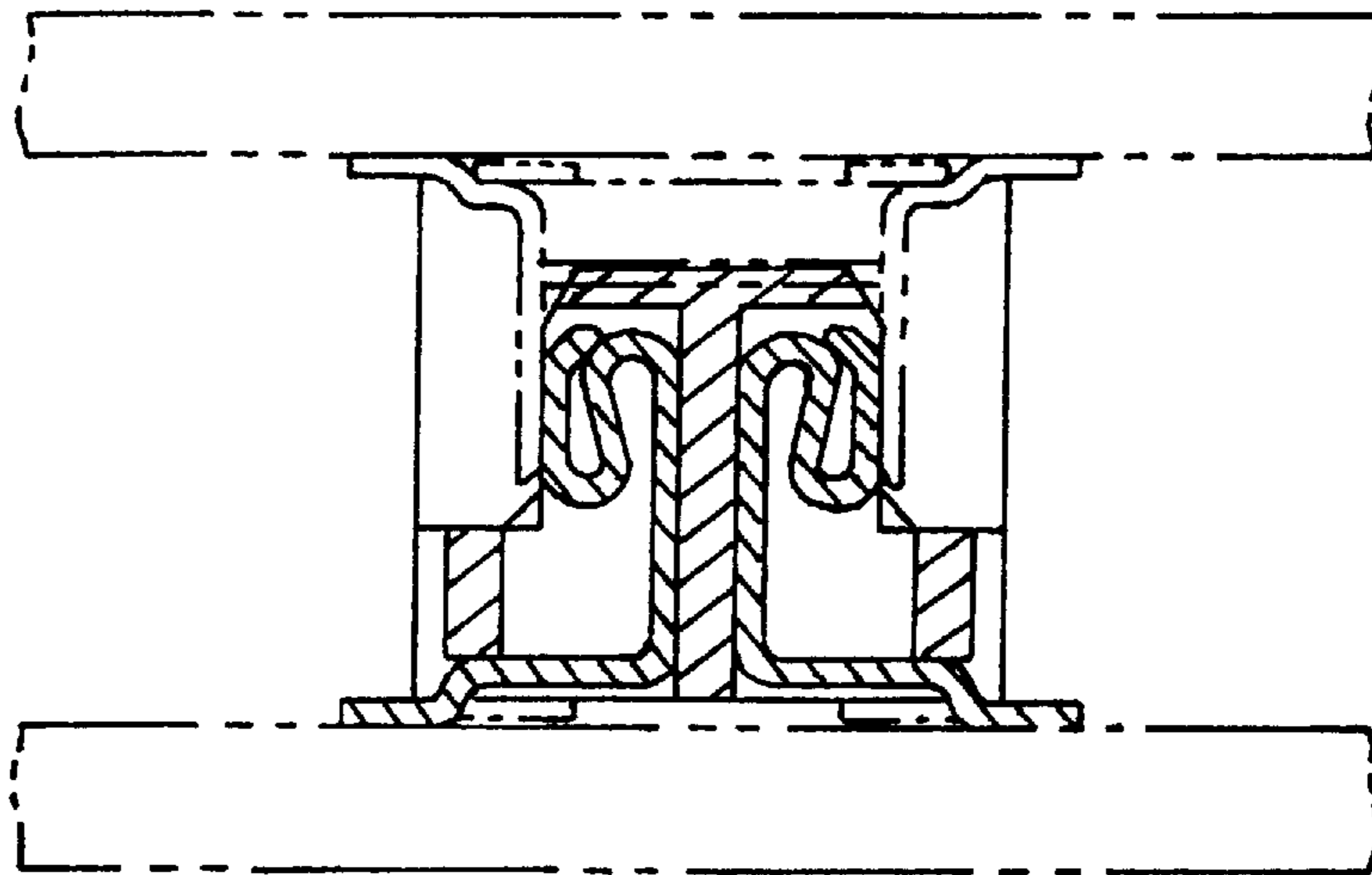


FIG. 8

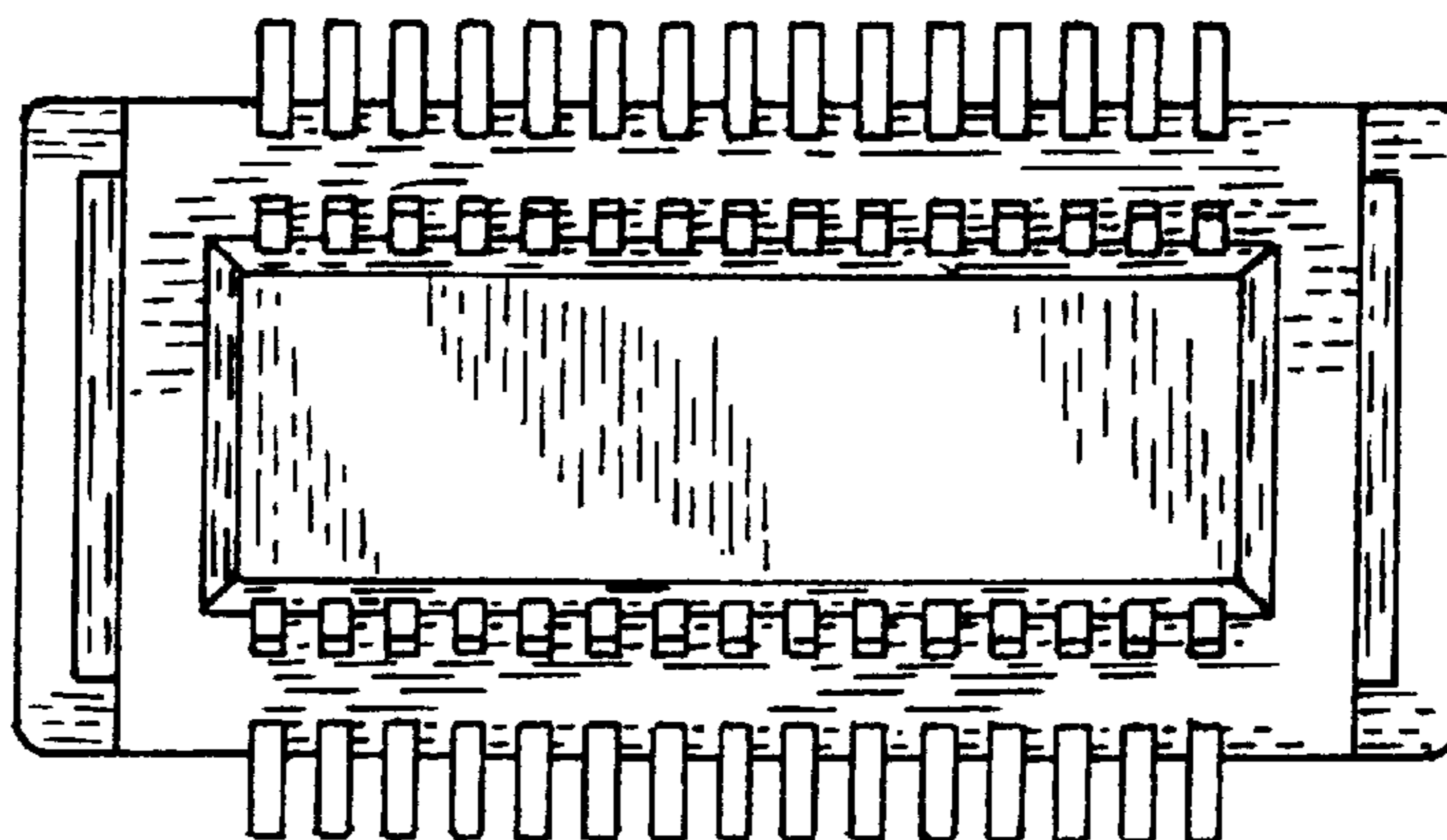


FIG.7 XI

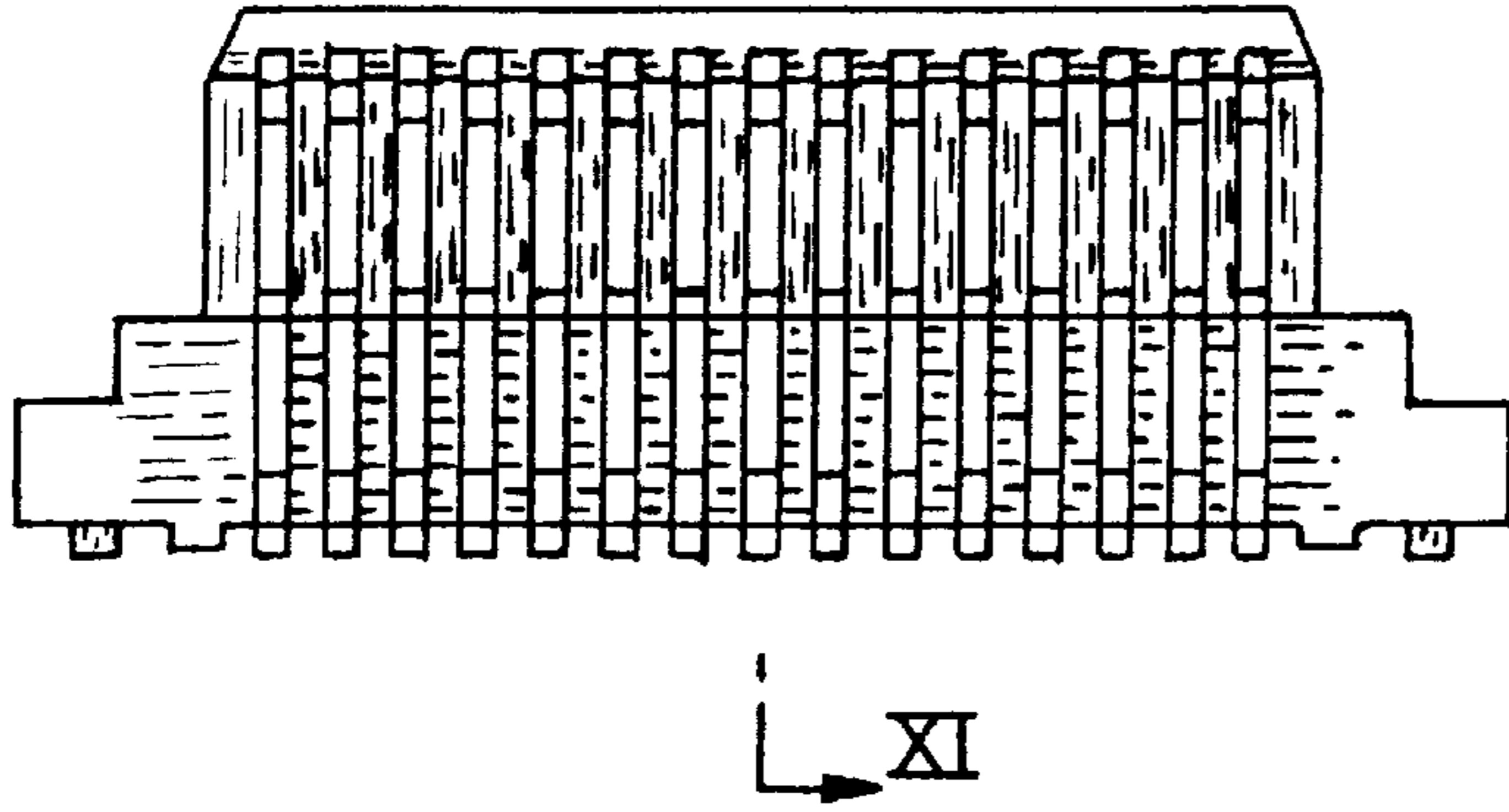


FIG.10

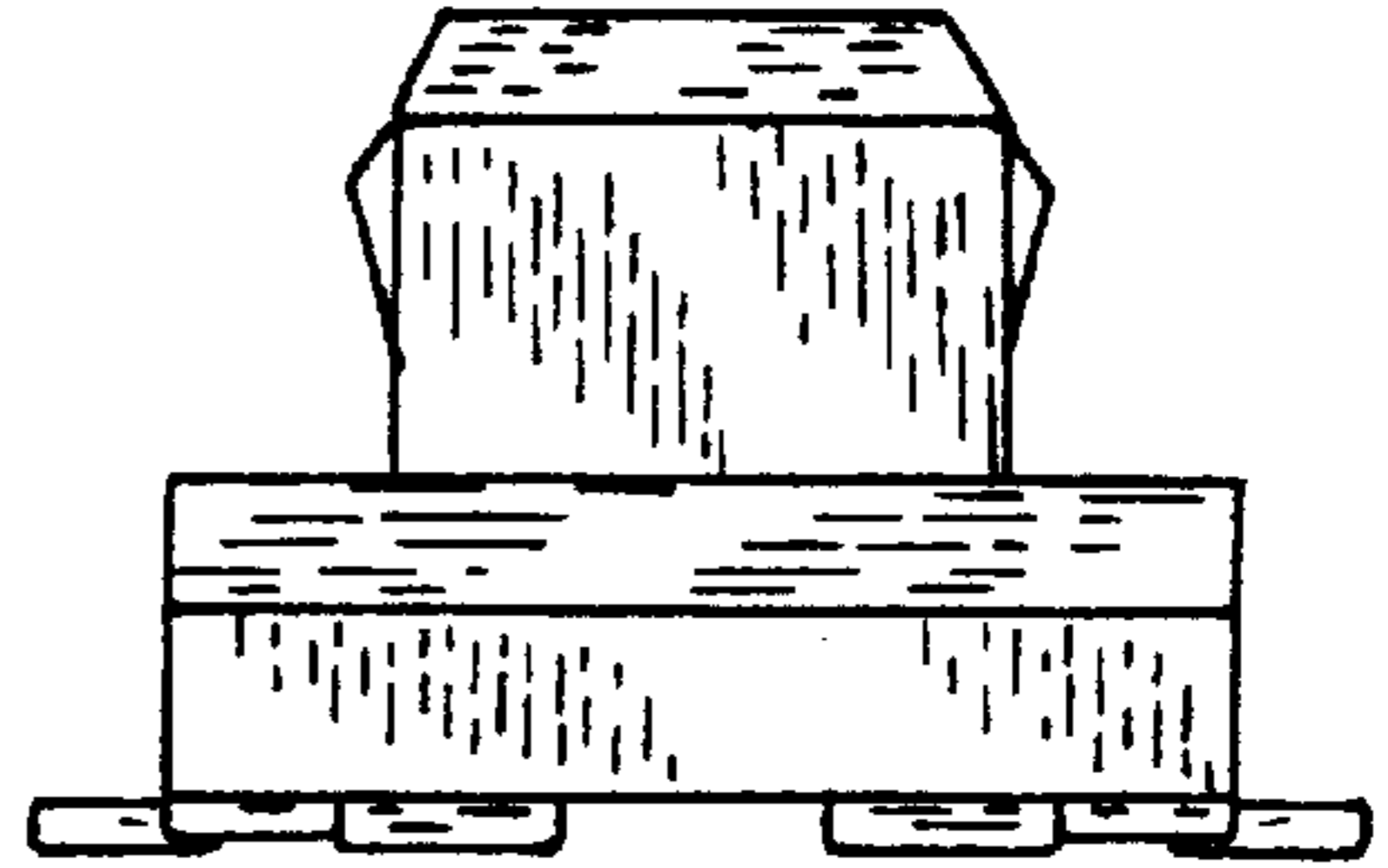


FIG.9

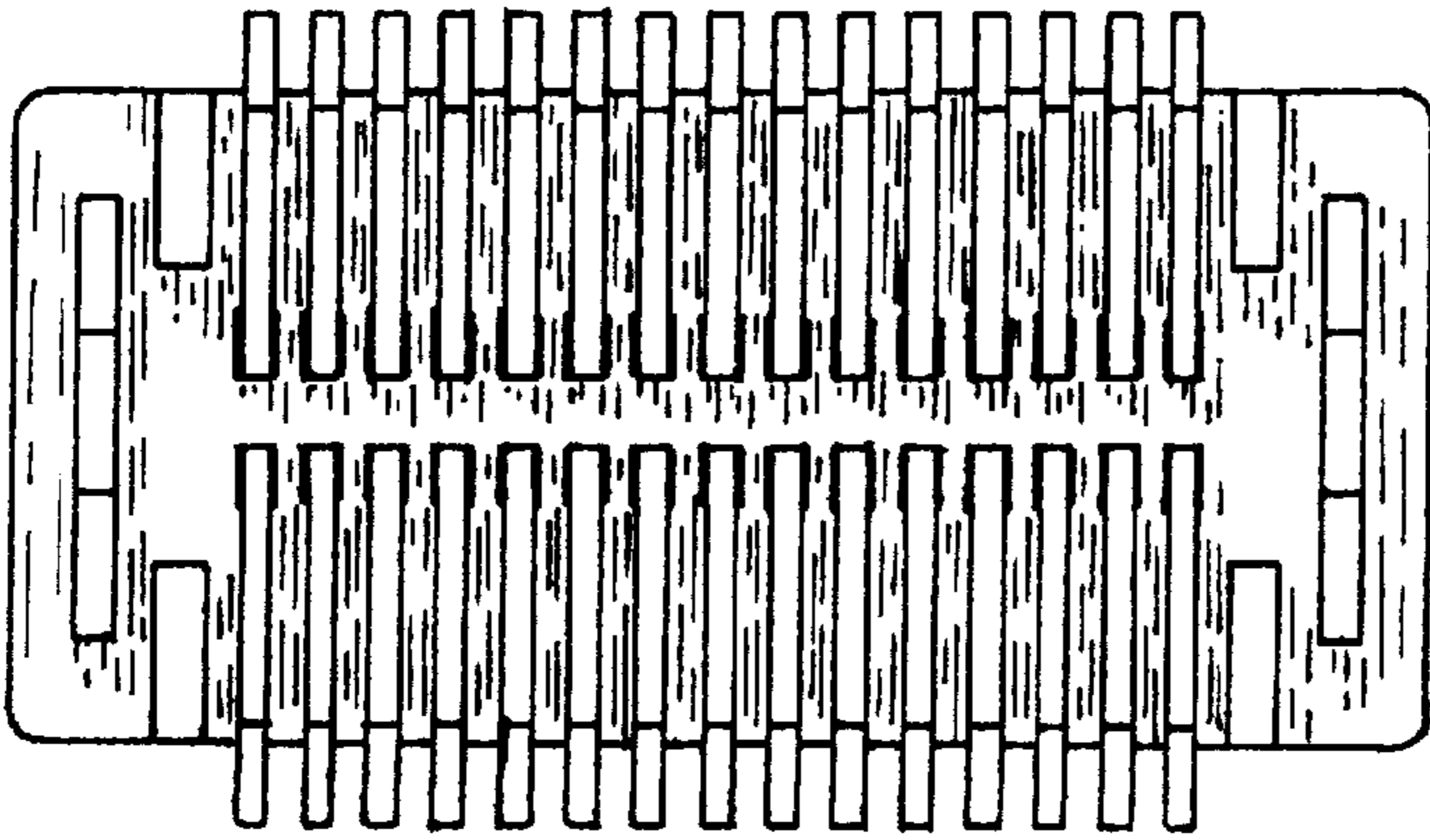


FIG.11

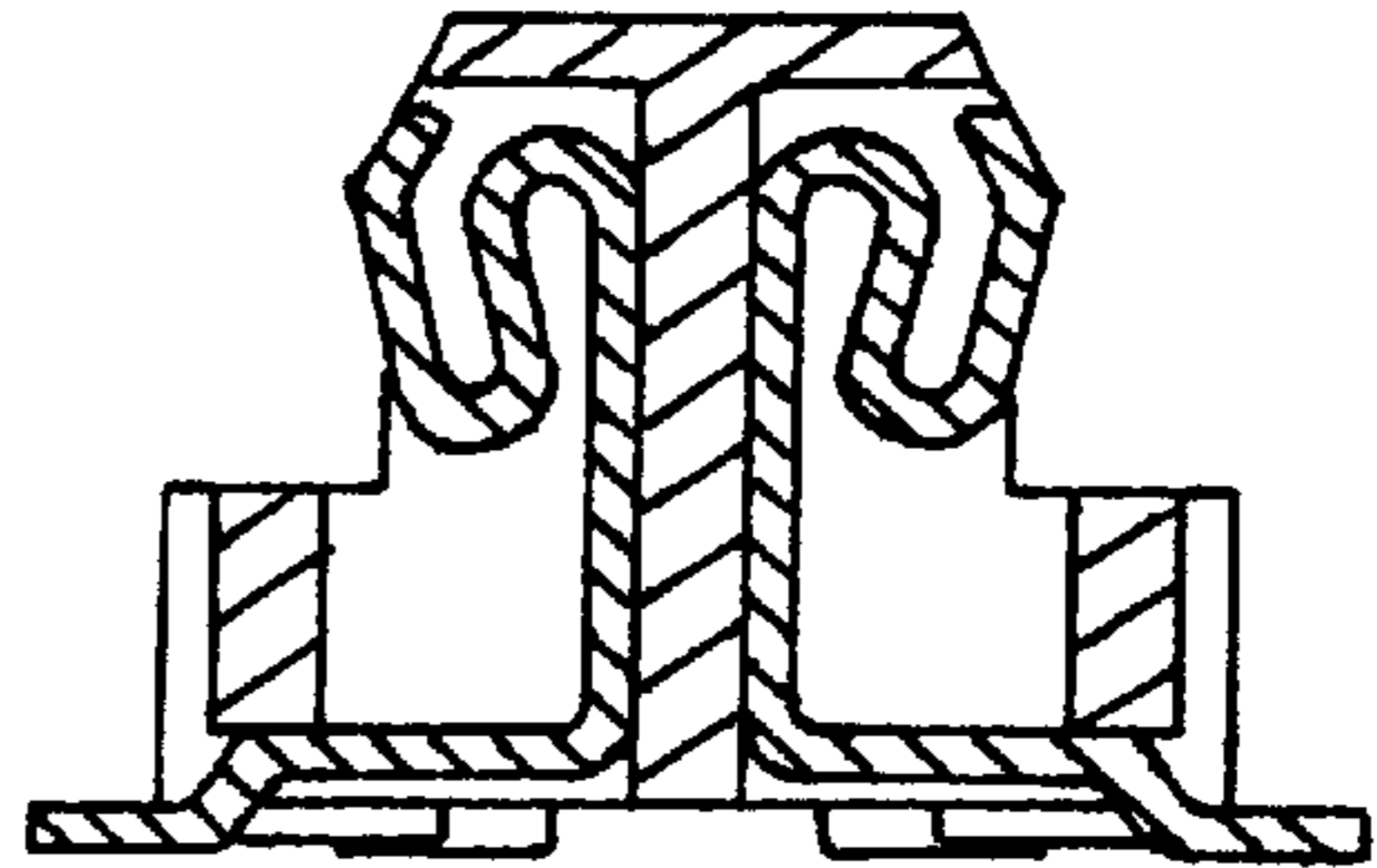
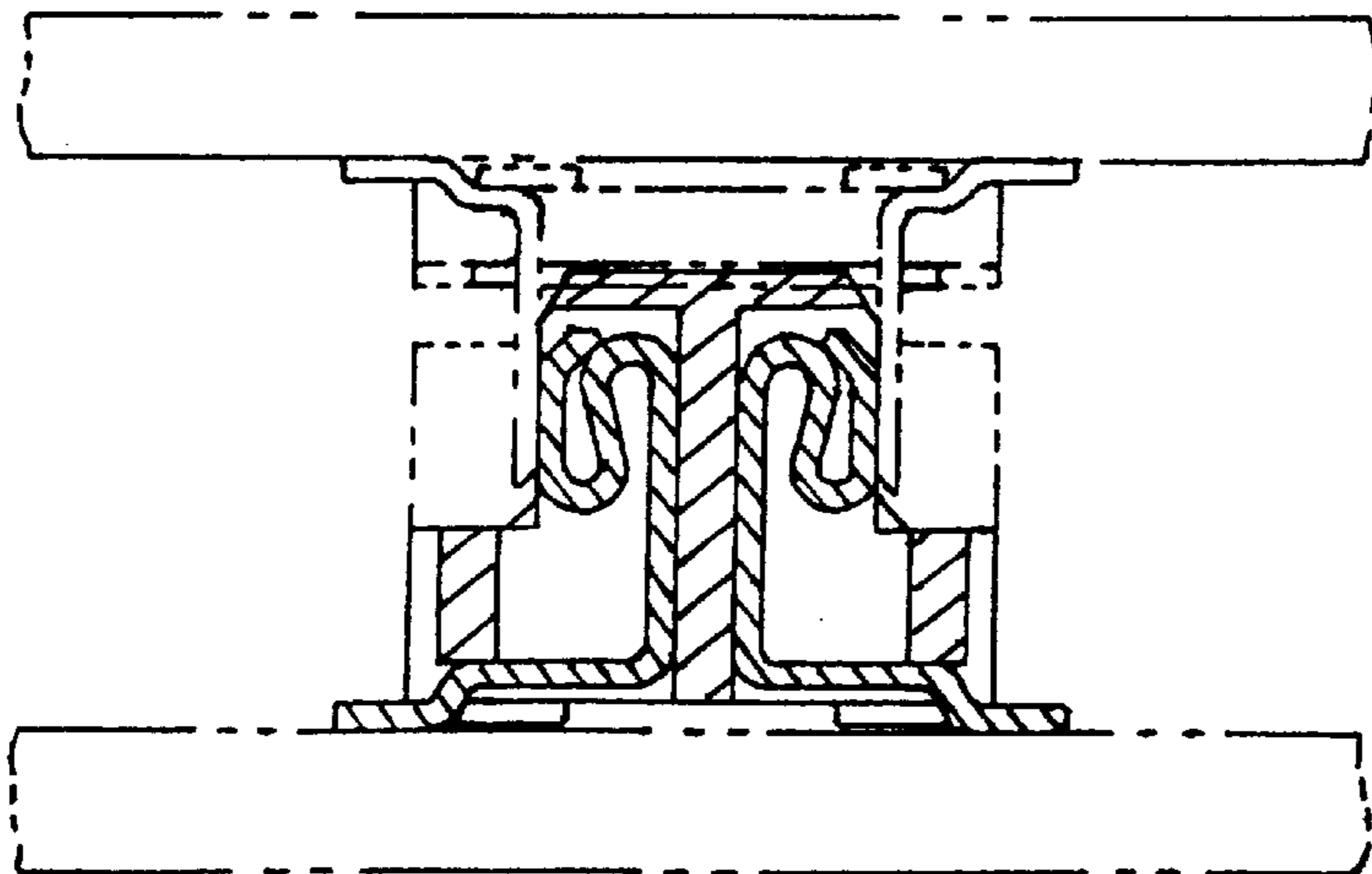


FIG.12



**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : Des. 402,273

DATED : Dec. 8, 1998

INVENTOR(S) : Kataoka et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Item

In [30] Foreign Application Priority Data, please add the following:

--Dec. 11, 1996 [JP] Japan.....8-37849--.

Signed and Sealed this

Twenty-third Day of March, 1999

Attest:



Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks