



US00D397092S

United States Patent [19]

Sano et al.

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[54] **INTEGRATED CIRCUIT PACKAGE**

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[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[**] Term: **14 Years**

[21] Appl. No.: **64,520**

[22] Filed: **Jan. 3, 1997**

[51] LOC (6) Cl. **13-03**

[52] U.S. Cl. **D13/182**

[58] **Field of Search** D13/182, 110; 174/16.3, 52.2-52.4; 257/666, 678-697, 700, 730; 361/773, 792, 813; 439/68, 70

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[57] **CLAIM**

The ornamental design for an integrated circuit package, as shown.

DESCRIPTION

FIG. 1 is a front elevational view of our new integrated circuit package;
FIG. 2 is a rear elevational view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a left side elevational view thereof;
FIG. 6 is a right side elevational view thereof; and,
FIG. 7 is a perspective view thereof.

1 Claim, 2 Drawing Sheets

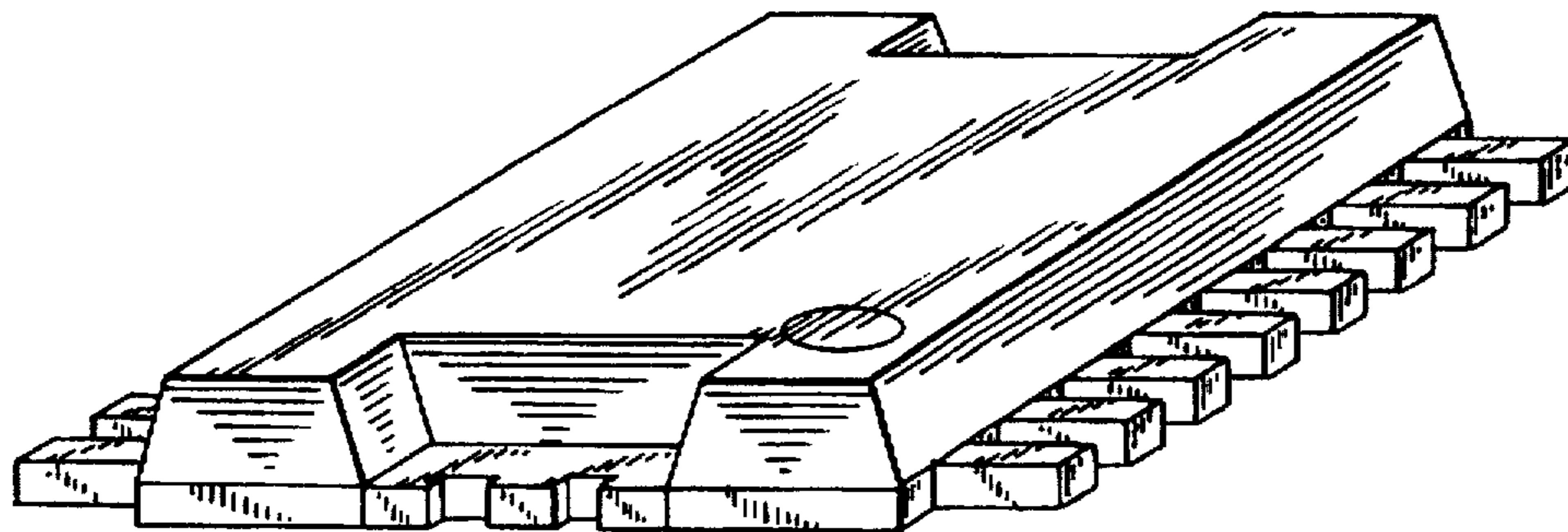


FIG. 1



FIG. 2



FIG. 3

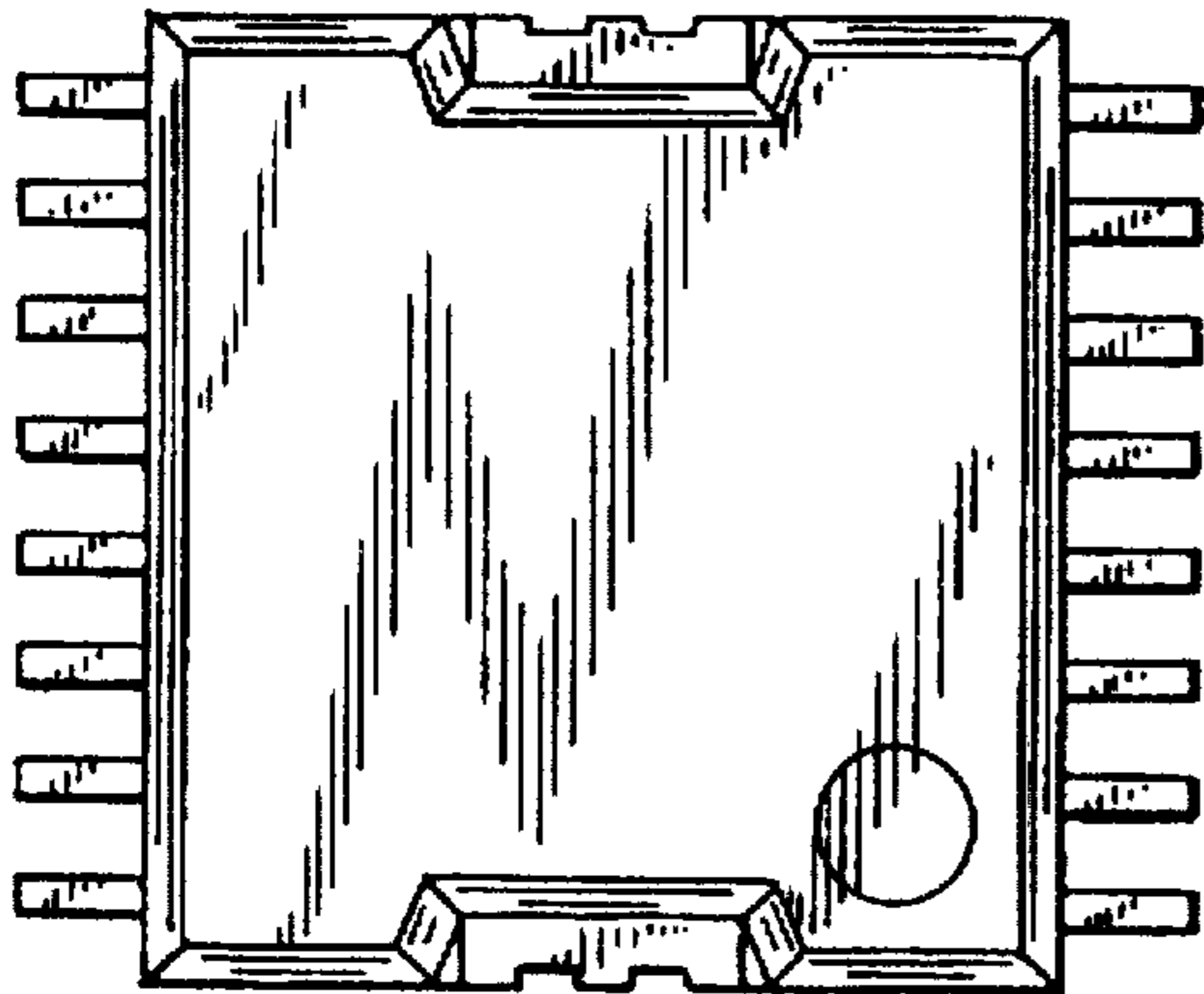


FIG. 4

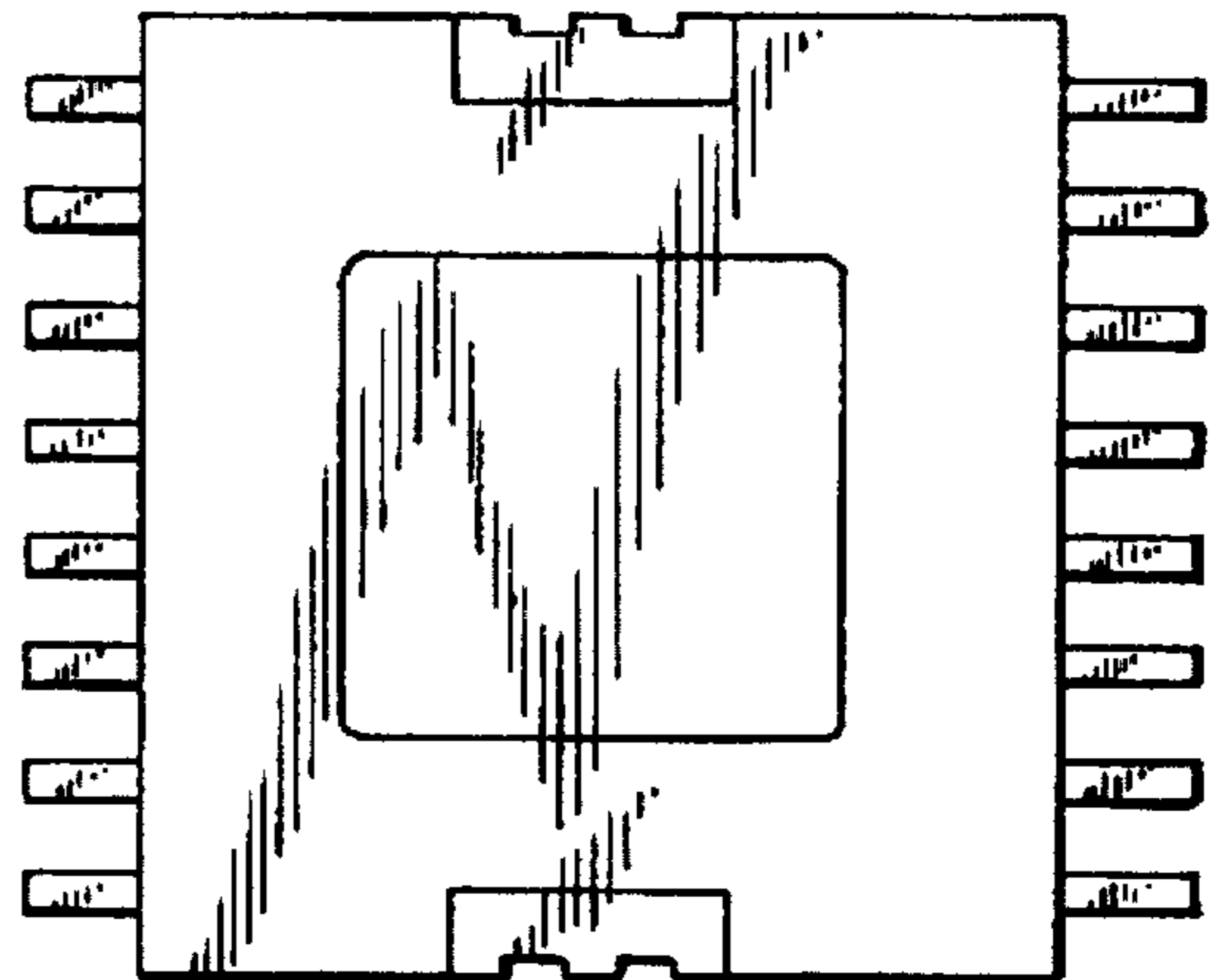


FIG. 5

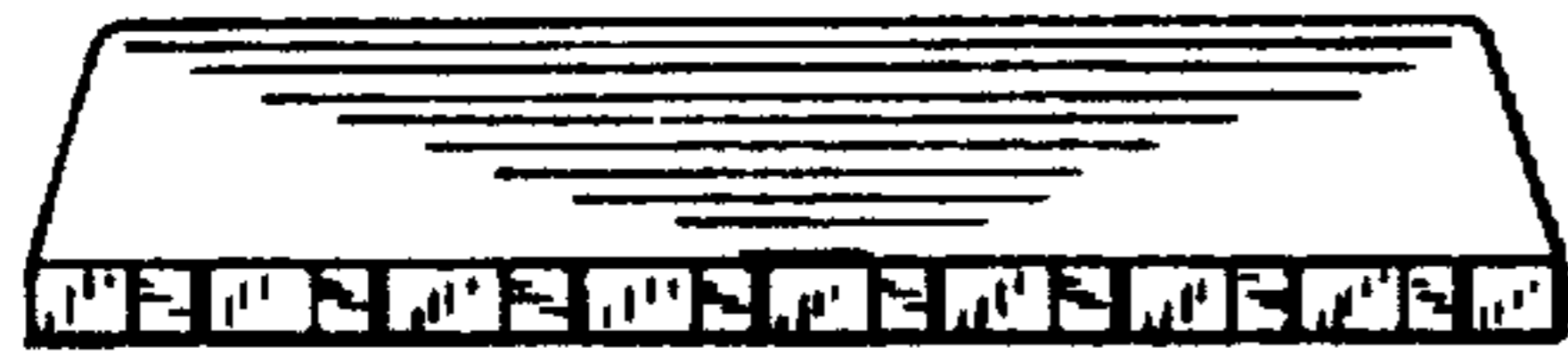


FIG. 6

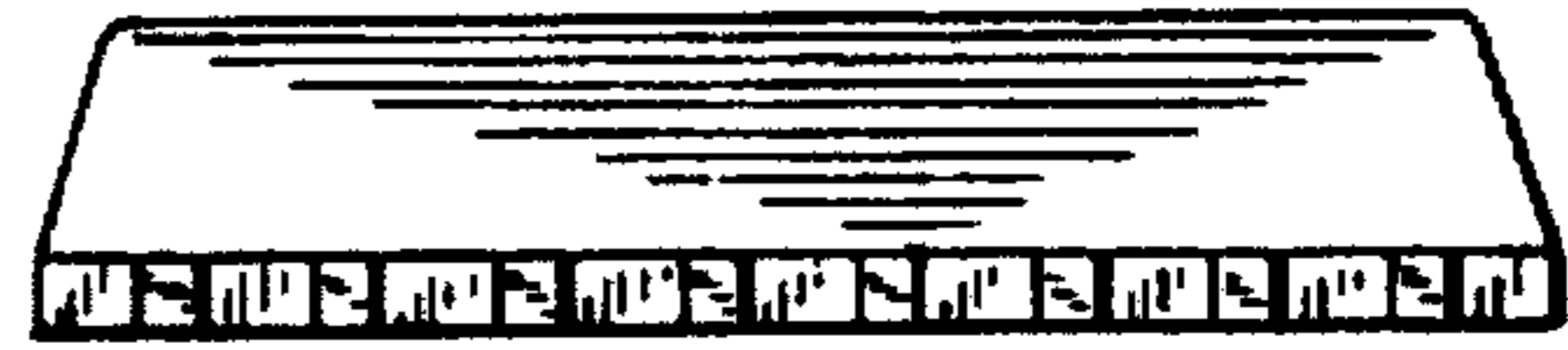


FIG. 7

