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United States Patent [19]

Takagi et al.

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[45] **Date of Patent: **Aug. 4, 1998**

[54] **SEMICONDUCTOR PACKAGE**

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[73] Assignee: **Sony Corporation**, Tokyo, Japan

[**] Term: **14 Years**

[21] Appl. No.: **65,264**

[22] Filed: **Jan. 30, 1997**

[51] **LOC (6) Cl.** **13-03**

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; 174/52.2–52.4; 206/710–719; 257/254, 659, 666, 678–697, 709, 730, 738, 780, 796; 437/183, 217, 220; 361/730

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Assistant Examiner—Cathron B. Matta
Attorney, Agent, or Firm—Foley & Lardner

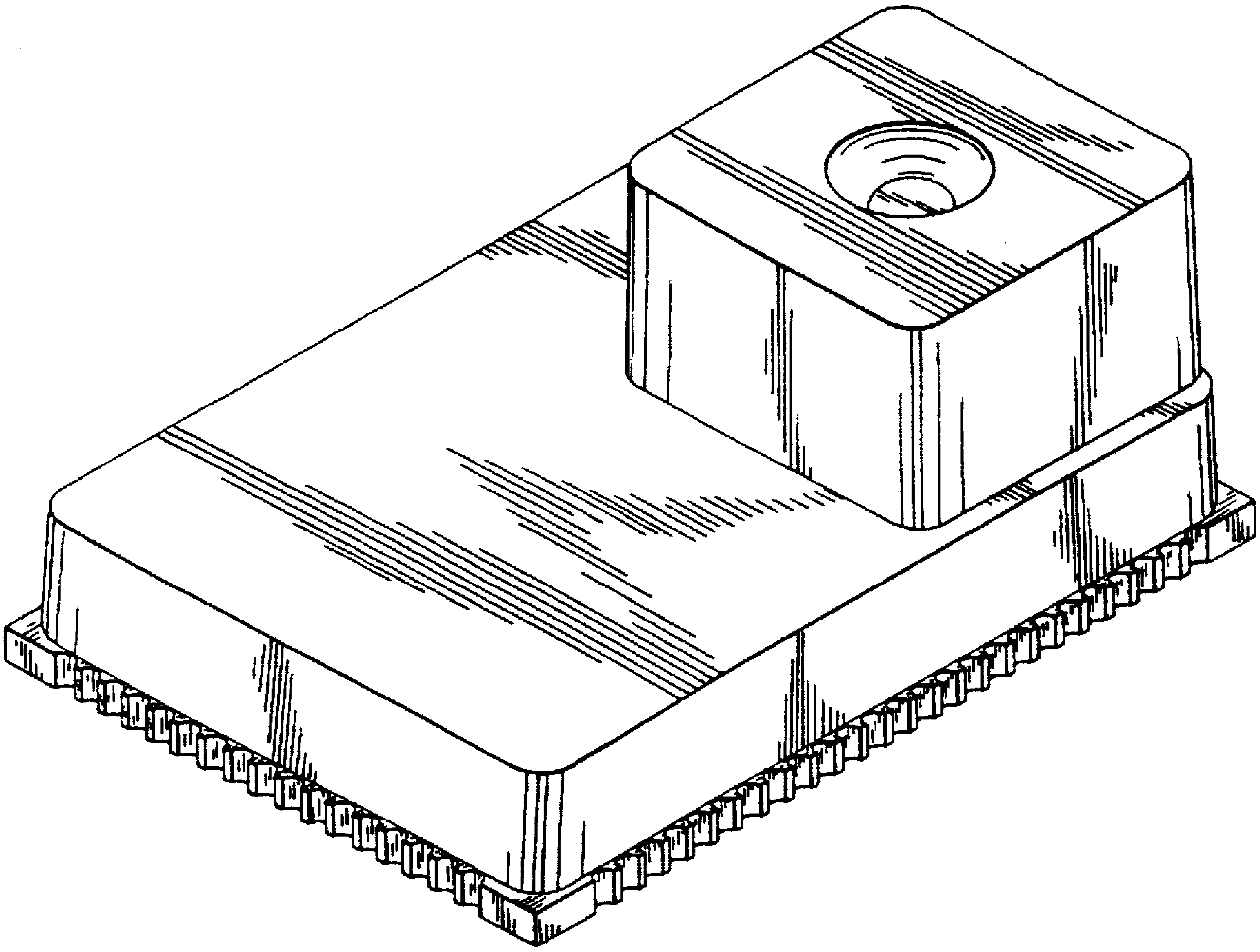
[57] **CLAIM**

The ornamental design for a semiconductor package, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of a semiconductor package showing our new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a left side elevational view thereof;
FIG. **4** is a front elevational view thereof;
FIG. **5** is a bottom plan view thereof;
FIG. **6** is a right side elevational view thereof;
FIG. **7** is a rear elevational view thereof;
FIG. **8** is a perspective view of another embodiment of a semiconductor package showing our new design; and,
FIG. **9** is a front elevational view of the embodiment of FIG. **8**. The rest of views of the embodiment of FIG. **8** are the same as those of the embodiment of FIG. **1**.

1 Claim, 4 Drawing Sheets



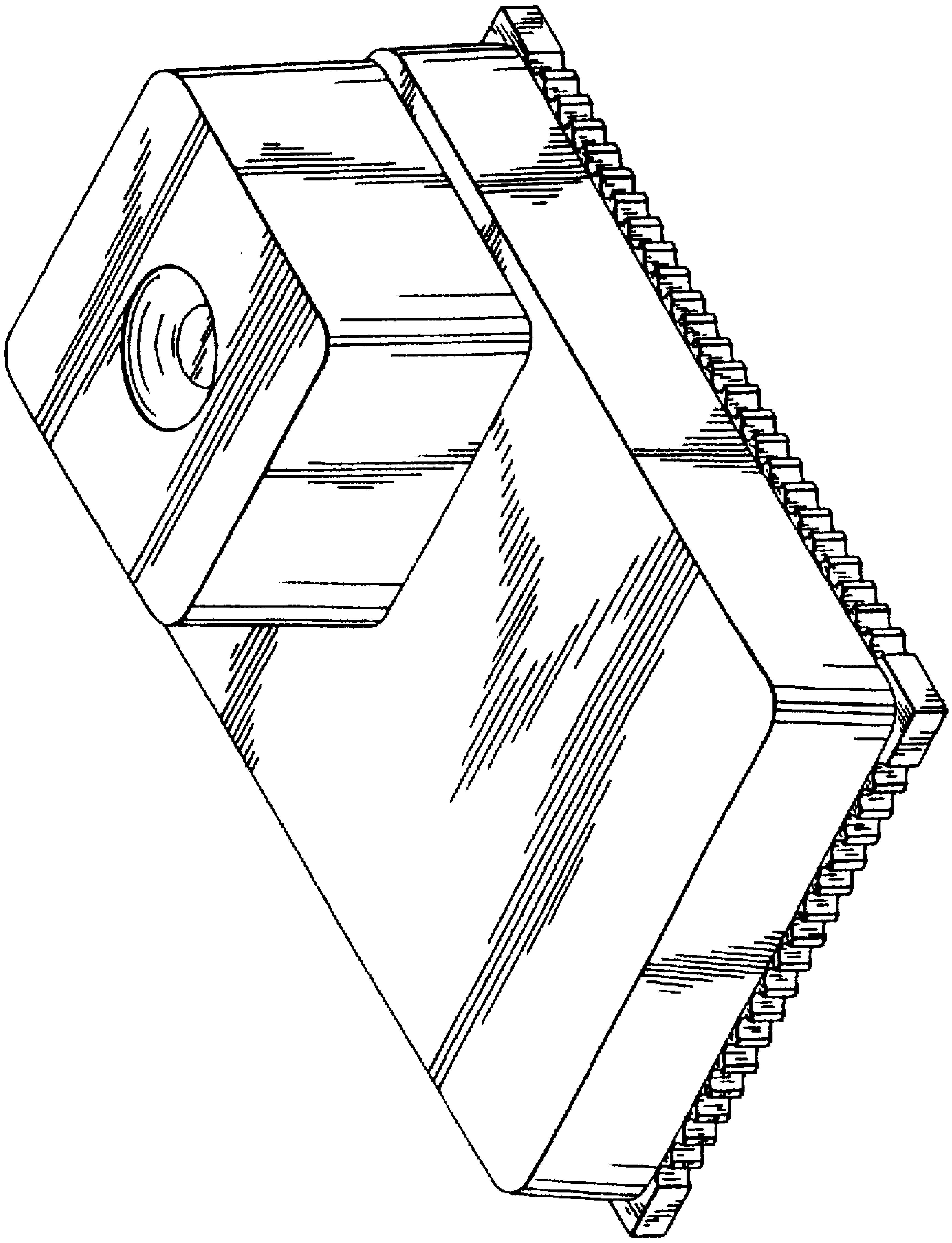


FIG. 1

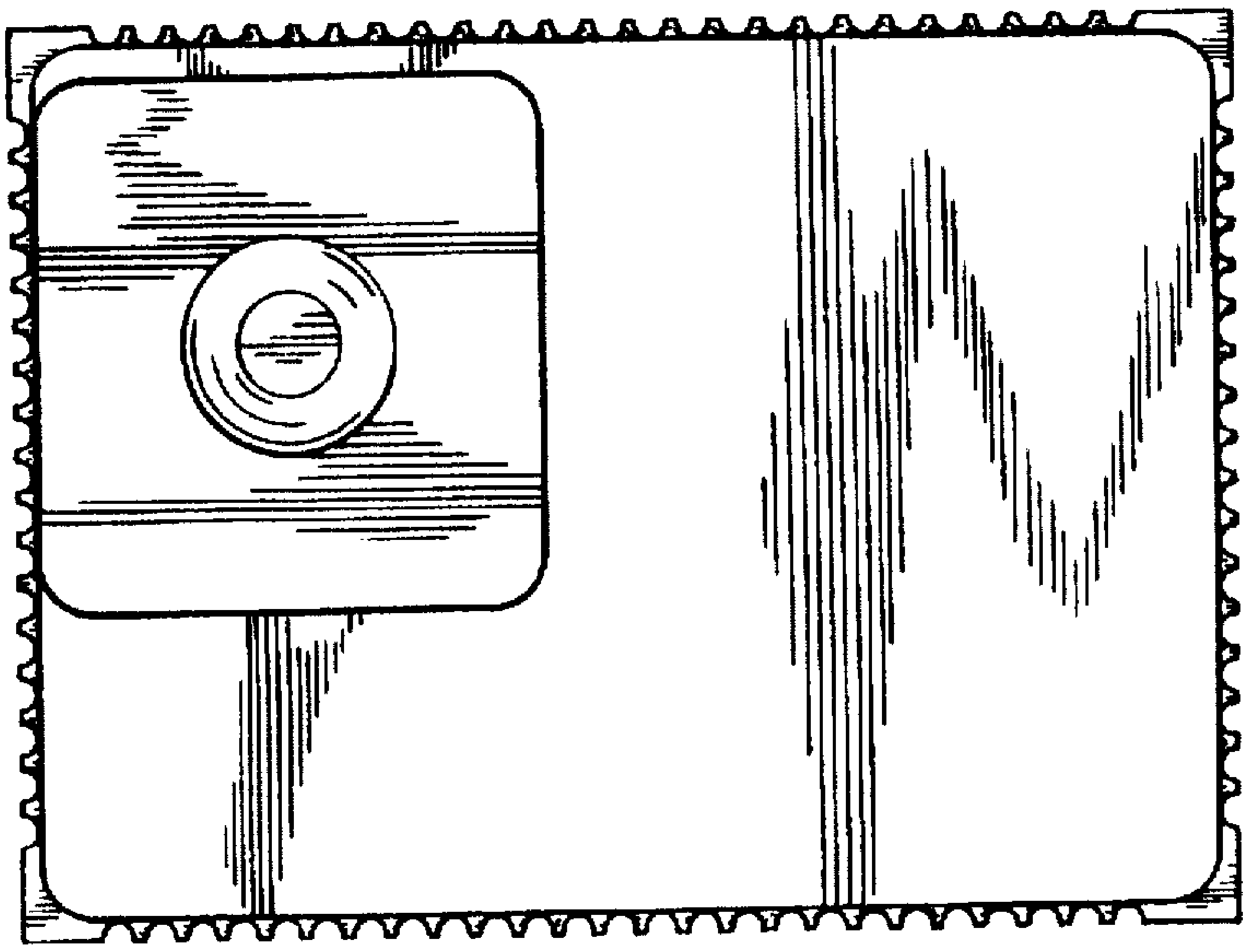


FIG. 4

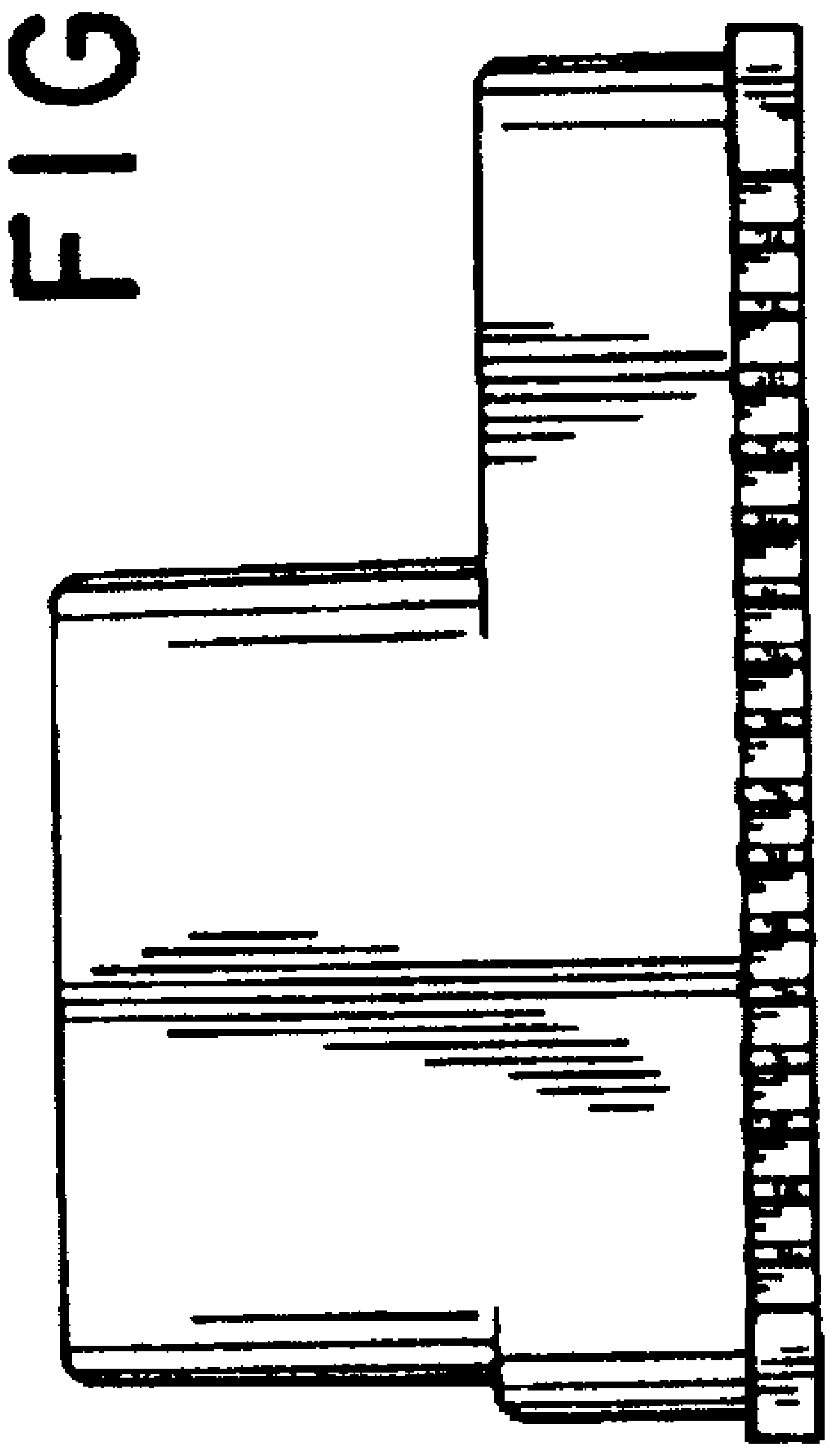


FIG. 2

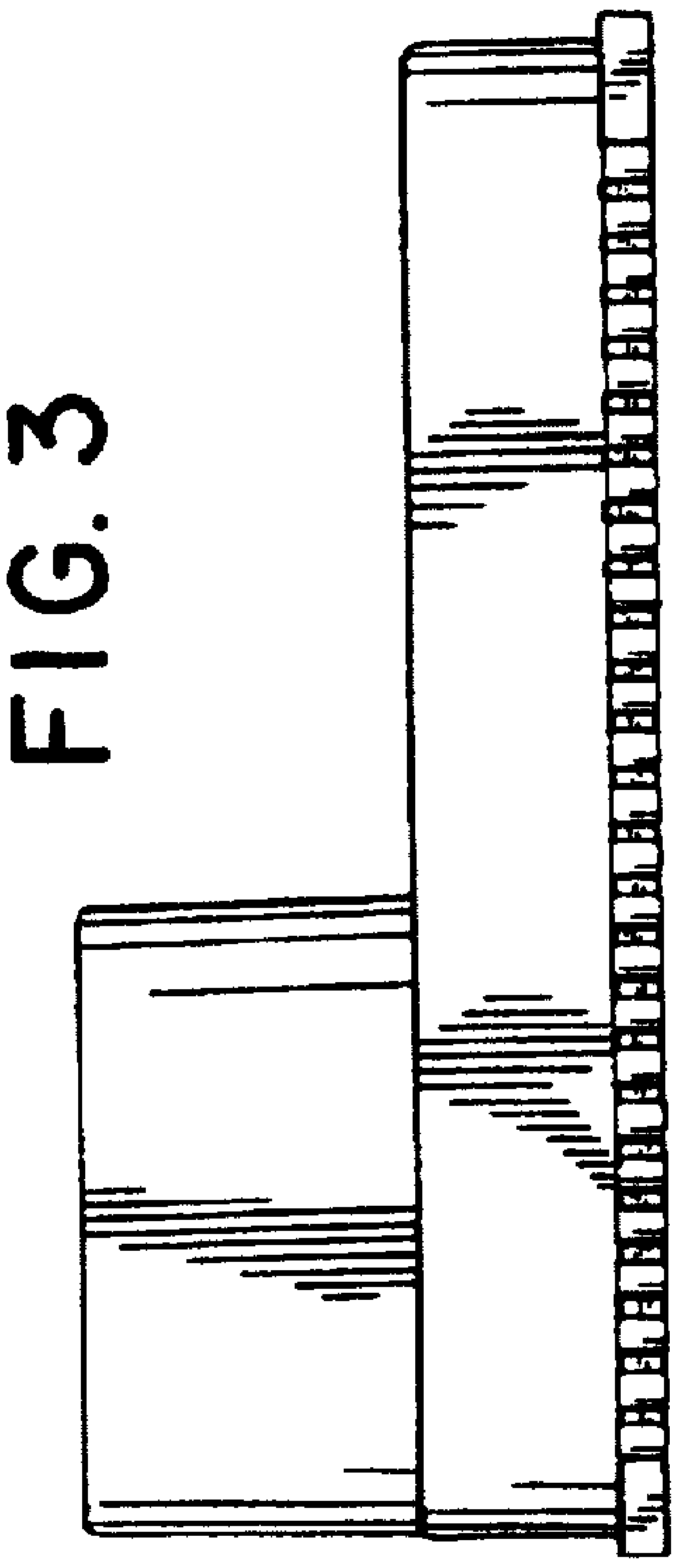


FIG. 3

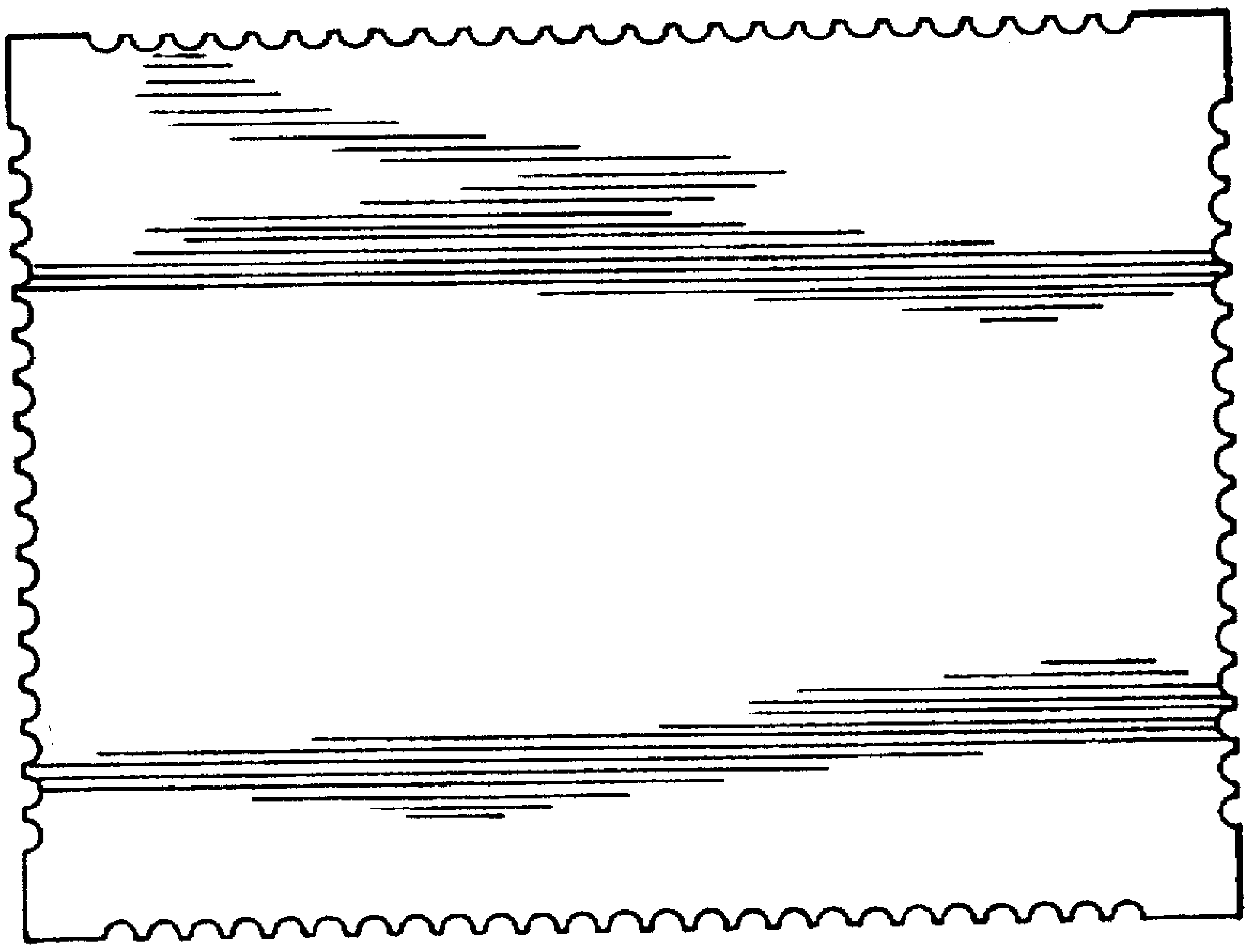


FIG.7

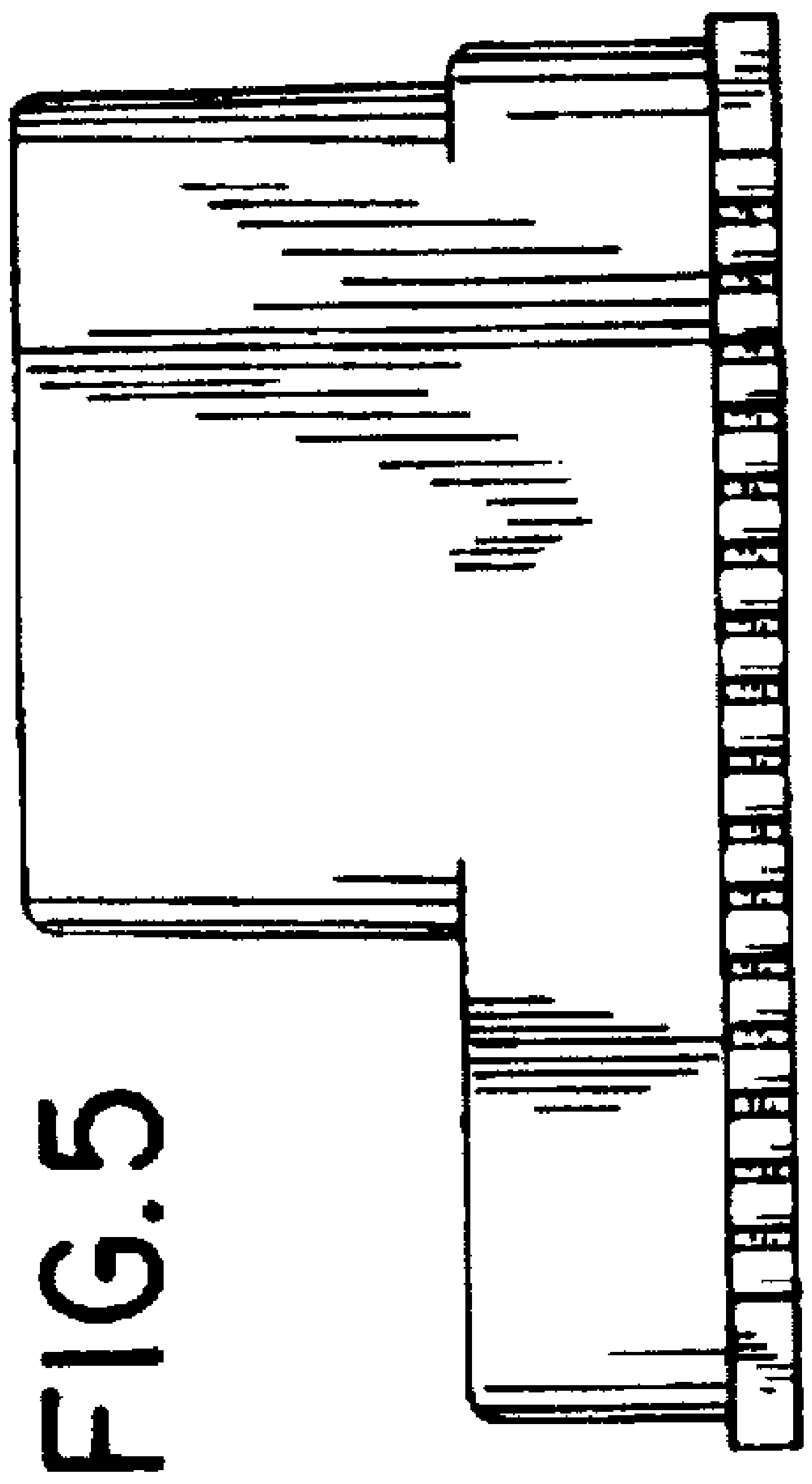


FIG.5

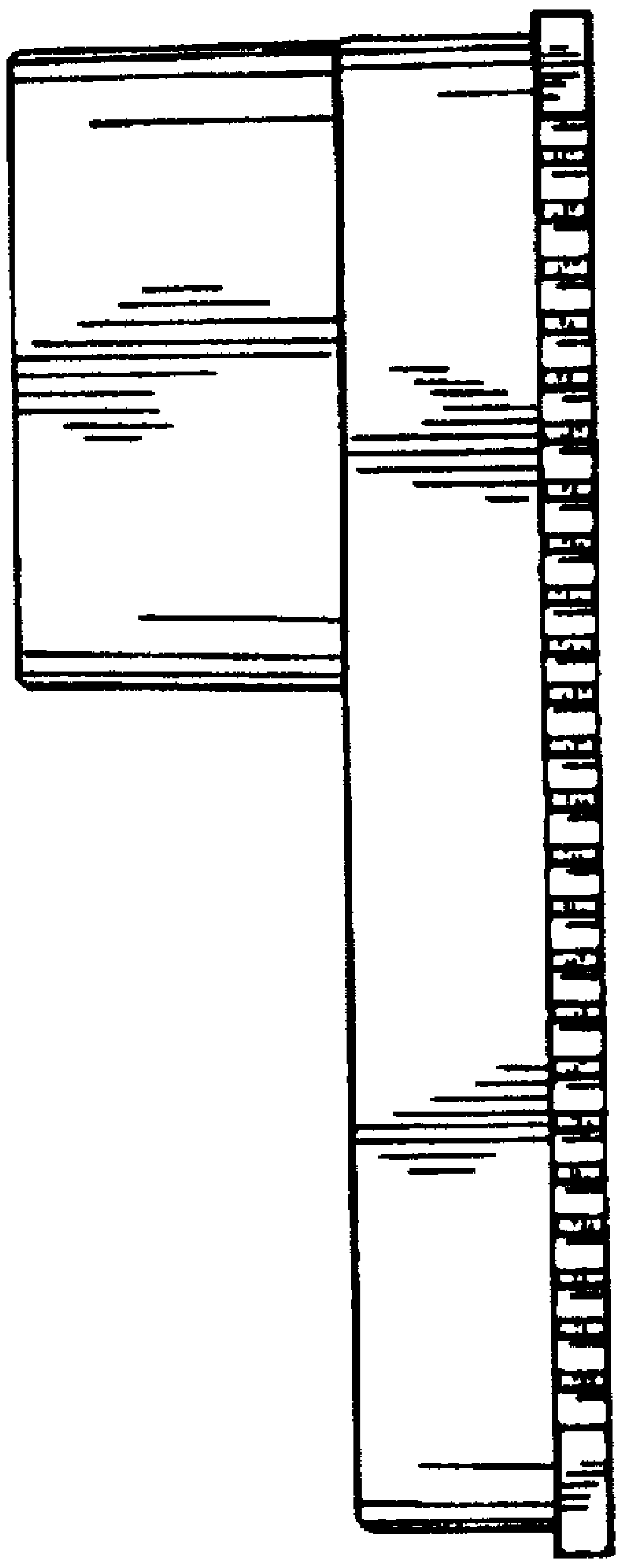


FIG.6

FIG. 8

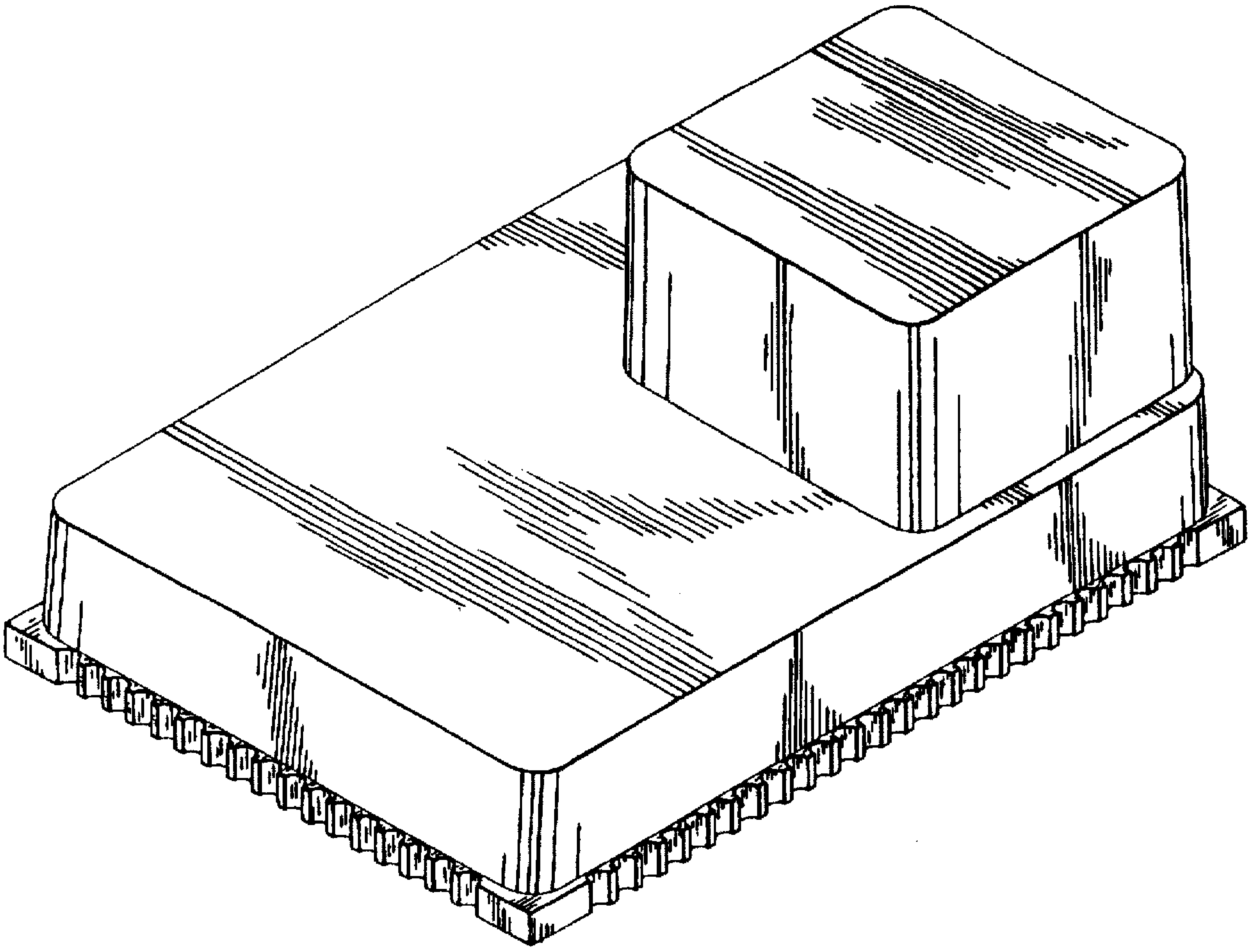


FIG. 9