



US00D396211S

United States Patent [19]

Enomoto et al.

[11] Patent Number: **Des. 396,211**

[45] Date of Patent: ****Jul. 21, 1998**

[54] **INTEGRATED CIRCUIT DEVICE**
[75] Inventors: **Yoshinari Enomoto; Satomi Kajiwara,**
both of Kanagawa, Japan

[73] Assignee: **Fuji Electric Co., Ltd., Kanagawa,**
Japan

[**] Term: **14 Years**

[21] Appl. No.: **68,462**

[22] Filed: **Mar. 3, 1997**

[30] **Foreign Application Priority Data**
Sep. 9, 1996 [JP] Japan 8-26833

[51] **LOC (6) Cl.** **13-03**
[52] **U.S. Cl.** **D13/182**
[58] **Field of Search** D13/123, 125,
D13/182; 174/52.1, 52.4; 439/55; 361/718,
820

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 317,592 6/1991 Yoshizawa D13/182
D. 345,731 4/1994 Owens et al. D13/182

D. 358,806 5/1995 Siegel et al. D13/182
D. 359,028 6/1995 Siegel et al. D13/182
D. 362,258 9/1995 Izumi et al. .
D. 362,259 9/1995 Izumi et al. .
4,868,349 9/1989 Chia 174/52.4
5,220,298 6/1993 Nagase 361/820 X
5,221,859 6/1993 Kobayashi et al. 174/52.4
5,585,670 12/1996 Isshiki et al. 361/820 X

Primary Examiner—Brian N. Vinson
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak
& Seas, PLLC

[57] **CLAIM**

The ornamental design for an integrated circuit device, as shown.

DESCRIPTION

FIG. 1 is a perspective view of the top, front and left side of an integrated circuit device showing our new design; FIG. 2 is a top plan view thereof; FIG. 3 is a bottom plan view thereof; FIG. 4 is a left side elevational view thereof; FIG. 5 is a right side elevational view thereof; FIG. 6 is a front elevational view thereof; and, FIG. 7 is a rear elevational view thereof.

1 Claim, 4 Drawing Sheets

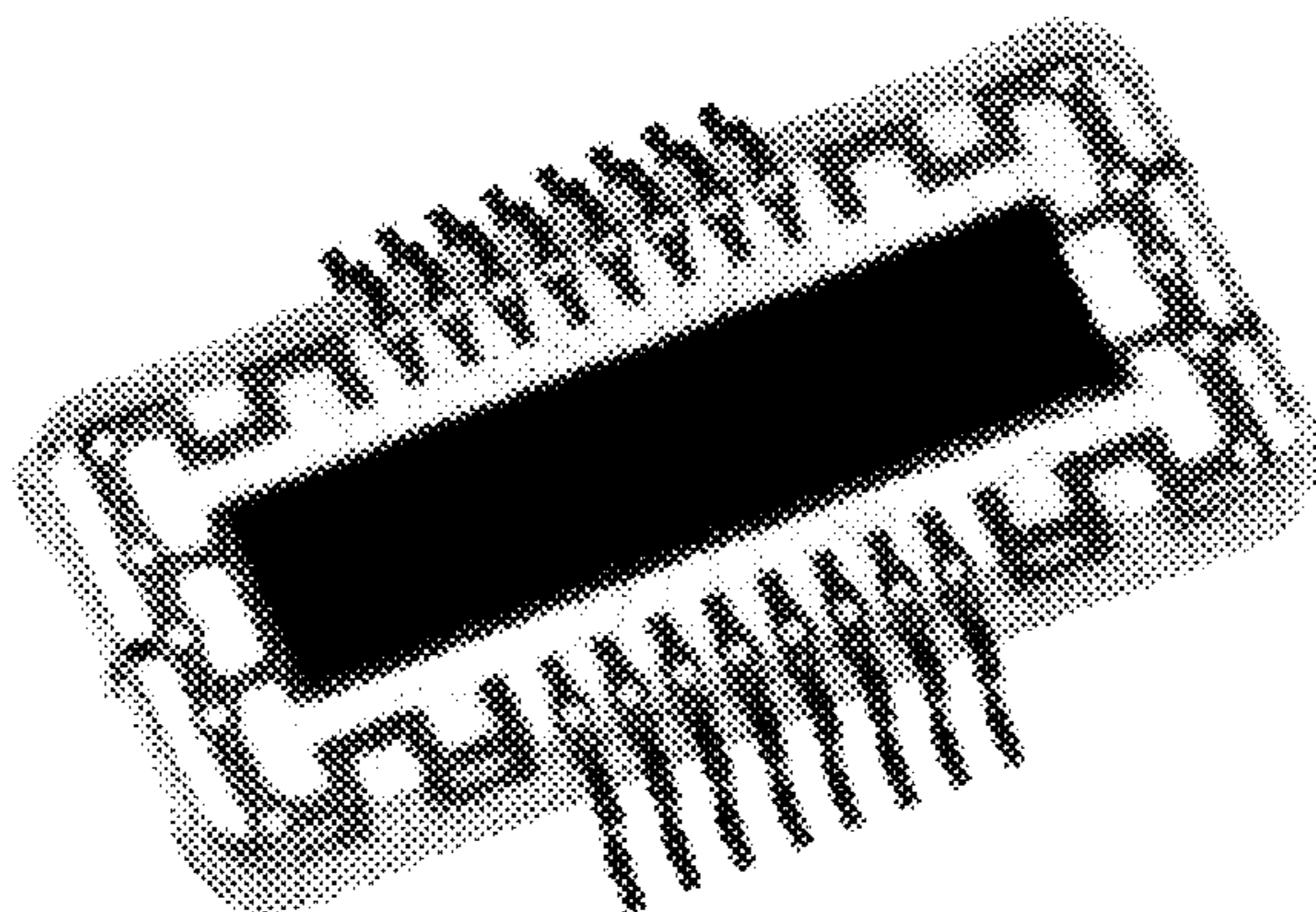


FIG. 1

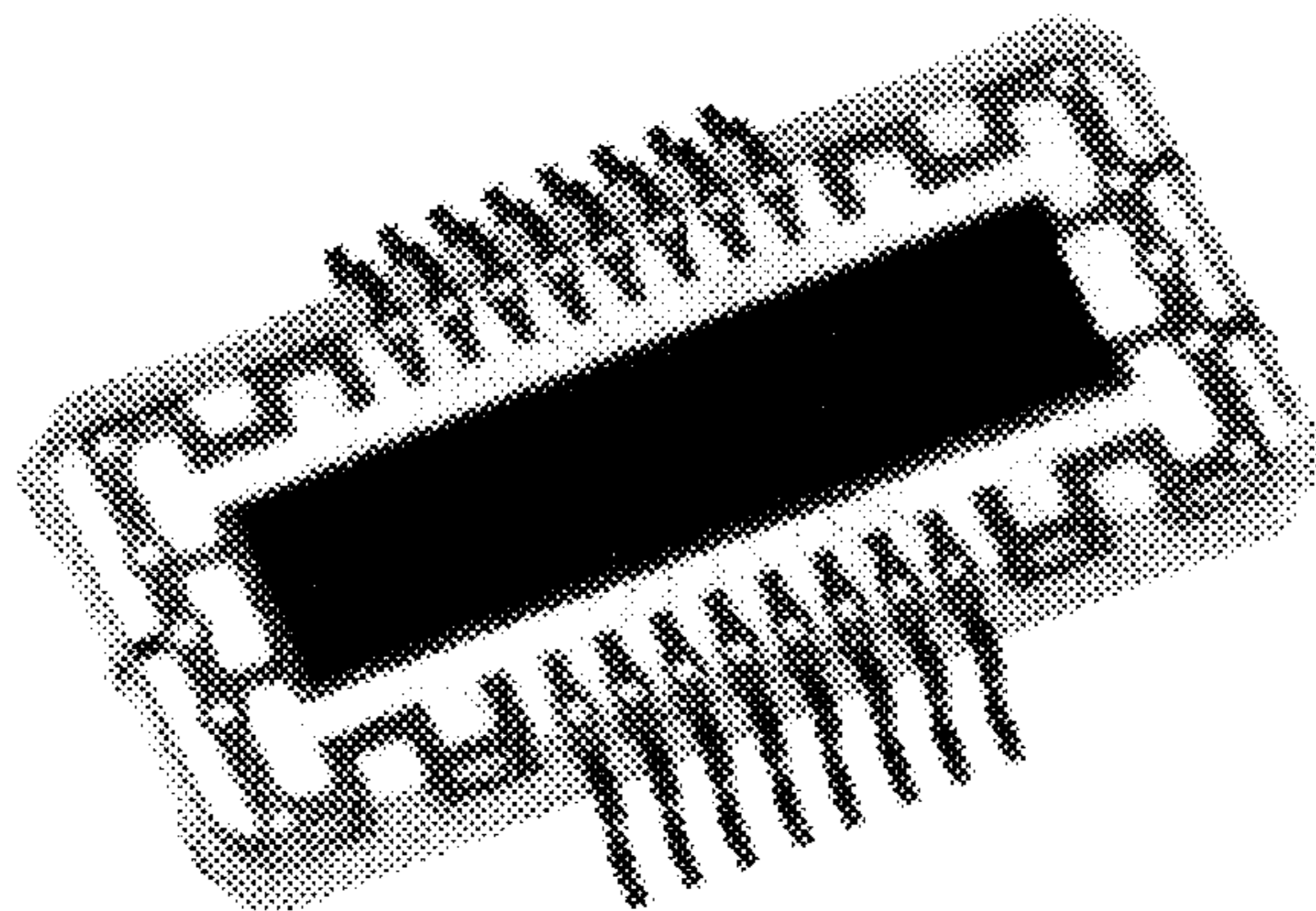


FIG. 2

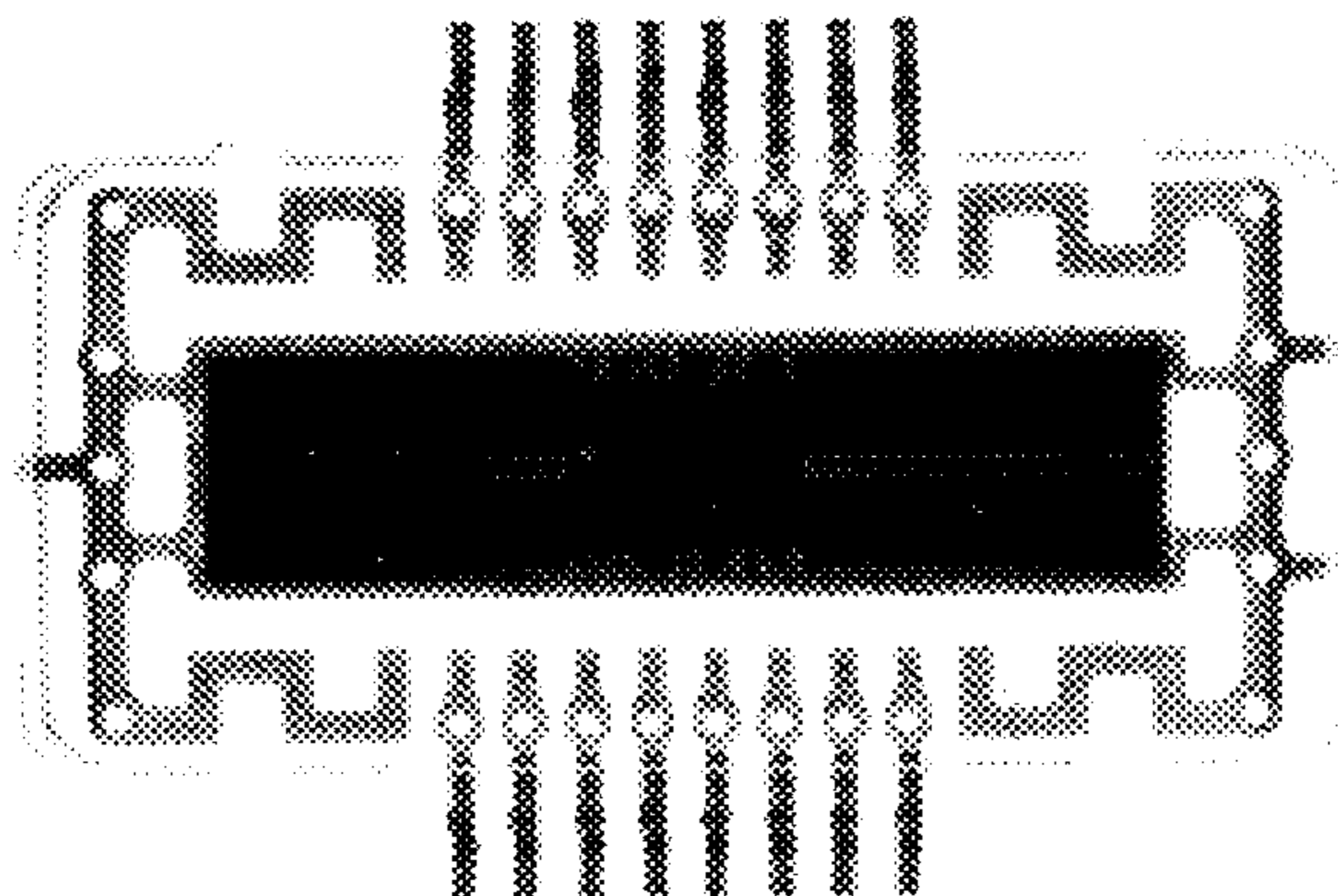


FIG. 3

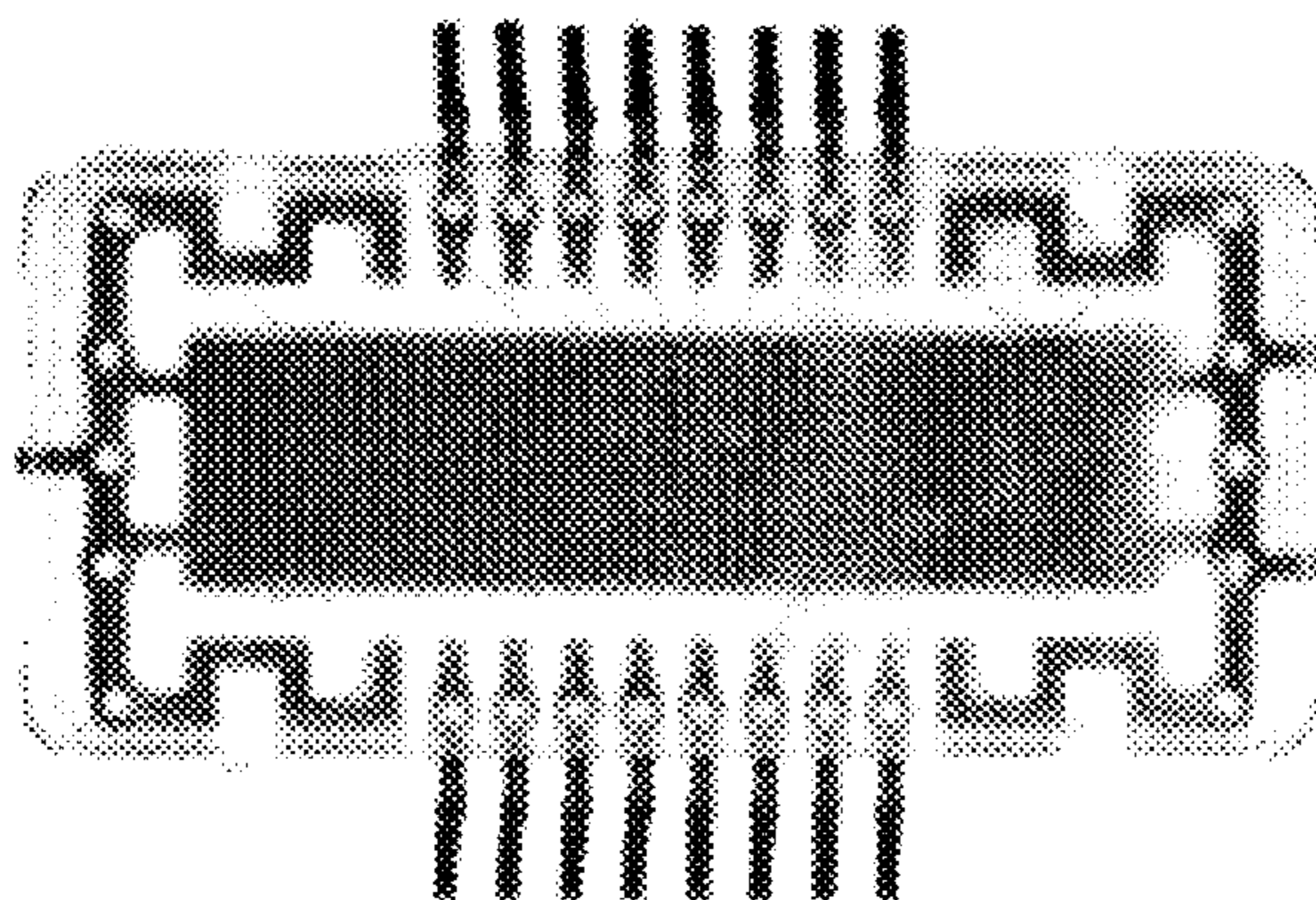


FIG. 4



FIG. 5



FIG. 6

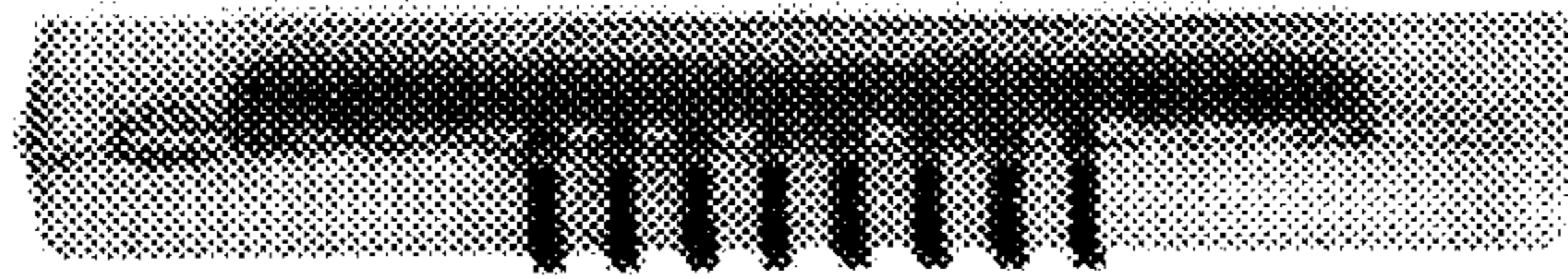


FIG. 7

