

US00D392544S

United States Patent [19]
Nakamura

[11] **Patent Number: Des. 392,544**
[45] **Date of Patent: **Mar. 24, 1998**

[54] **ELECTRONIC COMPONENT SPACER**

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[73] **Assignee: Shinagawa Shoko Co., Ltd., Tokyo, Japan**

[**] **Term: 14 Years**

[21] **Appl. No.: 69,569**

[22] **Filed: Apr. 29, 1997**

[30] **Foreign Application Priority Data**

Nov. 8, 1996 [JP] Japan 8-33572

[51] **LOC (6) Cl. 08-05**

[52] **U.S. Cl. D8/354**

[58] **Field of Search D8/354, 382; 174/138 D;
24/305, 453, 136 R; 403/408.1; 248/73,
71, 74.2, 74.3**

[56] **References Cited**

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[57] **CLAIM**

The ornamental design for an electronic component spacer, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of an electronic component spacer embodying the present design;
 FIG. 2 is a front view thereof;
 FIG. 3 is a rear view thereof;
 FIG. 4 is a top plan view thereof;
 FIG. 5 is a bottom view thereof;
 FIG. 6 is a left side view thereof;
 FIG. 7 is a right side view thereof;
 FIG. 8 is a perspective view thereof in an opened state;
 FIG. 9 is a front view thereof in an opened state;
 FIG. 10 is a rear view thereof in an opened state;
 FIG. 11 is a top plan view thereof in an opened state;
 FIG. 12 is a bottom view thereof in an opened state;
 FIG. 13 is a left side view thereof in an opened state;
 FIG. 14 is a right side view thereof in an opened state; and,
 FIG. 15 is a typical referential front view thereof when it is used.
 The elements shown in broken lines in FIG. 15 are for illustrative purposes only and form no part of the claimed design.

1 Claim, 5 Drawing Sheets

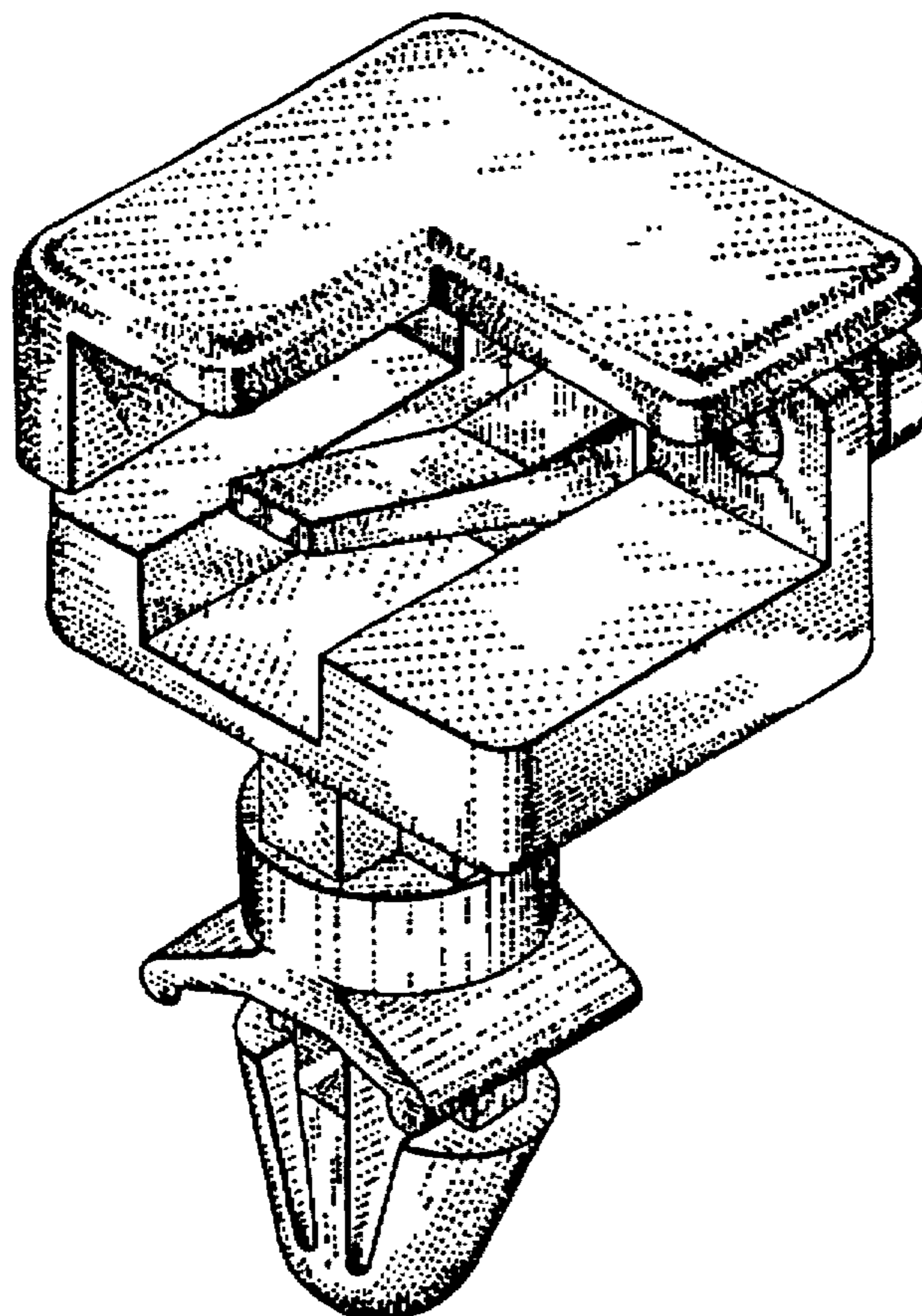


FIG. 1

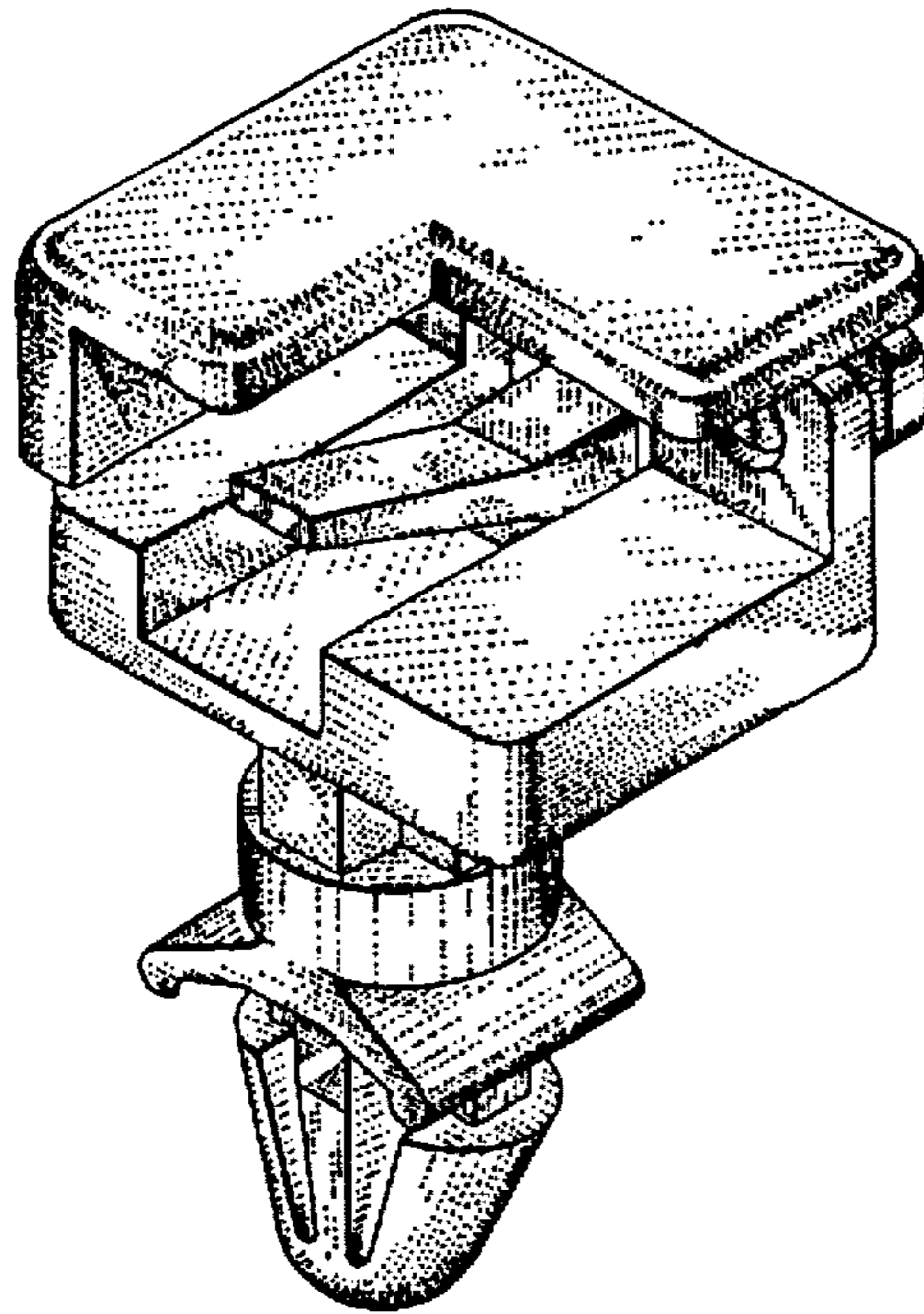


FIG. 2

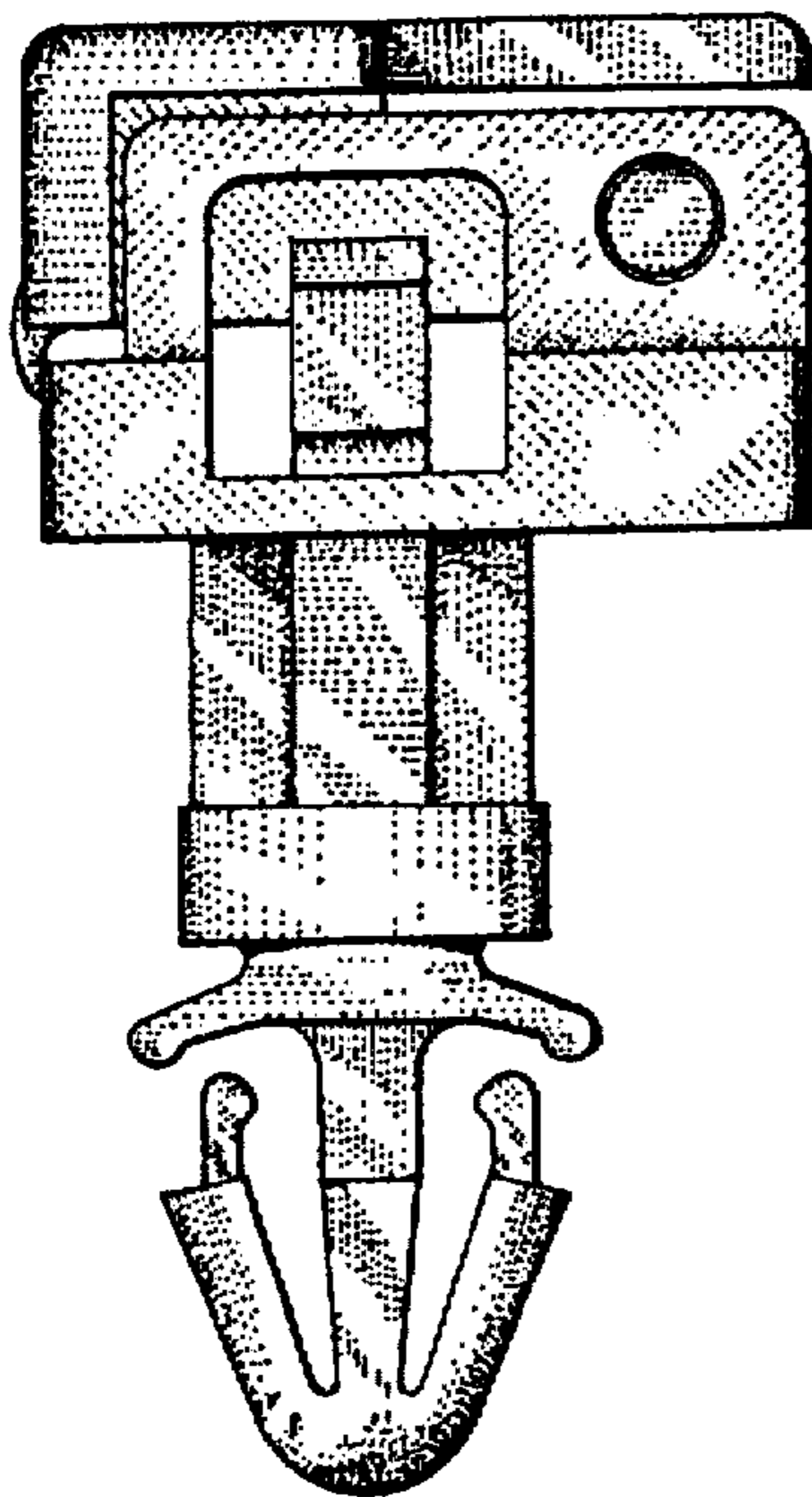


FIG. 3

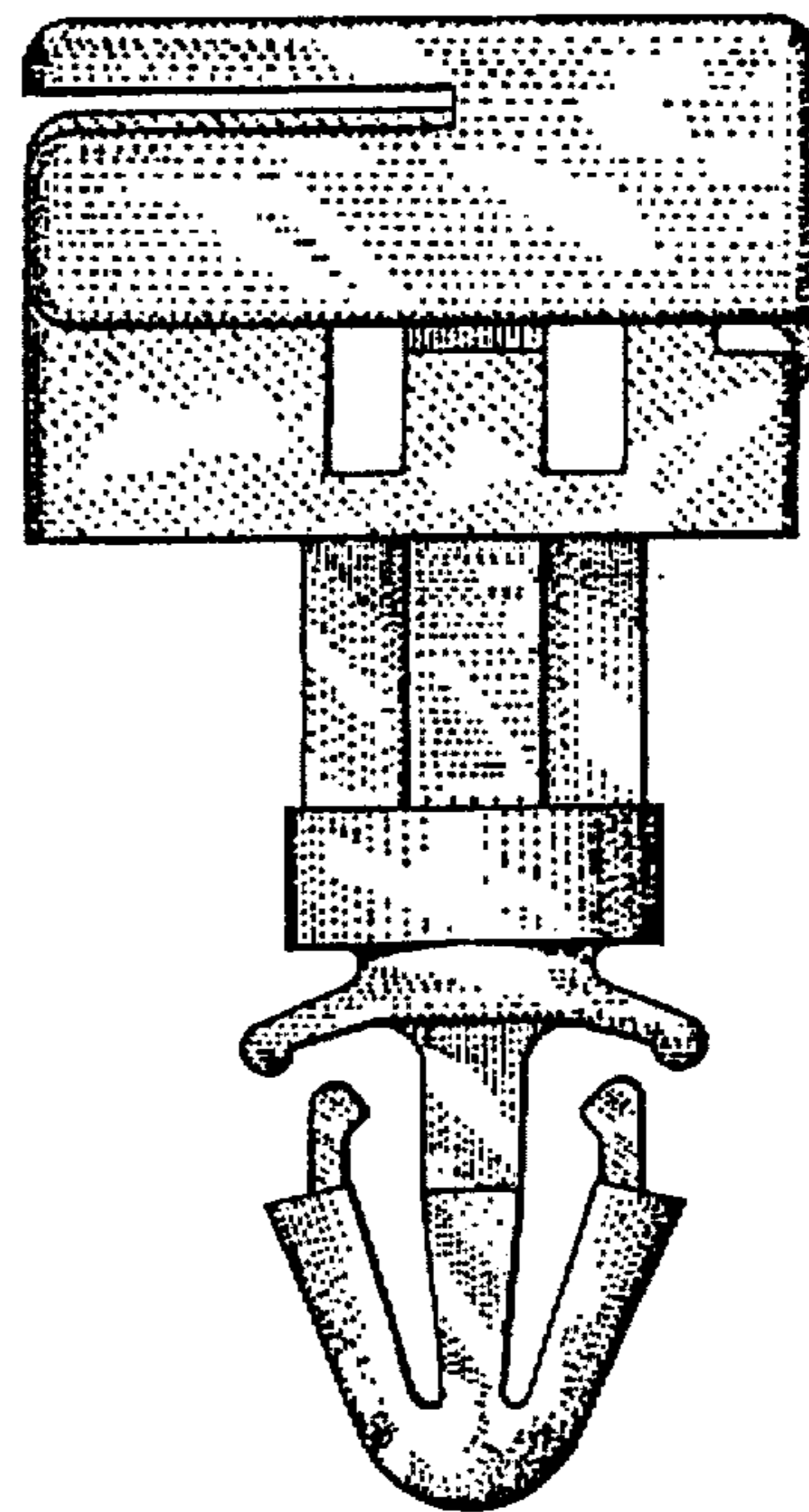


FIG. 4

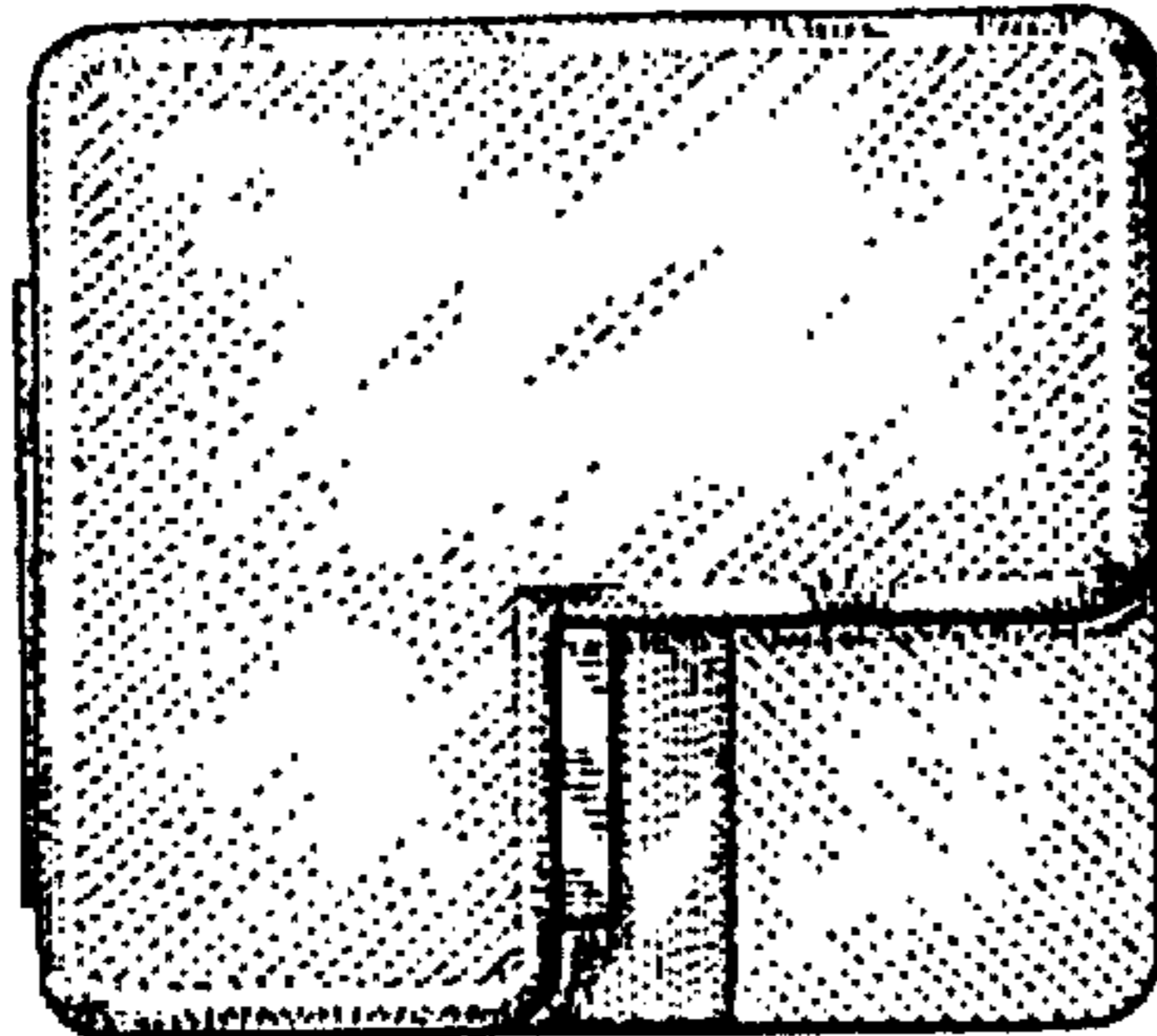


FIG. 5

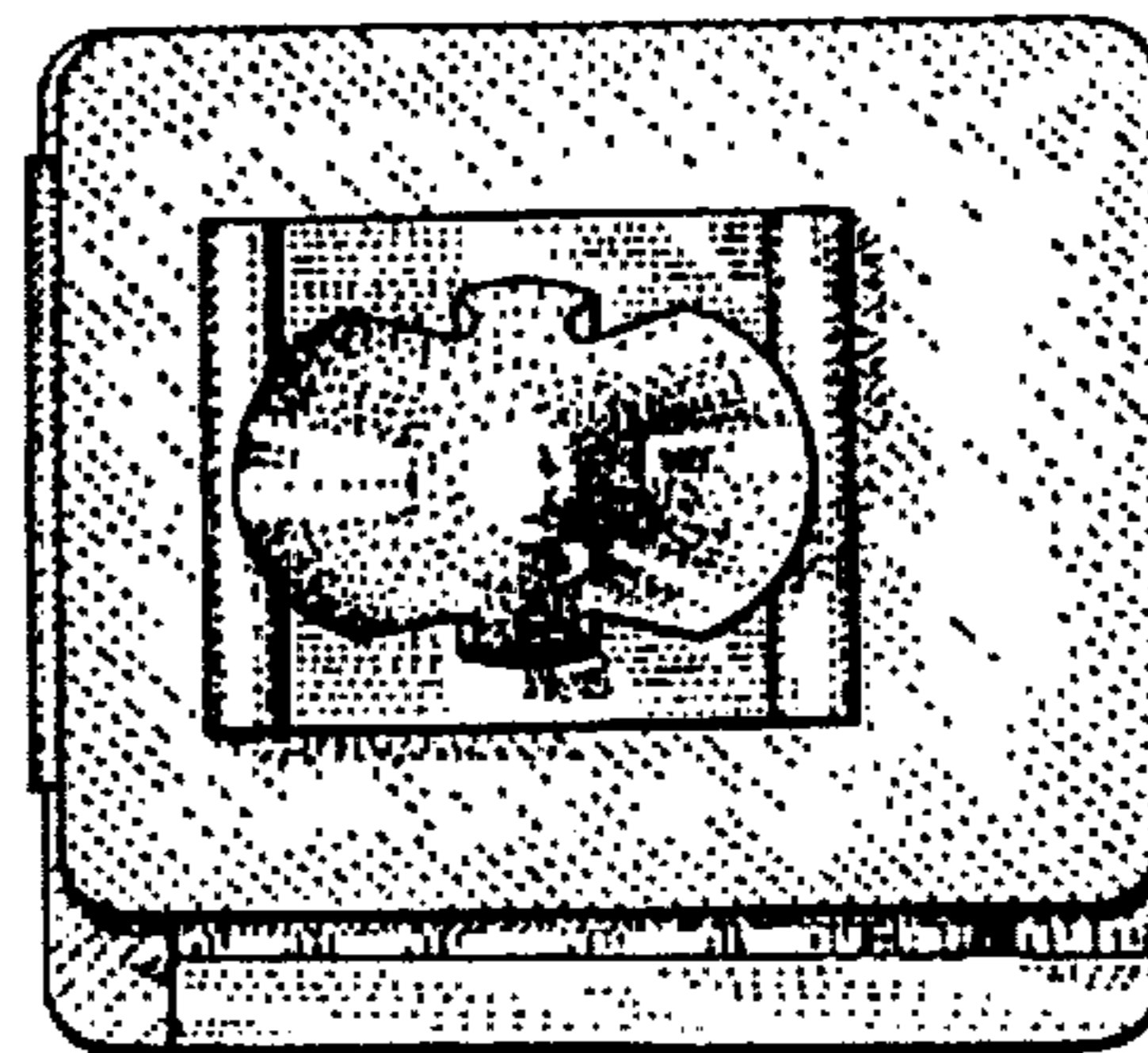


FIG. 6

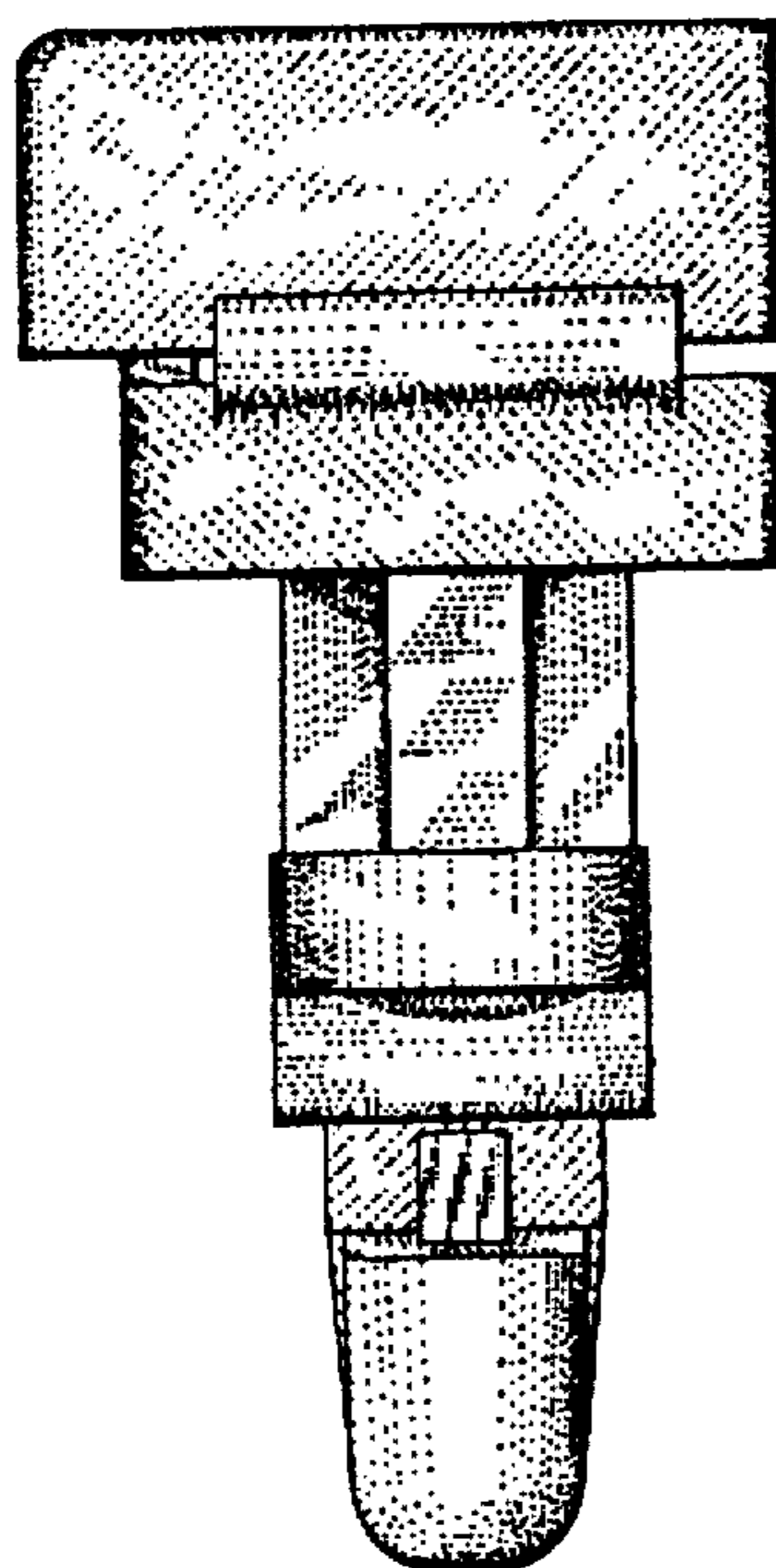


FIG. 7

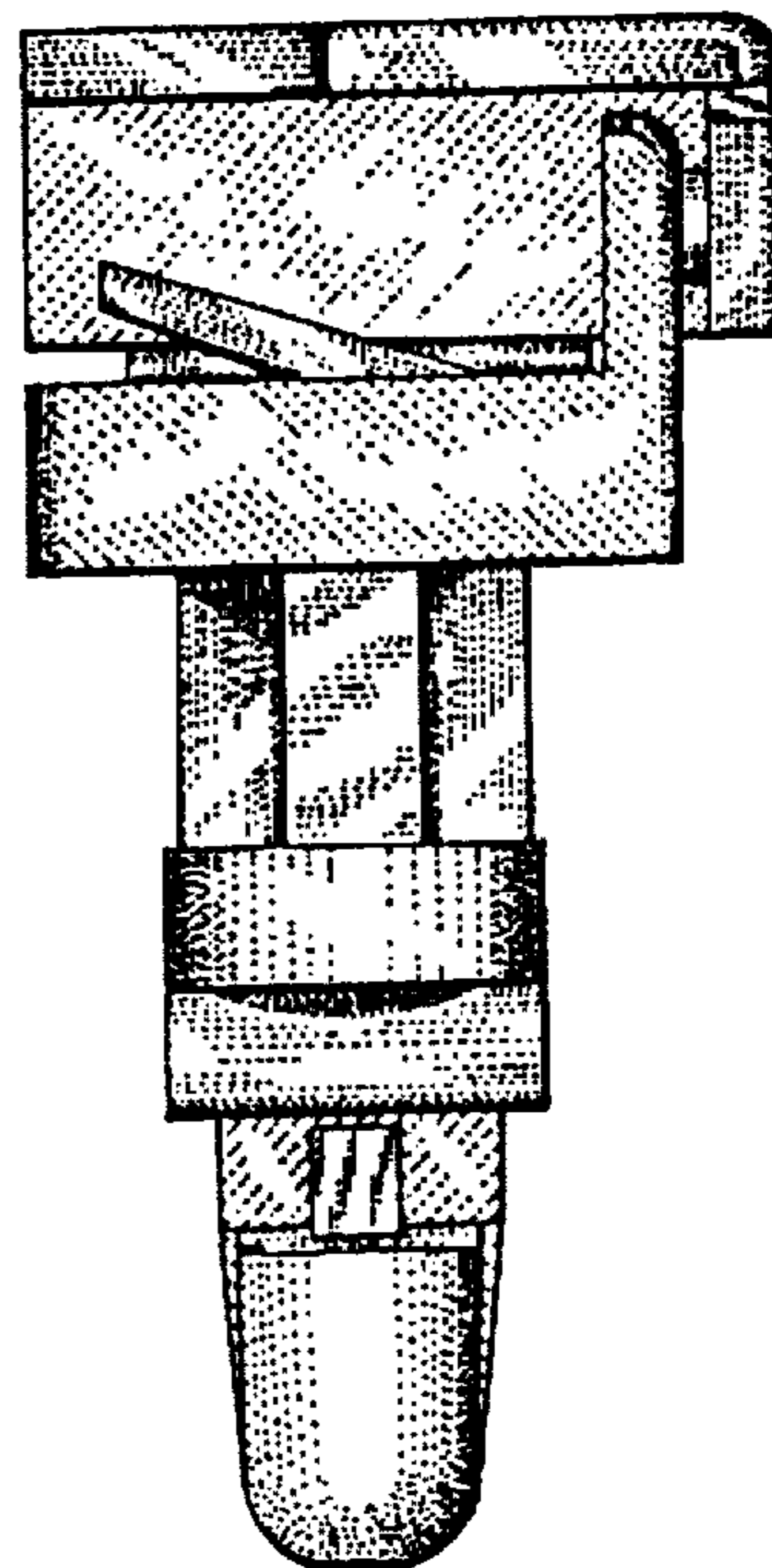


FIG. 8

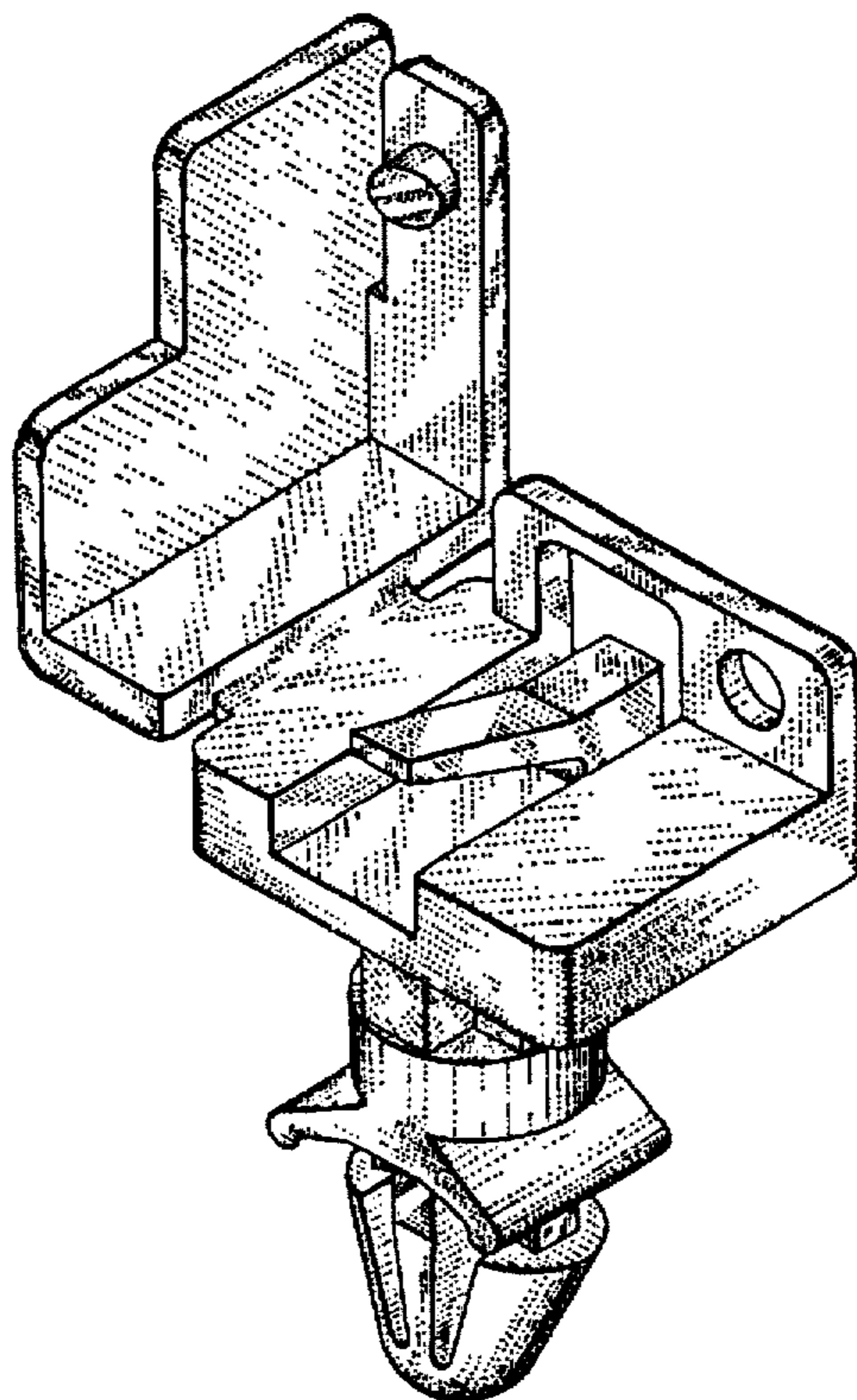


FIG. 9

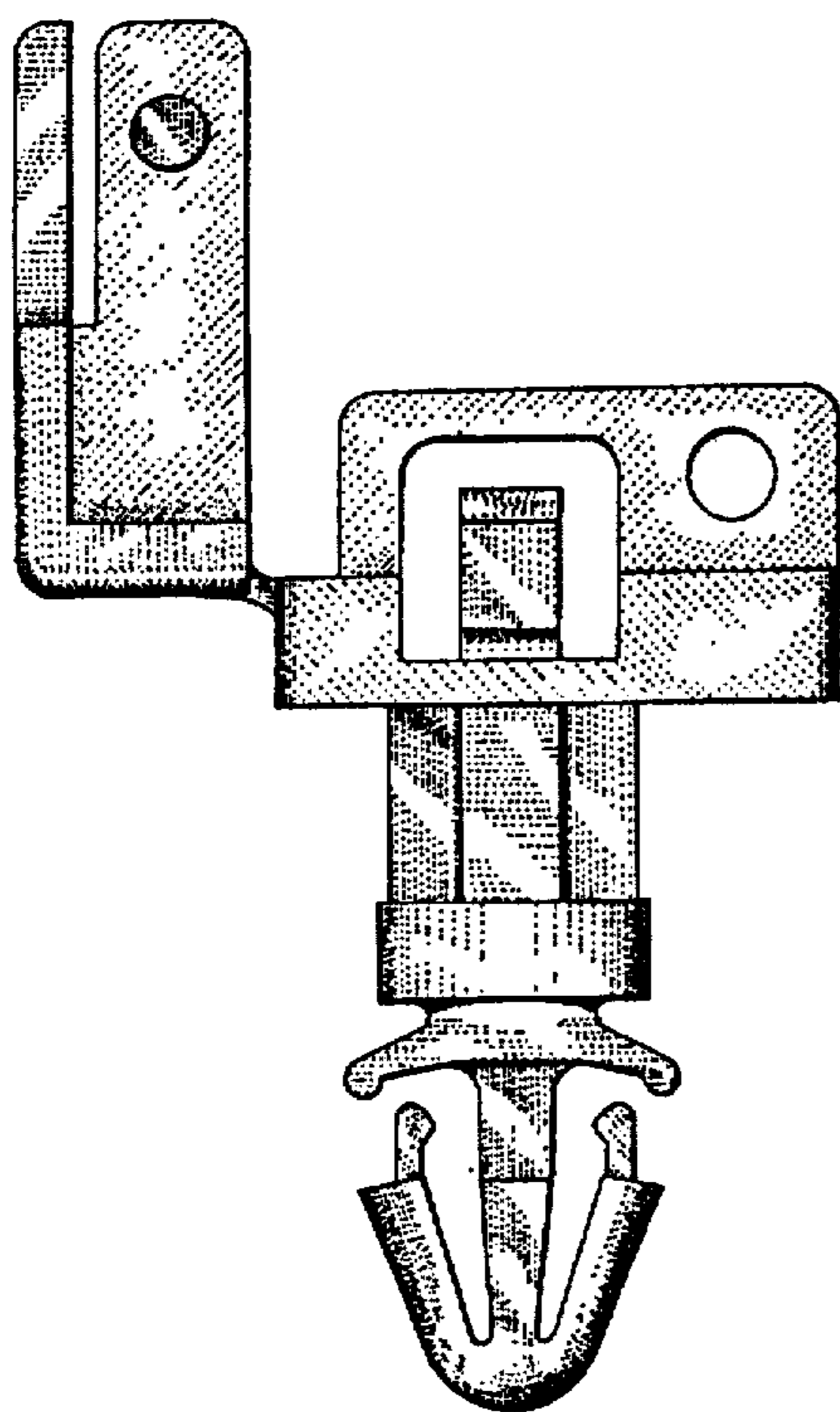


FIG. 10

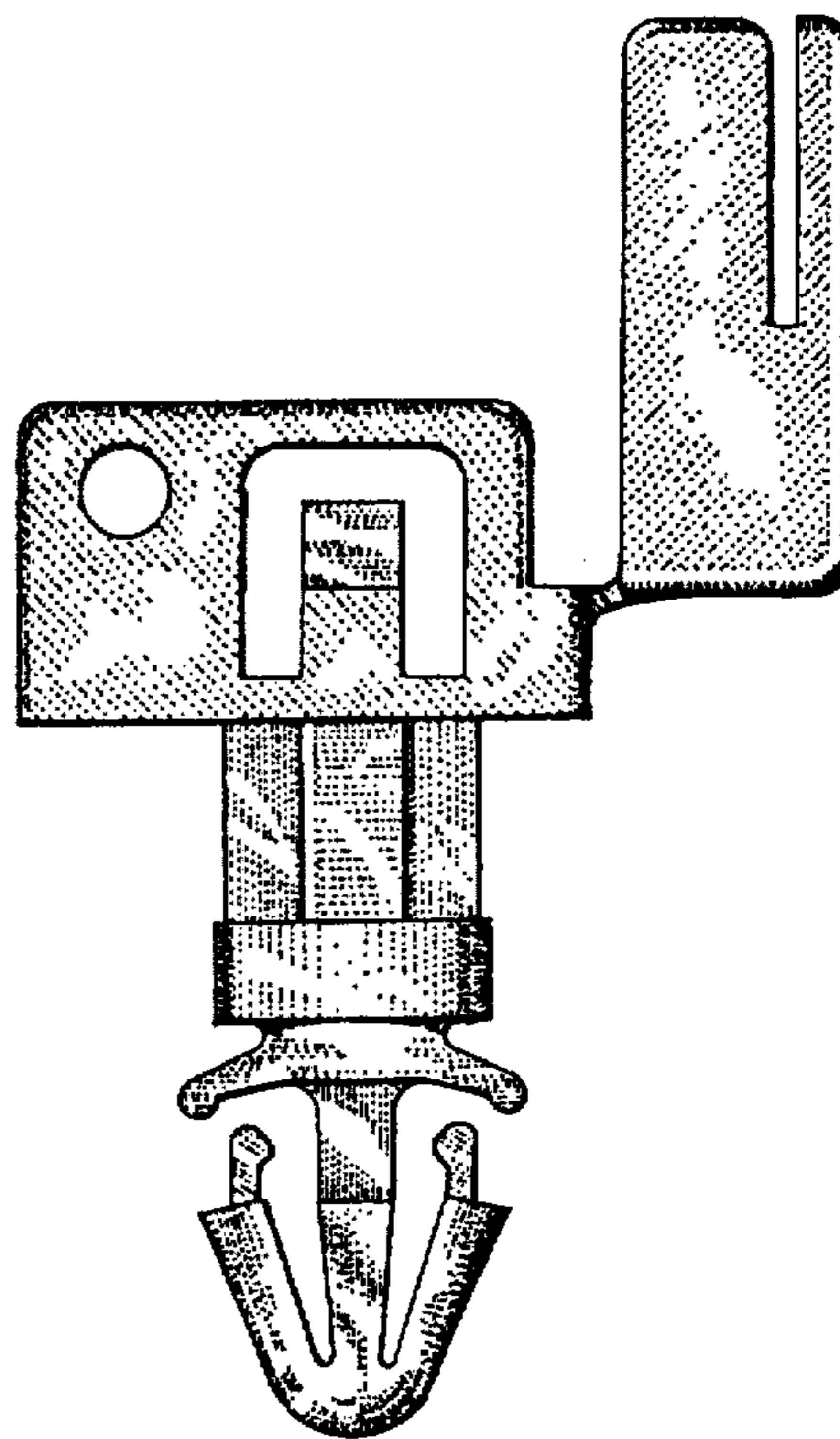


FIG. 11

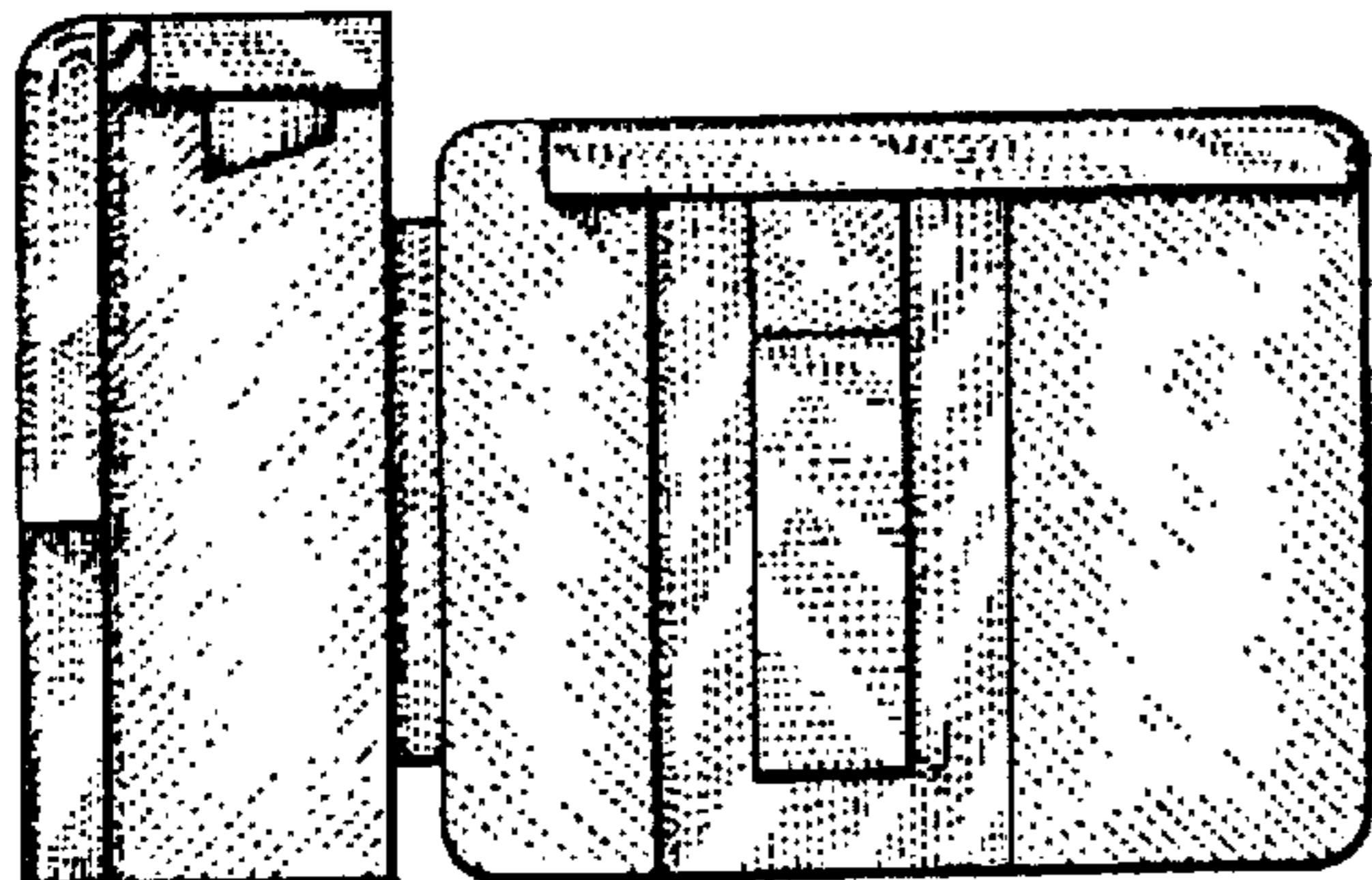


FIG. 12

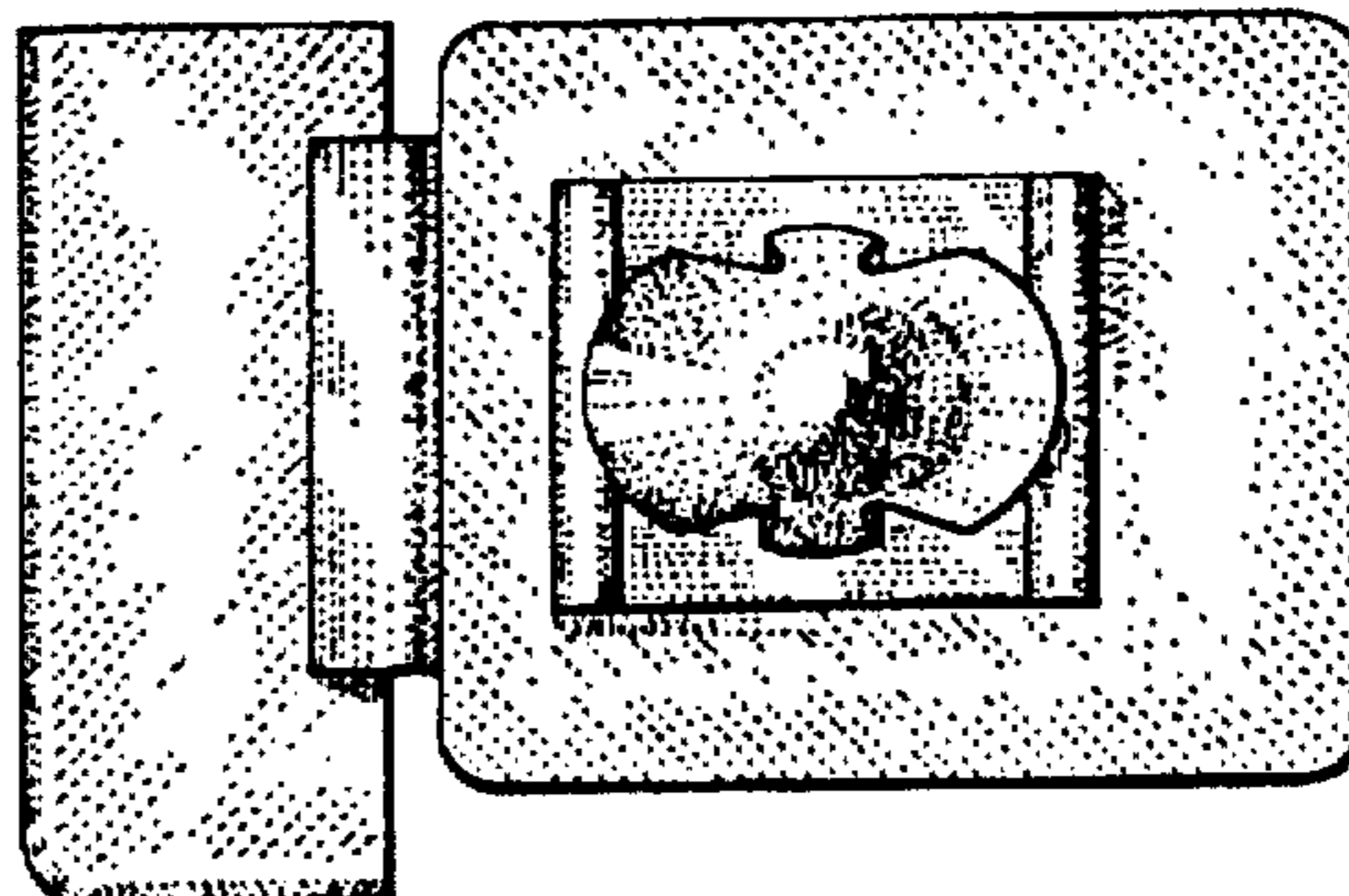


FIG. 13

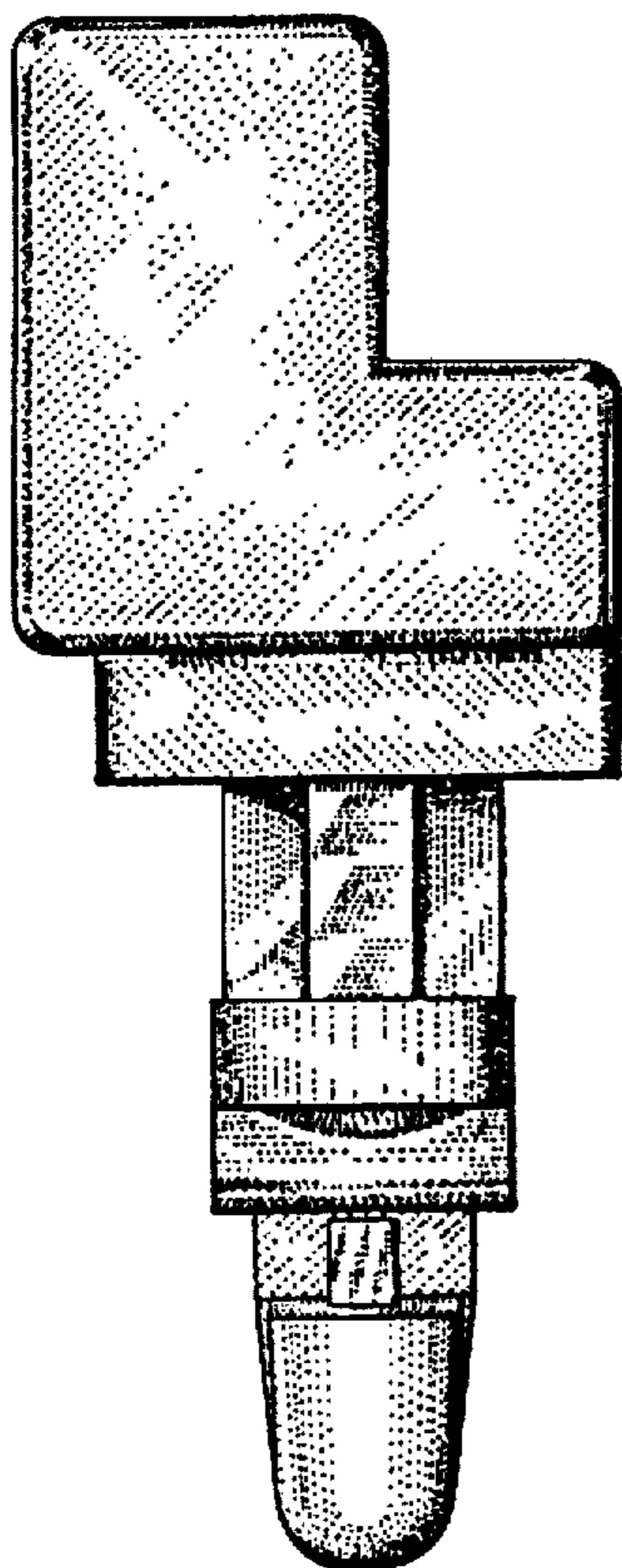


FIG. 14

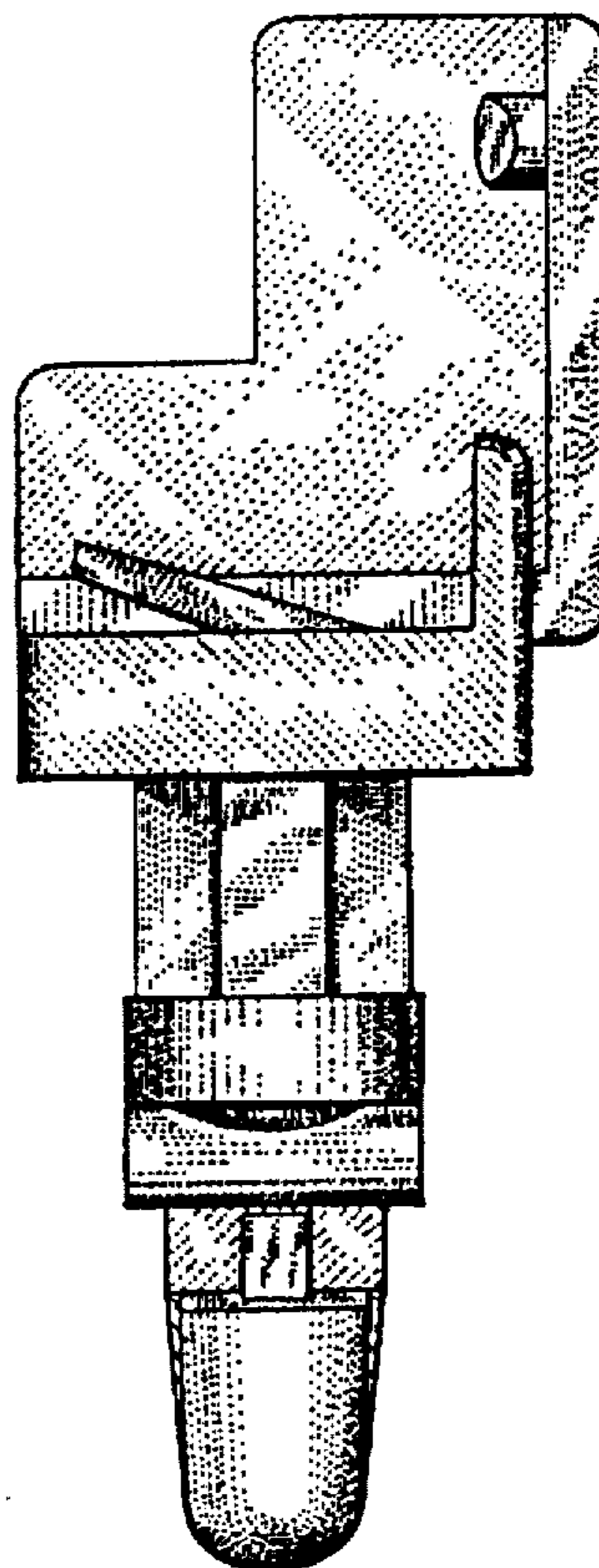


FIG. 15

