US00D375488S

United States Patent [19]

Ikenaga

[11] **Patent Number: Des. 375,488**

[45] **Date of Patent: **Nov. 12, 1996**

[54] **SIGNAL PROCESSOR**

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[73] Assignee: **Sony Kabushiki Kaisha**, Tokyo, Japan

[**] Term: **14 Years**

[21] Appl. No.: **44,064**

[22] Filed: **Sep. 15, 1995**

[52] **U.S. Cl.** **D14/107**

[58] **Field of Search** D14/100, 102, D14/107–109; D13/162, 184, 199; D6/432, 436, 445, 448; 312/208.1, 223.2, 223.3; 360/97.01, 97.04; 369/34, 36; 361/694, 696

[56] **References Cited**

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D. 314,189	1/1991	Horie	D14/102 X

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Attorney, Agent, or Firm—Morgan & Finnegan, L.L.P.

[57] **CLAIM**

The ornamental design for the signal processor, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of the signal processor in accordance with one aspect of the present invention;

FIG. **2** is a front elevation view of the signal processor of FIG. **1;**

FIG. **3** is a left-side elevation view of the signal processor of FIG. **1;**

FIG. **4** is a right-side elevation view of the signal processor of FIG. **1;**

FIG. **5** is a rear elevation view of the signal processor of FIG. **1;**

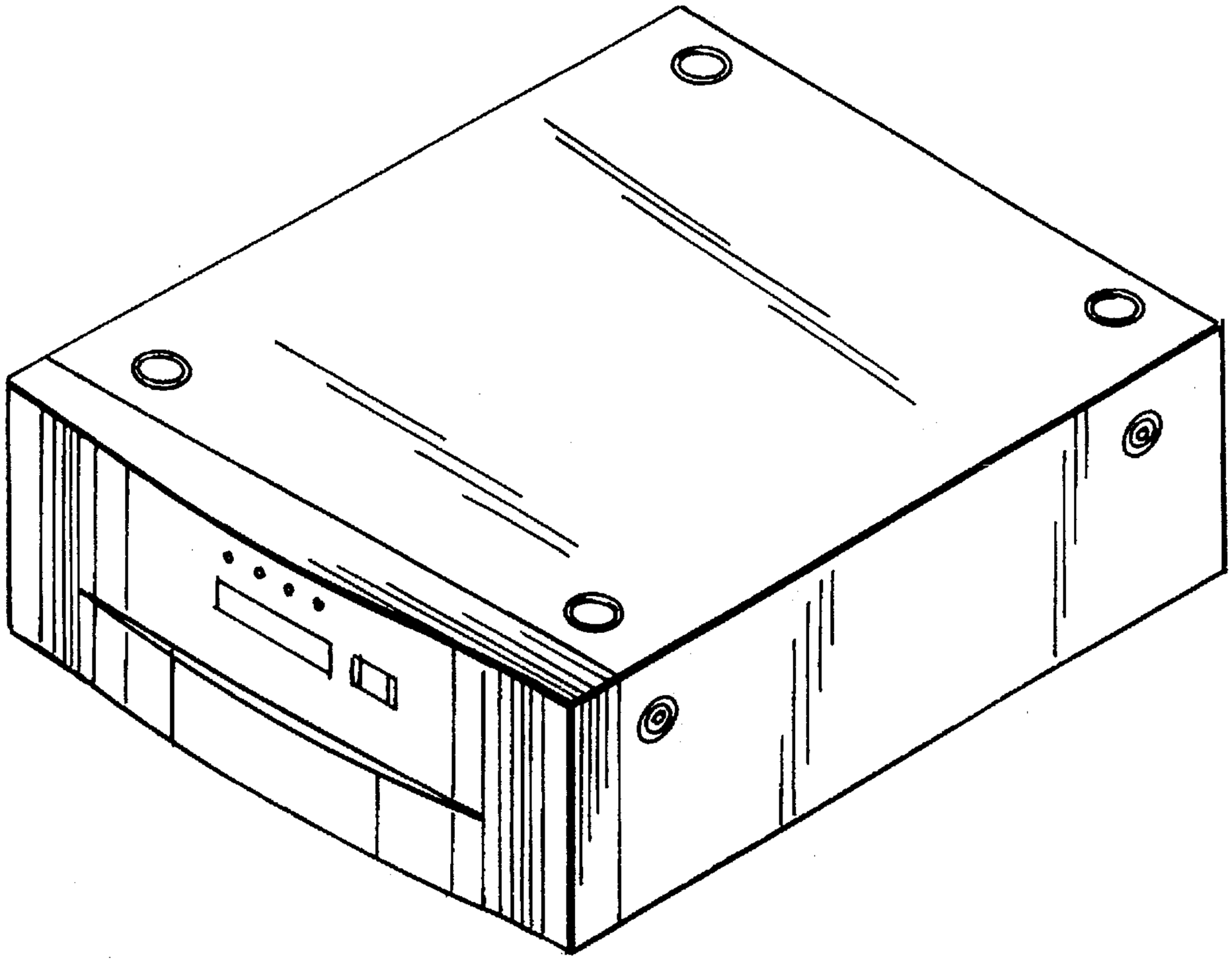
FIG. **6** is a top plan view of the signal processor of FIG. **1;**

FIG. **7** is a bottom plan view of the signal processor of FIG. **1;** and,

FIG. **8** is a perspective view showing the signal process of of FIG. **1** in operational use with a data recorder mounted on the top surface of the signal processor.

The data recorder is shown in broken lines for illustrative purposes only and forms no part of the claimed design.

1 Claim, 2 Drawing Sheets



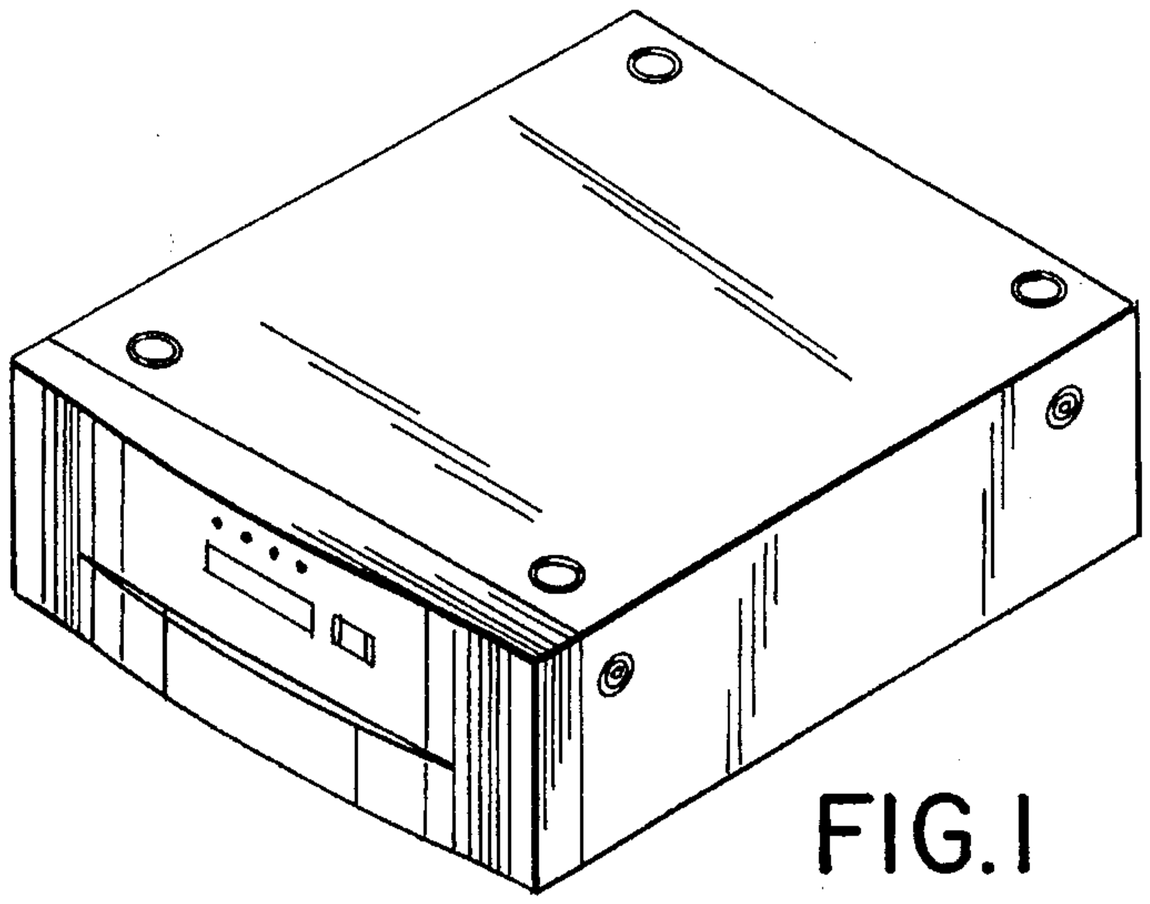


FIG.1

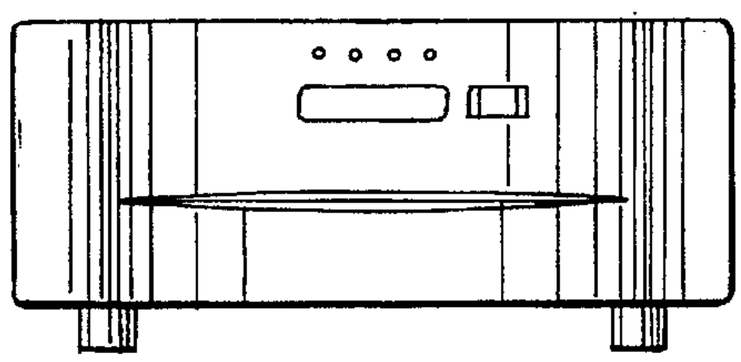


FIG.2

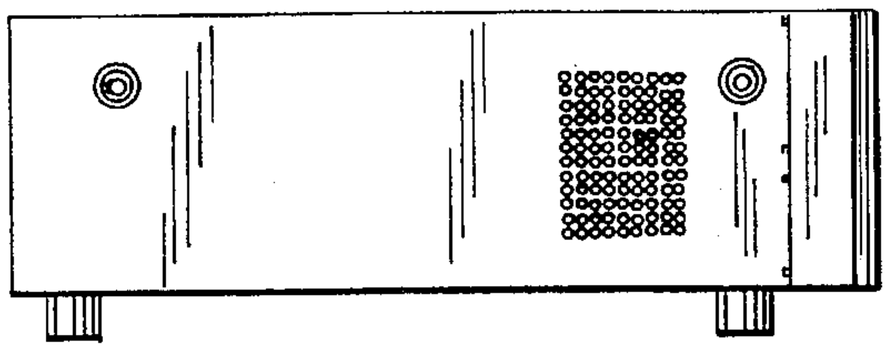


FIG.3

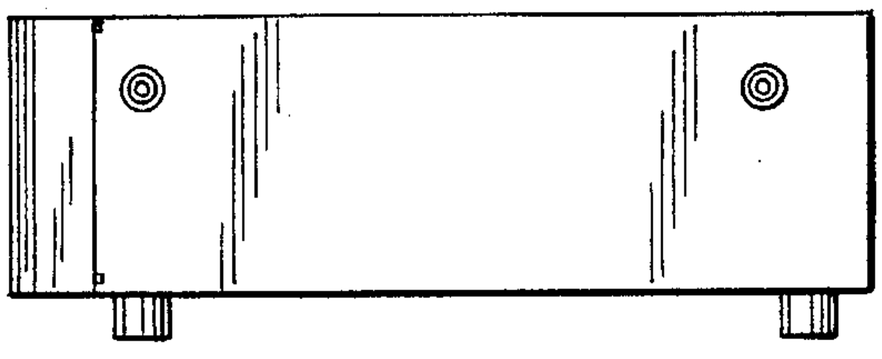


FIG.4

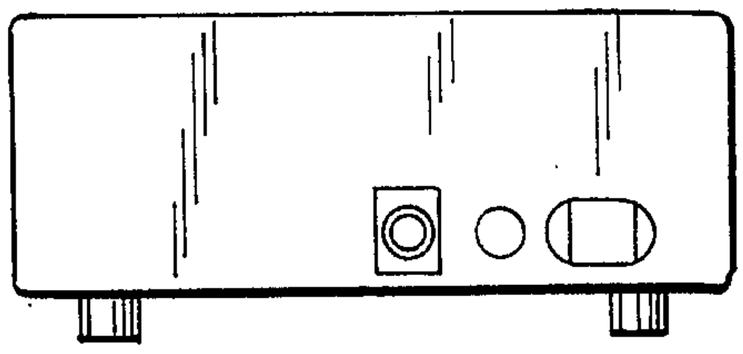


FIG.5

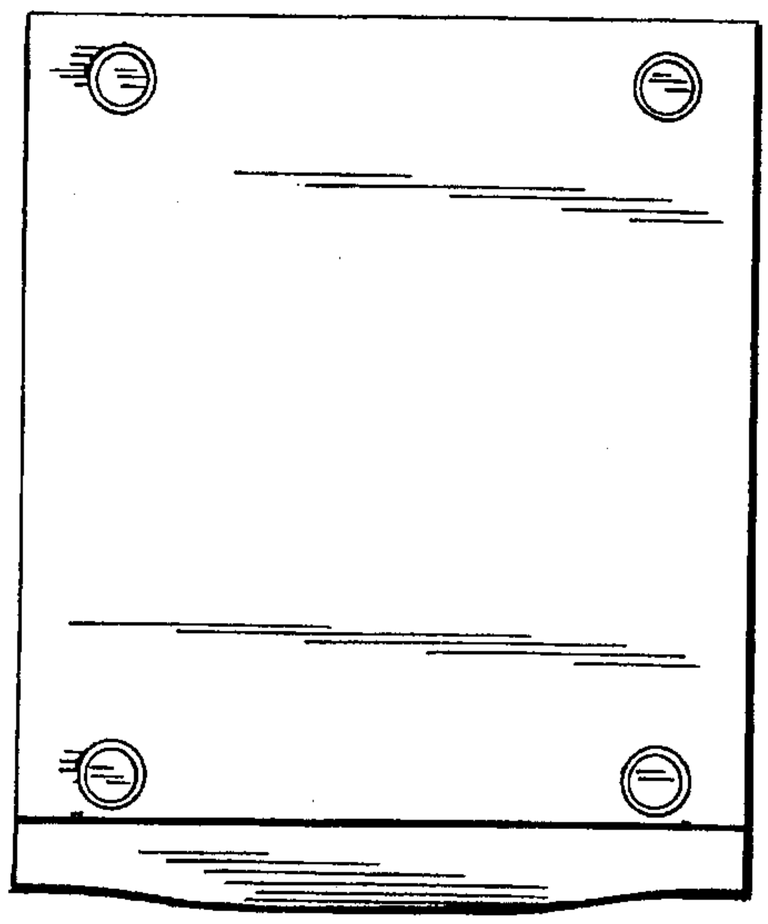


FIG.6

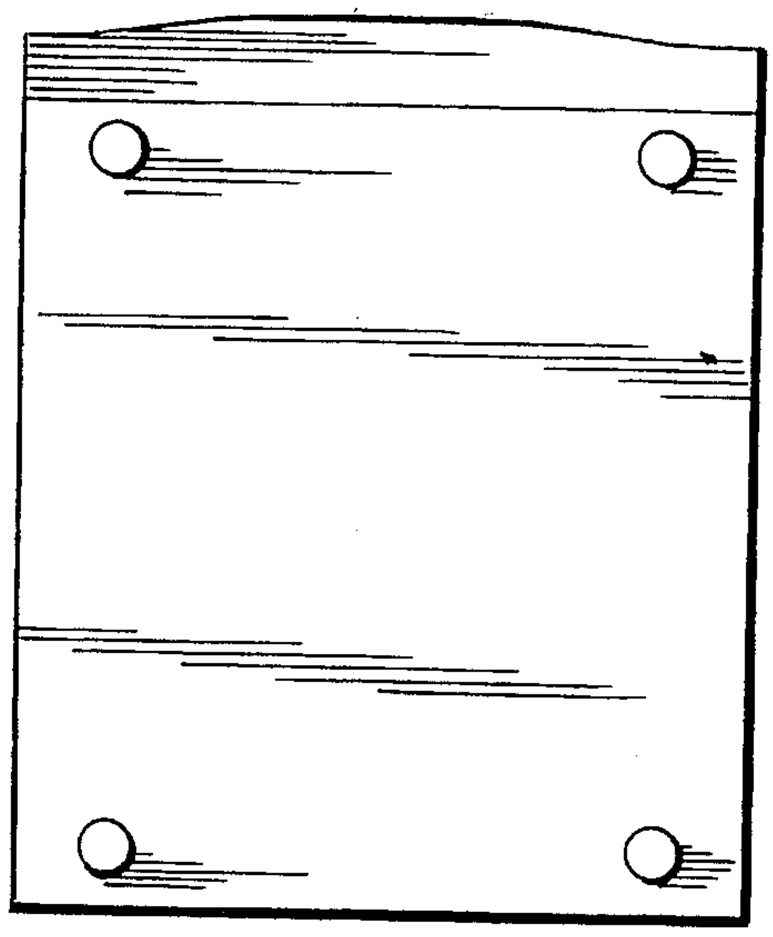


FIG.7

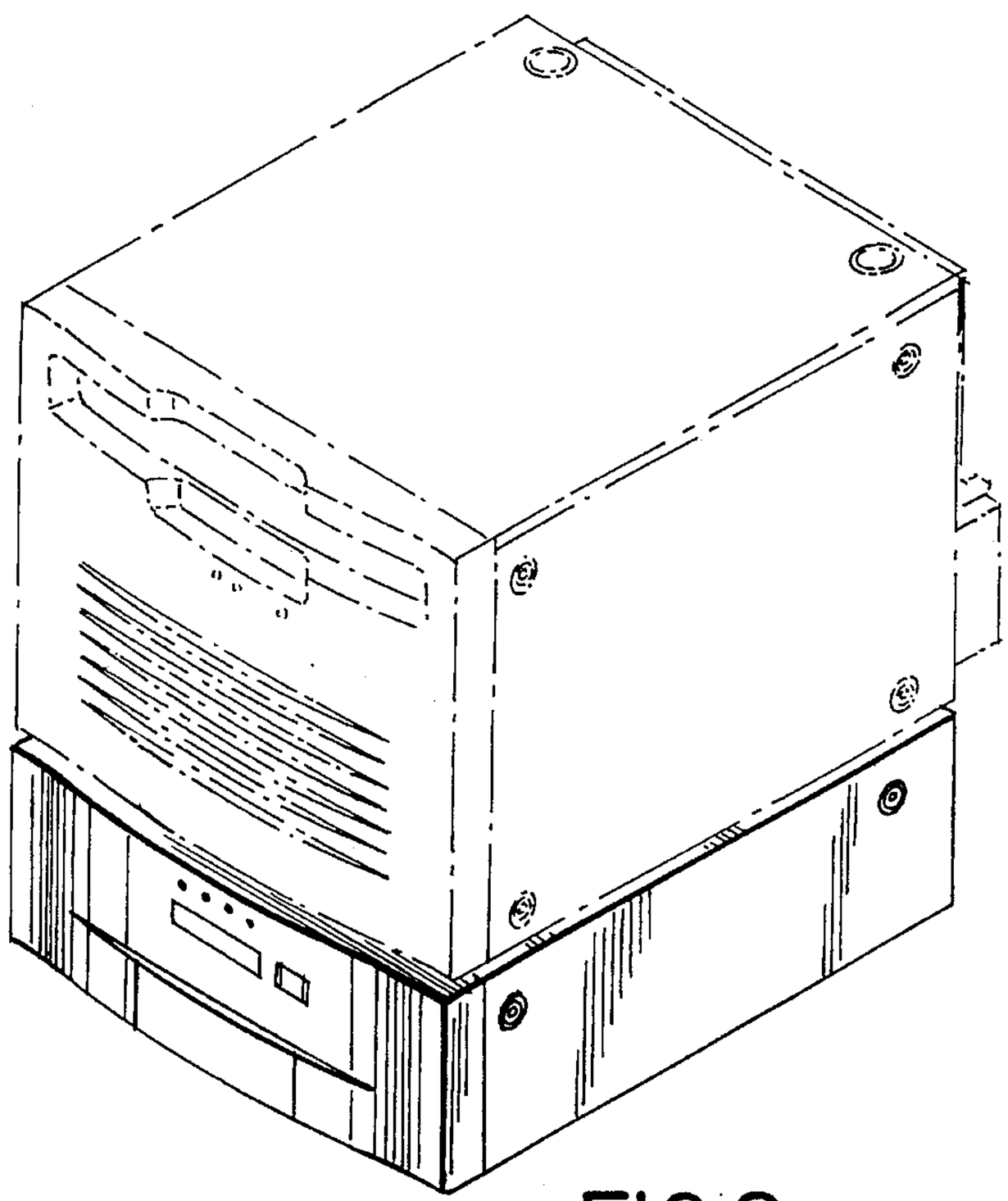


FIG.8