



US00D374866S

United States Patent [19]
Johnston

[11] **Patent Number: Des. 374,866**

[45] **Date of Patent: **Oct. 22, 1996**

[54] **SCALABLE PROCESSING ARCHITECTURE (SPARC) COMPUTER MOTHERBOARD**

5,397,919 3/1995 Tata et al. 257706 X

OTHER PUBLICATIONS

[75] Inventor: **Mark L. Johnston**, Los Altos, Calif.

Circuit boards on p. 233 of *EDN*, Jan. 21, 1991.

[73] Assignee: **Cycle Computer Corp.**, Cupertino, Calif.

Primary Examiner—Joel Sincavage
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[**] Term: **14 Years**

[57] **CLAIM**

[21] Appl. No.: **38,145**

The ornamental design for a scalable processing architecture (SPARC) computer motherboard, as shown and described.

[22] Filed: **Apr. 27, 1995**

DESCRIPTION

[52] **U.S. Cl.** **D13/182**

[58] **Field of Search** D13/182; 174/250, 174/252, 254, 255, 260, 261; 361/695, 718, 719, 720, 736, 748, 785

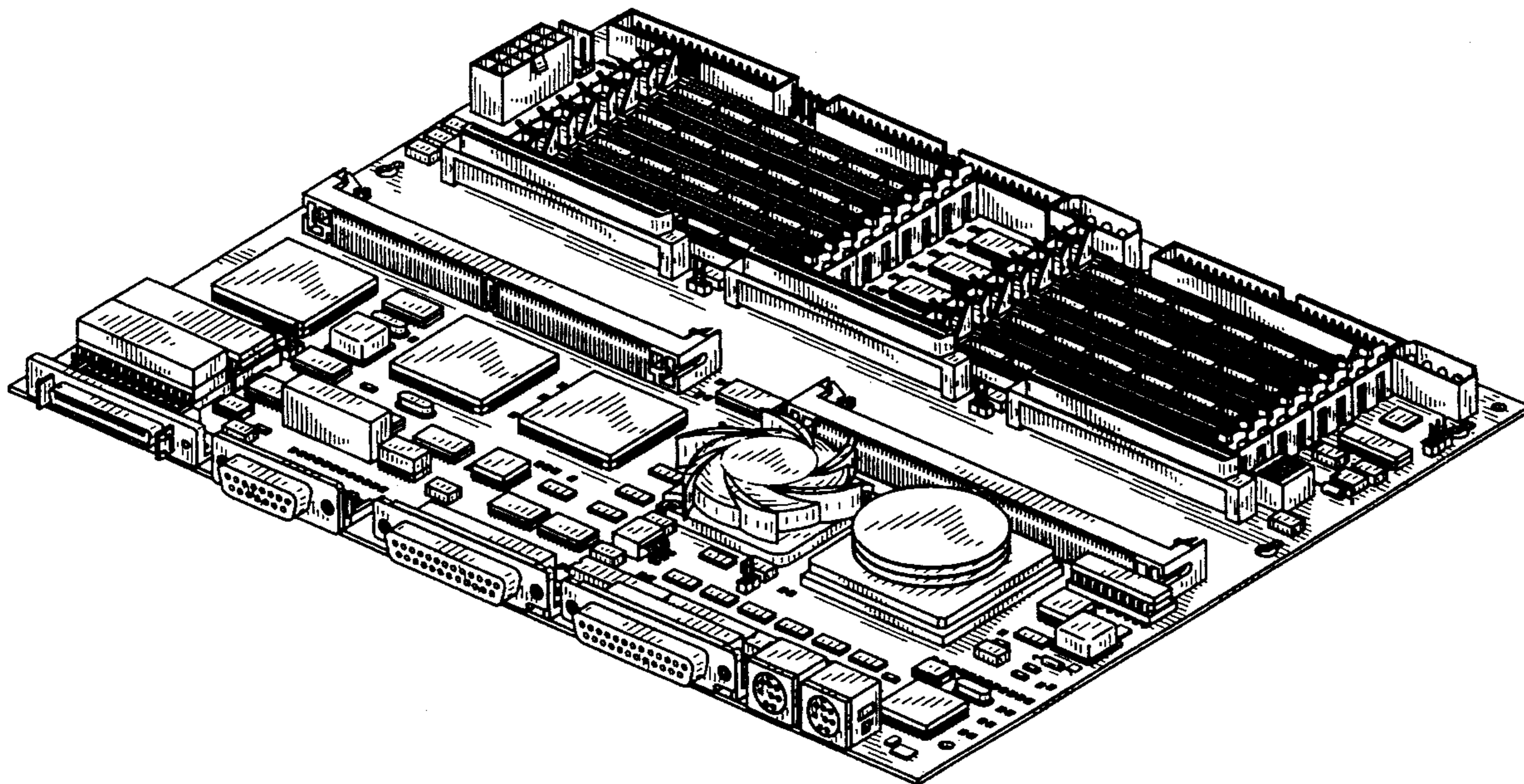
FIG. 1 is a perspective view of a first embodiment of the scalable processing architecture (SPARC) computer motherboard embodying my new design; FIG. 2 is a top elevational view thereof; FIG. 3 is a back side view thereof; FIG. 4 is a front side view thereof; FIG. 5 is a right side view thereof; FIG. 6 is a left side view thereof; and, FIG. 7 is a bottom view thereof.

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 275,279	8/1984	Littlefield et al.	D13/182
D. 304,441	11/1989	Edmonds	D13/147
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1 Claim, 5 Drawing Sheets



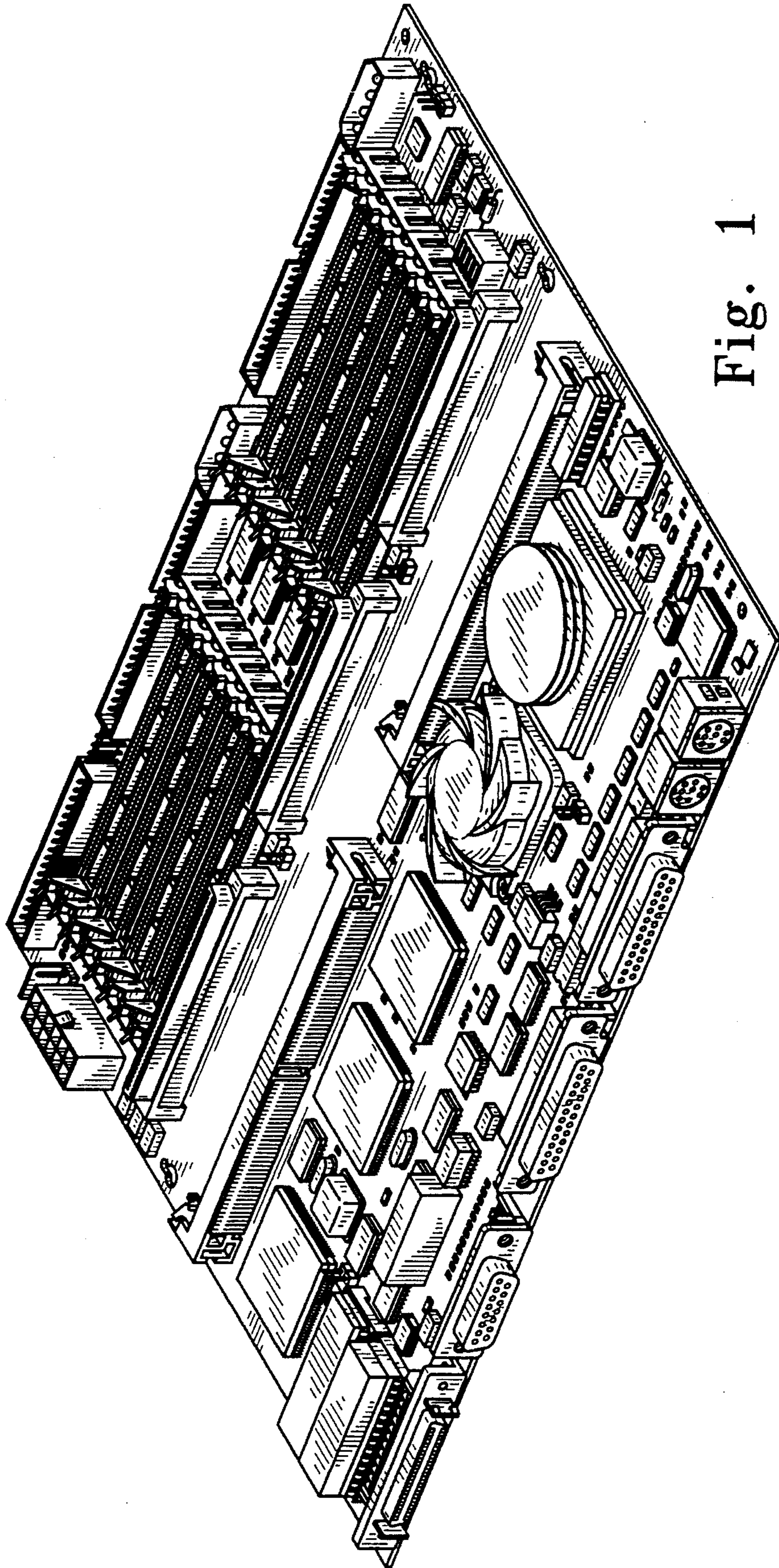


Fig. 1

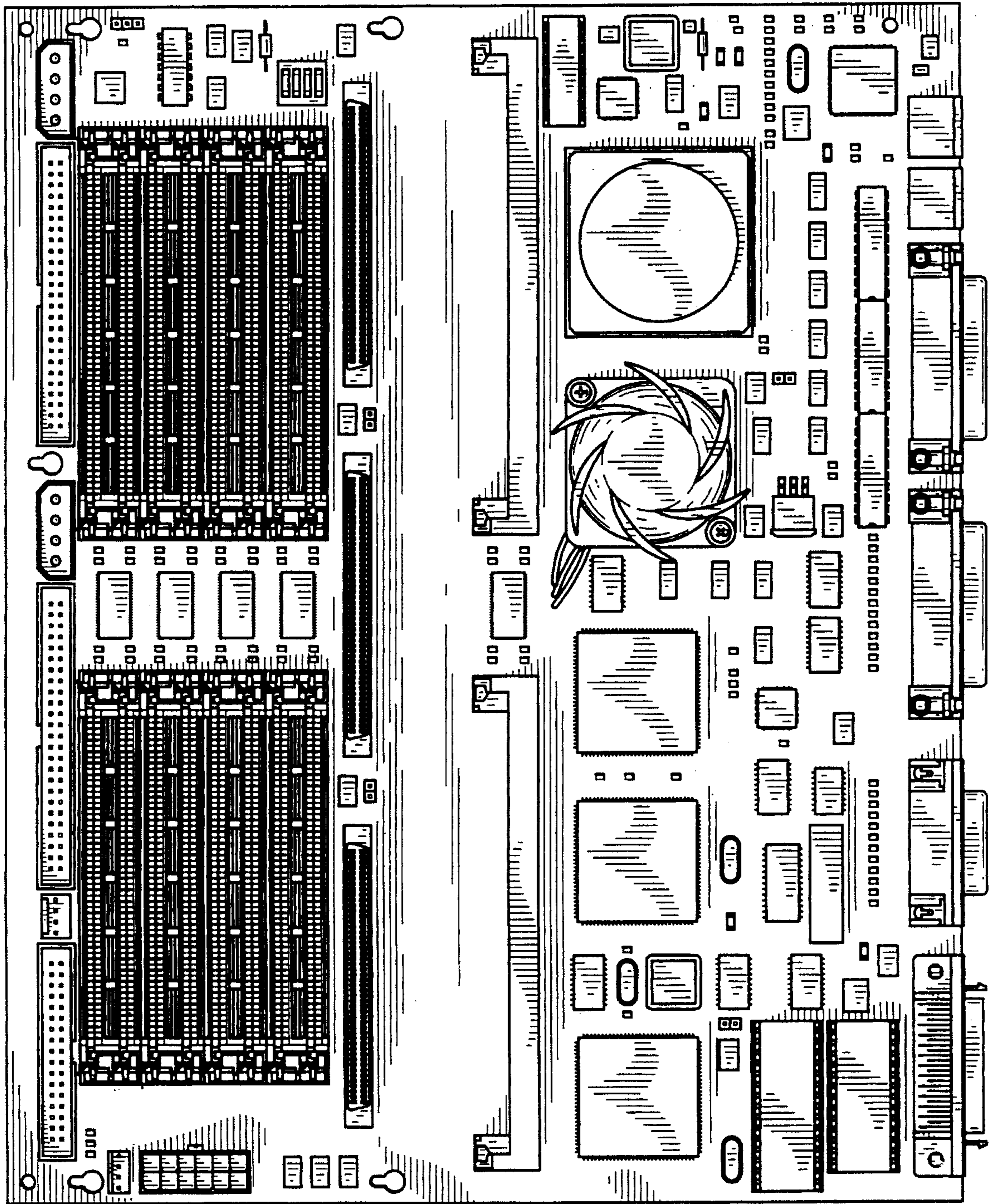


Fig. 2

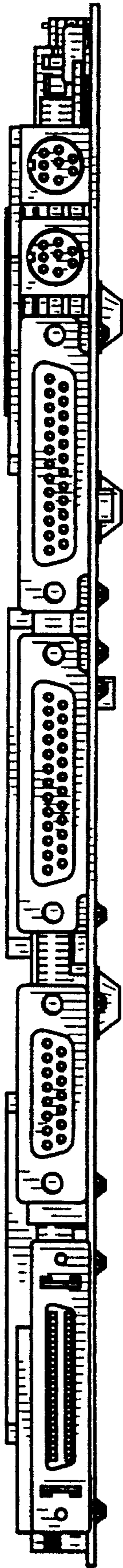


Fig. 3

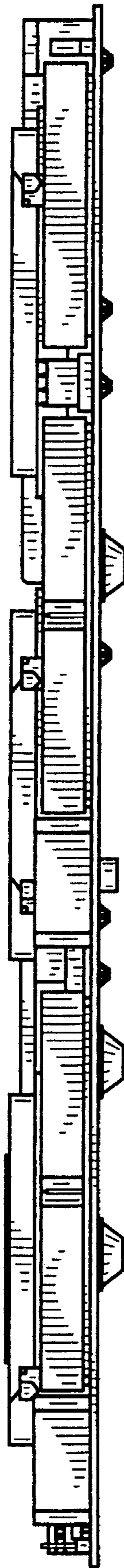


Fig. 4

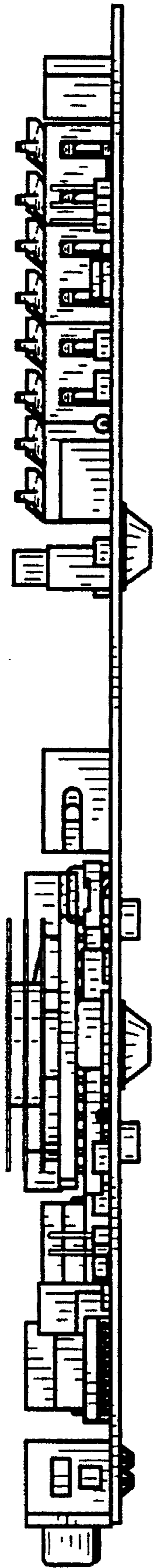


Fig. 5

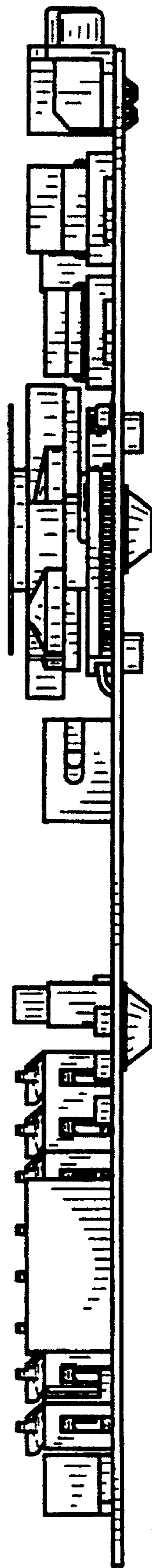


Fig. 6

Fig. 7

