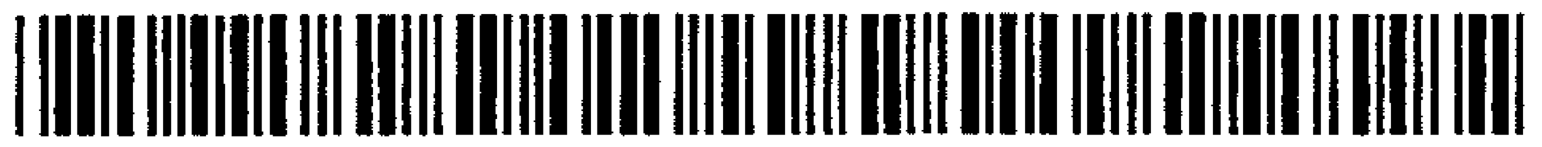


United States Patent [19]

Takao

[11] **Patent Number: Des. 350,490**

[45] **Date of Patent: ** Sep. 13, 1994**

[54] **SEMICONDUCTOR WAFER TESTING APPARATUS**

[75] Inventor: **Itaru Takao,** Nirasaki, Japan

[73] Assignees: **Tokyo Electron Kabushiki Kaisha,** Tokyo; **Tokyo Electron Yamanashi Kabushiki Kaisha,** Irasaki, both of Japan

[**] Term: **14 Years**

[21] Appl. No.: **6,815**

[22] Filed: **Apr. 7, 1993**

[30] **Foreign Application Priority Data**

Oct. 8, 1992 [JP] Japan 4-29499

[52] **U.S. Cl.** **D10/46;** D10/75

[58] **Field of Search** .... 269/13, 14, 20, 21, 269/296, 903; 324/158 P; 414/222, 225, 589, 590, 627, 673, 752; D10/46, 75, 81

[56] **References Cited**

U.S. PATENT DOCUMENTS

D, 323,628 2/1992 Takao D10/46
5,141,212 8/1992 Beeding 269/21
5,264,069 11/1993 Dietrich et al. .... 269/21 X

OTHER PUBLICATIONS

Fully Automatic Wafer Prober Model 785, Tokyo Electron Limited, p. 2.

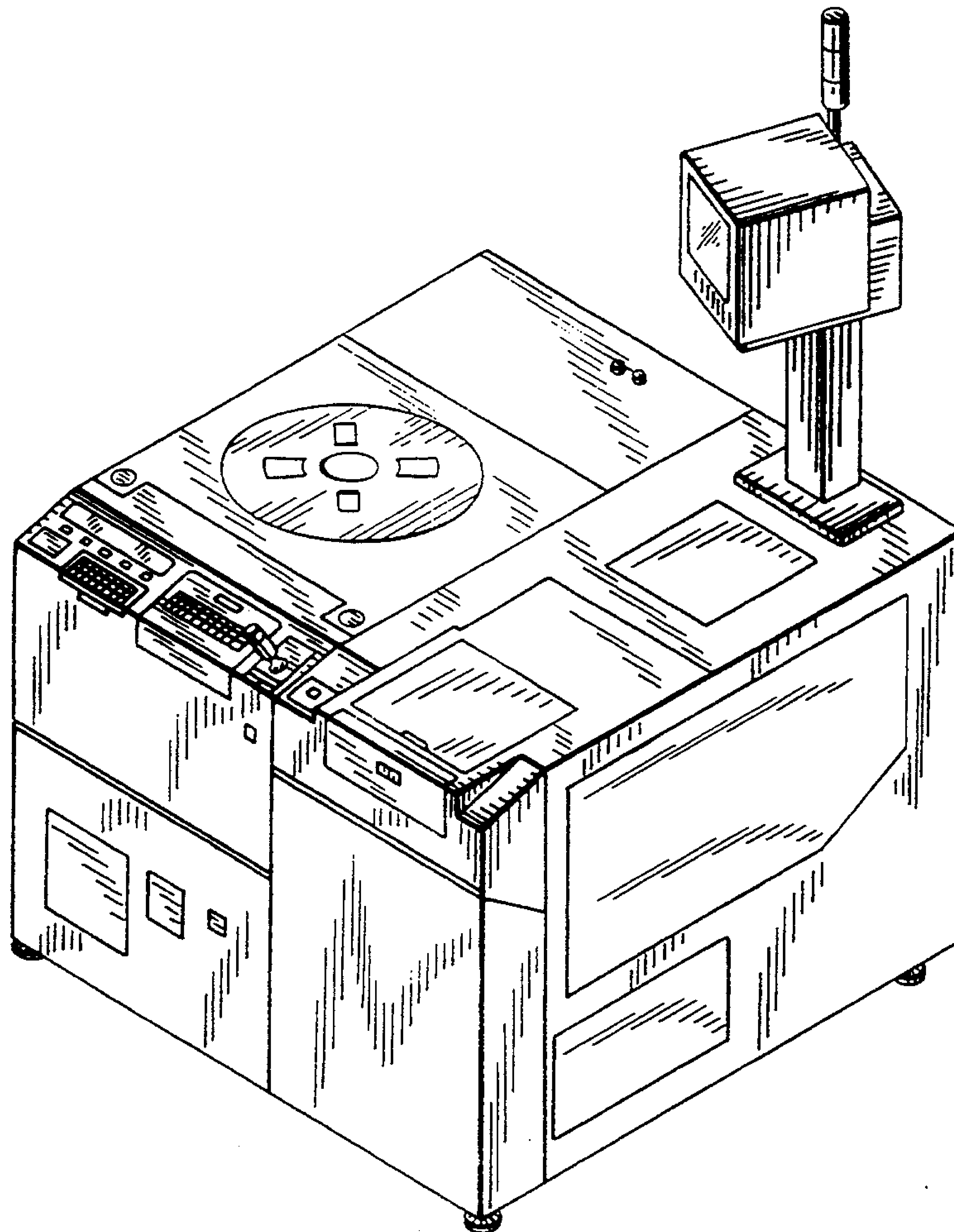
Primary Examiner—Alan P. Douglas
Assistant Examiner—Antoine D. Davis
Attorney, Agent, or Firm—Ladas & Parry

[57] **CLAIM**

The ornamental design for semiconductor wafer testing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a top, front and right side perspective view of a semiconductor wafer testing apparatus showing my new design;
FIG. **2** is a top plan view;
FIG. **3** is a front elevational view;
FIG. **4** is a left side elevational view;
FIG. **5** is a right side elevational view;
FIG. **6** is a rear elevational view; and,
FIG. **7** is a bottom plan view thereof.



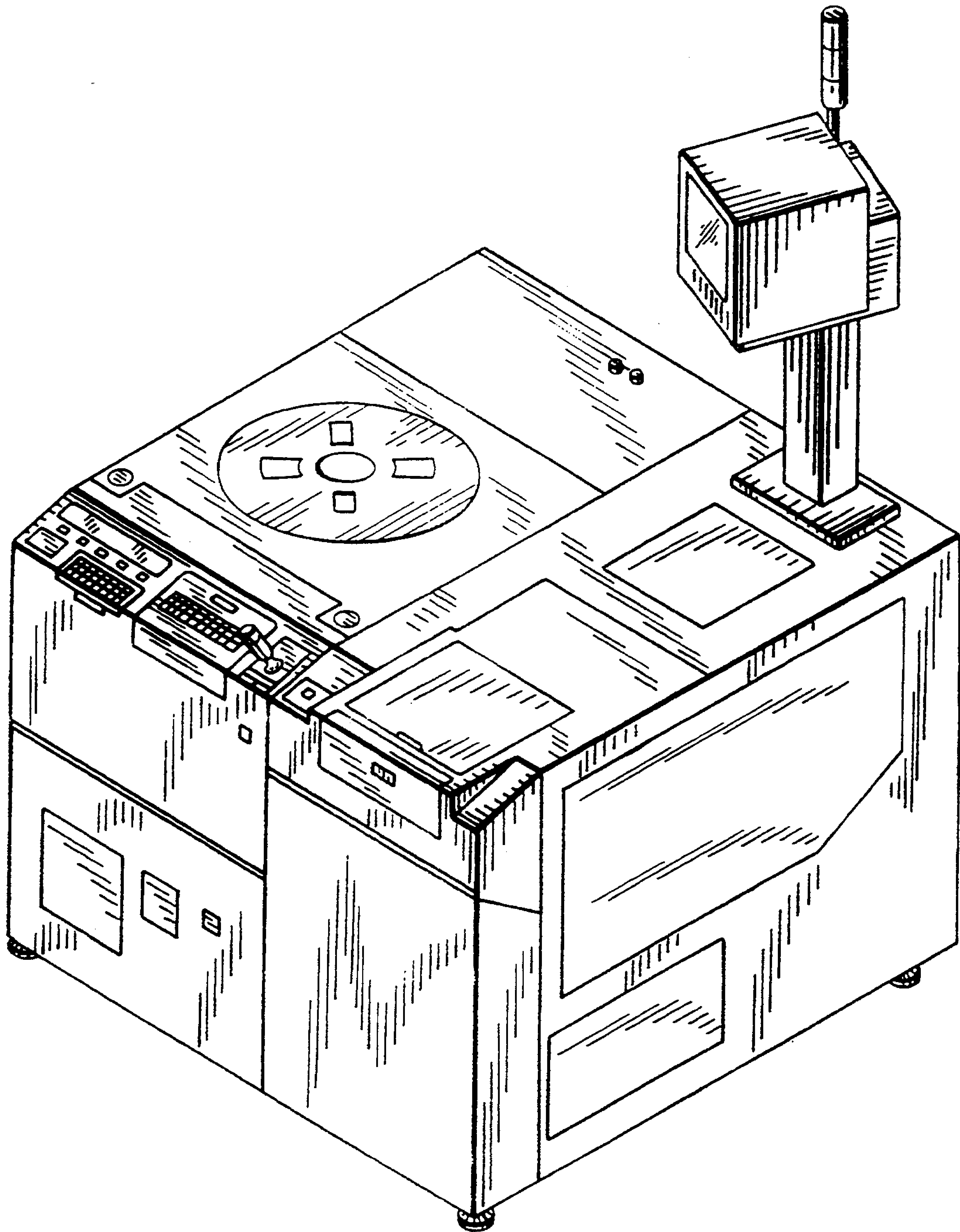


FIG. 1

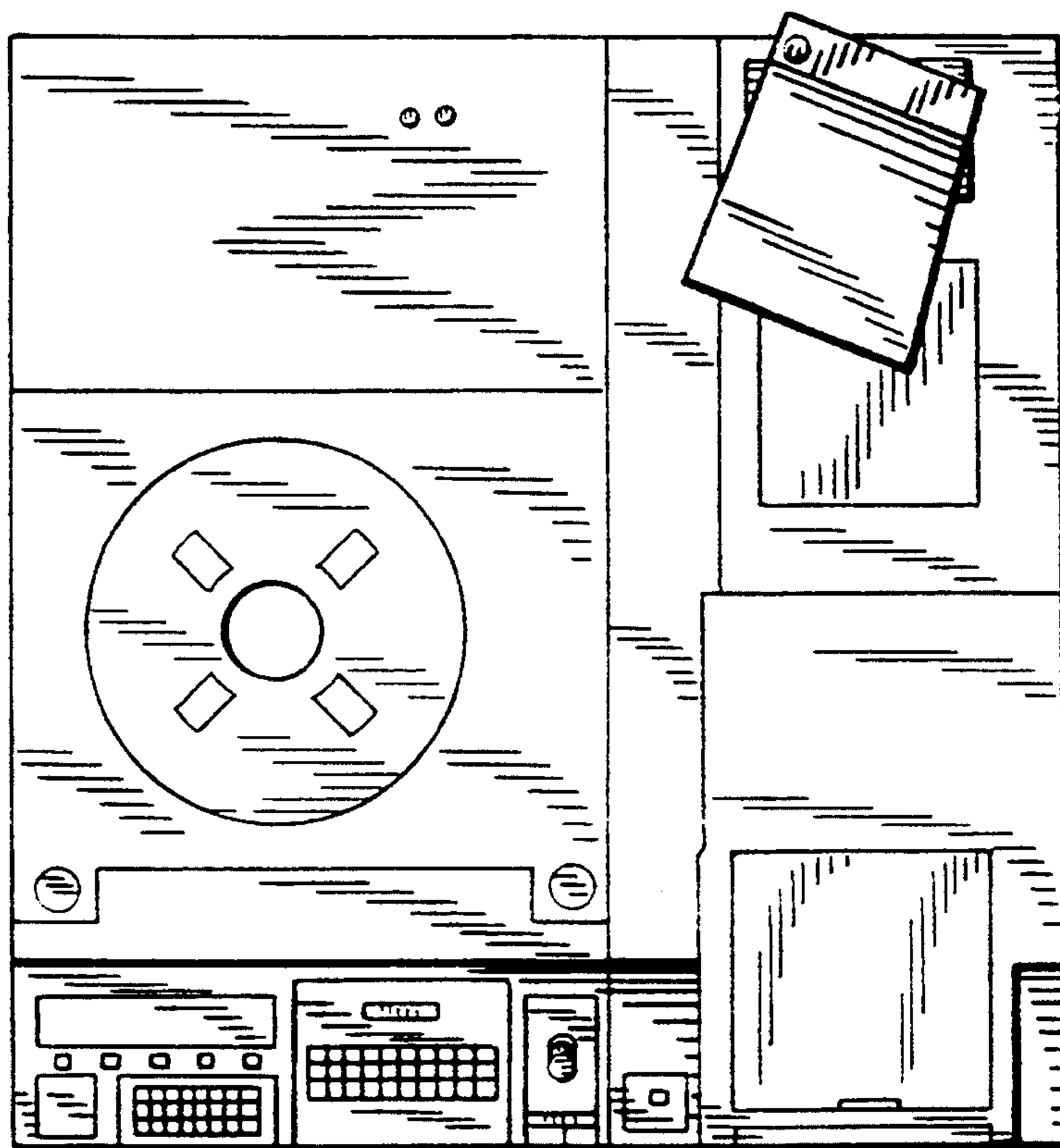


FIG. 2

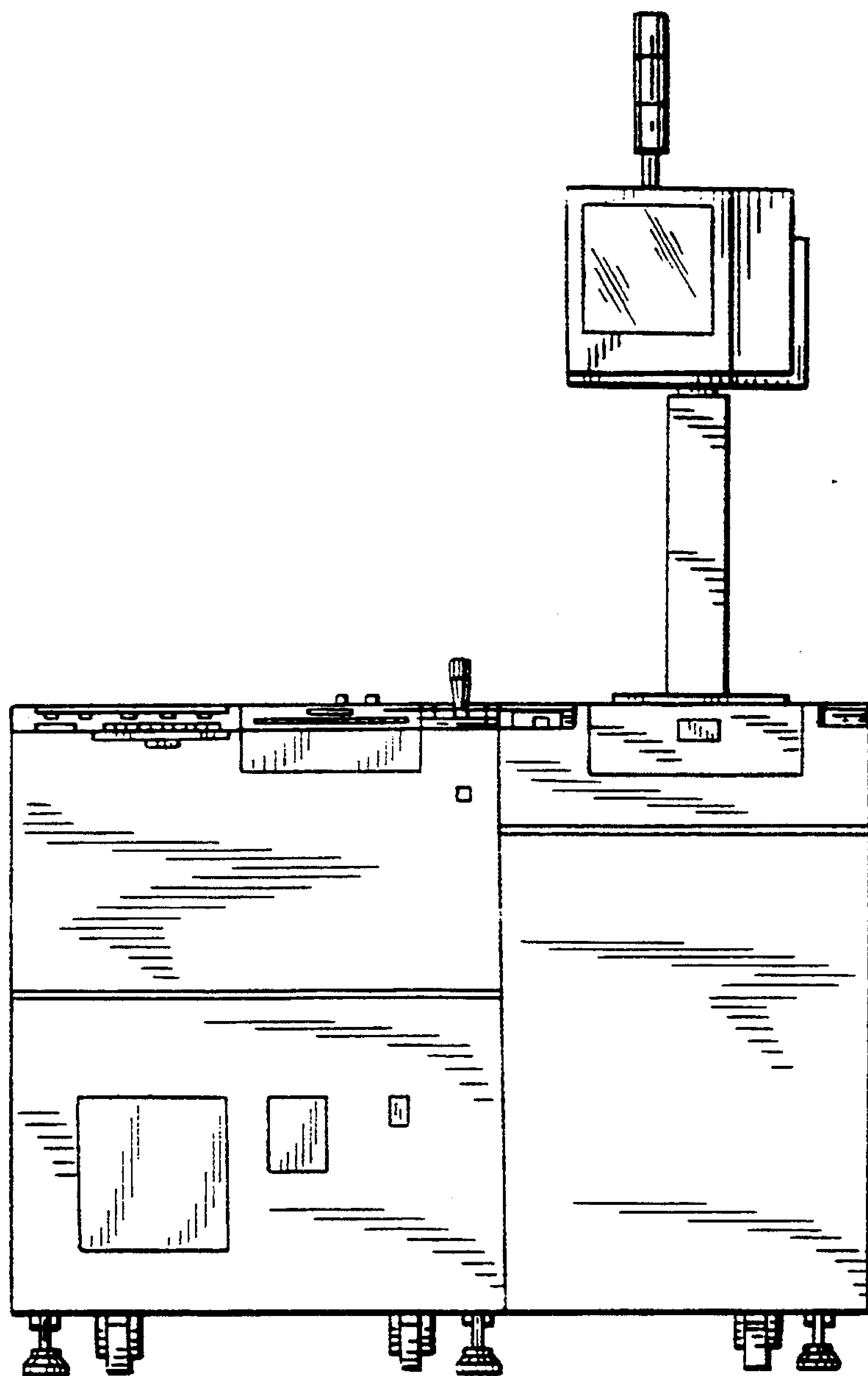


FIG. 3

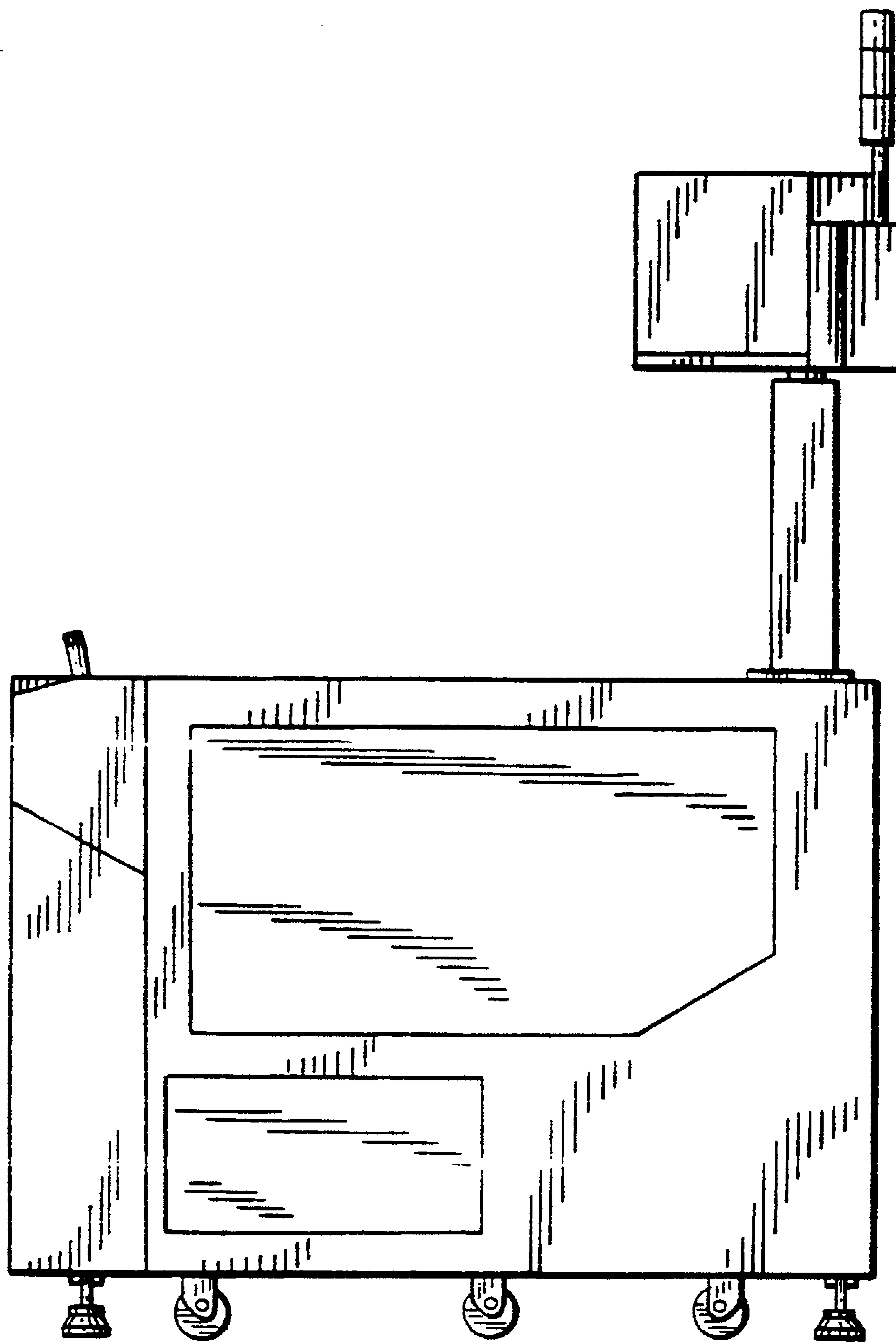


FIG. 4

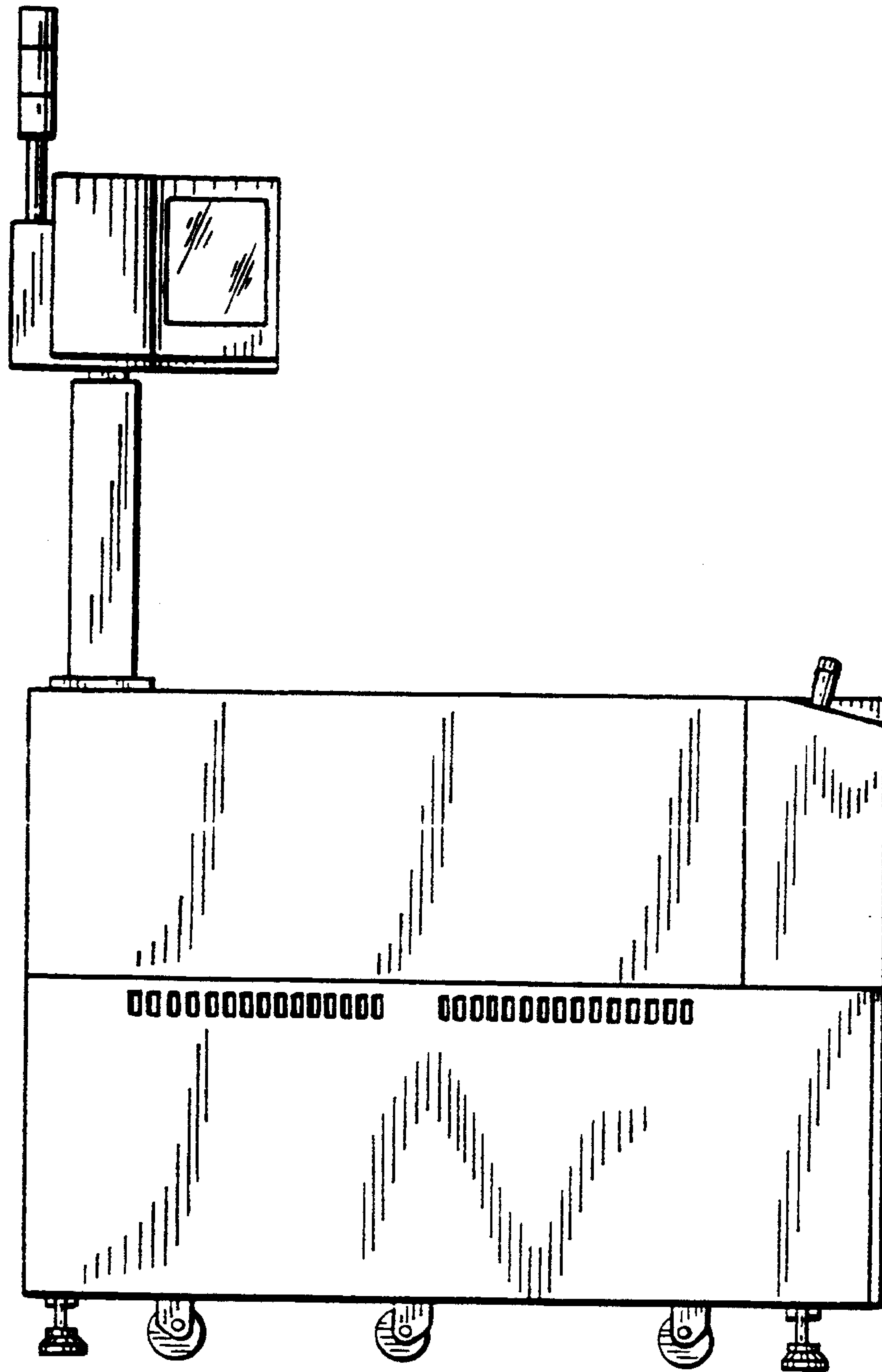


FIG. 5

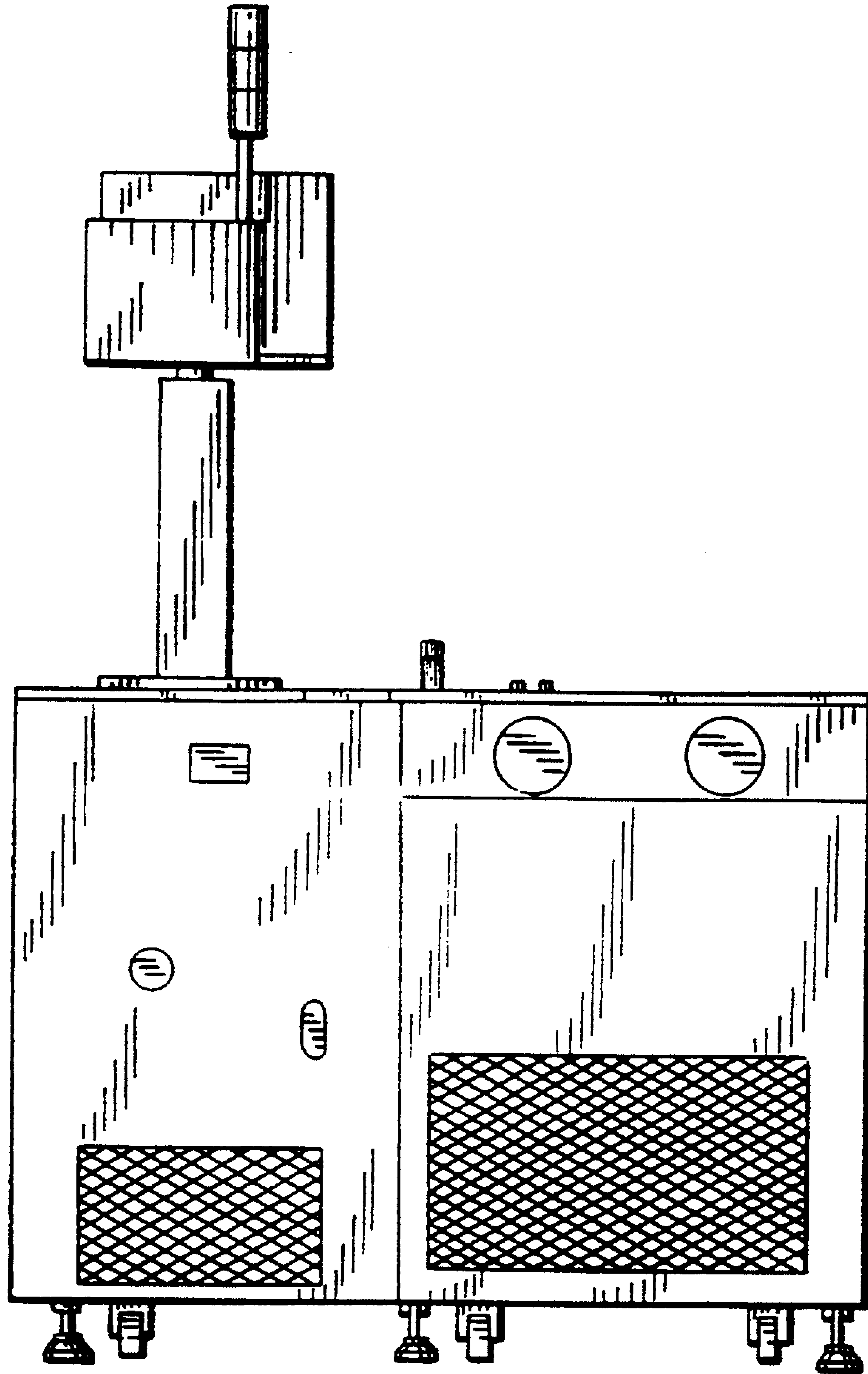


FIG.6

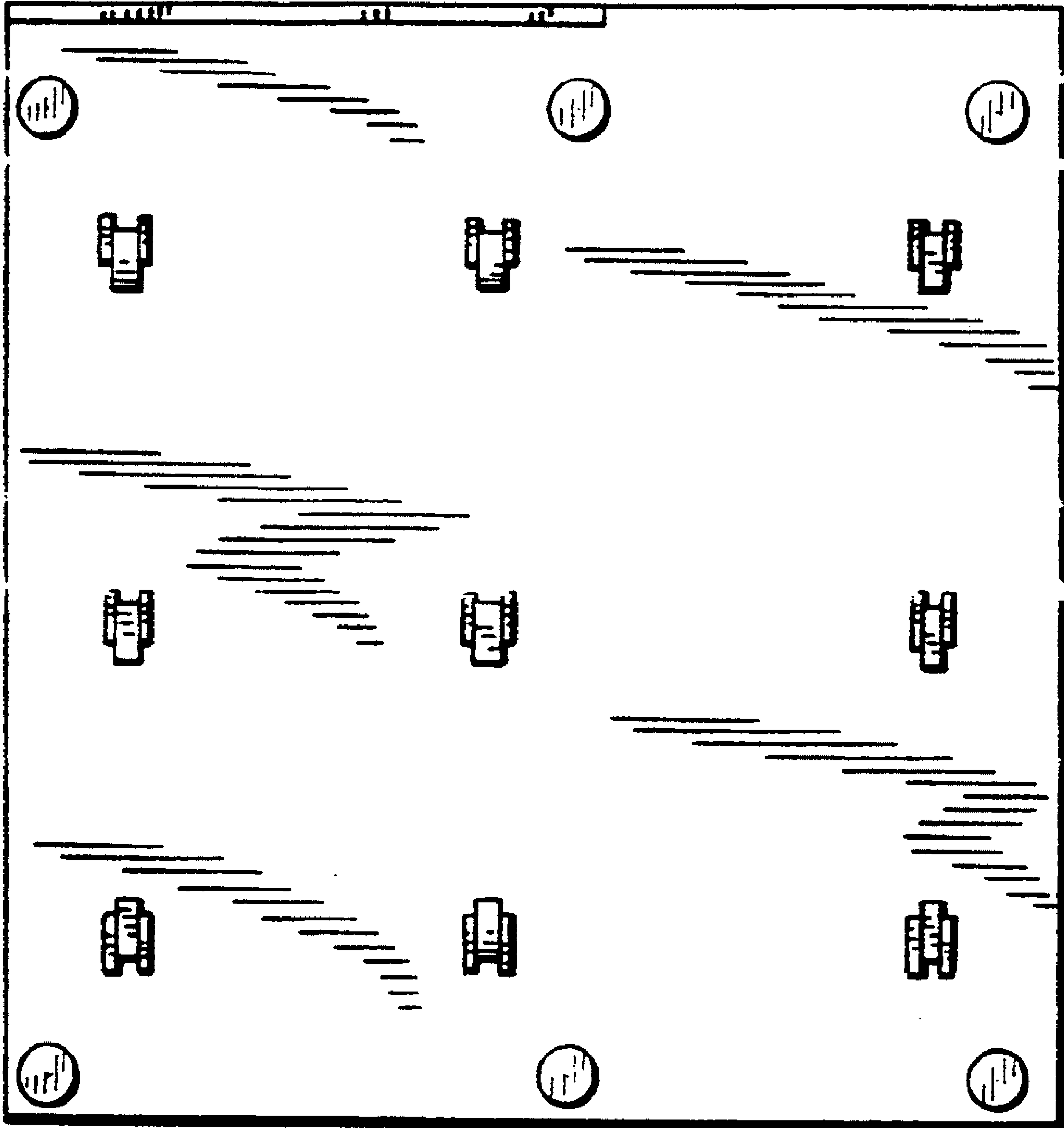


FIG. 7