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United States Patent [19]

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Kanaya et al.

[45] Date of Patent: **** Apr. 12, 1994**

[54] HYBRID INTEGRATED CIRCUIT

[56] References Cited

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[73] Assignee: **Sanyo Electric Co., Ltd.**, Osaka, Japan

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NEC 5.5V capacitor on p. 27 of *EDN* Feb. 18, 1991.

[**] Term: **14 Years**

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[21] Appl. No.: **876,211**

[57] CLAIM

The ornamental design for a hybrid integrated circuit, as shown.

[22] Filed: **Apr. 29, 1992**

DESCRIPTION

[30] Foreign Application Priority Data

Oct. 30, 1991 [JP] Japan 3-33055

[52] U.S. Cl. **D13/182**

[58] Field of Search 174/52.4, 255, 256, 174/257, 258; 361/380, 384, 392, 395, 397, 399; 364/600, 708; D13/182

FIG. 1 is a top, front and right side perspective view of our new design for a hybrid integrated circuit; FIG. 2 is a front elevational view thereof; FIG. 3 is a rear elevational view thereof; FIG. 4 is a top plan view thereof; FIG. 5 is a bottom plan view thereof; FIG. 6 is a right side elevational view thereof; and, FIG. 7 is a left side elevational view thereof.

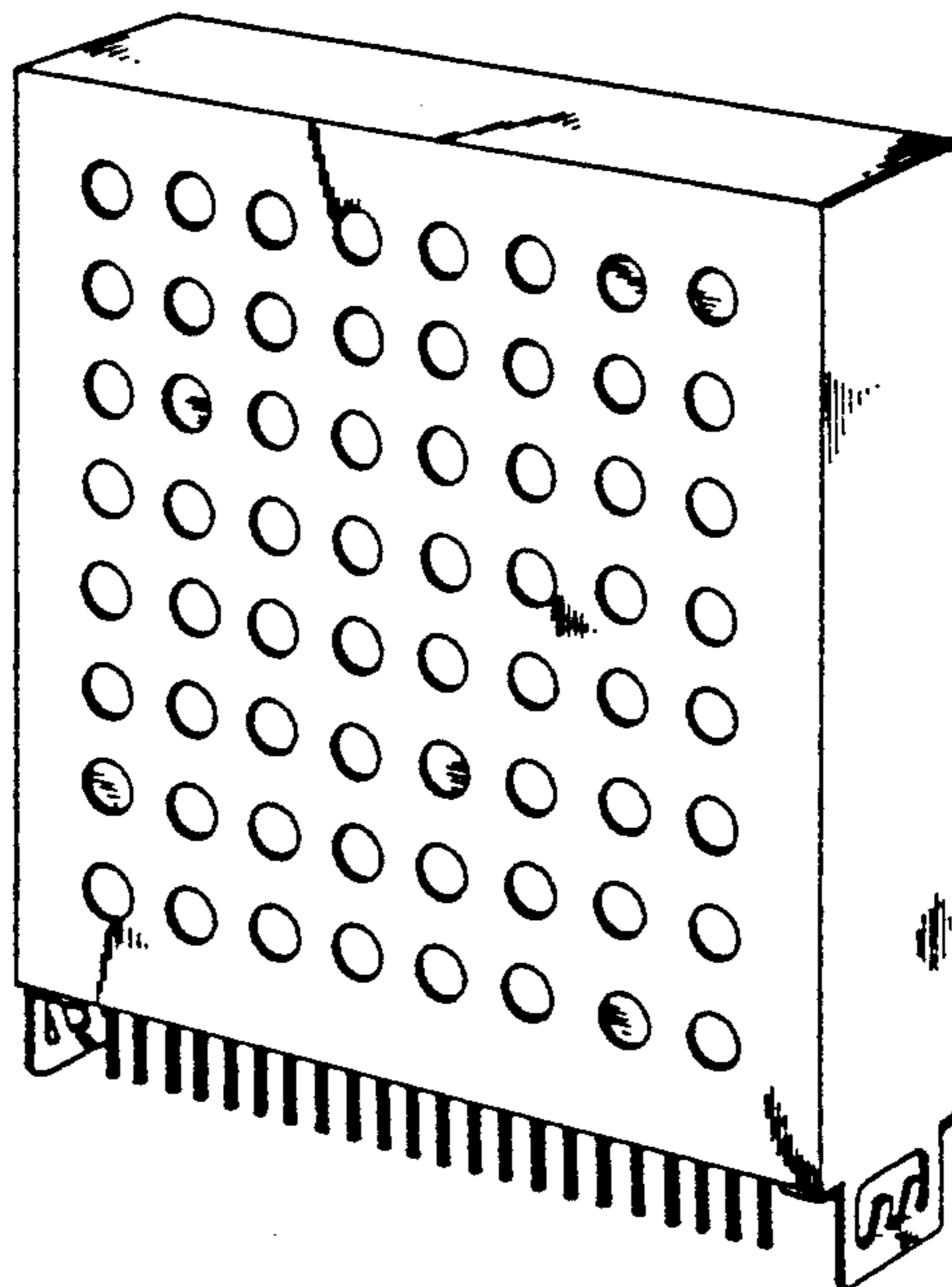


FIG. 1

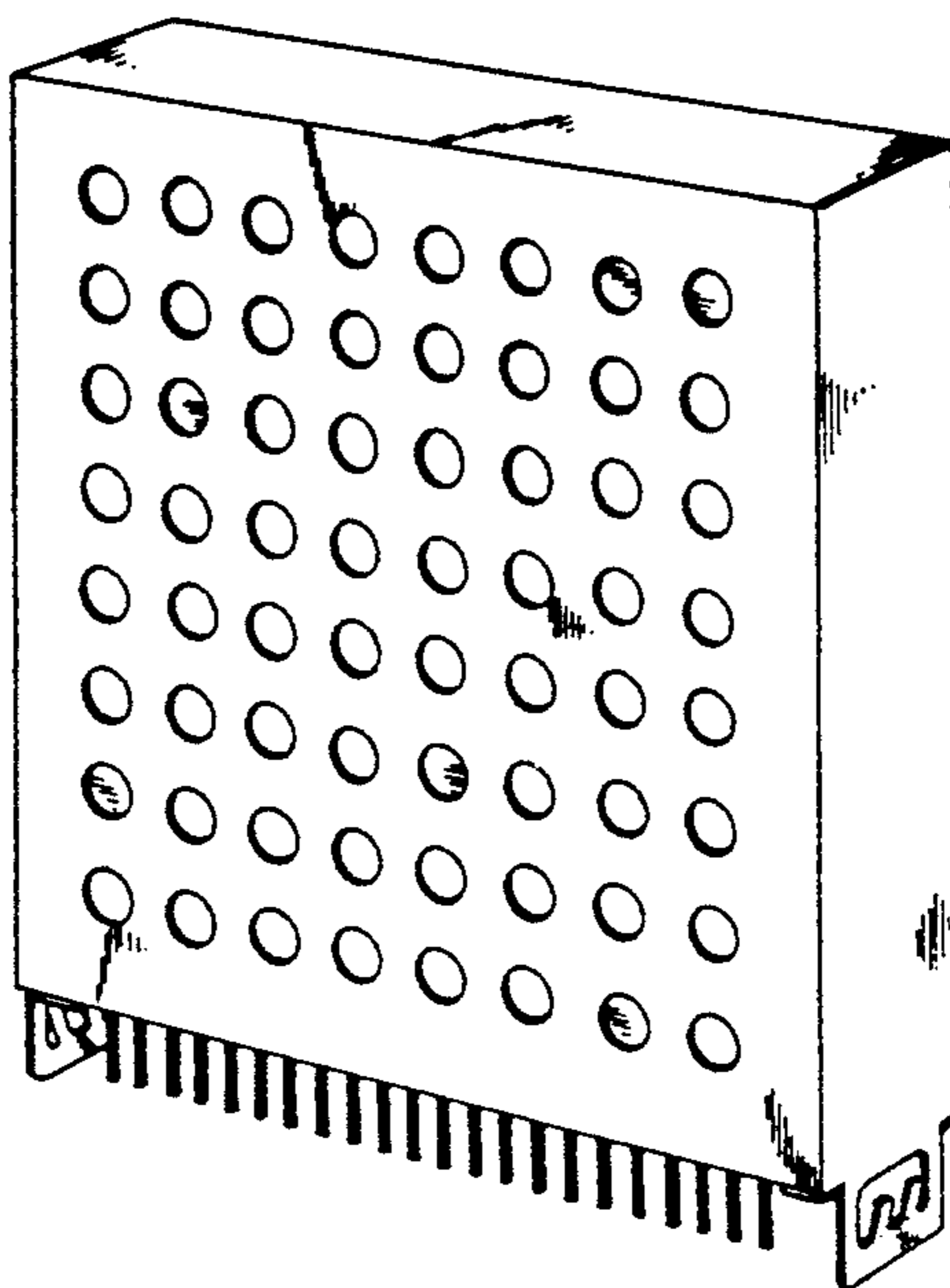


FIG. 2

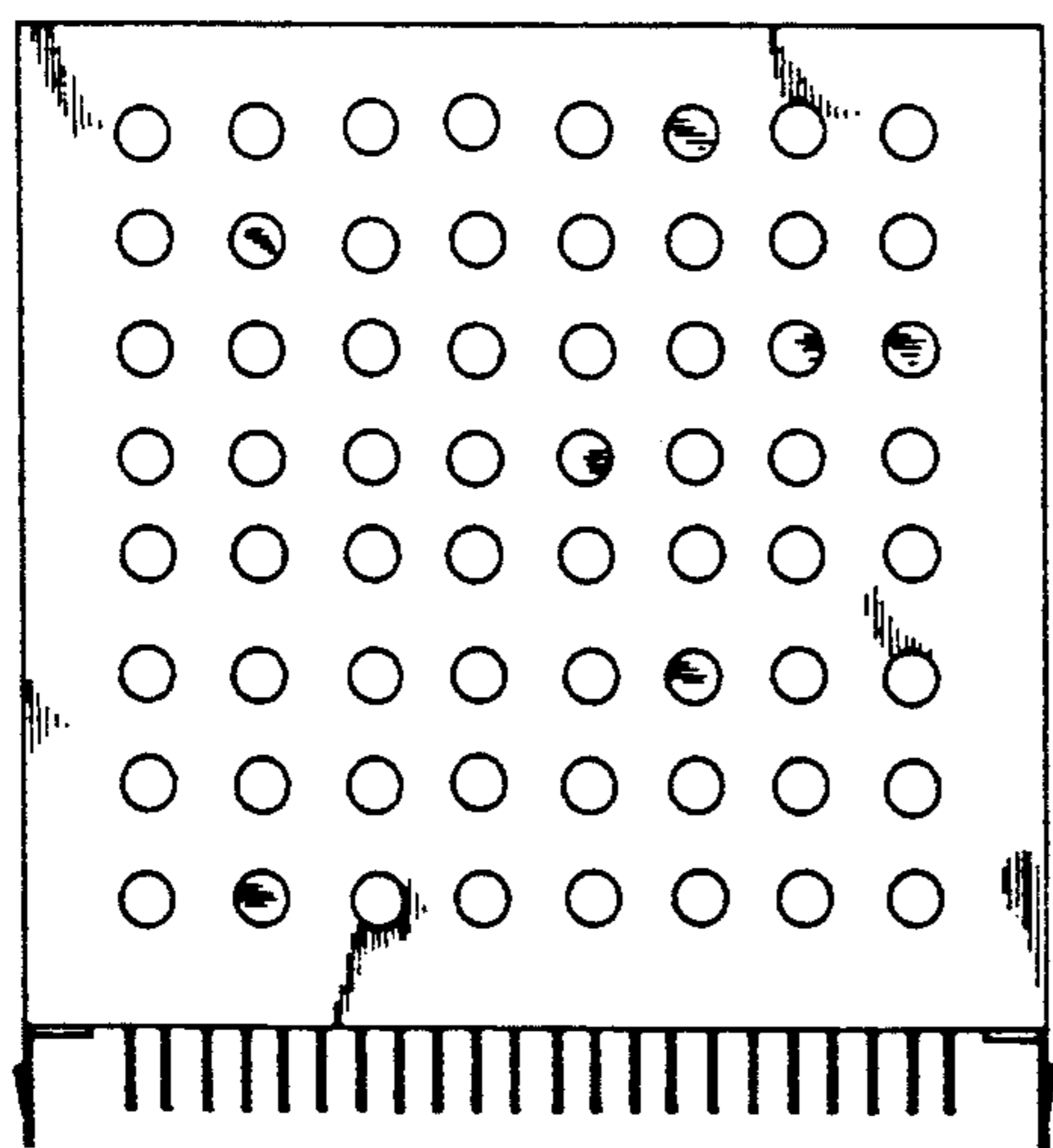


FIG. 3

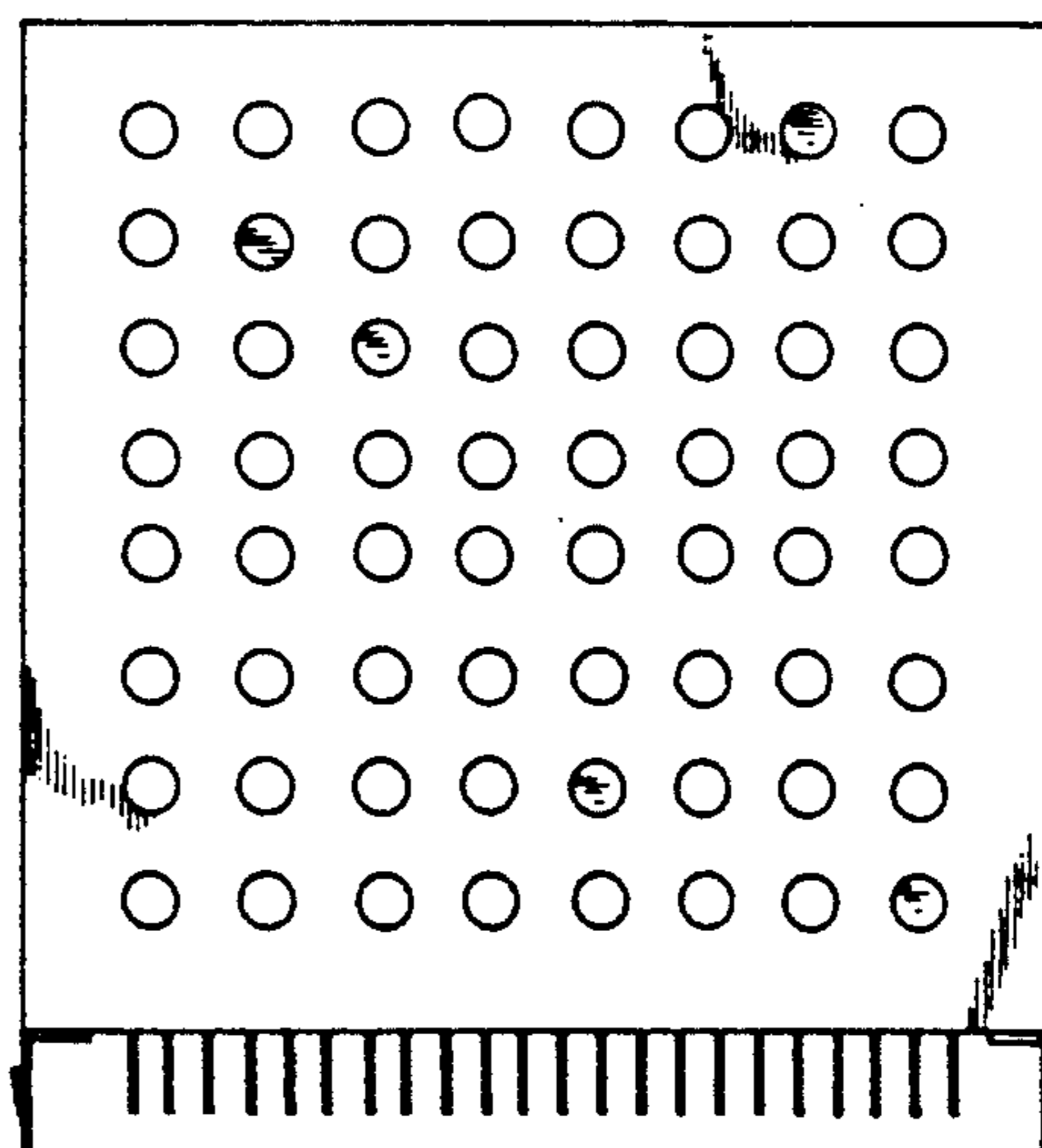


FIG. 4



FIG. 5

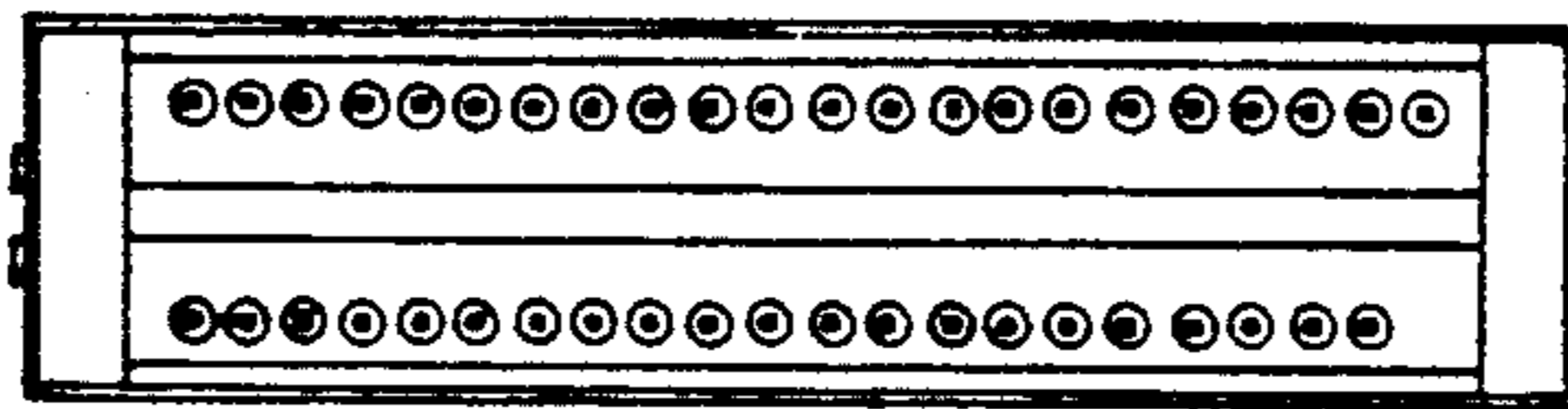


FIG. 6

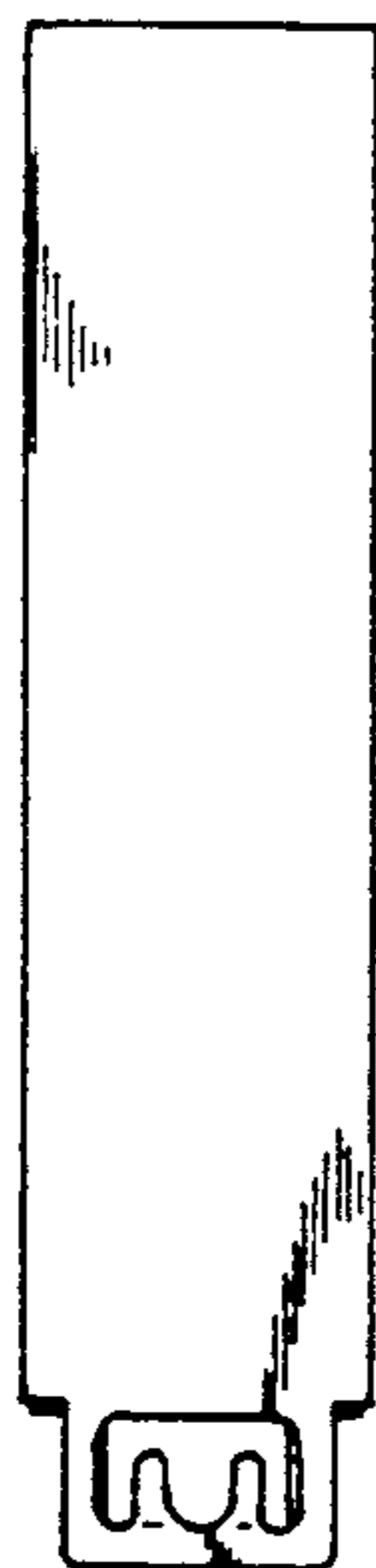


FIG. 7

