



US00D345111S

# United States Patent [19]

[11] Patent Number: **Des. 345,111**

Tracewell

[45] Date of Patent: **\*\* Mar. 15, 1994**

[54] ENCLOSURE FOR TESTING CIRCUIT BOARDS

4,528,504 7/1985 Thornton et al. .... 324/158 F

[76] Inventor: **Larry L. Tracewell**, 8653 Finlarig Dr., Dublin, Ohio 43017

*Primary Examiner*—Alan P. Douglas  
*Assistant Examiner*—Antoine D. Davis  
*Attorney, Agent, or Firm*—Mueller and Smith

[\*\*] Term: **14 Years**

[57] **CLAIM**

[21] Appl. No.: **949,012**

The ornamental design for an enclosure for testing circuit boards, as shown.

[22] Filed: **Sep. 21, 1992**

**DESCRIPTION**

[52] U.S. Cl. .... **D10/75**

[58] Field of Search ..... 307/64, 66, 150;  
324/158 F; 340/606, 660; 361/384, DIG. 184;  
D10/75

FIG. 1 is a front view of the enclosure for testing circuit boards showing my new design;

FIG. 2 is a rear view of the enclosure shown in FIG. 1;

FIG. 3 is a right side view of the enclosure of FIG. 1;

FIG. 4 is a left side view of the enclosure of FIG. 1;

FIG. 5 is a top view of the enclosure of FIG. 1;

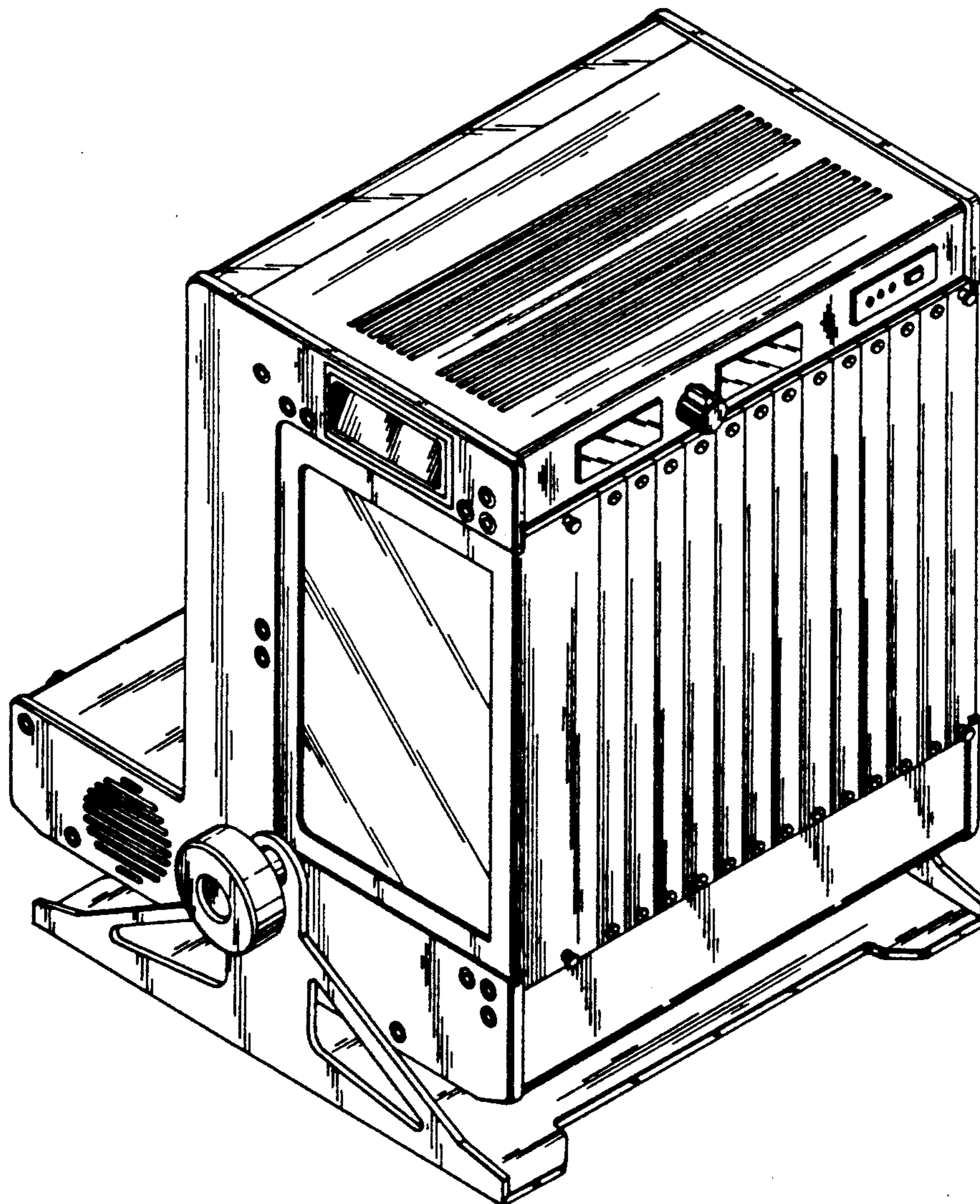
FIG. 6 is a bottom view of the enclosure of FIG. 1; and,

FIG. 7 is a perspective view of the enclosure of FIG. 1.

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

D. 338,416 8/1993 Berry et al. .... D10/75



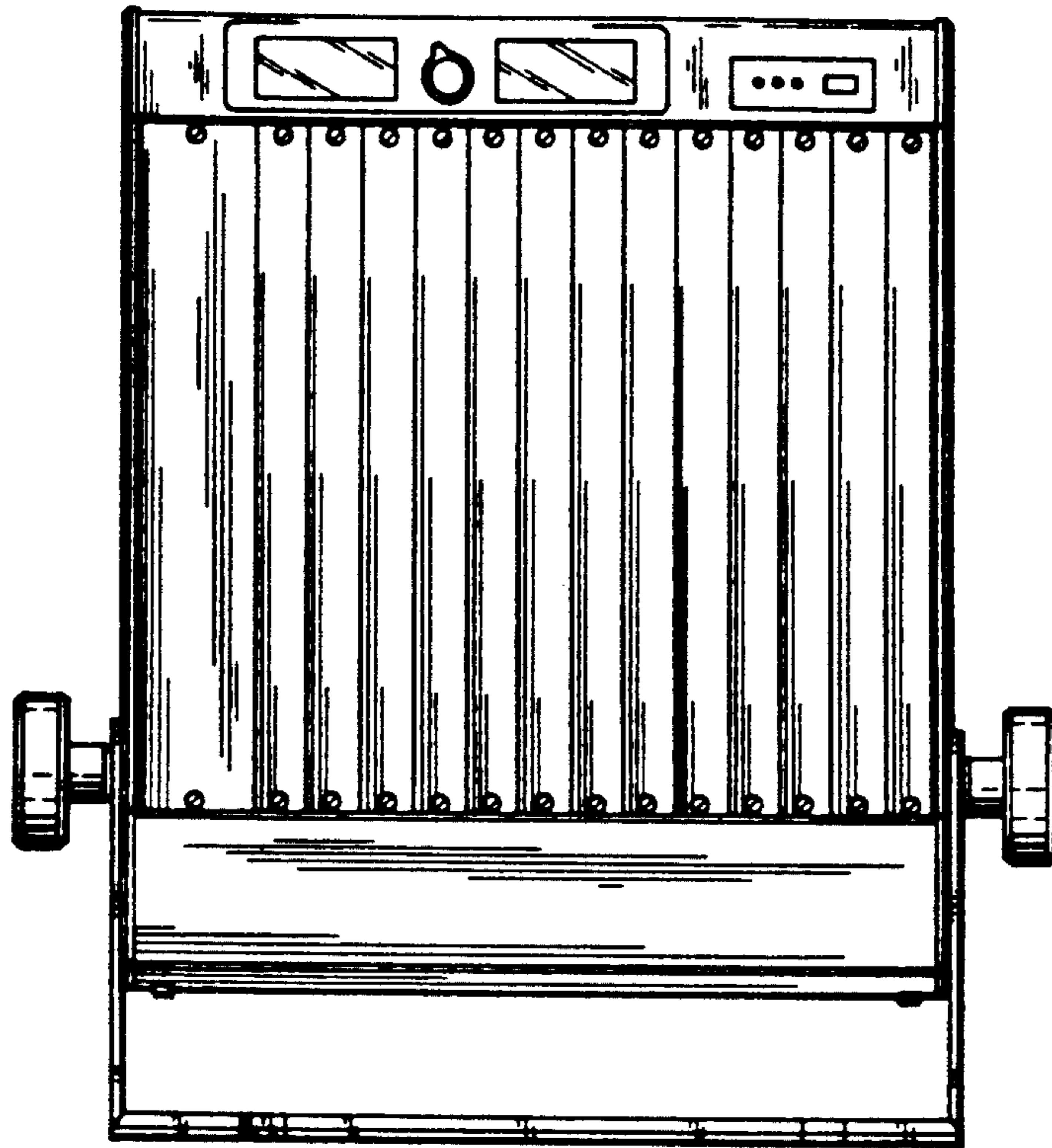


FIG. 1

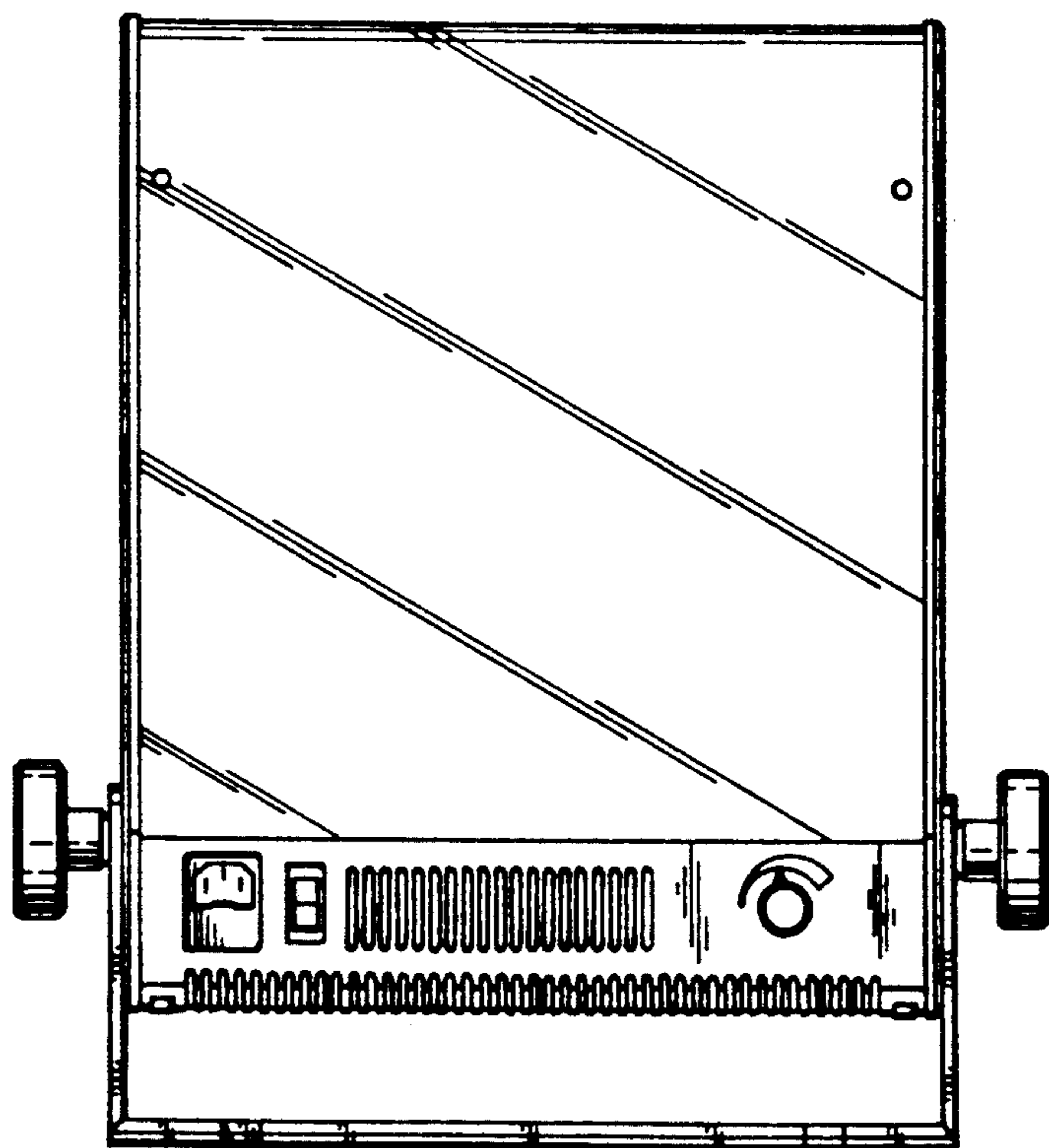


FIG. 2

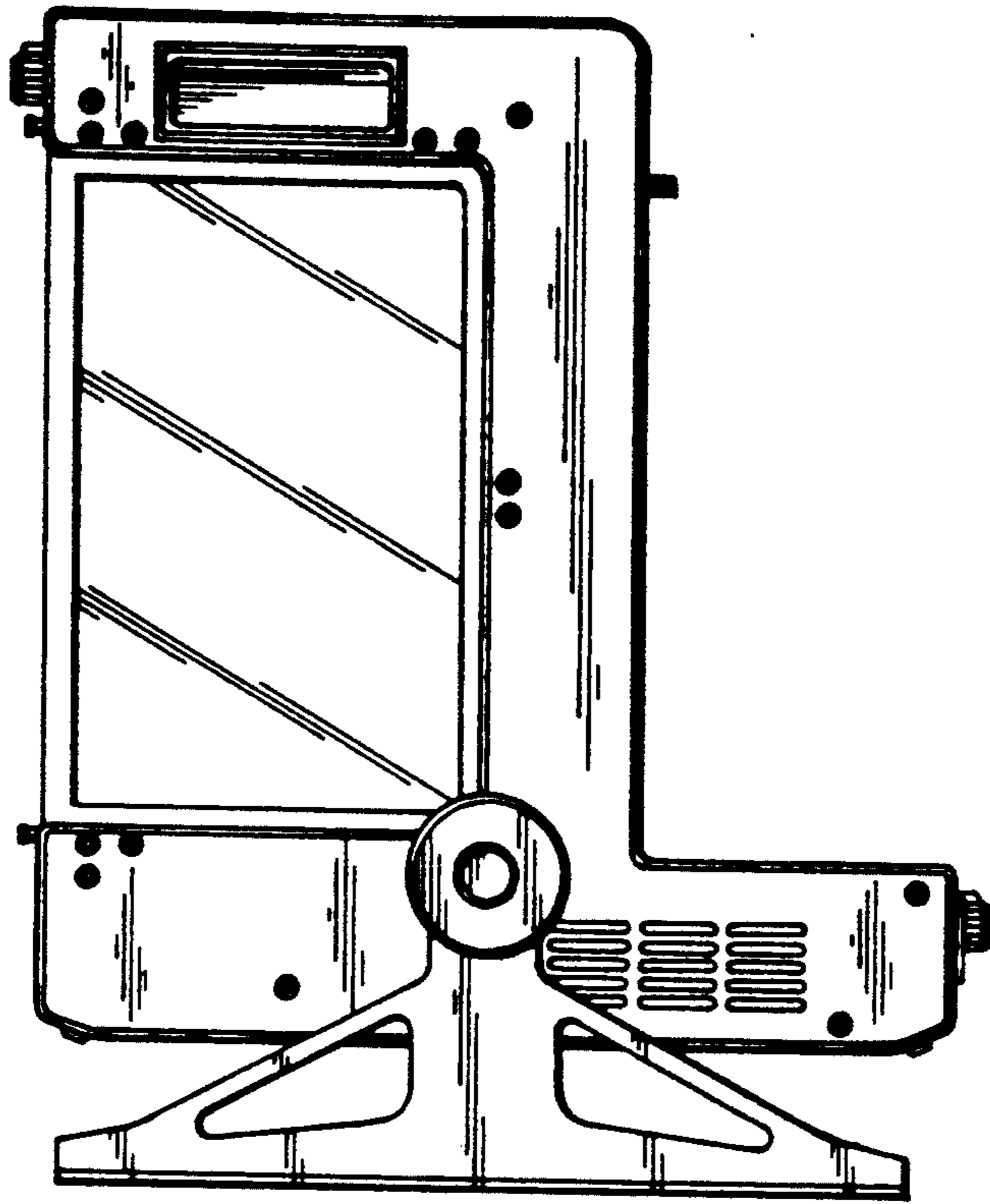


FIG. 3

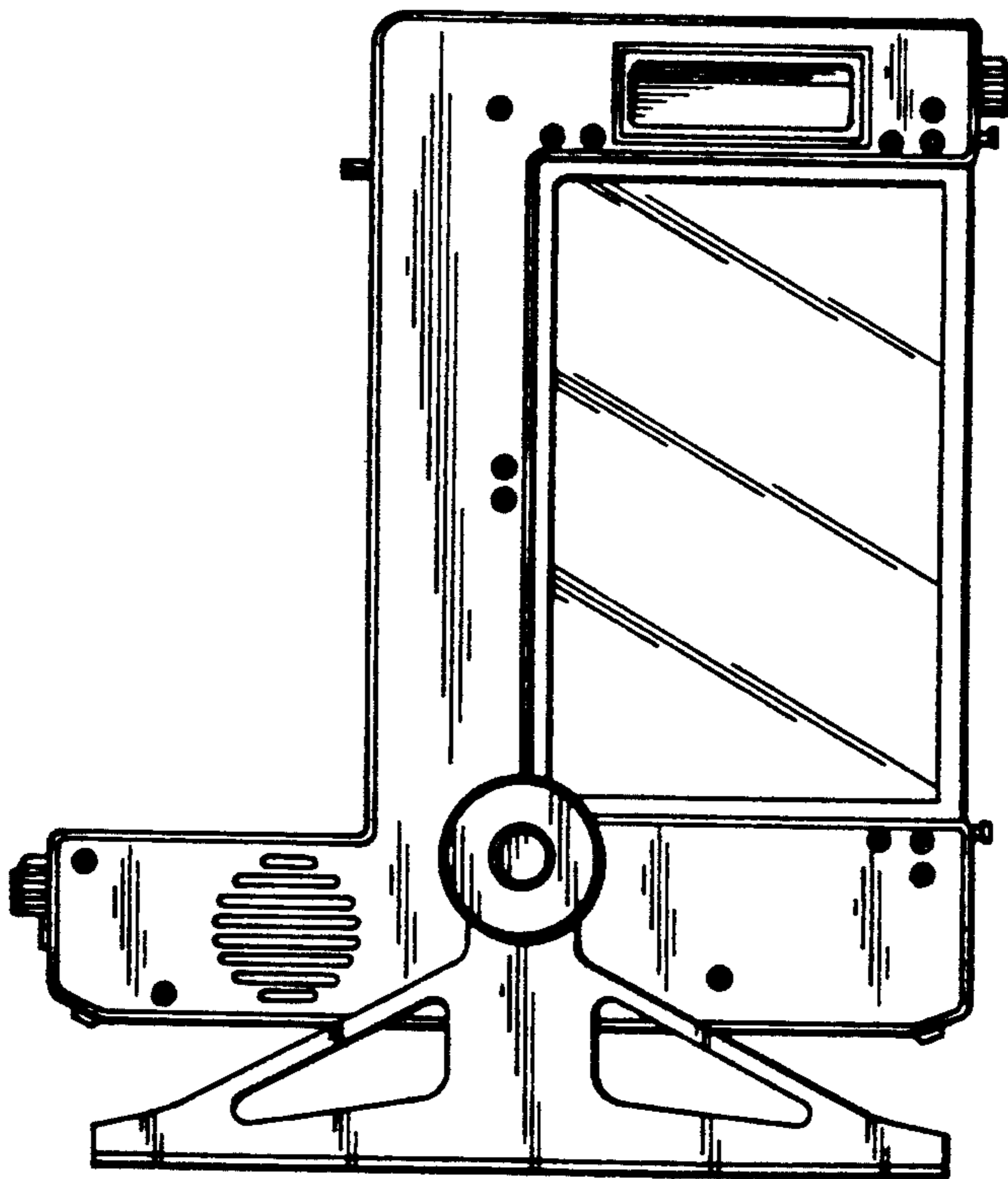


FIG. 4



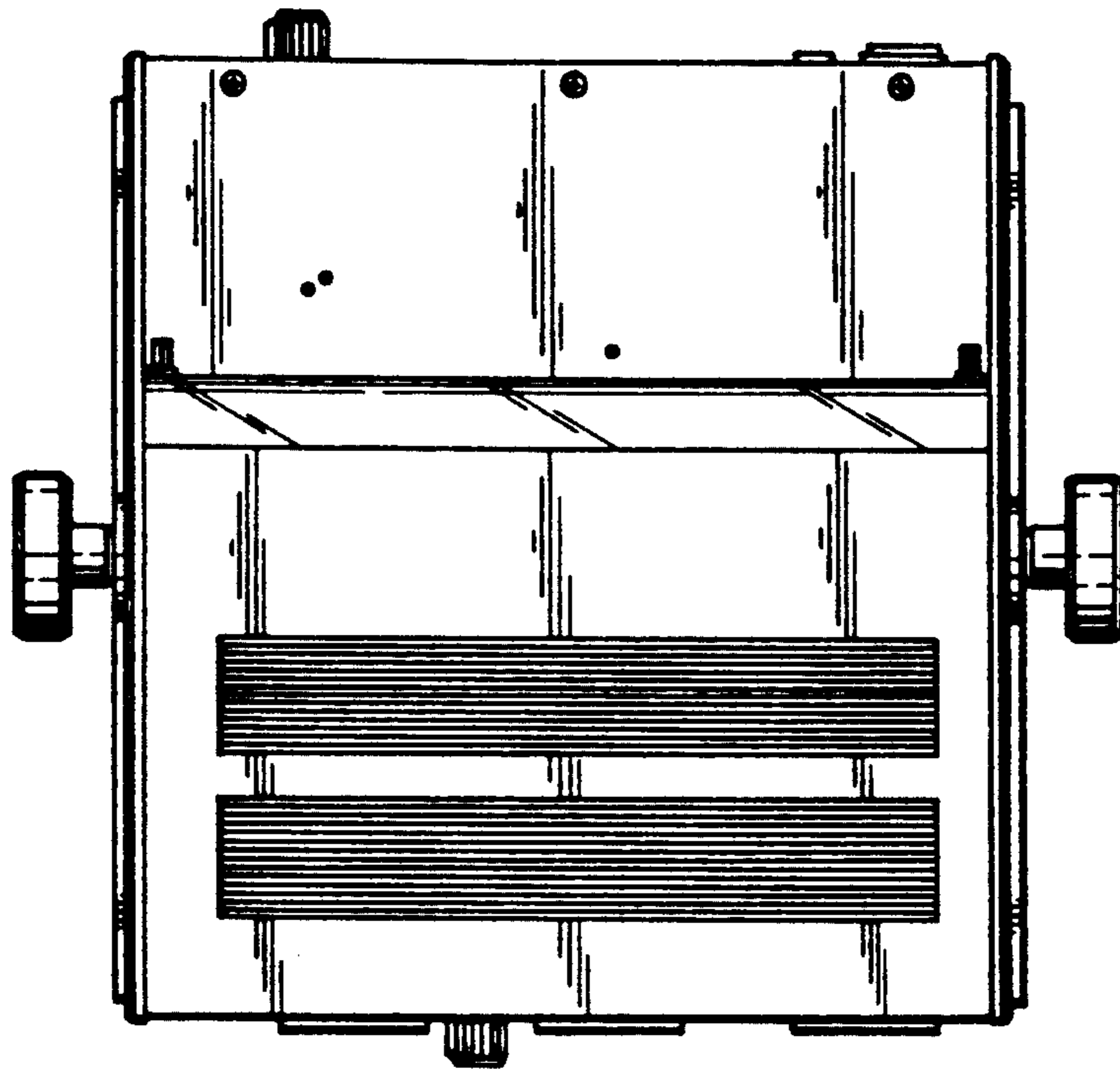


FIG. 5

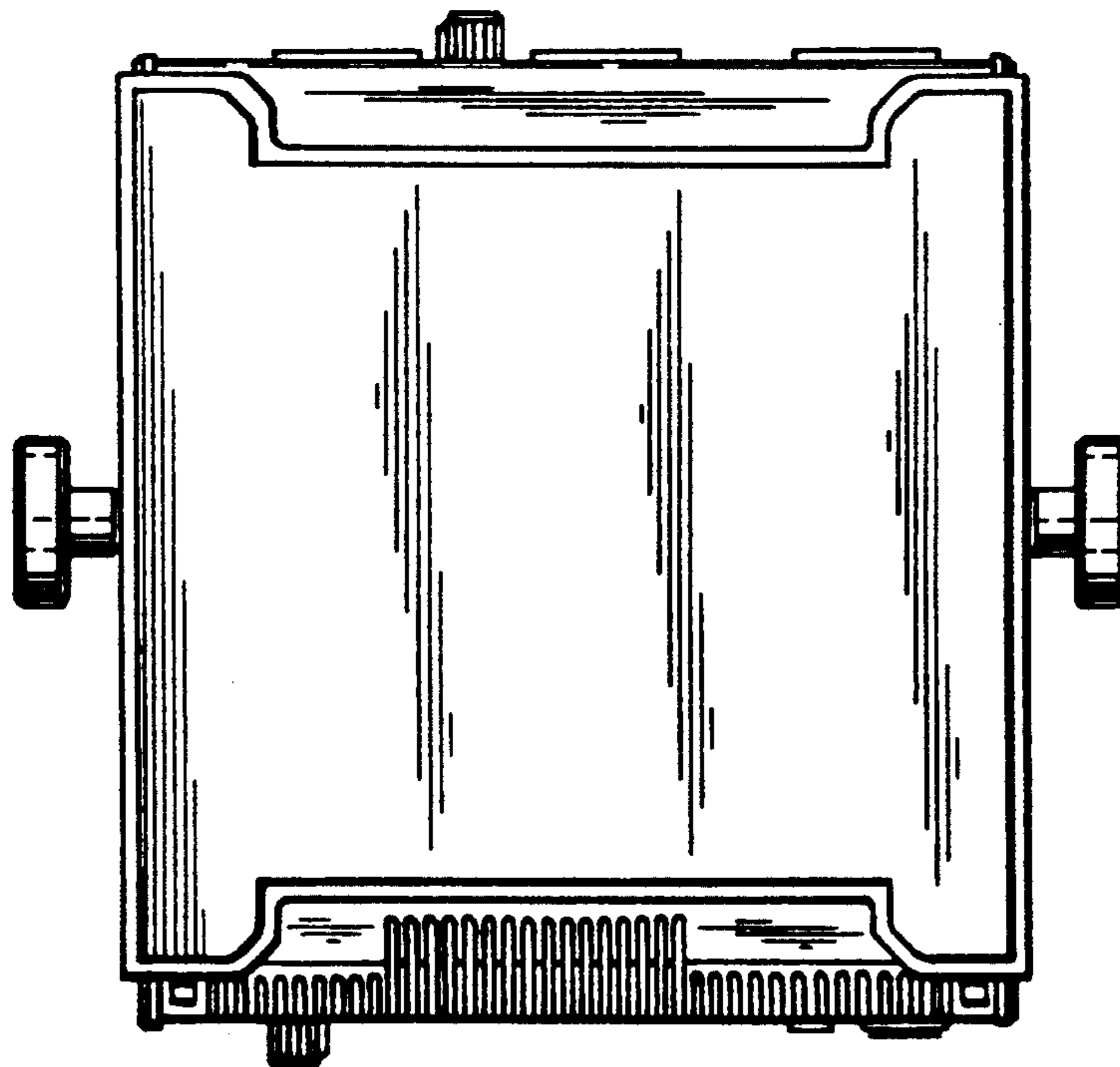


FIG. 6

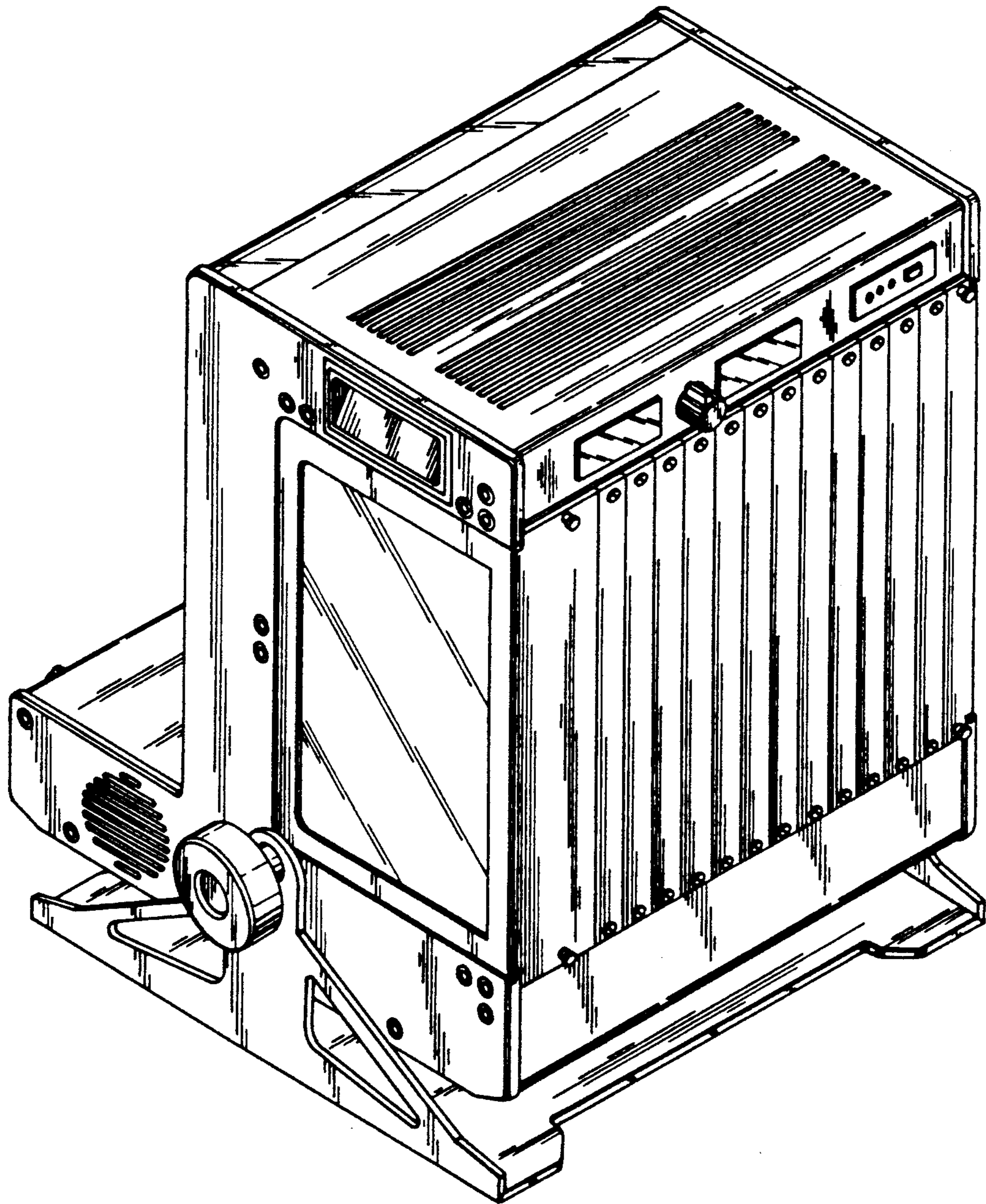


FIG. 7