



US00D342721S

United States Patent [19]

[11] Patent Number: **Des. 342,721**

Itoh

[45] Date of Patent: **** Dec. 28, 1993**

[54] **HEAT DISSIPATING DEVICE FOR A SEMICONDUCTOR PACKAGE**

5,155,579 10/1992 Yeung 174/16.3 X

[75] Inventor: **Akira Itoh, Osaka, Japan**

FOREIGN PATENT DOCUMENTS

0054597 6/1982 European Pat. Off. 361/386

[73] Assignee: **Itoh Research & Development Laboratory Co., Ltd., Osaka, Japan**

OTHER PUBLICATIONS

[**] Term: **14 Years**

Air-Cooled Module on p. 1007 of *IBM Technical Disclosure Bulletin* vol. 20 No. 3 Aug. 1977.

[21] Appl. No.: **933,503**

Heat Removal Module on p. 2249 of *IBM Technical Disclosure Bulletin* vol. 22 No. 6 Nov. 1979.

[22] Filed: **Aug. 21, 1992**

Primary Examiner—Wallace R. Burke

Assistant Examiner—Joel Sincavage

[30] Foreign Application Priority Data

Attorney, Agent, or Firm—W. G. Fasse; D. H. Kane, Jr.

Mar. 4, 1992 [JP] Japan 4-6202

[52] U.S. Cl. **D13/179**

[57] CLAIM

[58] Field of Search 437/902; 165/80.2, 80.3, 165/104.33; 257/713, 720; 361/383, 386; 174/52.1, 15.2, 16.3; D13/179, 182

The ornamental design for a heat dissipating device for a semiconductor package, as shown and described.

[56] References Cited

DESCRIPTION

U.S. PATENT DOCUMENTS

- D. 276,719 12/1984 Sugimoto et al. D13/179 X
- 3,241,605 3/1966 Tabor D13/179 X
- 3,406,753 10/1968 Habdas 165/80.2 X
- 3,572,428 3/1971 Monaco 361/383 X
- 3,589,046 5/1971 Jordan 174/52.1
- 3,884,293 5/1975 Pessolano et al. 361/386 X
- 4,292,647 9/1981 Lee 165/80.3 X
- 4,644,385 2/1987 Nakanishi et al. 257/713
- 4,716,494 12/1987 Bright et al. 174/16.3 X
- 5,087,888 2/1992 Mountz et al. 361/383 X

FIG. 1 is a front view of an embodiment of the heat dissipating device for a semiconductor package;

FIG. 2 is a top plan view thereof;

FIG. 3 is a bottom plan view thereof;

FIG. 4 is a right side view thereof;

FIG. 5 is a perspective view thereof;

FIG. 6 is a sectional view taken along section line 6—6 in FIG. 2; and,

FIG. 7 is the same view as in FIG. 4 showing the heat dissipating device attached to a semiconductor package shown in broken lines since the packages do not form any part of the claimed design.

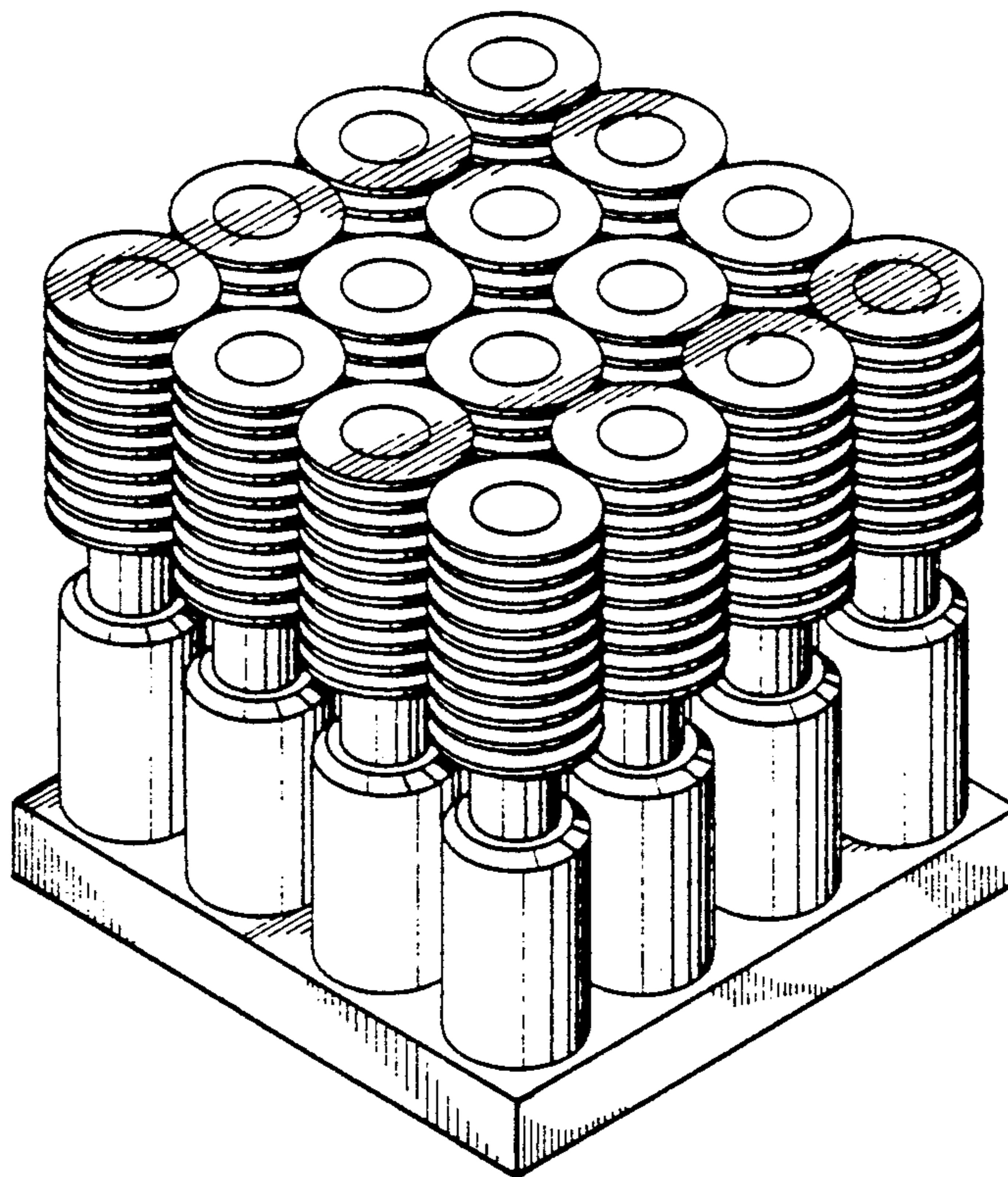


FIG. 1

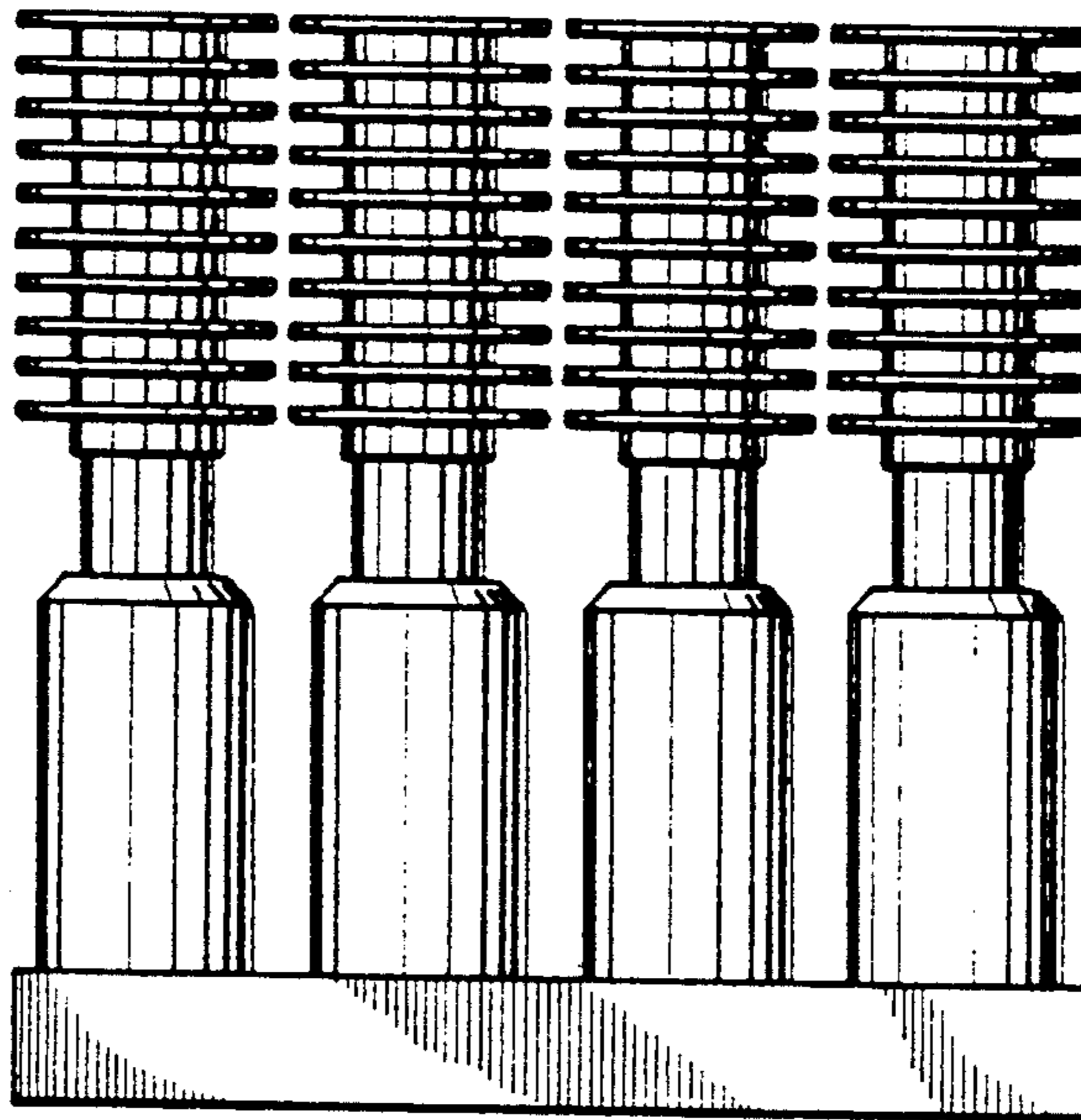


FIG. 4

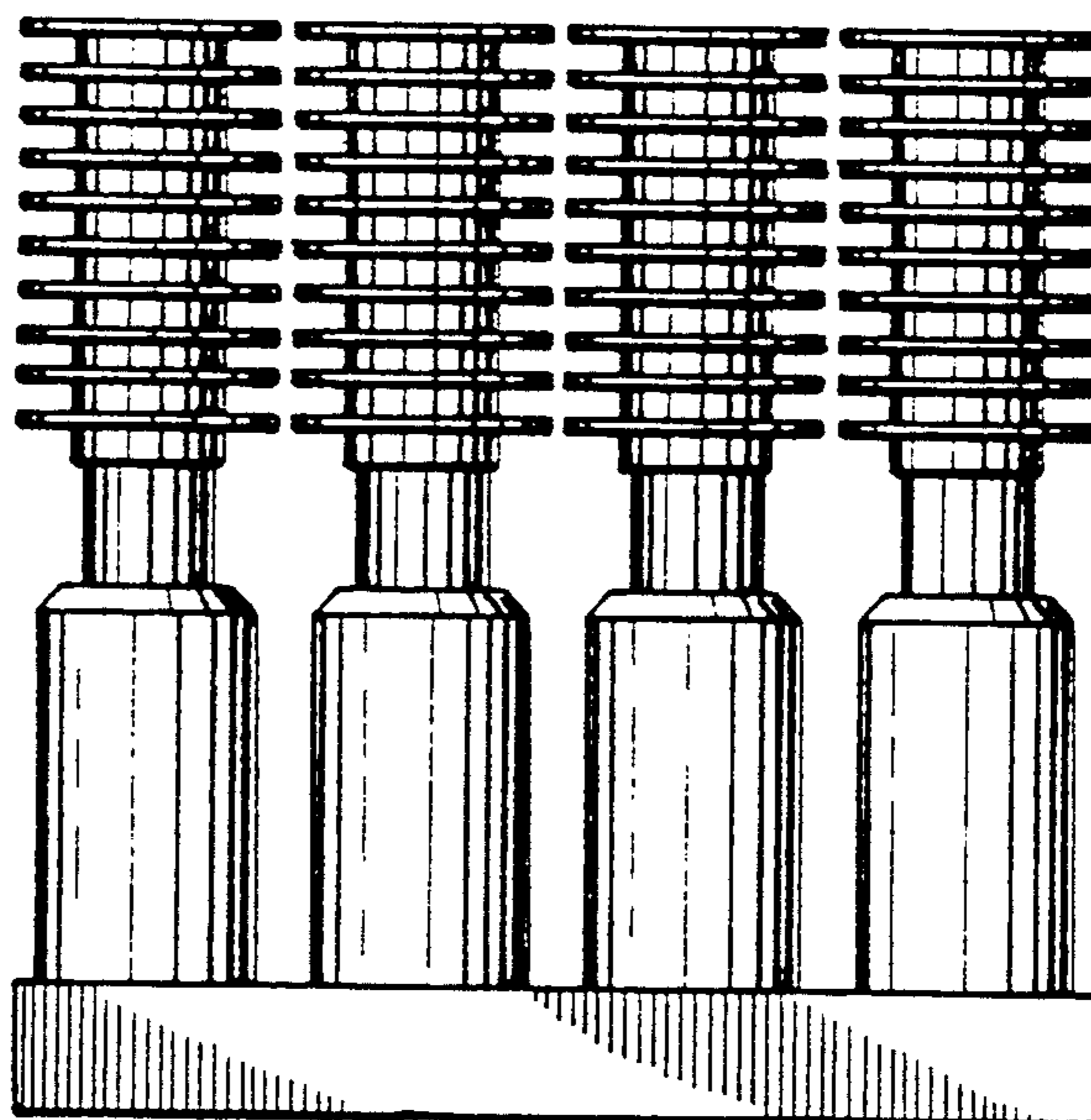


FIG. 2

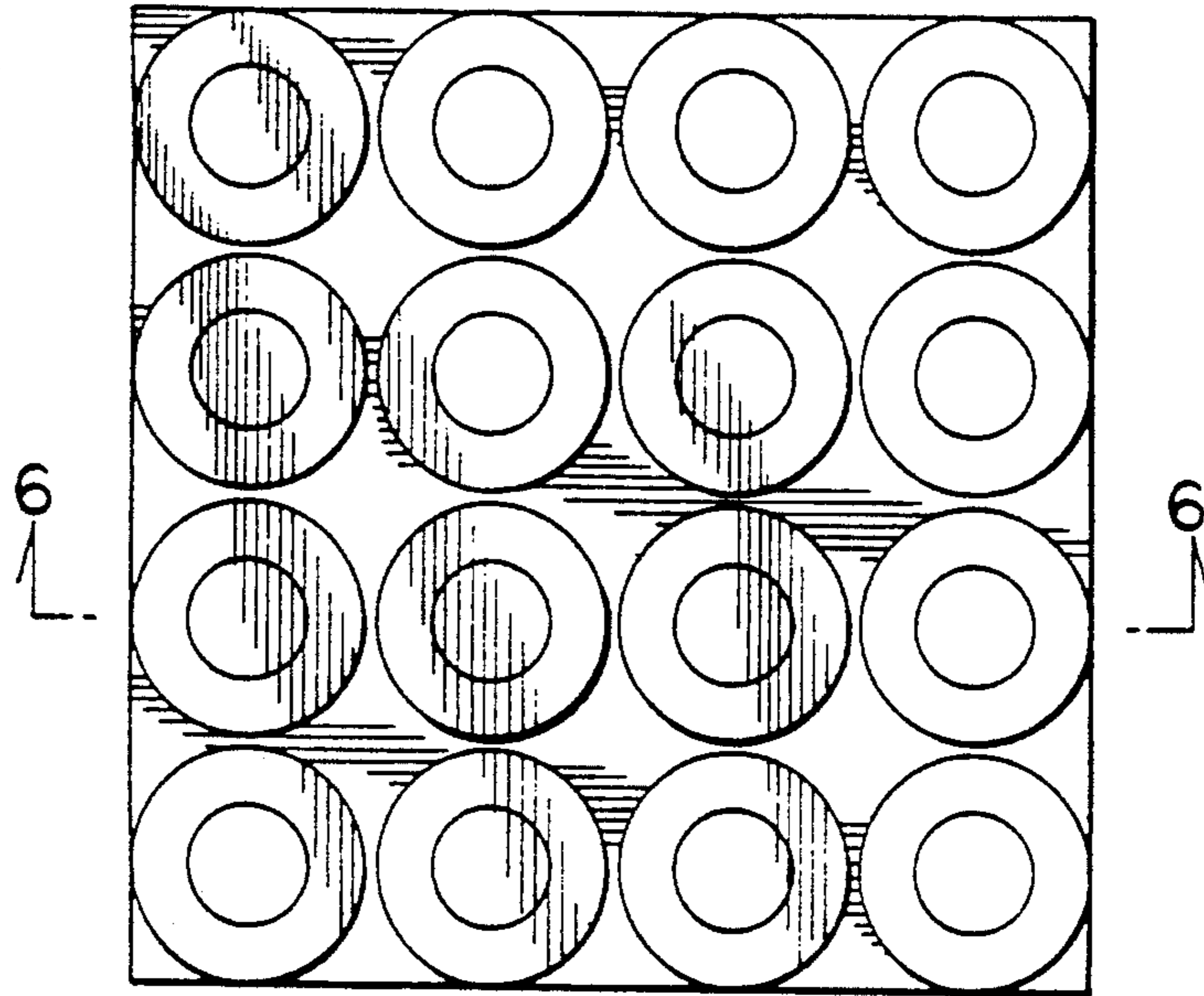


FIG. 3

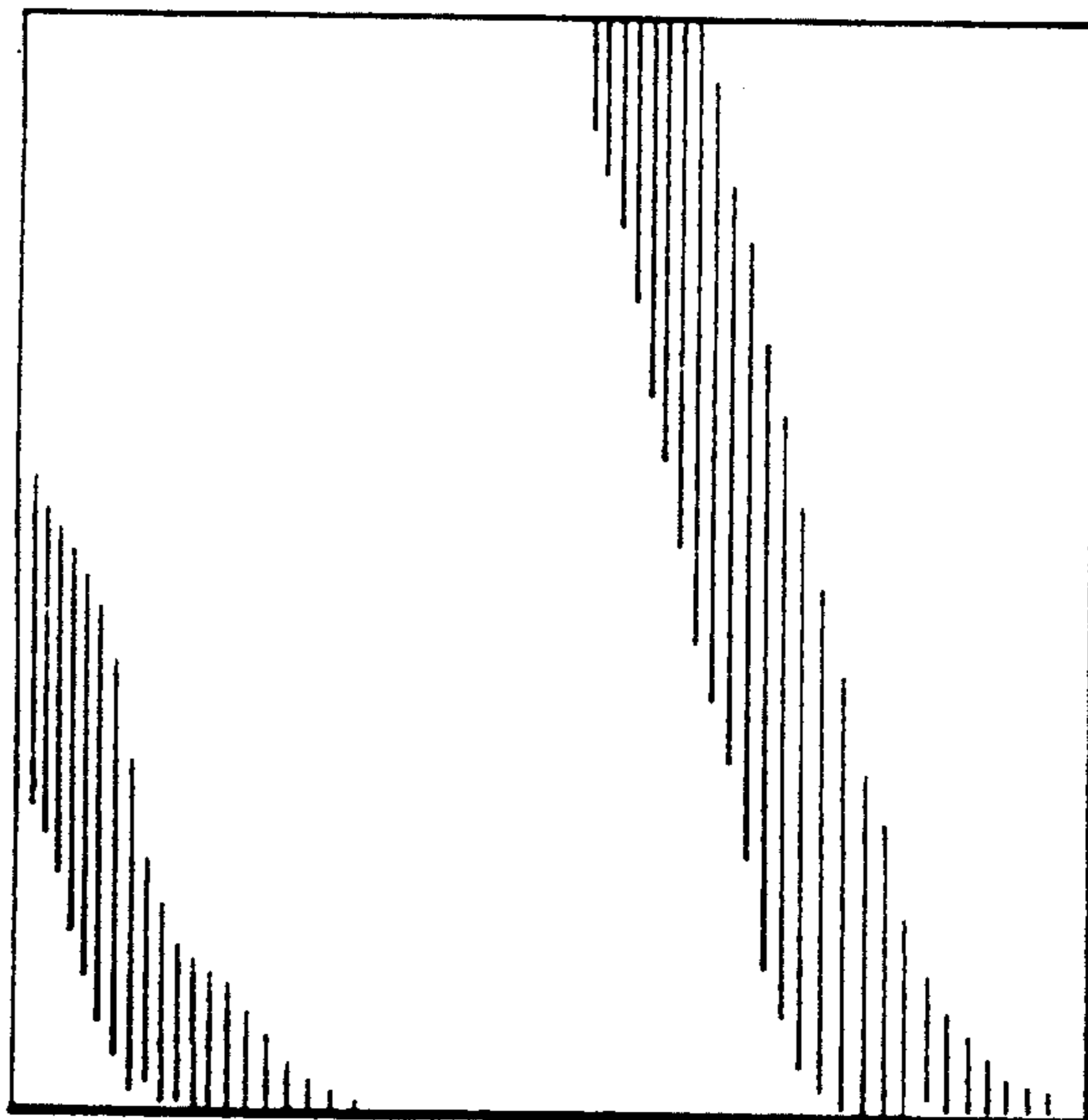


FIG. 5

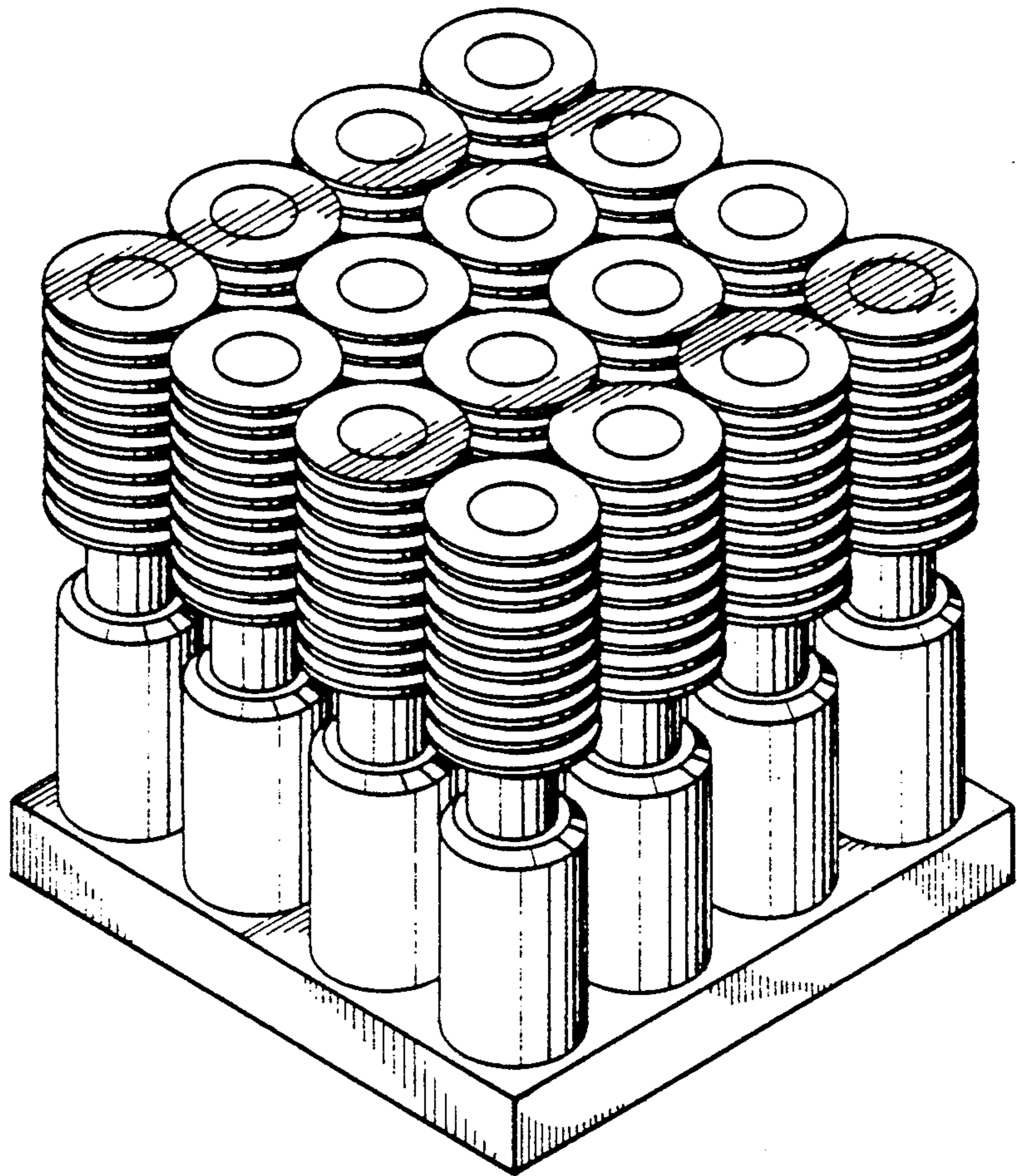


FIG. 6

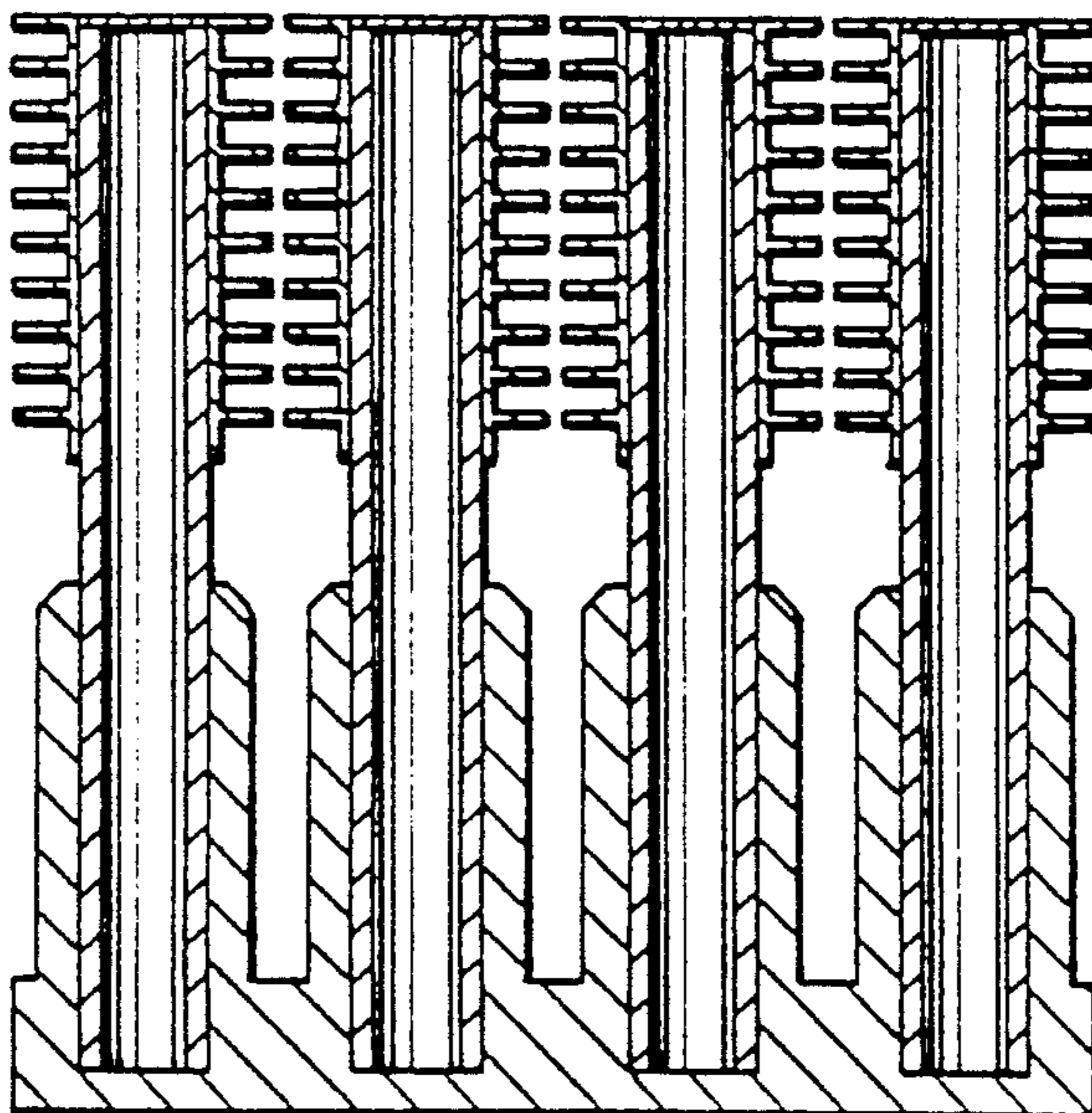
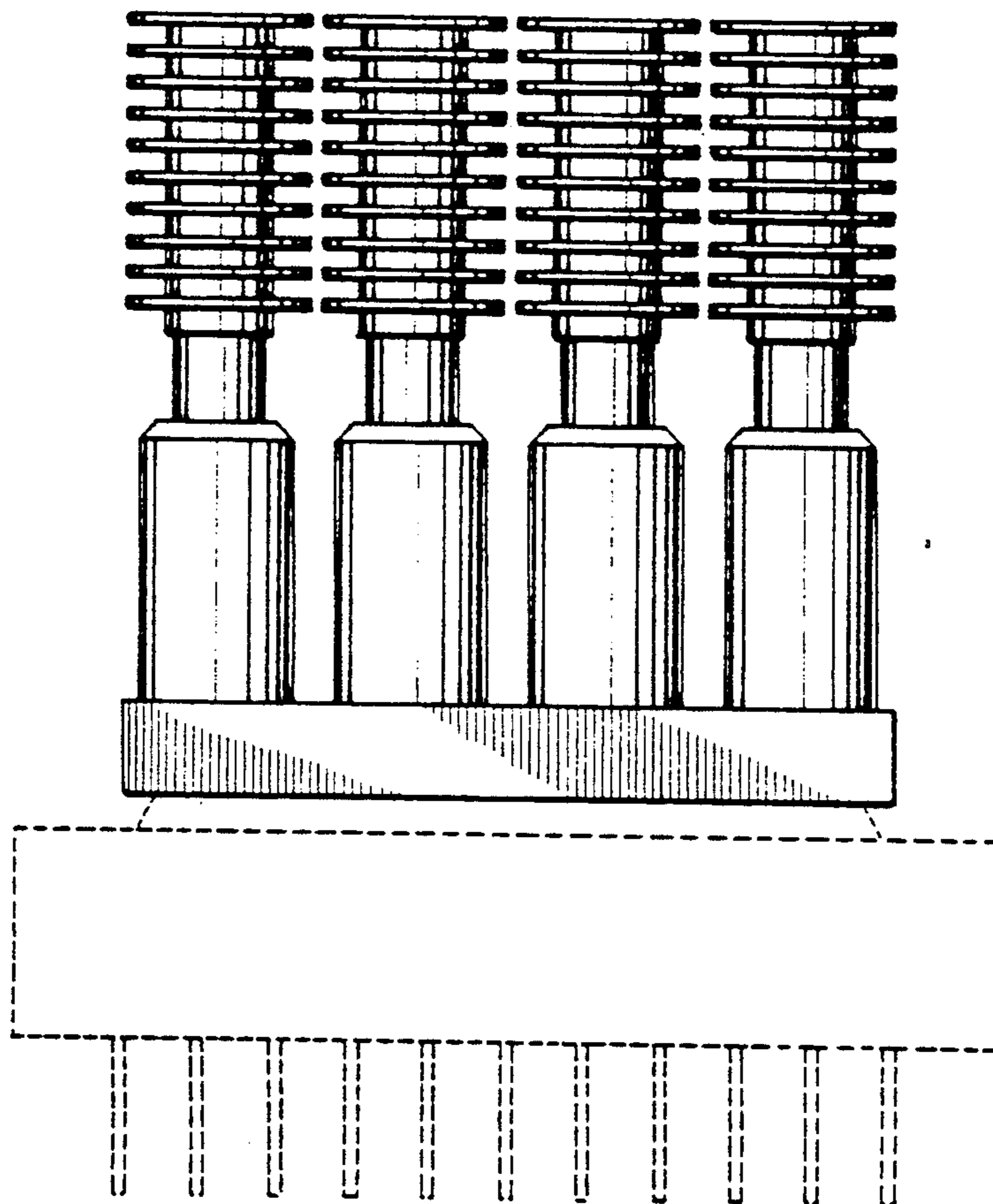


FIG. 7



UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : Des. 342,721

DATED : Dec. 28, 1993

INVENTOR(S) : Akira Itoh

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Insert item [63]

— The present Design Application relates to U. S. Design Application USSN: 07/933,532, filed on August 21, 1992. —

Signed and Sealed this
Fifth Day of December, 1995

Attest:



Attesting Officer

BRUCE LEHMAN

Commissioner of Patents and Trademarks