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United States Patent [19]

Barabi et al.

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[45] **Date of Patent:** ** **Mar. 23, 1993**

[54] **PROBE INTERFACE TEST BOARD**

[75] Inventors: **Nasser Barabi; Iraj Barabi,** both of Oakland, Calif.

[73] Assignee: **Oz Technologies, Inc.,** Hayward, Calif.

[**] Term: **14 Years**

[21] Appl. No.: **684,356**

[22] Filed: **Apr. 12, 1991**

[52] **U.S. Cl.** **D13/182;** D10/80

[58] **Field of Search** D13/182; D10/75, 80; 439/219, 329, 325, 482, 669, 912

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 255,351	6/1980	Pettijohn	D13/182
D. 261,760	11/1981	Dlugos	D13/182 X
D. 275,659	9/1984	Hackamack	D13/182 X
D. 319,629	9/1991	Hasegawa et al.	D13/182
3,496,514	1/1970	Gallentine	439/912 X
3,813,644	5/1974	Shlesinger, Jr.	439/723
4,540,229	9/1985	Madden	439/325
4,582,383	4/1986	Jo et al.	439/482
4,655,535	4/1987	Kysiak	439/669
5,008,614	4/1991	Shreeve et al.	D13/182 X

OTHER PUBLICATIONS

Circuit boards on p. 144F of *Electronic Design,* Jan. 4, 1979.

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Attorney, Agent, or Firm—Donald L. Beeson

[57] **CLAIM**

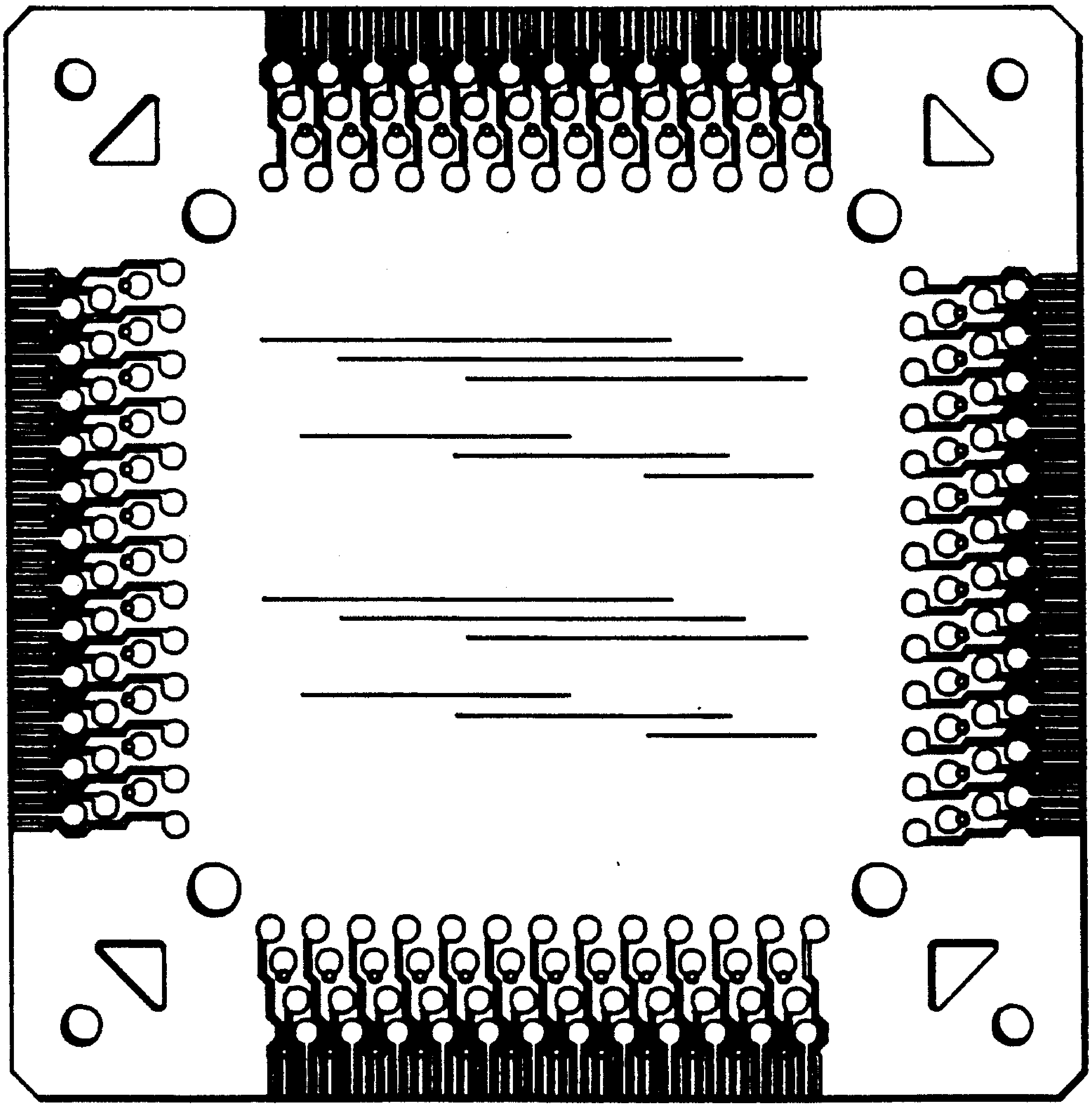
The ornamental design for a probe interface test board, as shown and described.

DESCRIPTION

FIG. **1** is a top plan view of a probe interface test board showing our new design;

FIG. **2** is a bottom plan view thereof; and,

FIG. **3** is a front side elevational view thereof, the left, right, and rear elevational views being a mirror image.



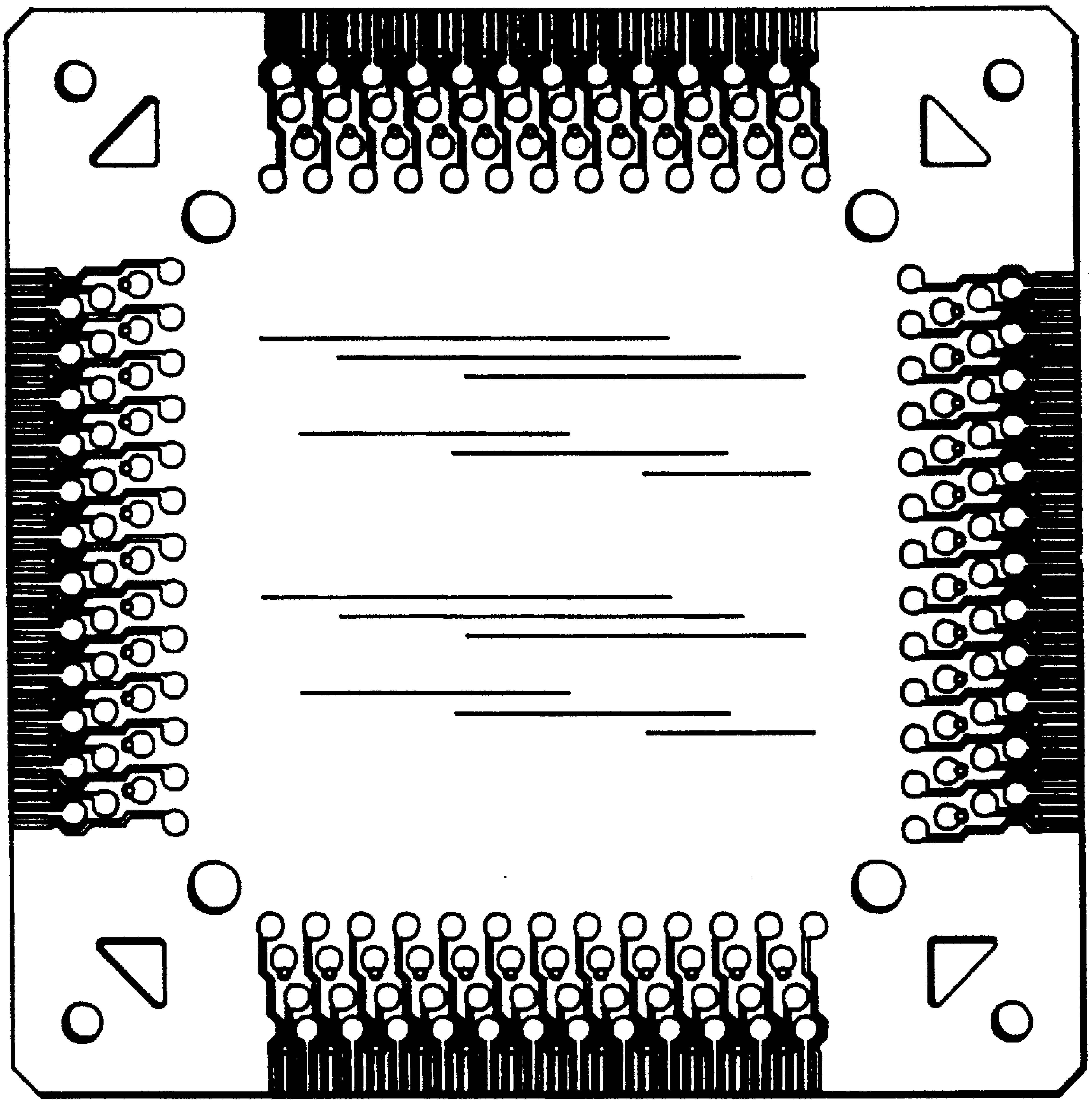


FIG.-1

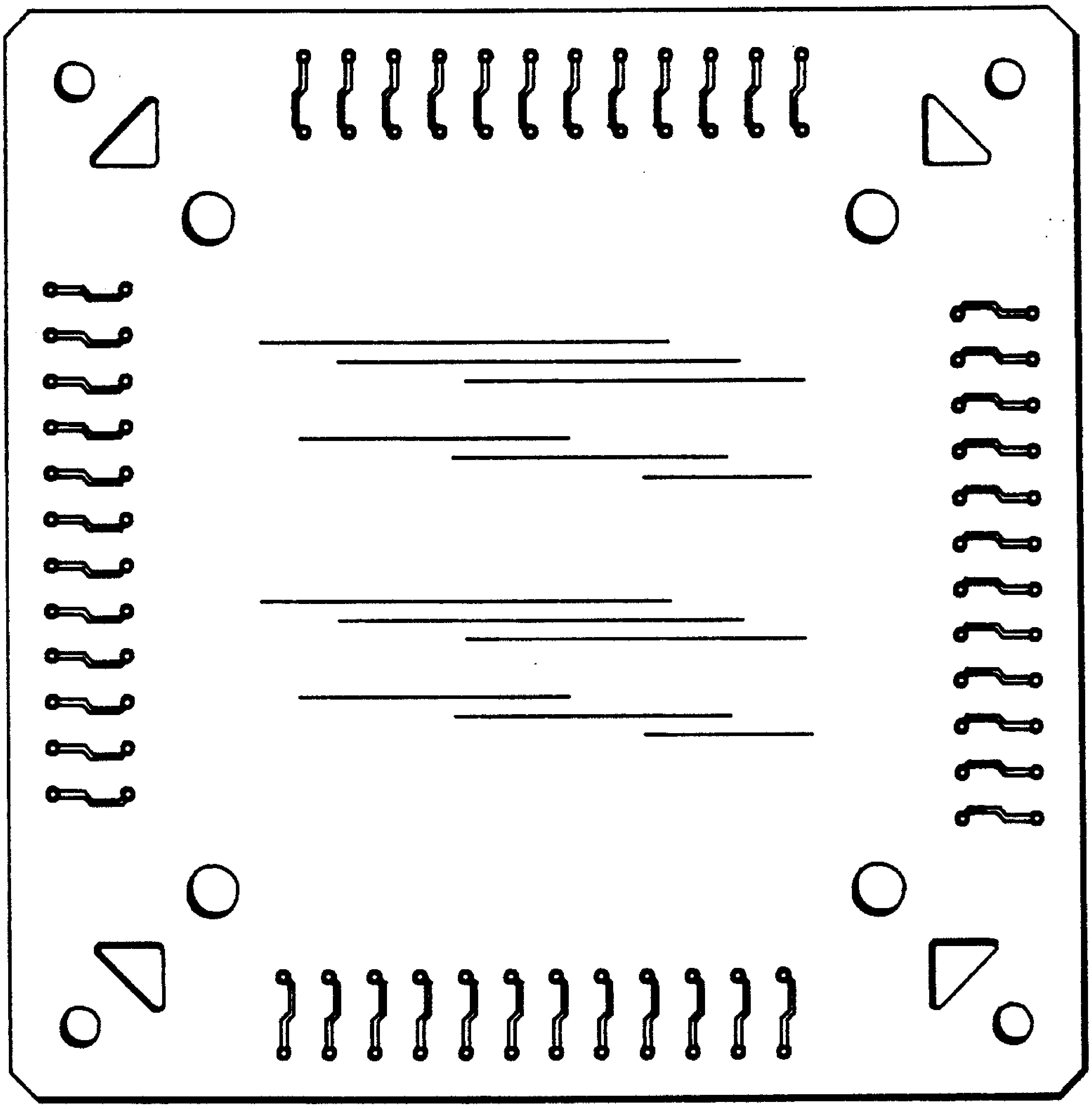


FIG.-2

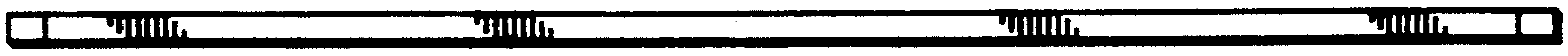


FIG.-3