



US00D329639S

United States Patent [19]

[11] Patent Number: **Des. 329,639**

Arvanitakis et al.

[45] Date of Patent: **** Sep. 22, 1992**

[54] **OPTOELECTRONIC ASSEMBLY**

[75] Inventors: **Nicolaos C. Arvanitakis, Vestal, N.Y.; Vincent J. Black, Austin, Tex.; Richard G. Nolan, Binghamton, N.Y.**

4,647,148 3/1987 Katagiri 350/96.20
 4,719,358 1/1987 Matsumoto et al. 250/551
 4,755,017 7/1988 Kapany 350/96.18
 4,762,388 8/1988 Tanaka et al. 350/96.20
 4,807,956 2/1989 Tournereau et al. 350/96.20
 4,976,510 11/1990 Davila et al. 385/53
 5,005,939 4/1991 Arvanitakis et al. 385/53

[73] Assignee: **International Business Machines Corporation, Armonk, N.Y.**

Primary Examiner—Wallace R. Burke
Assistant Examiner—Joel Sincavage
Attorney, Agent, or Firm—Lawrence R. Fraley

[**] Term: **14 Years**

[21] Appl. No.: **499,832**

[57] CLAIM

[22] Filed: **Mar. 26, 1990**

The ornamental design for an optoelectronic assembly, as shown and described.

[52] U.S. Cl. **D13/165; D13/133; D13/179**

DESCRIPTION

[58] Field of Search **D13/133, 146, 147, 152, D13/179; 250/227.24, 551; 385/53, 58, 59, 90, 88, 92, 94; 361/394, 395**

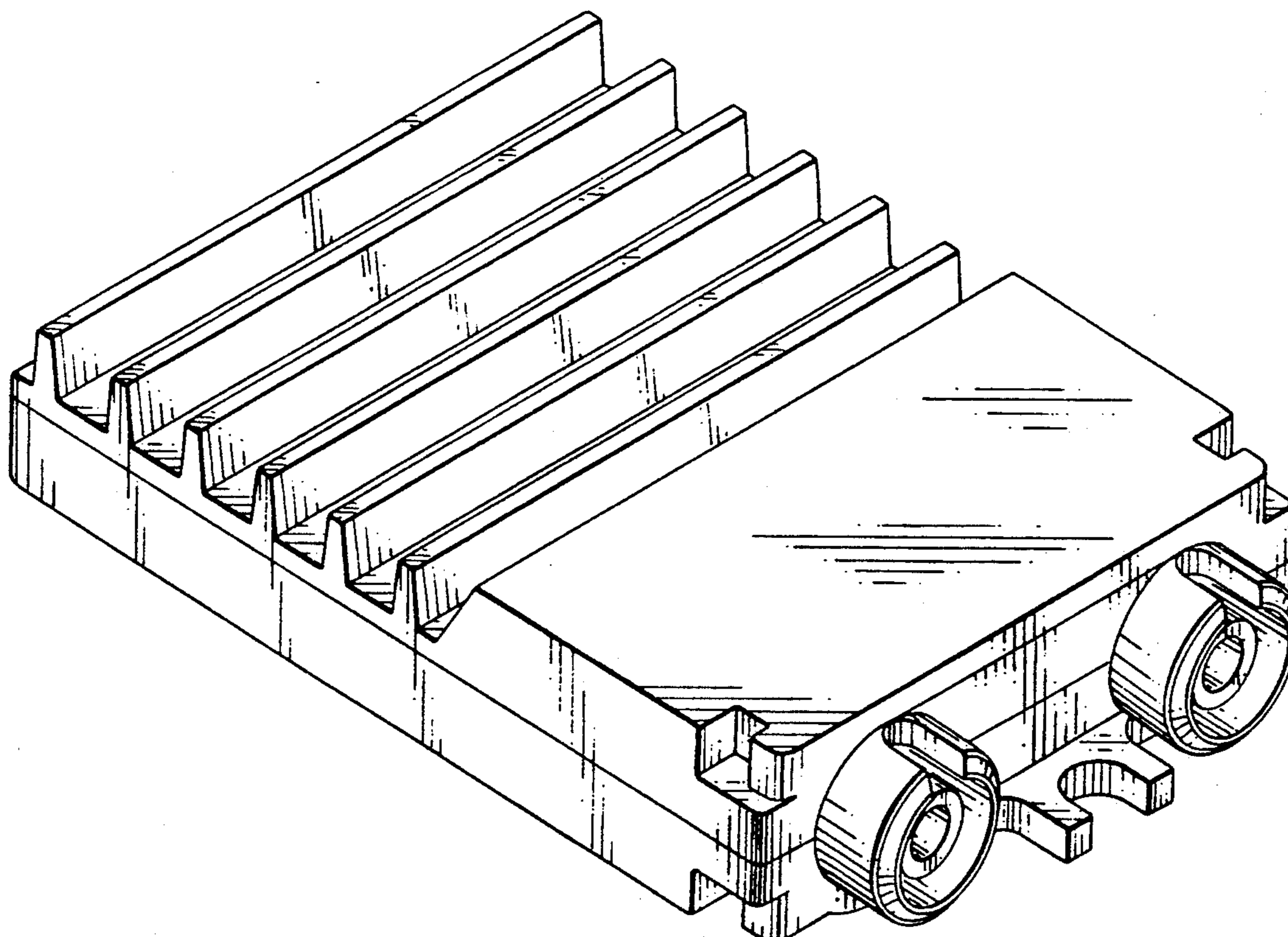
FIG. 1 is a perspective view of an optoelectronic assembly, illustrating our new design;
 FIG. 2 is a front elevational view thereof, on a reduced scale;
 FIG. 3 is a rear elevational view thereof, on a reduced scale;
 FIG. 4 is a side elevational view thereof, on a reduced scale, the opposite side being a mirror image;
 FIG. 5 is a top plan view thereof, on a reduced scale; and,
 FIG. 6 is a bottom plan view thereof, on a reduced scale.

[56] References Cited

U.S. PATENT DOCUMENTS

D. 186,222	9/1959	Atkin	D13/152
D. 286,770	11/1986	Melcher	D13/179 X
3,904,812	9/1975	Daffron	361/395 X
4,273,413	6/1981	Bendiksen et al.	350/96.20
4,384,368	5/1983	Rosenfeldt et al.	361/394 X
4,427,879	1/1984	Becher et al.	250/215
4,547,039	10/1985	Caron et al.	350/96.20
4,549,314	10/1985	Masuda et al.	455/618
4,611,886	9/1986	Cline et al.	350/96.20
4,625,333	11/1986	Takezawa et al.	455/612

The terminal pins shown in FIGS. 2, 3, 4 and 6 are illustrated in dashed form for environmental purposes only.



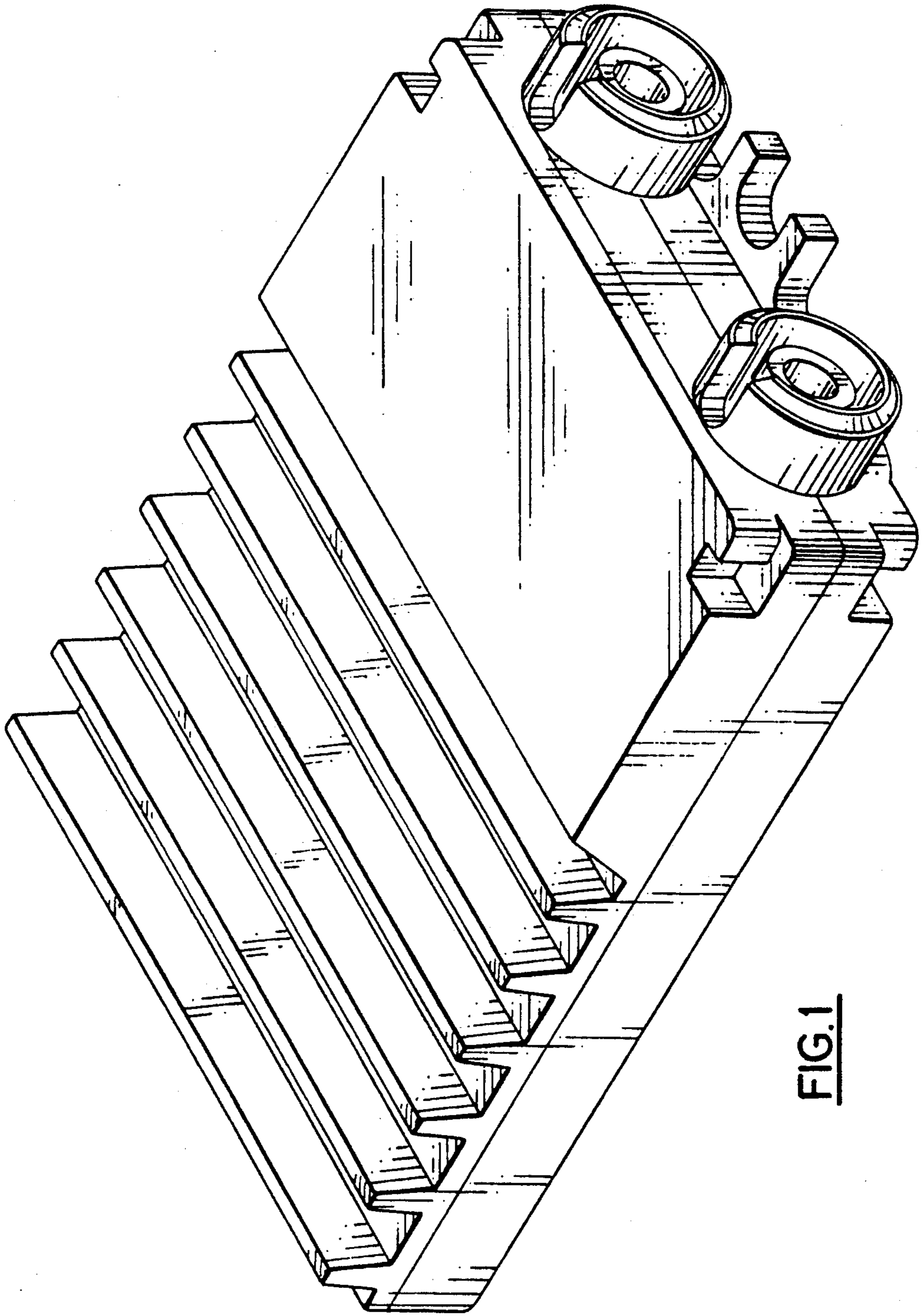


FIG.1

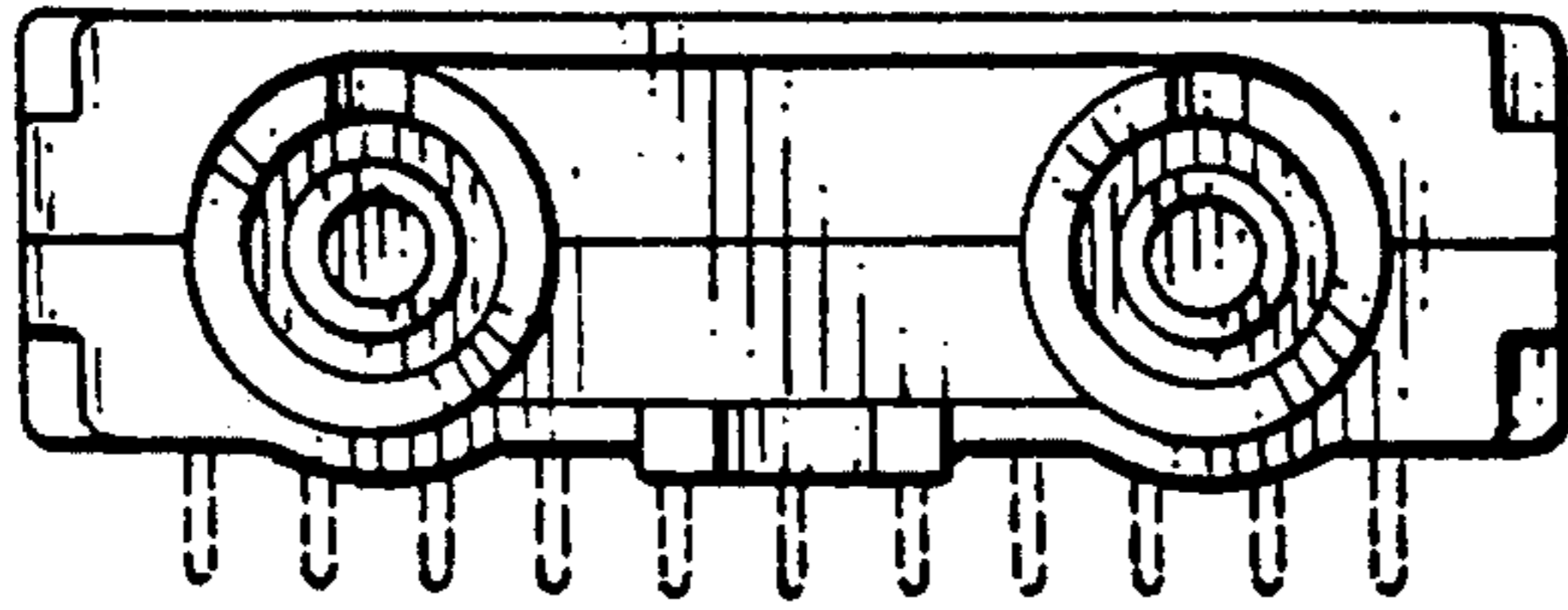


FIG. 2

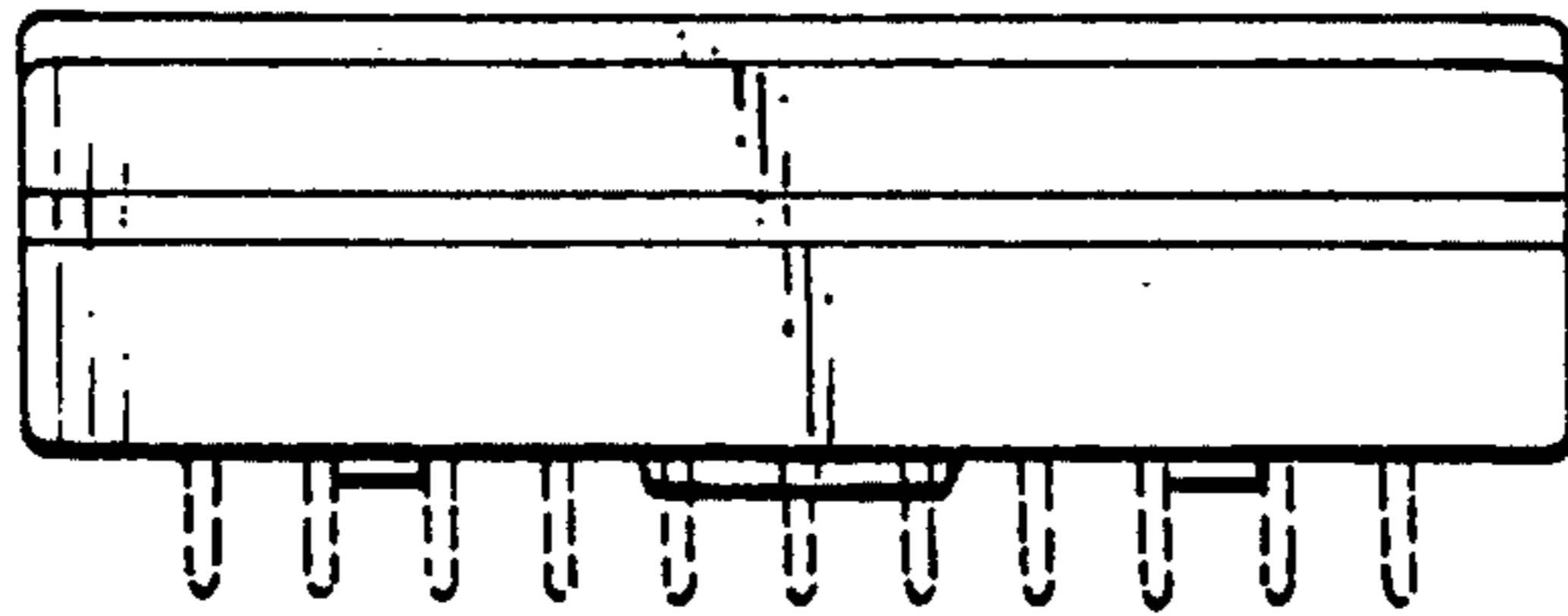


FIG. 3

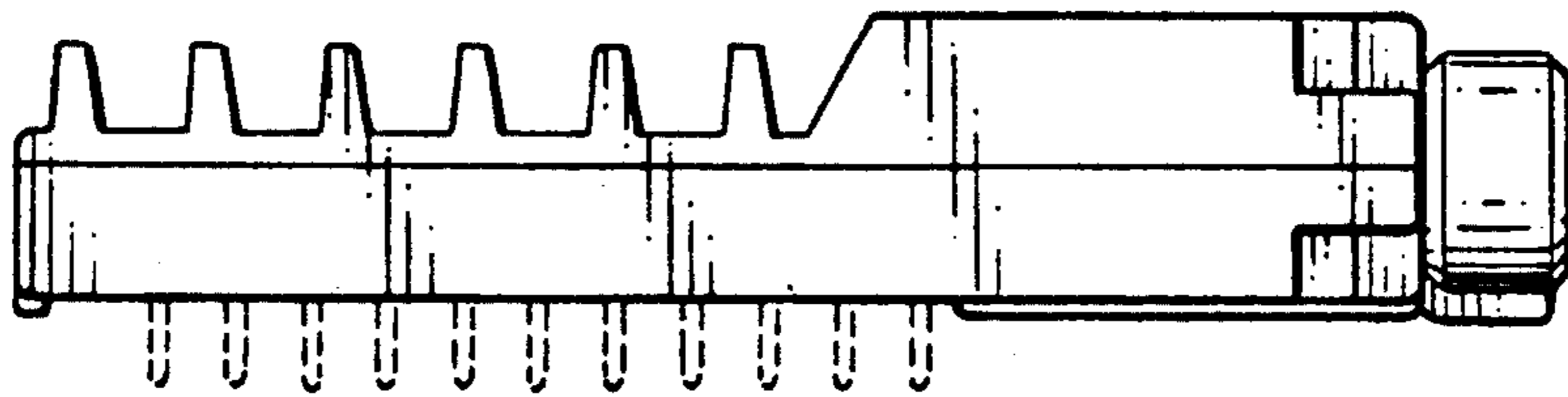


FIG. 4

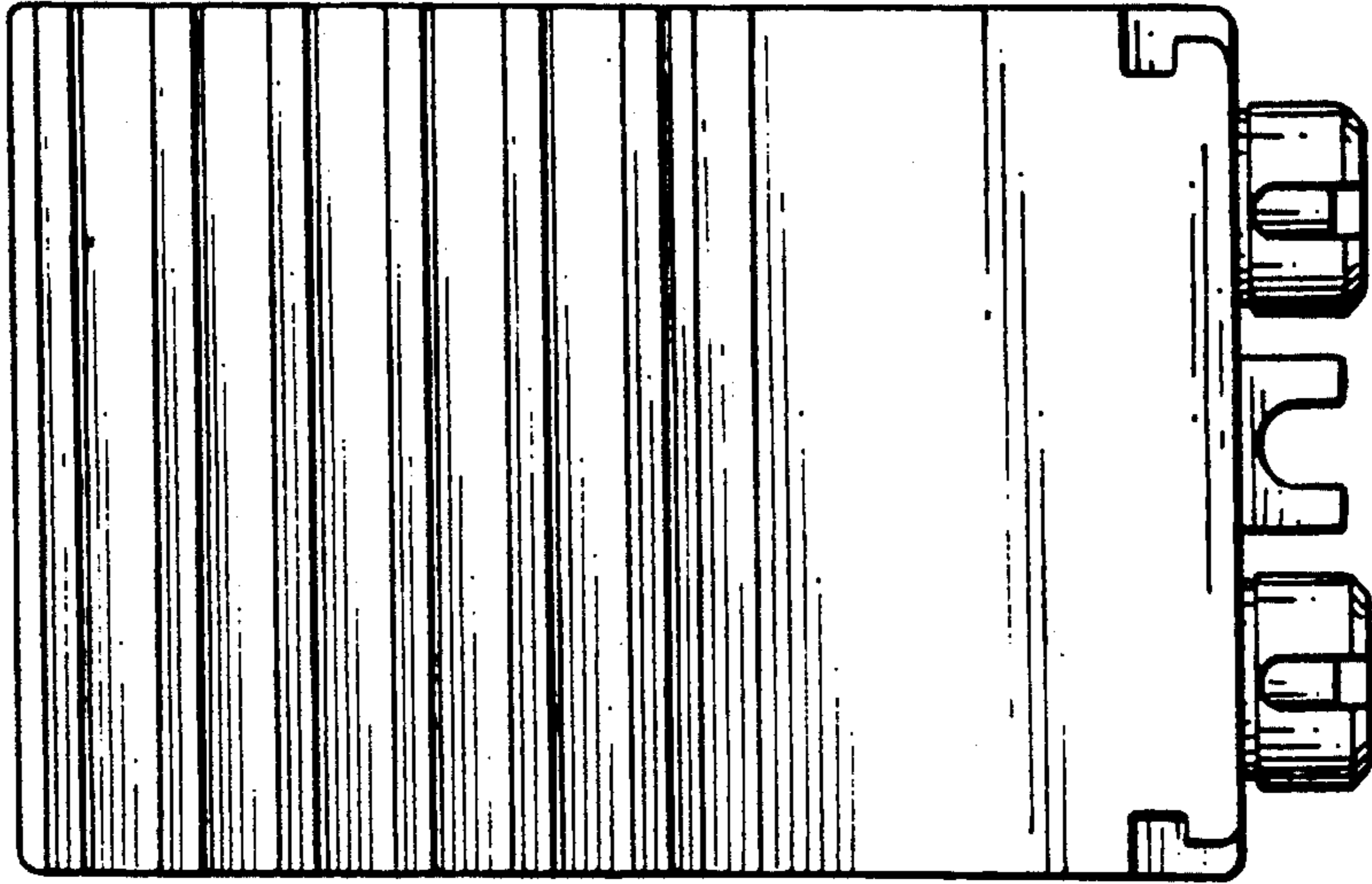


FIG. 5

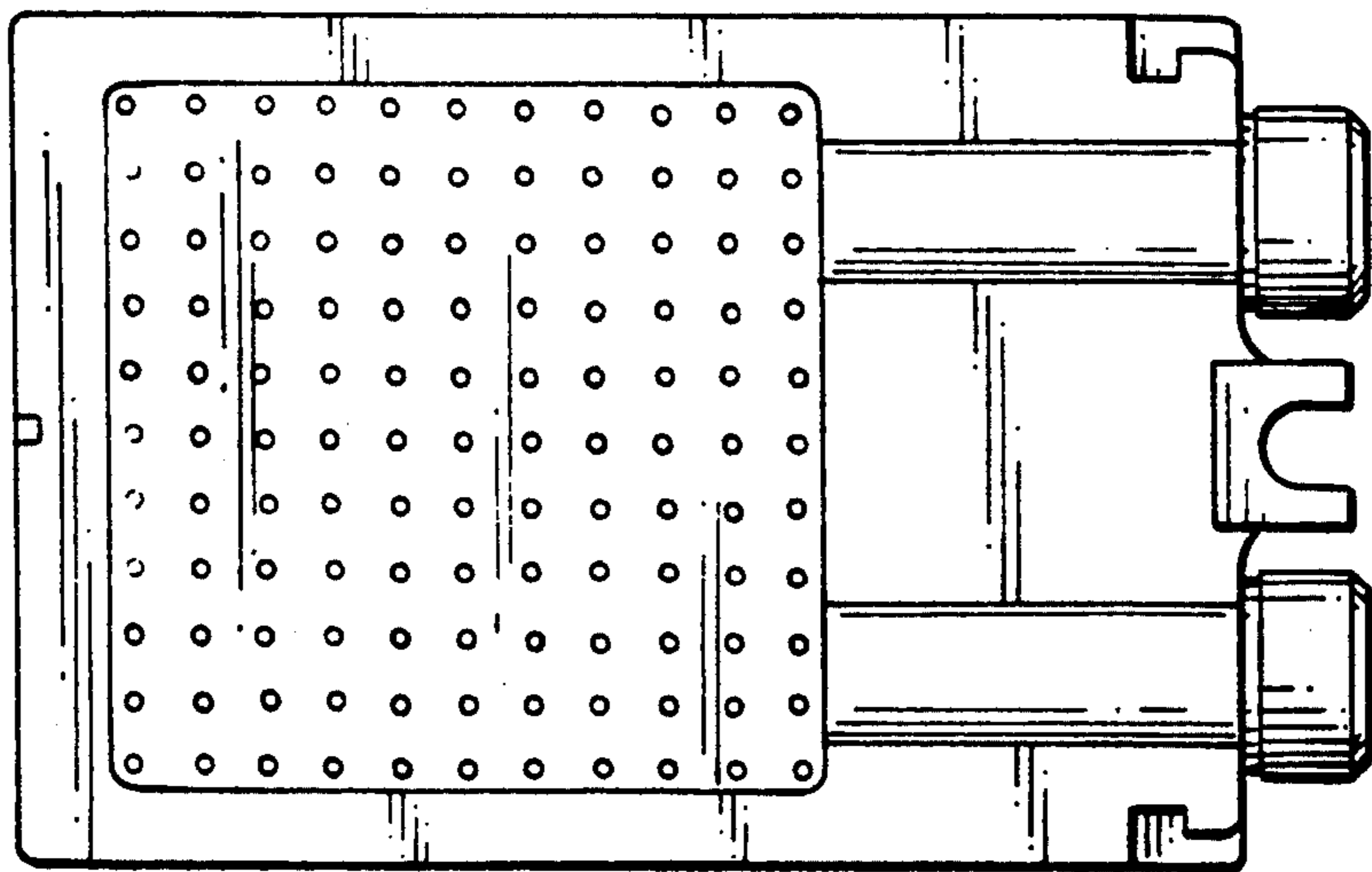


FIG. 6