



US00D323628S

United States Patent [19]

[11] Patent Number: **Des. 323,628**

Takao

[45] Date of Patent: **** Feb. 4, 1992**

[54] **SEMICONDUCTOR WAFER MEASURING INSTRUMENT**

[75] Inventor: **Itaru Takao, Yamanashi, Japan**

[73] Assignee: **Tokyo Electron Limited, Tokyo, Japan**

[**] Term: **14 Years**

[21] Appl. No.: **343,124**

[22] Filed: **Apr. 25, 1989**

[52] U.S. Cl. **D10/46**

[58] Field of Search **D10/46, 75, 81; 269/13, 269/14, 20, 21, 296, 903; 324/158 P; 414/222, 225, 589, 590, 627, 673, 752**

4,719,705	1/1988	Laganza et al.	269/21 X
4,723,766	2/1988	Beeding	269/21
4,907,931	3/1990	Mallory et al.	414/752 X
4,938,654	7/1990	Schram	414/752 X
4,941,800	7/1990	Koike et al.	414/752
4,955,590	9/1990	Narushima et al.	269/21

FOREIGN PATENT DOCUMENTS

733184 1/1988 Japan .

Primary Examiner—Bruce W. Dunkins
Assistant Examiner—Antoine D. Davis
Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt

[57] CLAIM

The ornamental design for a semiconductor wafer measuring instrument, as shown and described.

DESCRIPTION

FIG. 1 is a top, front and right side perspective view of a semiconductor wafer measuring instrument showing my new design;
FIG. 2 is a front elevational view;
FIG. 3 is a right side elevational view, the left side elevational view being a mirror image;
FIG. 4 is a top plan view;
FIG. 5 is a rear elevational view; and
FIG. 6 is a bottom plan view thereof.

[56] References Cited

U.S. PATENT DOCUMENTS

D. 188,789	9/1960	Hannon	D10/75
D. 223,174	3/1972	Pettavel	D10/46
D. 262,950	2/1982	Orr, II	D10/46
D. 277,979	3/1985	Brown et al.	D10/81 X
D. 307,397	4/1990	Lehtikoski	D10/46
D. 314,347	2/1991	Garnish et al.	D10/46
4,530,635	7/1985	Engelbrecht et al.	269/21 X
4,684,113	8/1987	Douglas et al.	269/21
4,700,488	10/1987	Curti	269/21 X

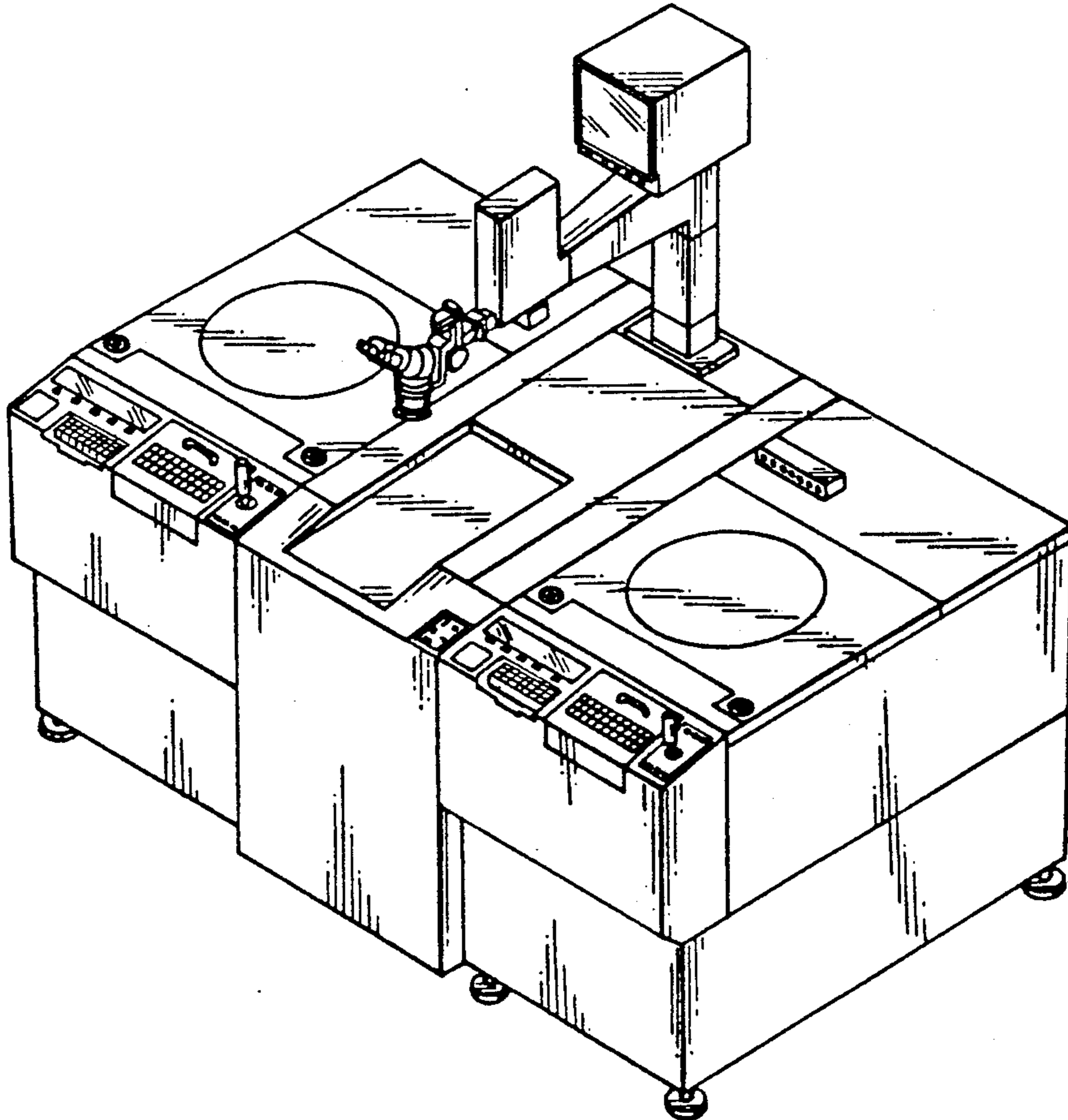


FIG. 1

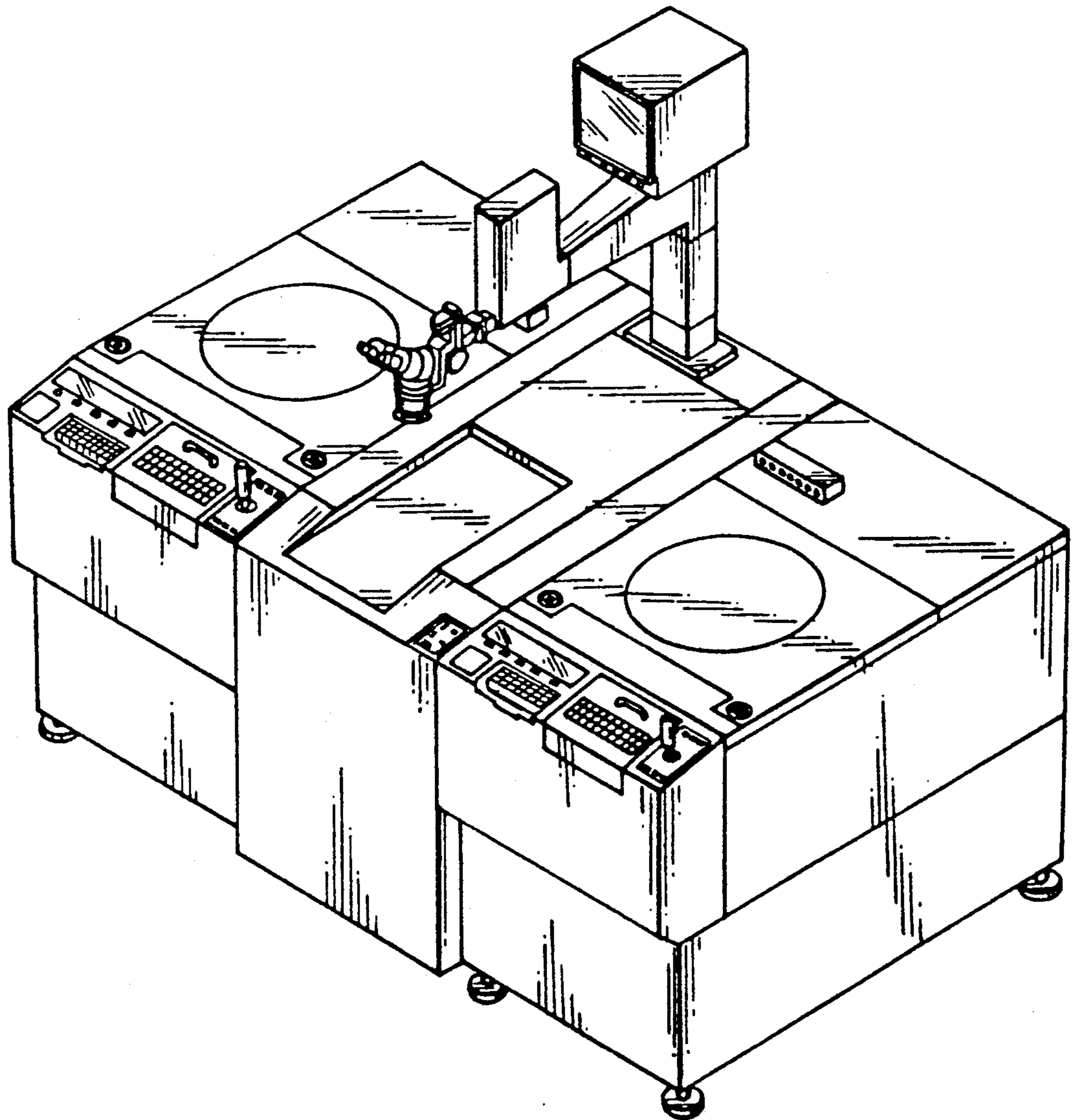


FIG. 2

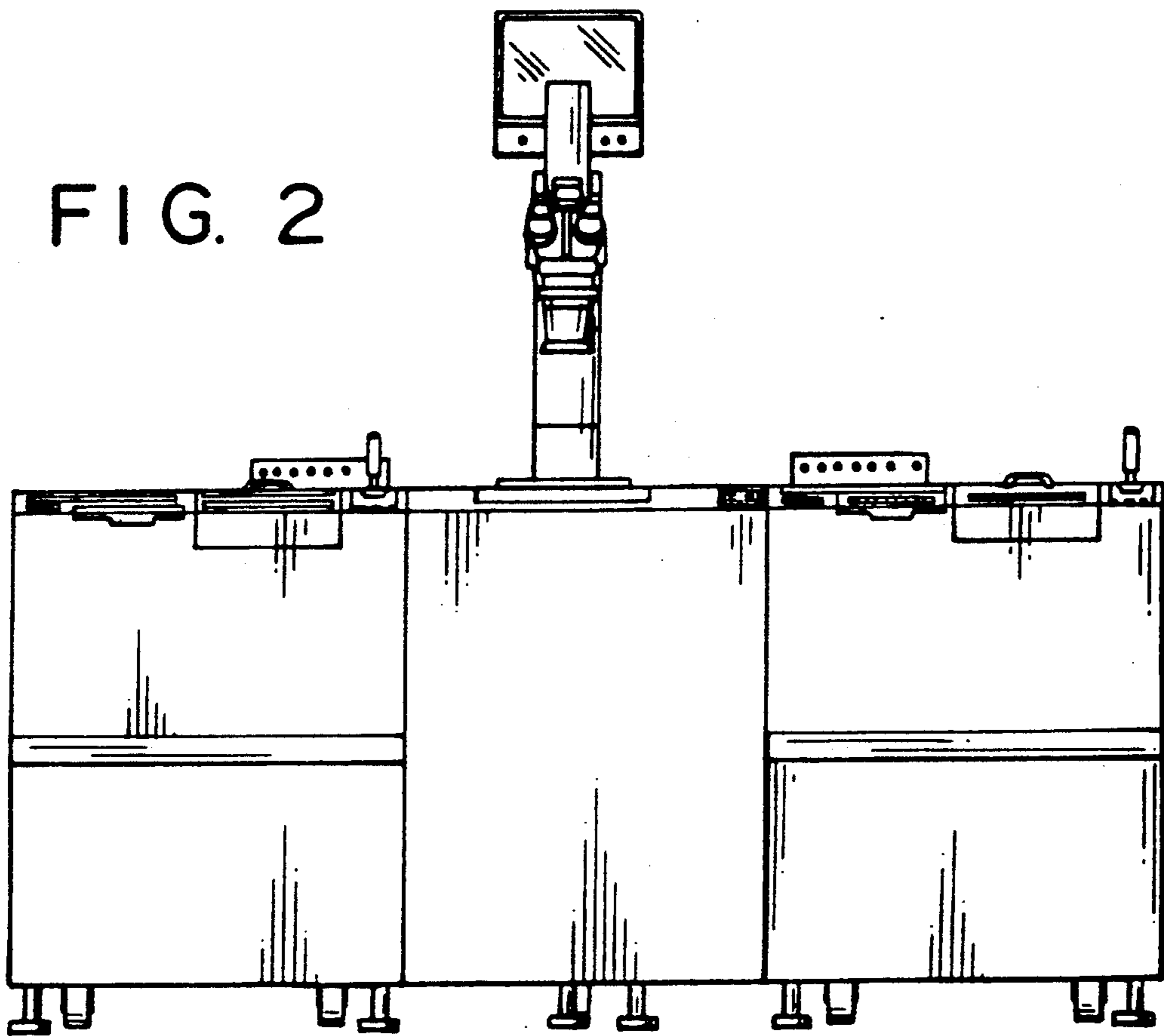


FIG. 3

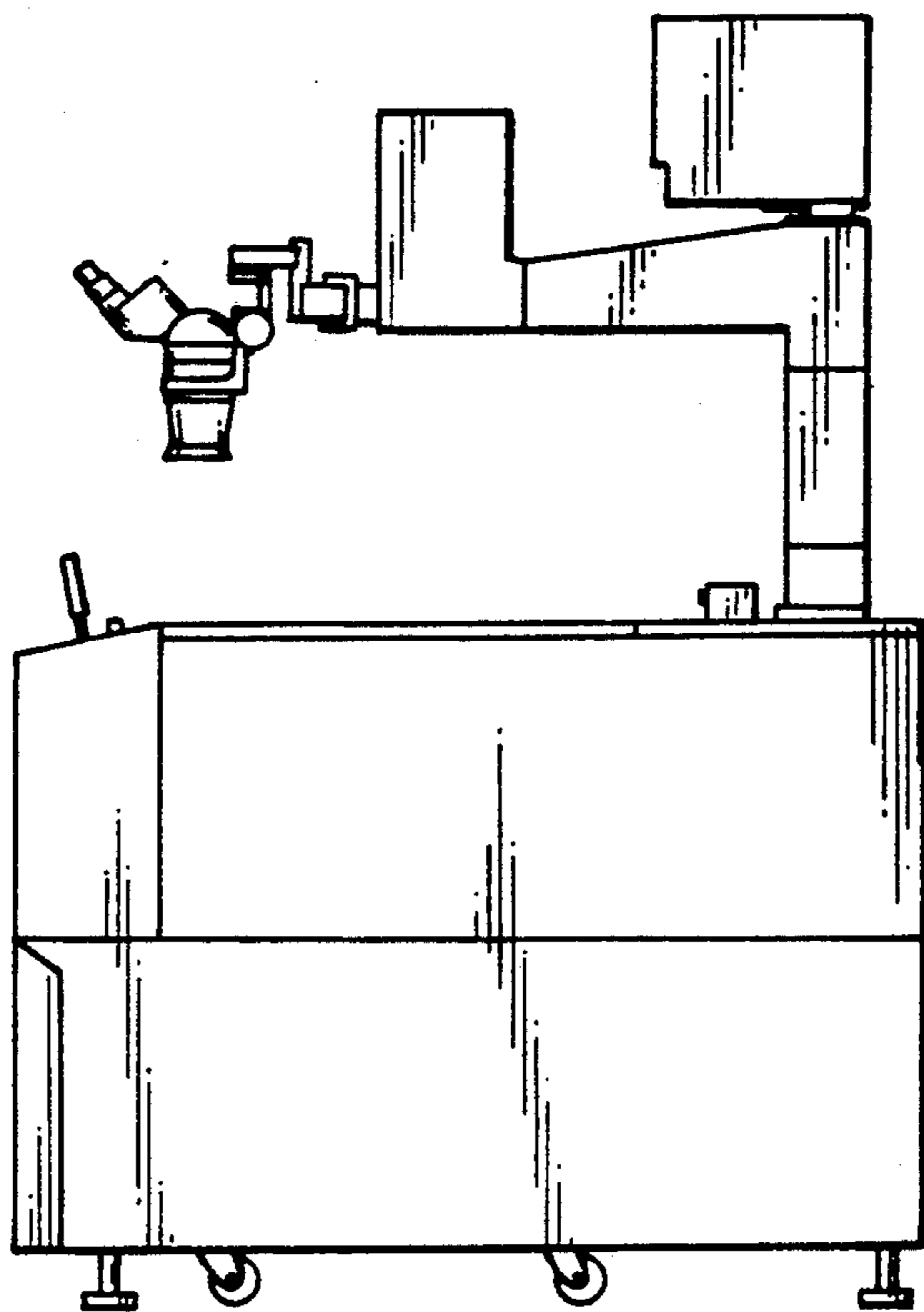


FIG. 4

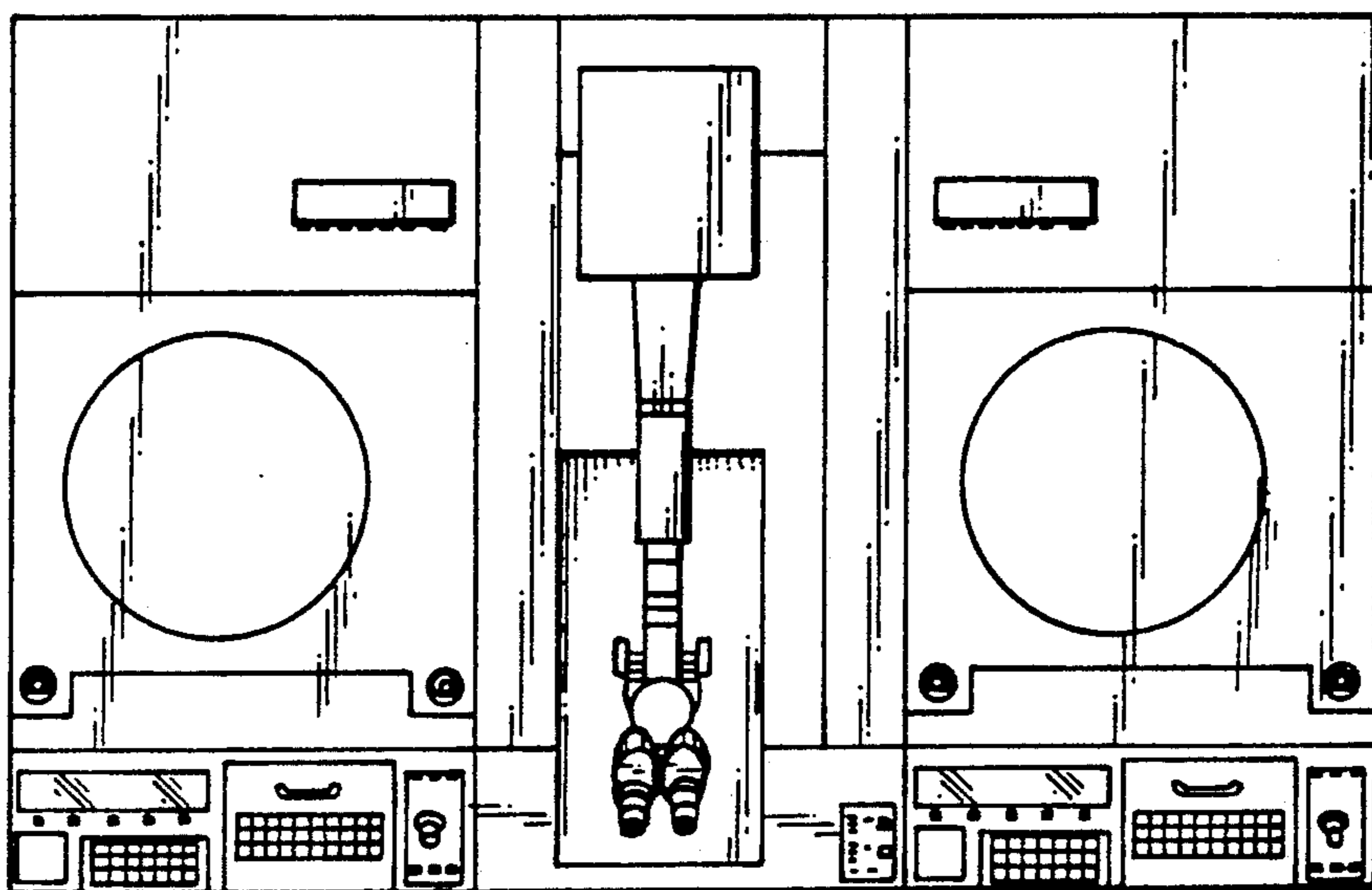


FIG. 5

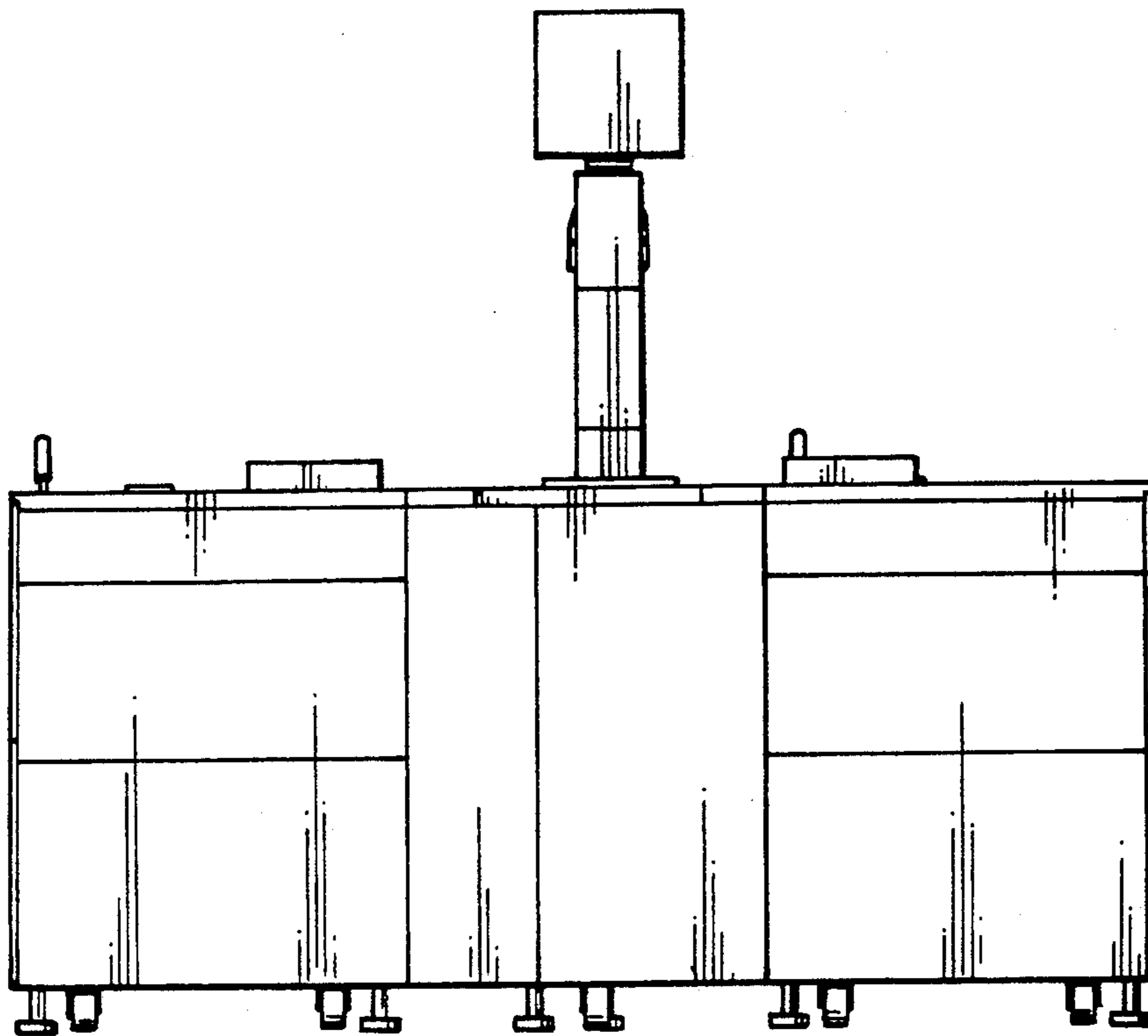


FIG. 6

