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# United States Patent [19]

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**Takao**

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[54] **SEMICONDUCTOR WAFER MEASURING INSTRUMENT**

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[73] Assignee: **Tokyo Electron Limited, Tokyo, Japan**

[\*\*] Term: **14 Years**

[21] Appl. No.: **343,124**

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[52] U.S. Cl. .... **D10/46**

[58] Field of Search ..... **D10/46, 75, 81; 269/13, 269/14, 20, 21, 296, 903; 324/158 P; 414/222, 225, 589, 590, 627, 673, 752**

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*Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt

### [57] CLAIM

The ornamental design for a semiconductor wafer measuring instrument, as shown and described.

### DESCRIPTION

FIG. 1 is a top, front and right side perspective view of a semiconductor wafer measuring instrument showing my new design;  
FIG. 2 is a front elevational view;  
FIG. 3 is a right side elevational view, the left side elevational view being a mirror image;  
FIG. 4 is a top plan view;  
FIG. 5 is a rear elevational view; and  
FIG. 6 is a bottom plan view thereof.

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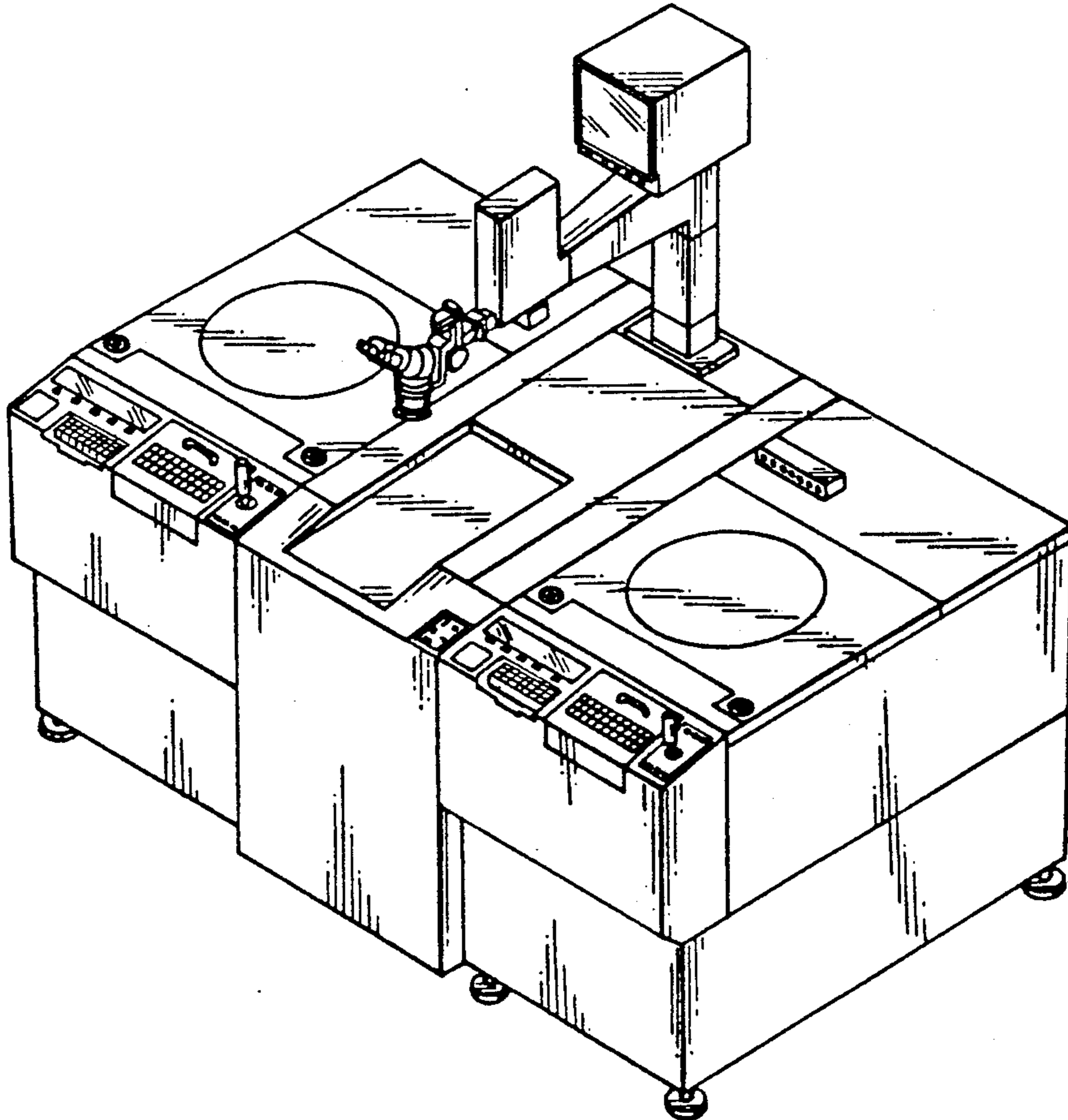


FIG. 1

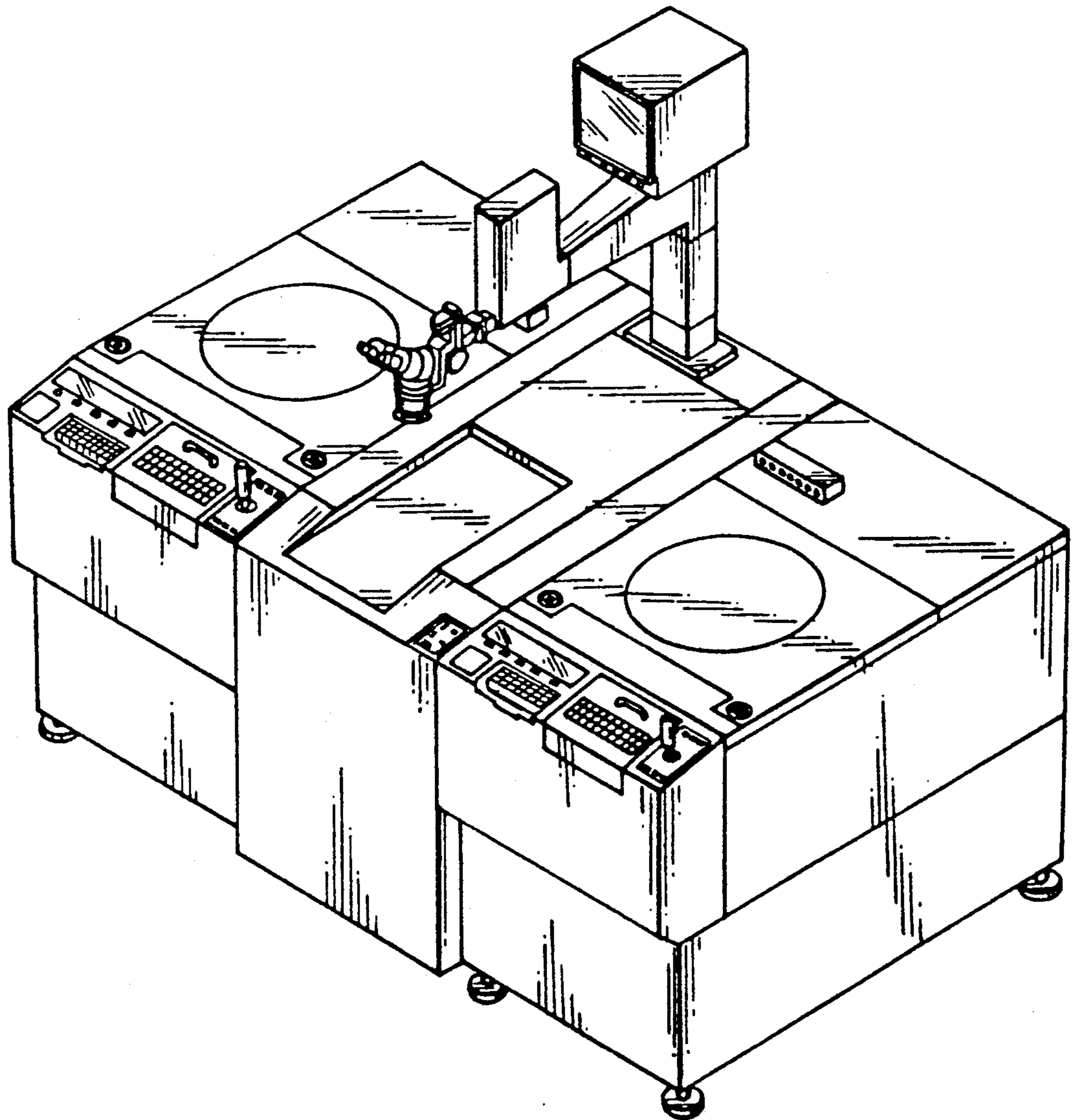


FIG. 2

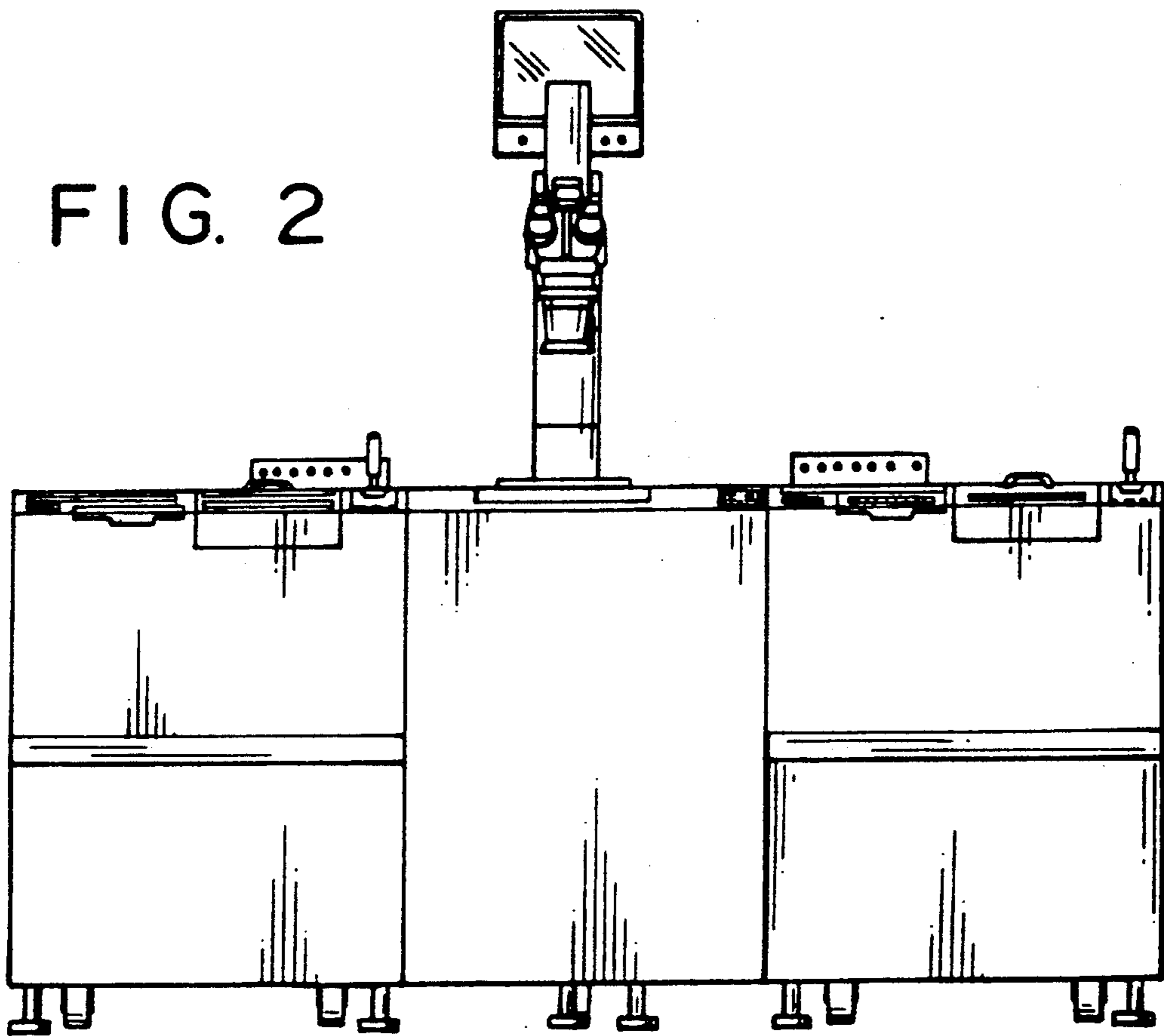


FIG. 3

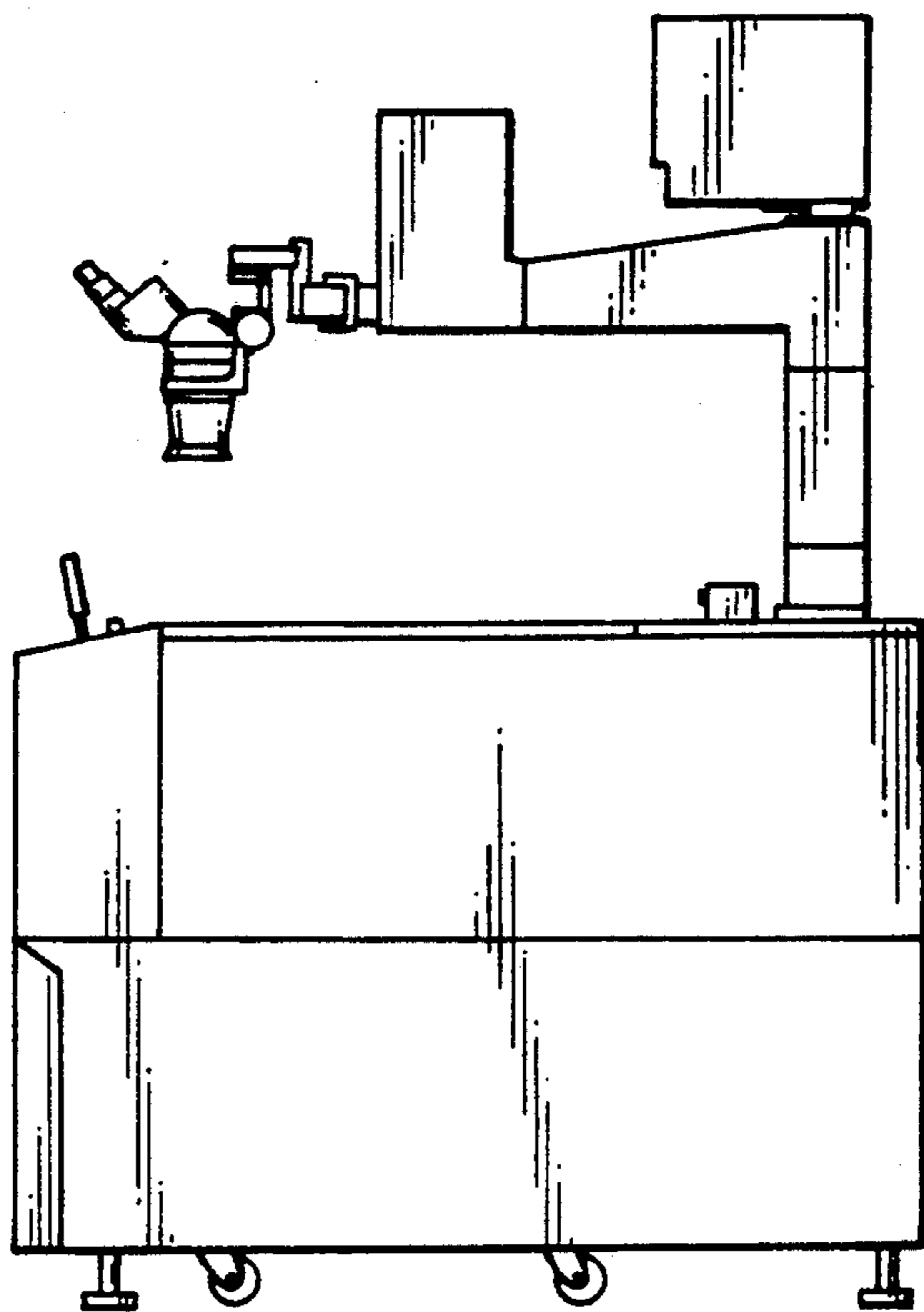


FIG. 4

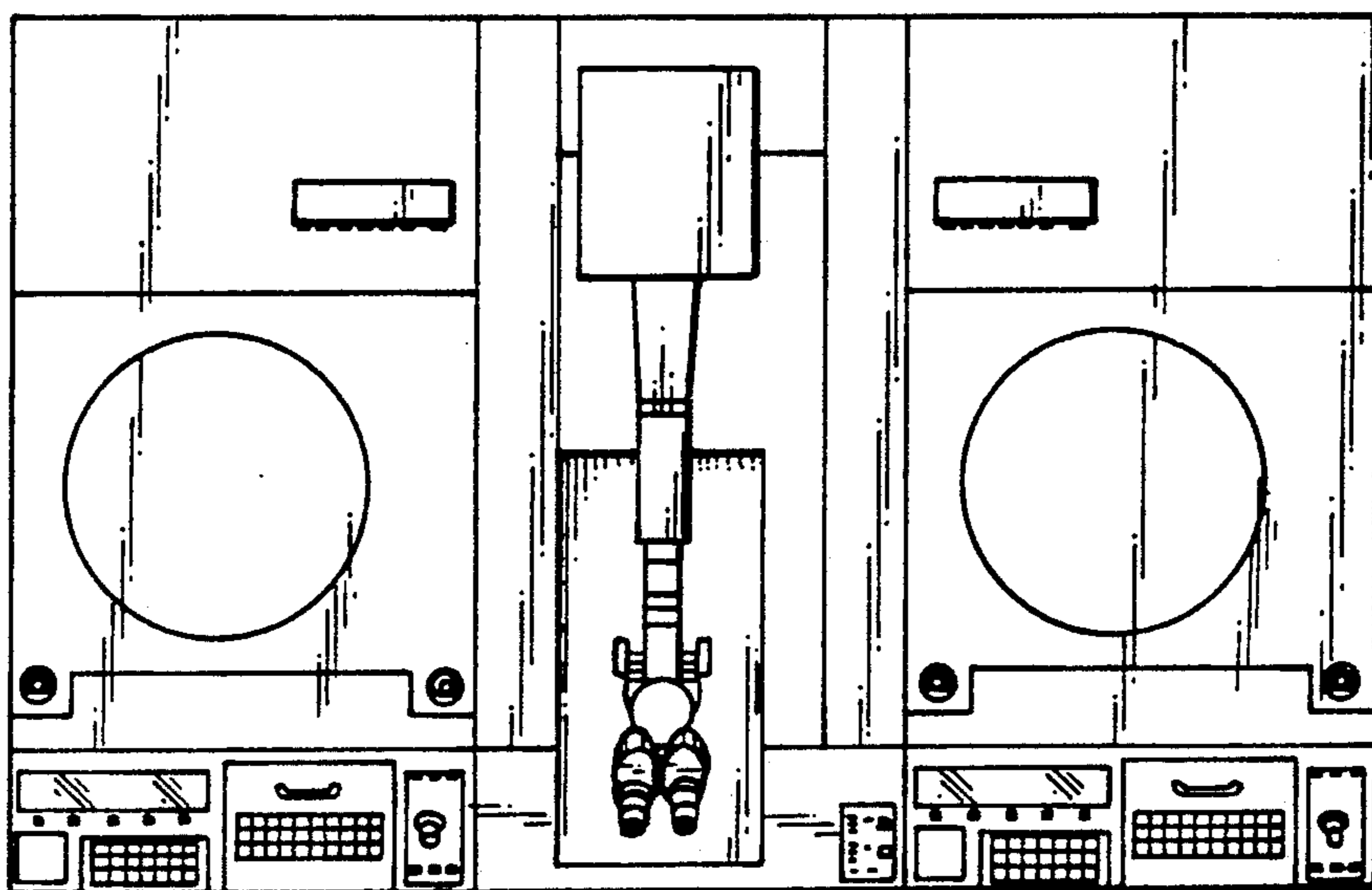


FIG. 5

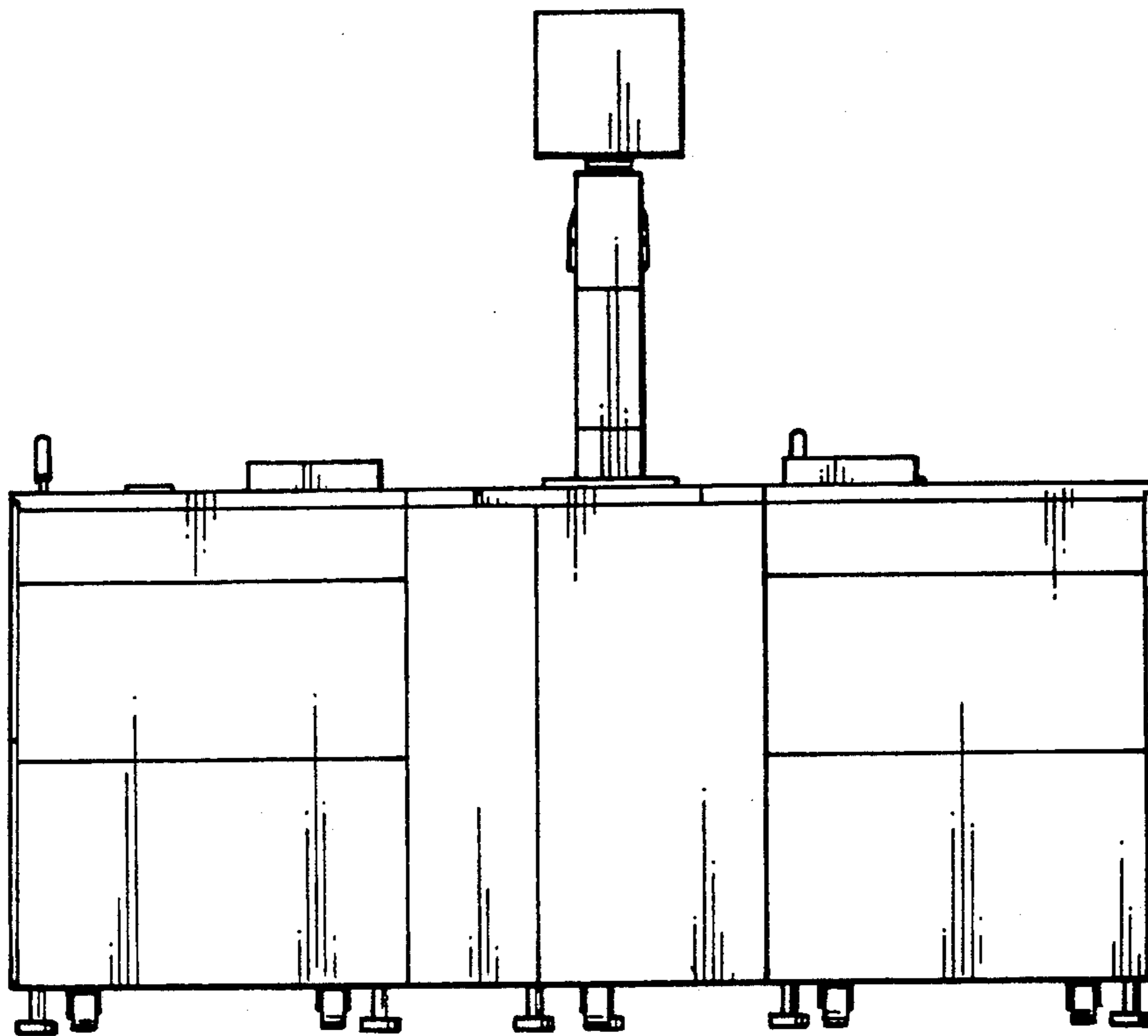


FIG. 6

