United States Patent [19]
Dahlberg et al.

[11] **Patent Number: Des. 320,755**
[45] **Date of Patent: ** Oct. 15, 1991**

[54] **INTERGRATED CIRCUIT TESTER**

[75] Inventors: **Bjorn M. Dahlberg; Charles H. Schwar,** both of Irvine; **Mauro V. Tegethoff,** Mission Viejo, all of Calif.

[73] Assignee: **Hilevel Technology,** Irvine, Calif.

[**] Term: **14 Years**

[21] Appl. No.: **296,185**

[22] Filed: **Jan. 11, 1989**
[52] **U.S. Cl.** **D10/75**
[58] **Field of Search** .... D10/46, 75; D14/102, D14/103, 104; 324/158 F, 158 P; 439/68, 78

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,504,783	3/1985	Zasio et al.	324/158 F X
4,528,504	7/1985	Thornton, Jr. et al.	324/158 F
4,782,289	11/1988	Schwar et al. .	
4,782,291	11/1988	Blandin	324/158 F
4,970,461	11/1990	Lepage	324/158 F

OTHER PUBLICATIONS

HILEVEL Technology, Inc. news release dated Jun. 12, 1988.
"VSLI Systems Design" publication dated Jun. 1988.
HILEVEL Technology, Inc. advertising brochure for TOPAZ-V.

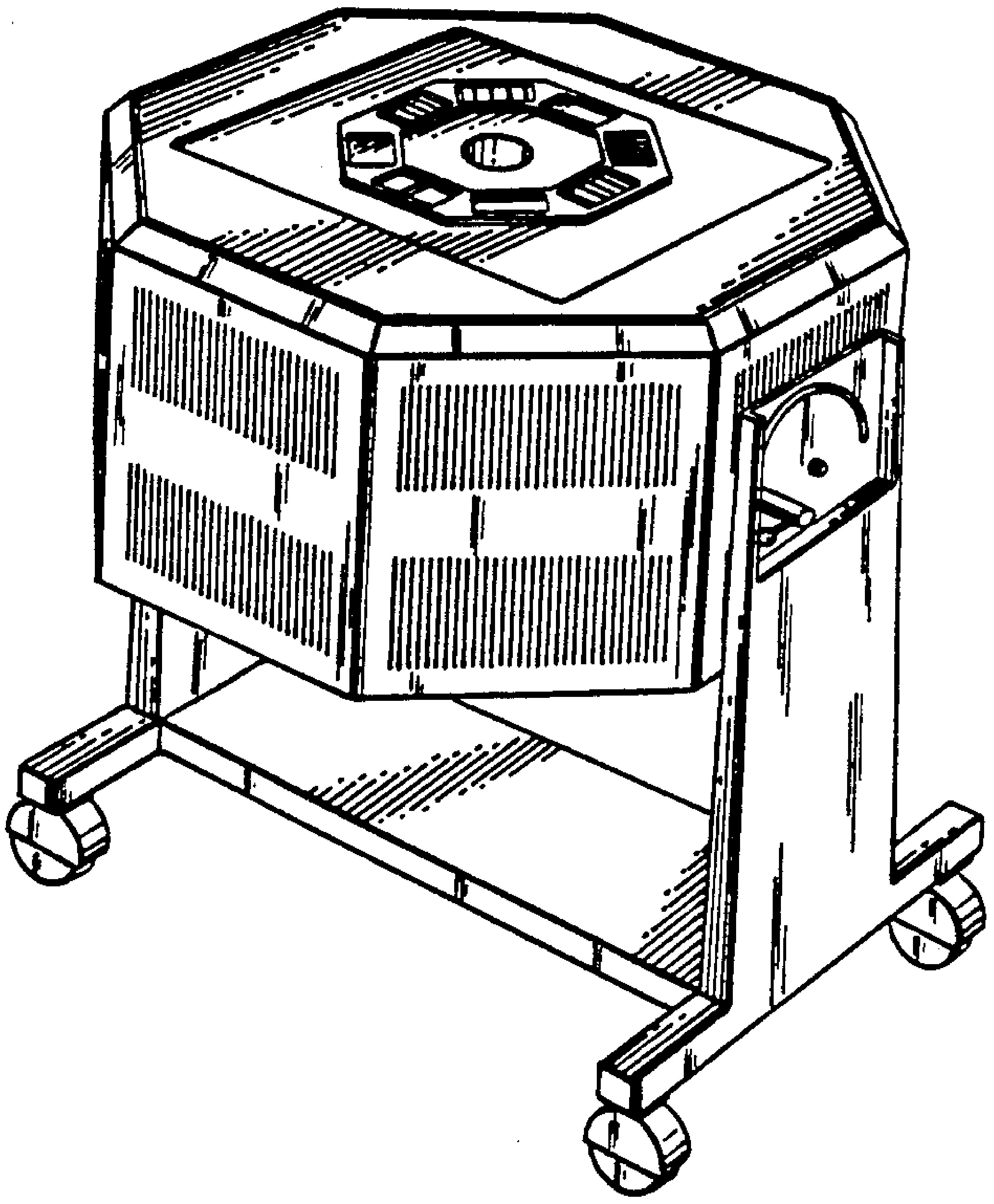
Primary Examiner—Nelson C. Holtje
Assistant Examiner—Antoine D. Davis
Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear

[57] **CLAIM**

The ornamental design for a intergrated circuit tester, as shown and described.

DESCRIPTION

FIG. **1** is a top, front and right side perspective view of a intergrated circuit tester showing our new design;
FIG. **2** is a top, front and right side perspective view, with the circuitry enclosure rotated 180 degrees;
FIG. **3** is a top plan view;
FIG. **4** is a right side elevational view;
FIG. **5** is a front elevational view;
FIG. **6** is a rear elevational view;
FIG. **7** is a top, front and right side perspective view of a second embodiment of our new design of FIGS. **1-6;**
FIG. **8** is a top, front and right side perspective view, with the circuitry enclosure rotated 180 degrees;
FIG. **9** is a top plan view;
FIG. **10** is a right side elevational view, the left side elevational view being a mirror image;
FIG. **11** is a front elevational view;
FIG. **12** is a rear elevational view;
FIG. **13** is a top, front and right side perspective view of a third embodiment of our new design of FIGS. **1-6;**
FIG. **14** is a top, front and right side perspective view, with the circuitry enclosure rotated 180 degrees;
FIG. **15** is a top plan view;
FIG. **16** is a right side elevational view, the left side elevational view being a mirror image;
FIG. **17** is a front elevational view; and
FIG. **18** is a rear elevational view thereof.



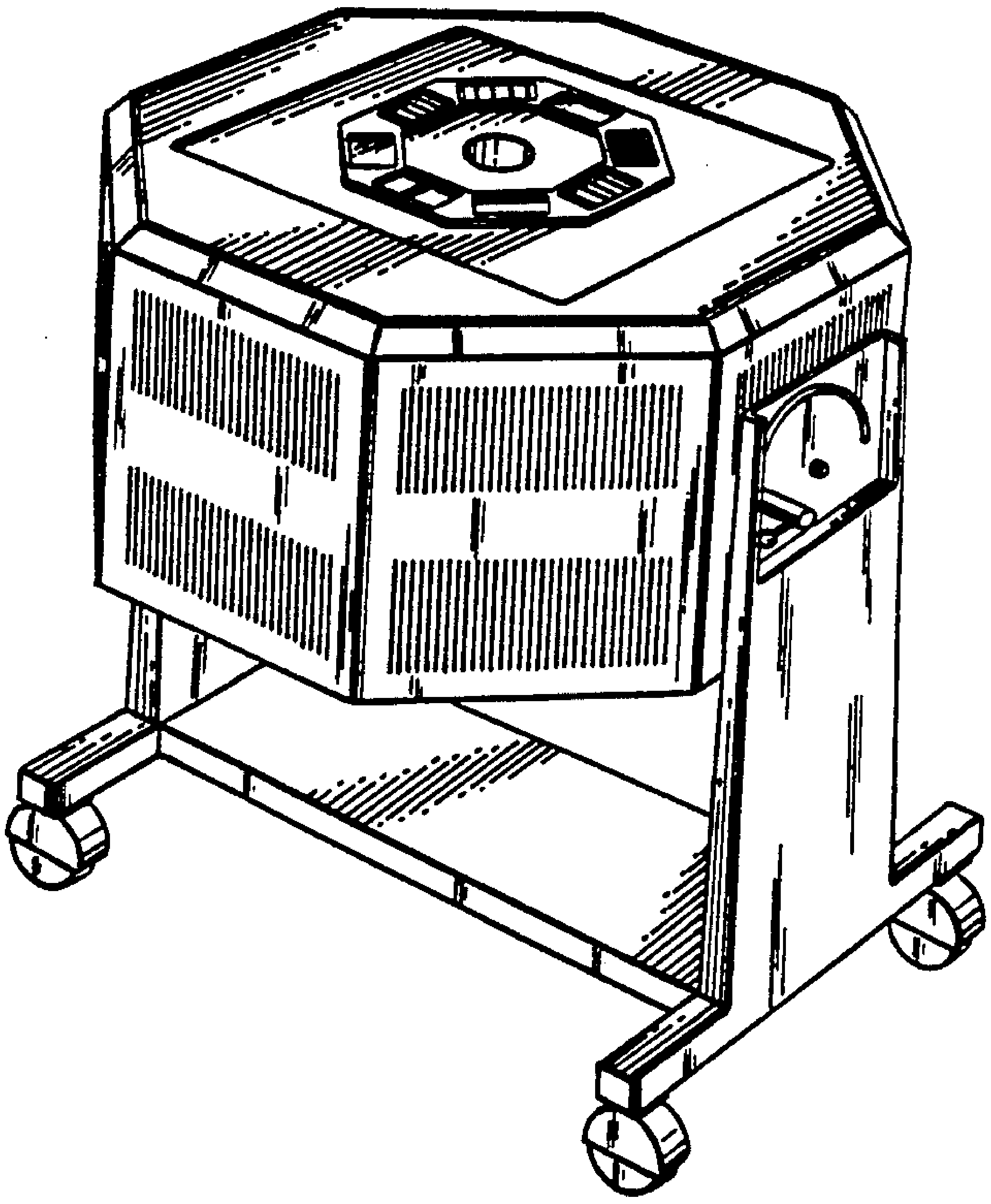


Fig. 1

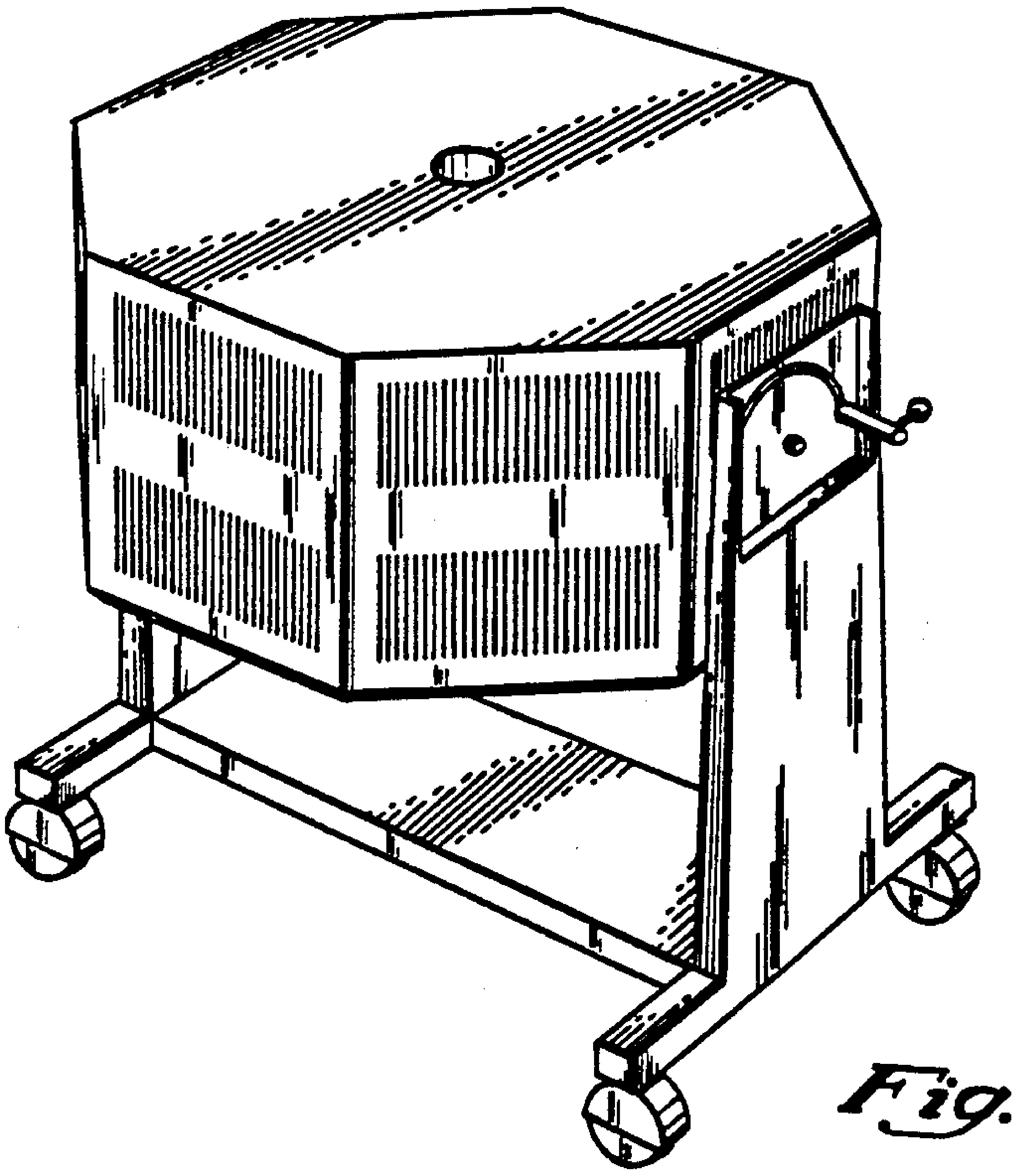
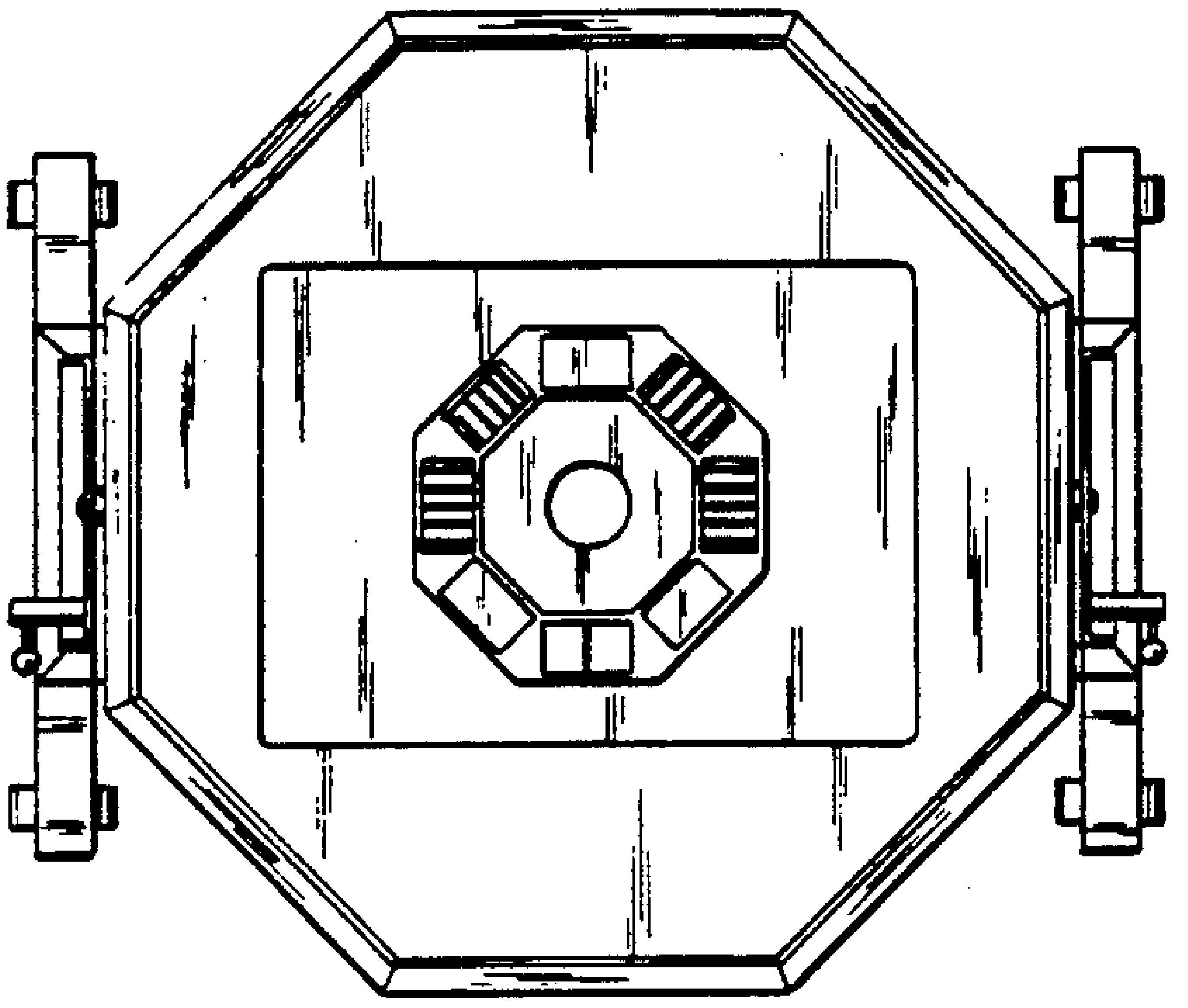


Fig. 2

Fig. 3



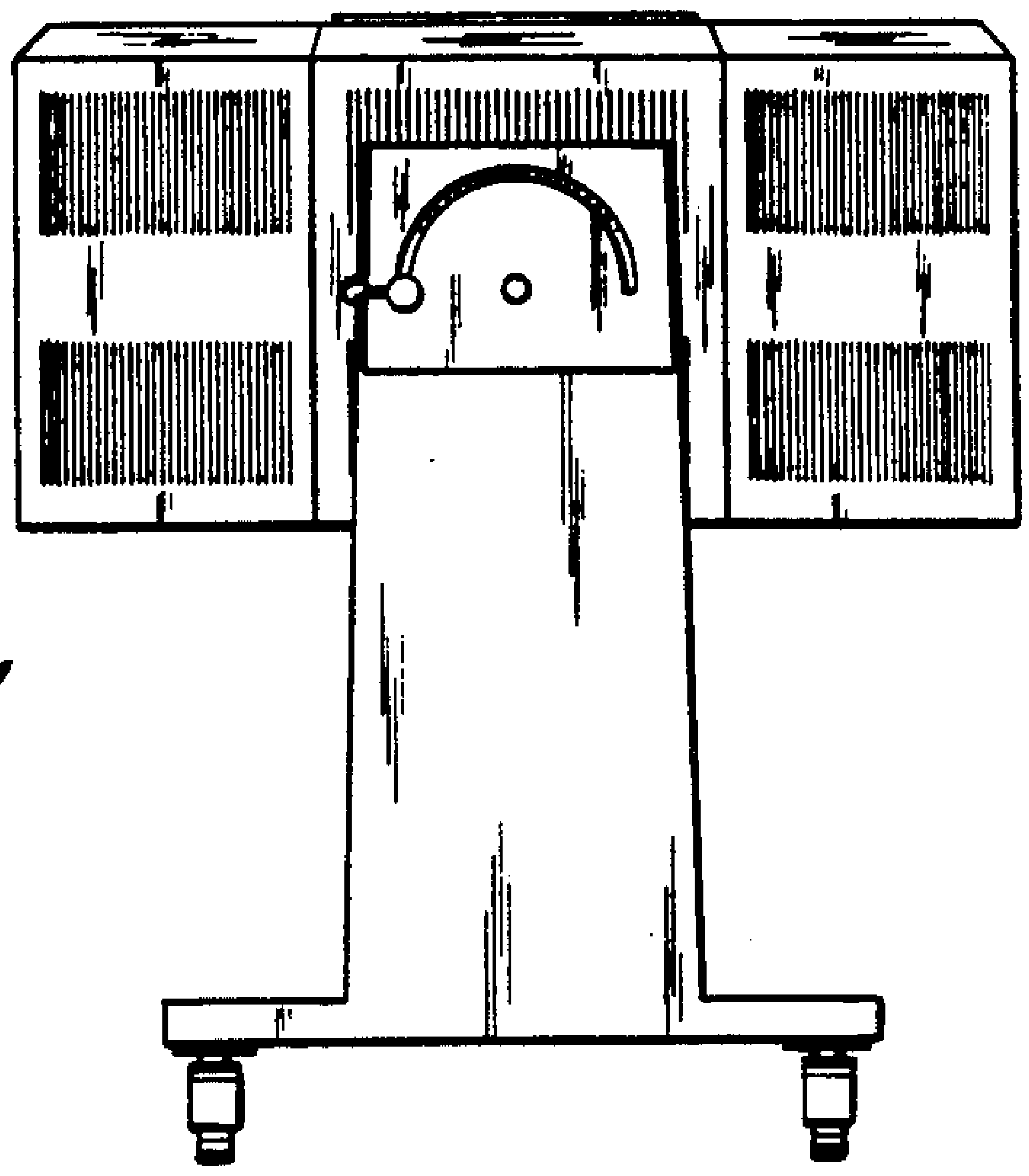


Fig. 4

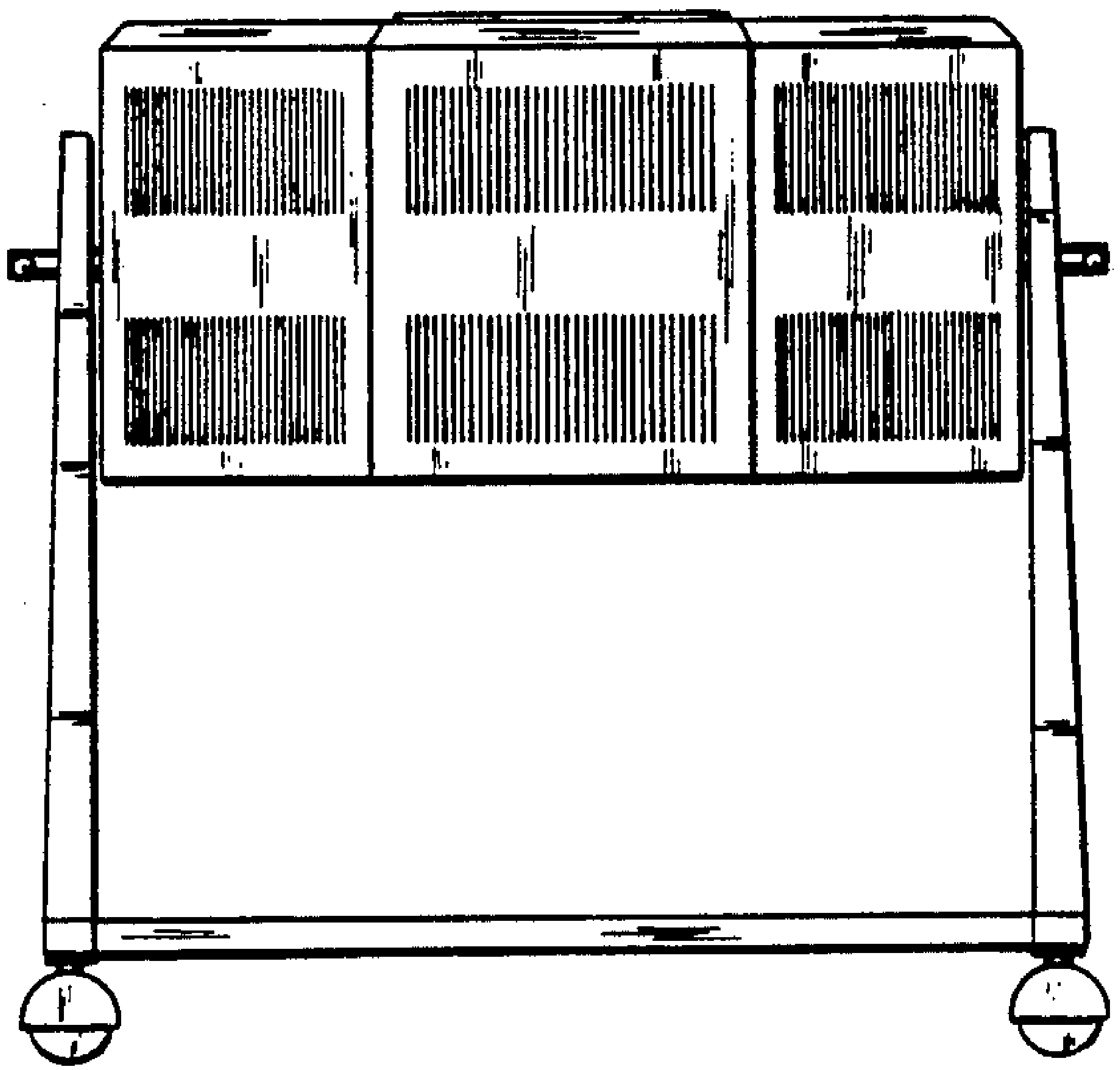


Fig. 5

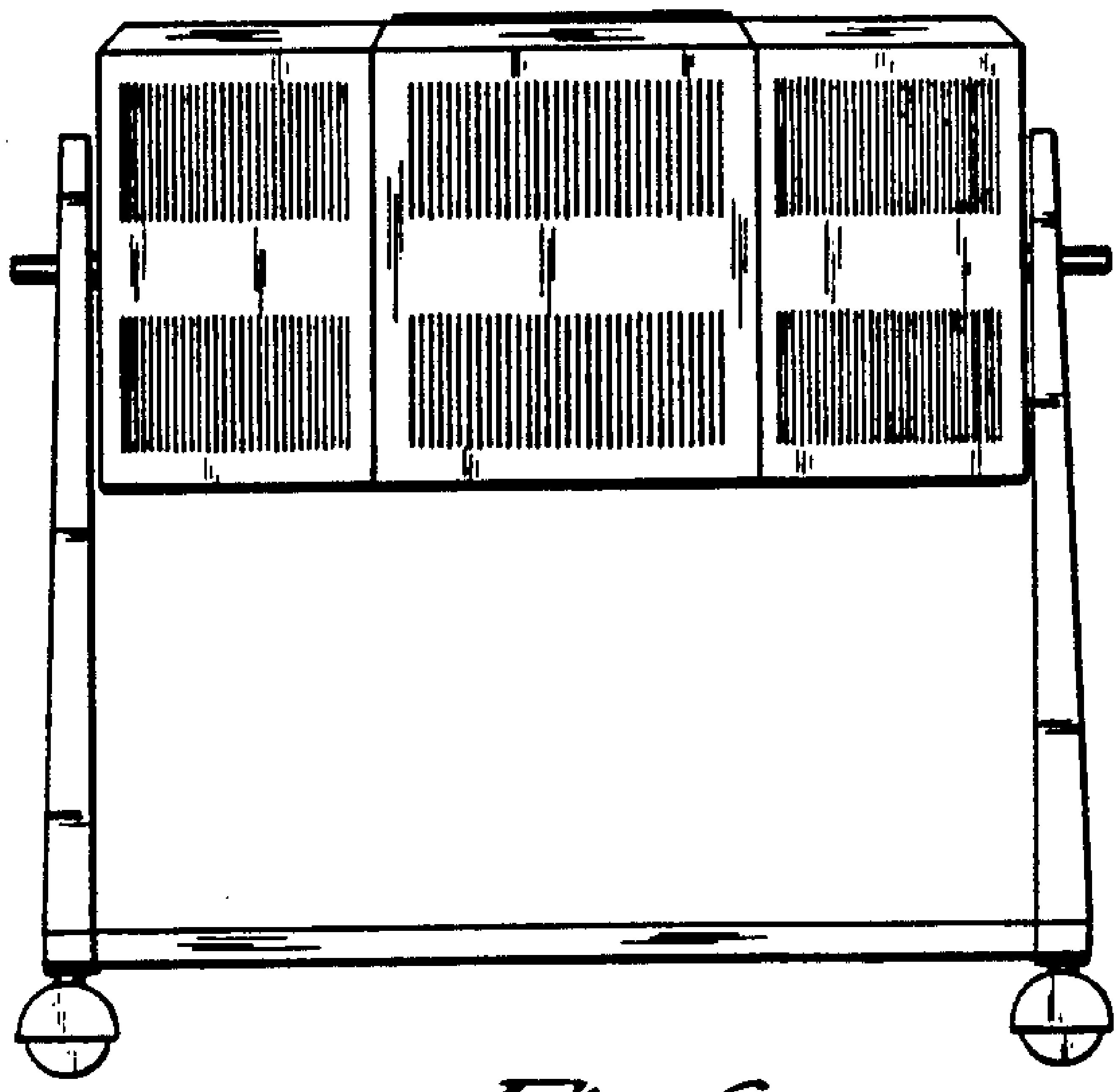
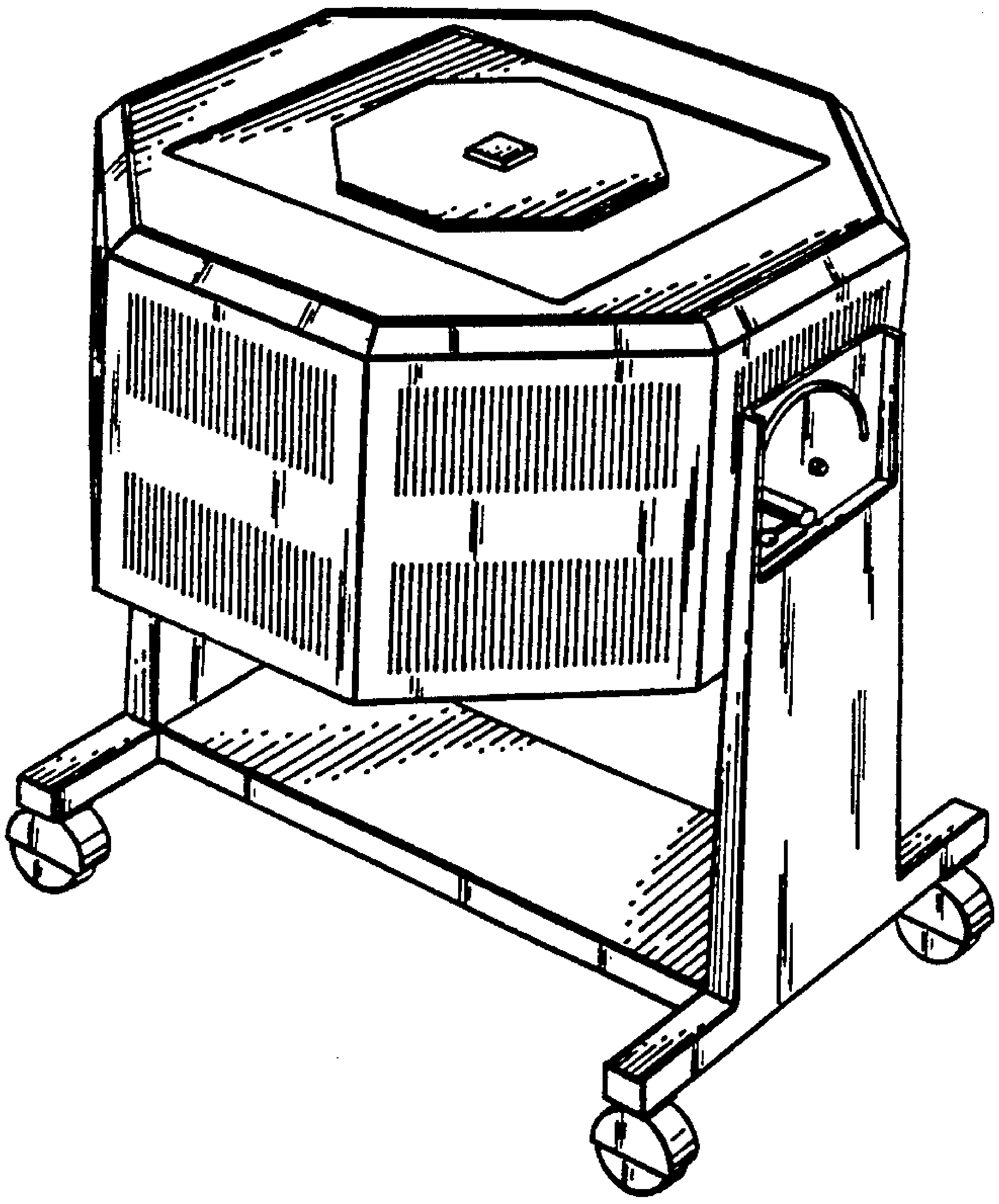


Fig. 6

Fig. 7



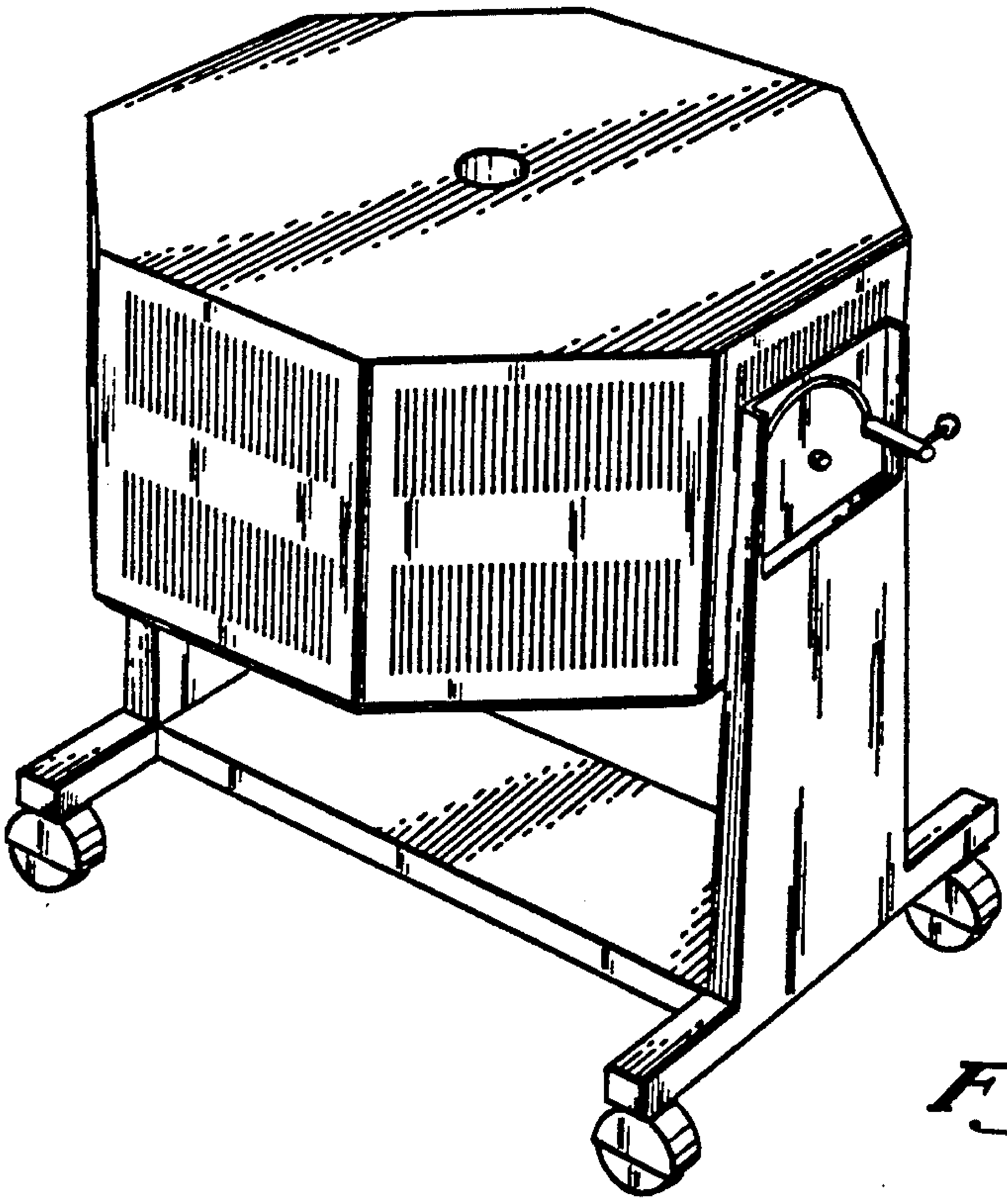
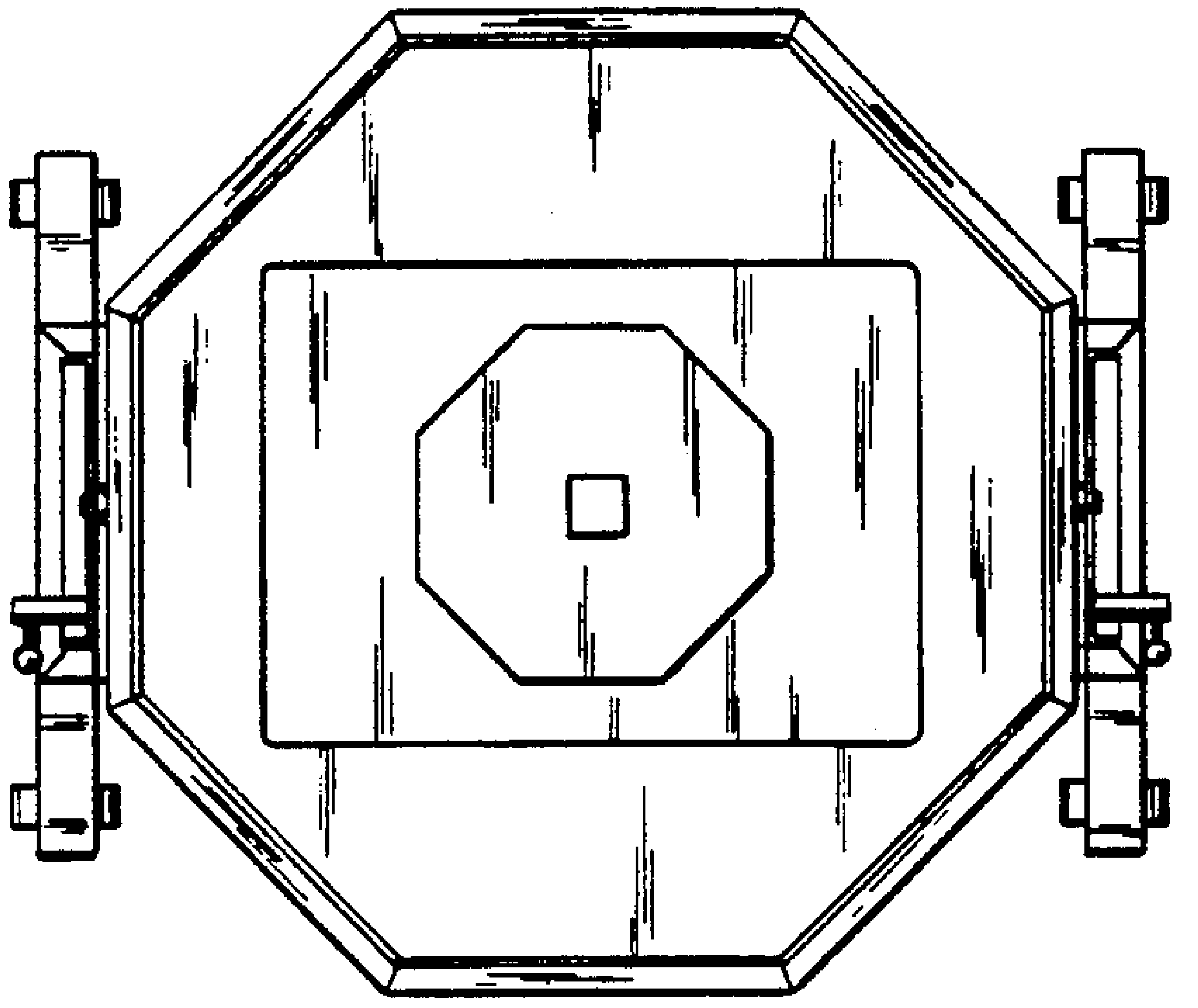


Fig. 8

Fig. 9



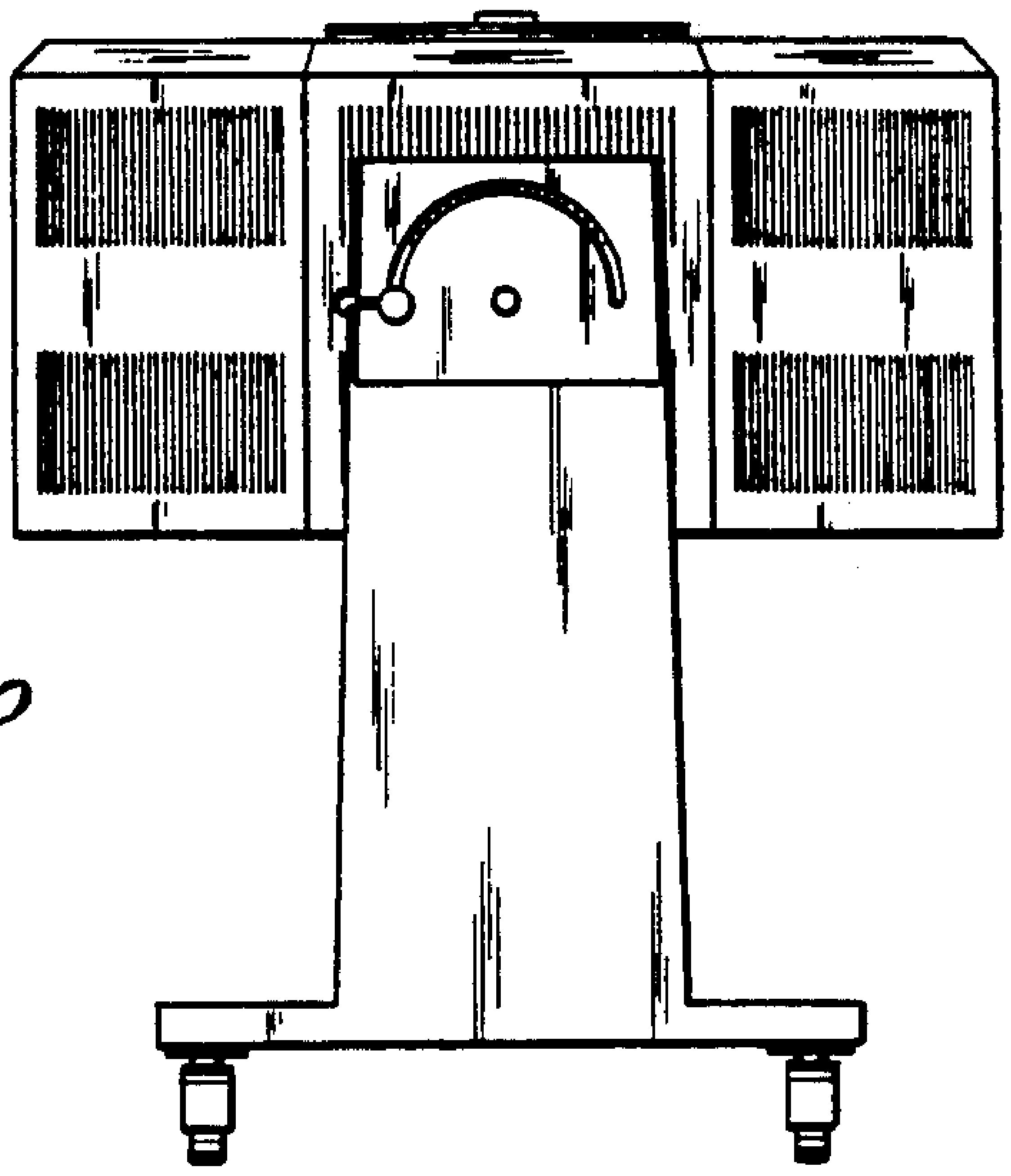


Fig. 10

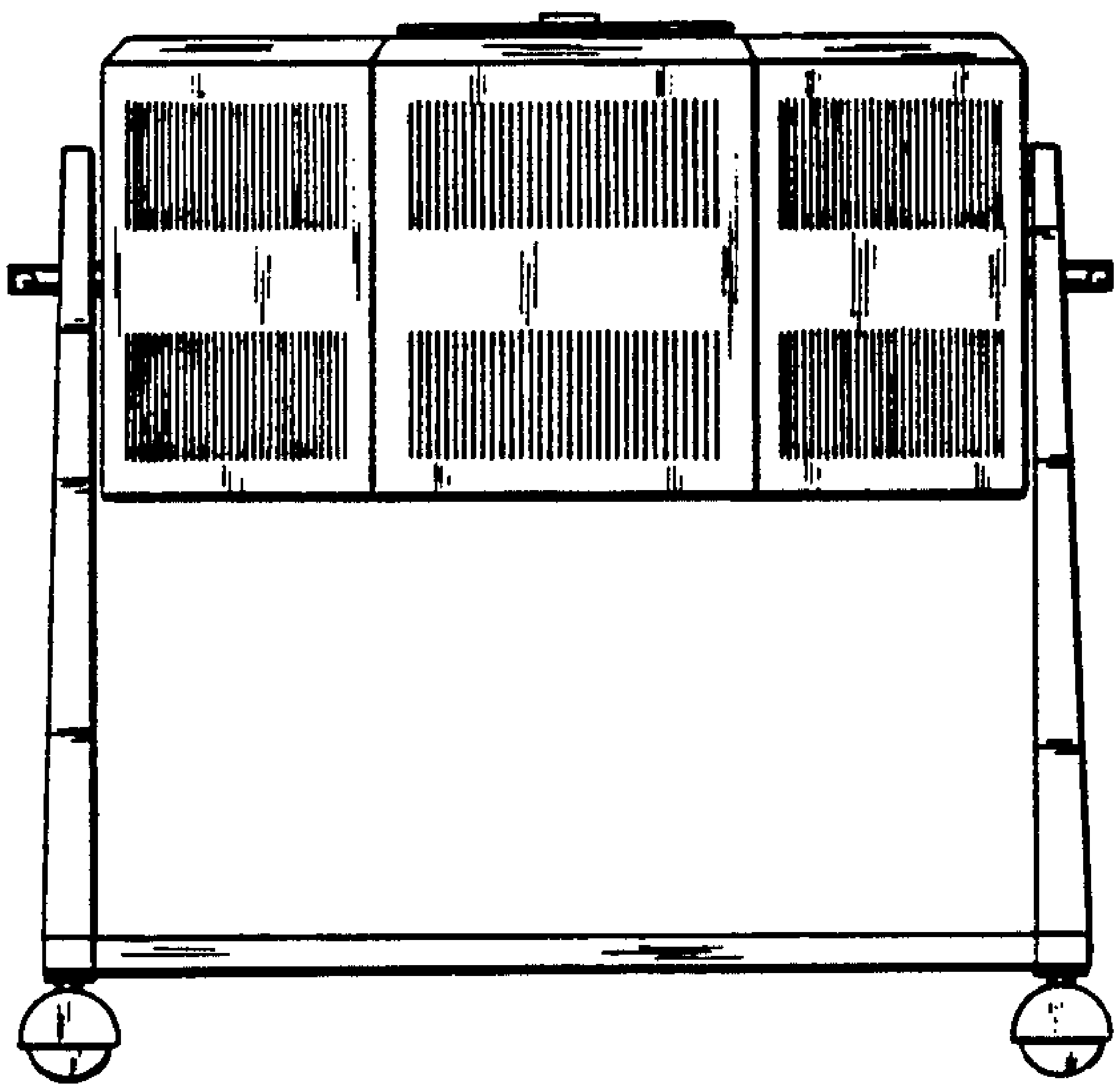


Fig. 11

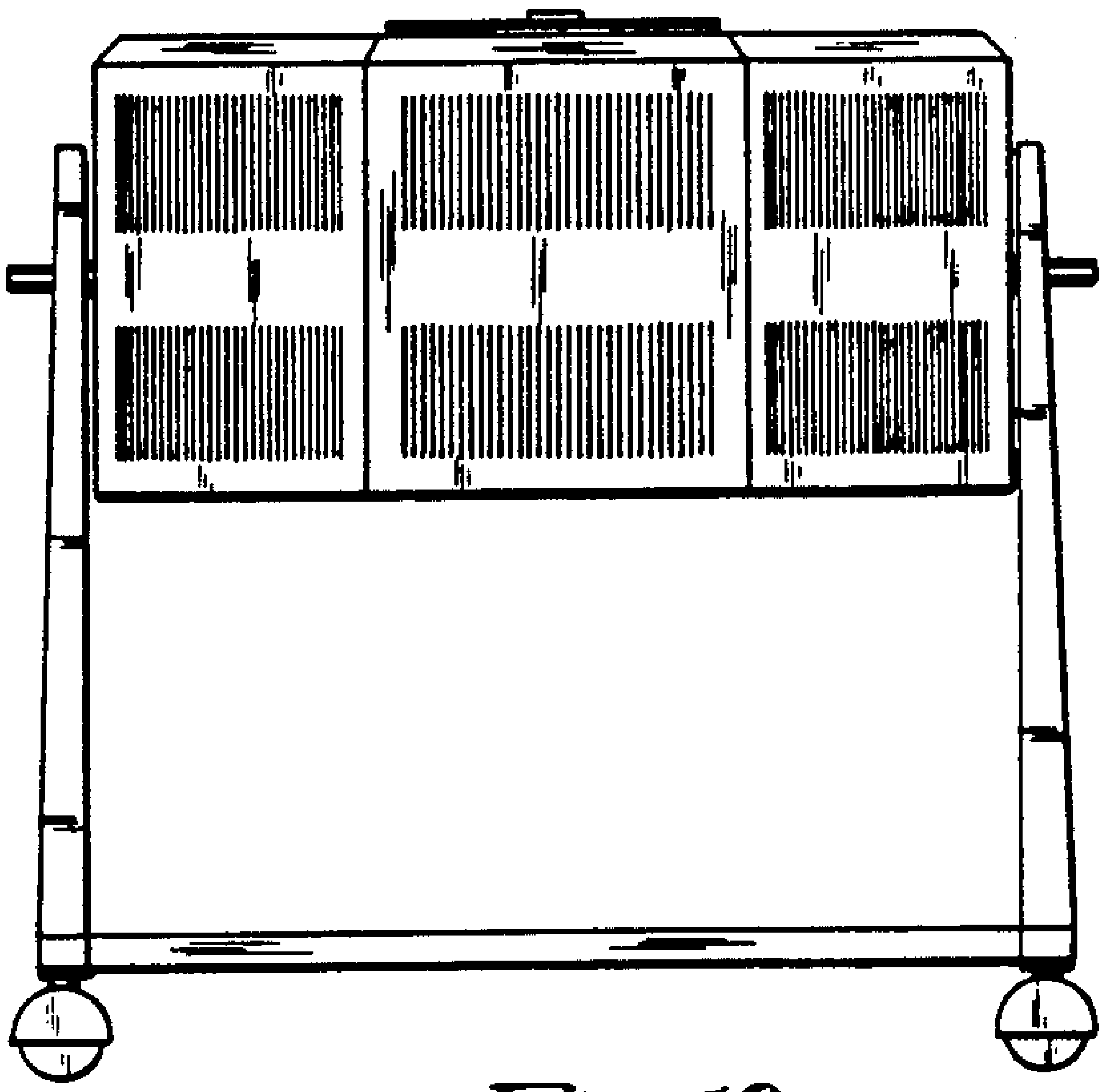
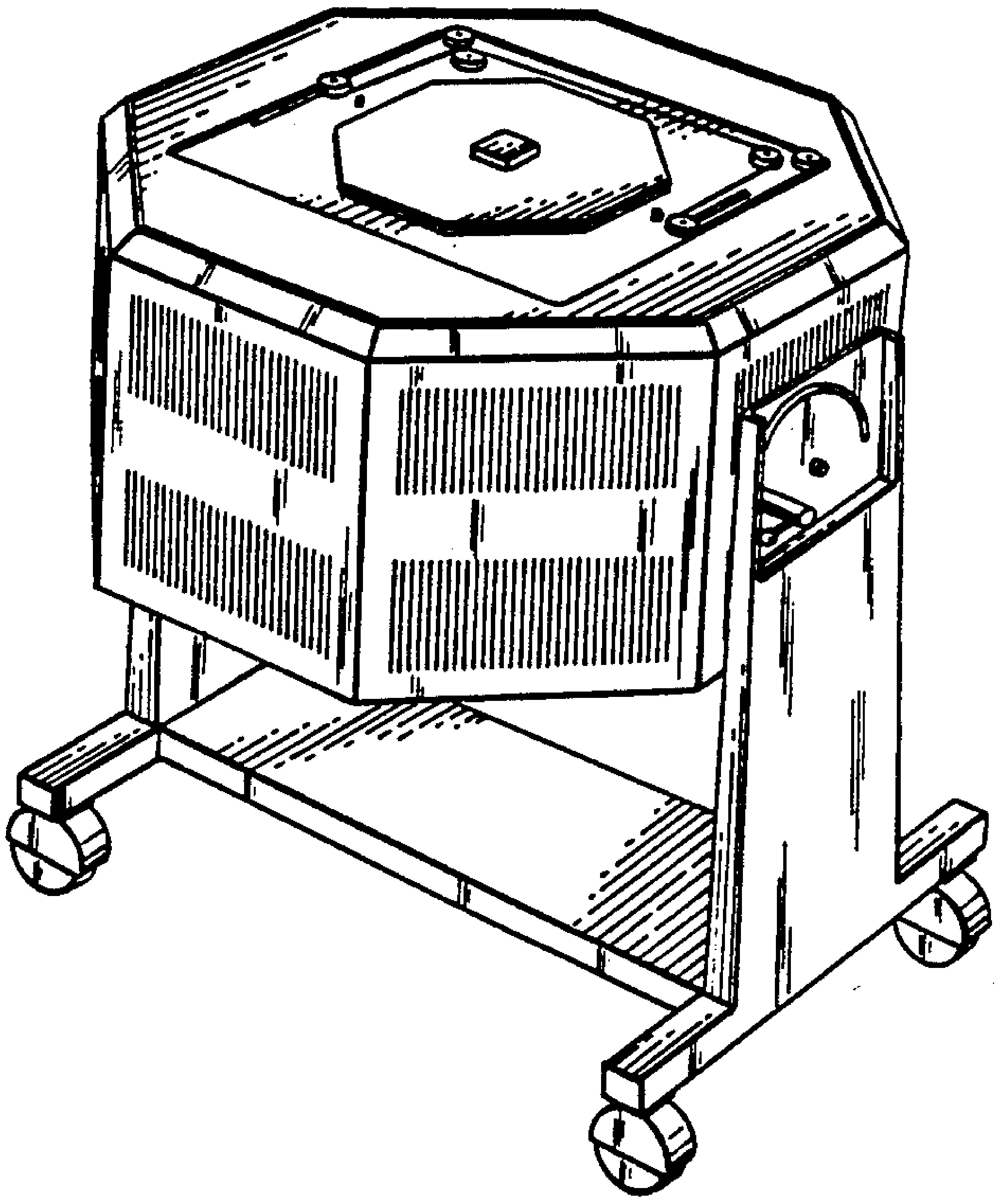


Fig. 12

Fig. 13



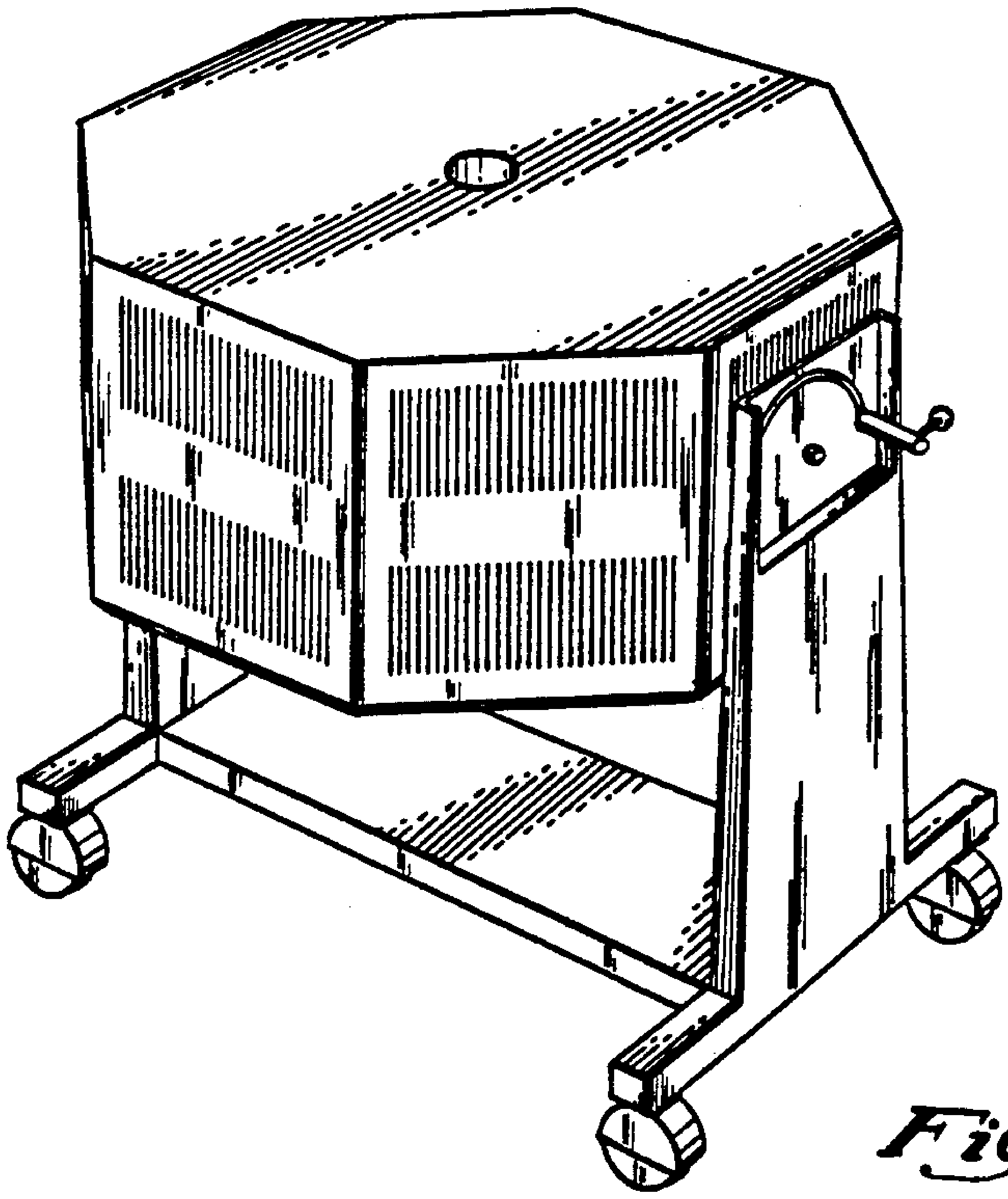


Fig. 14

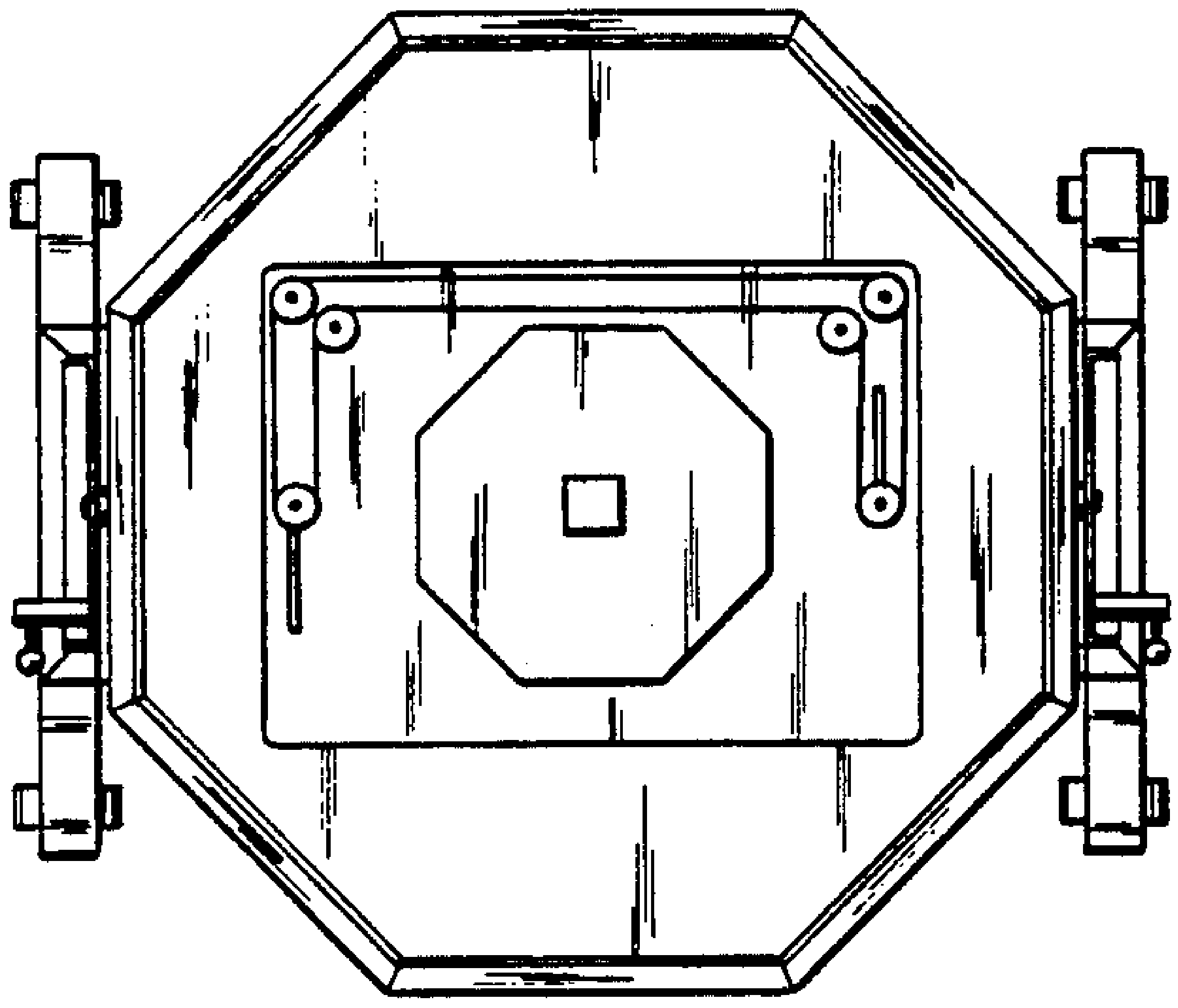


Fig. 15

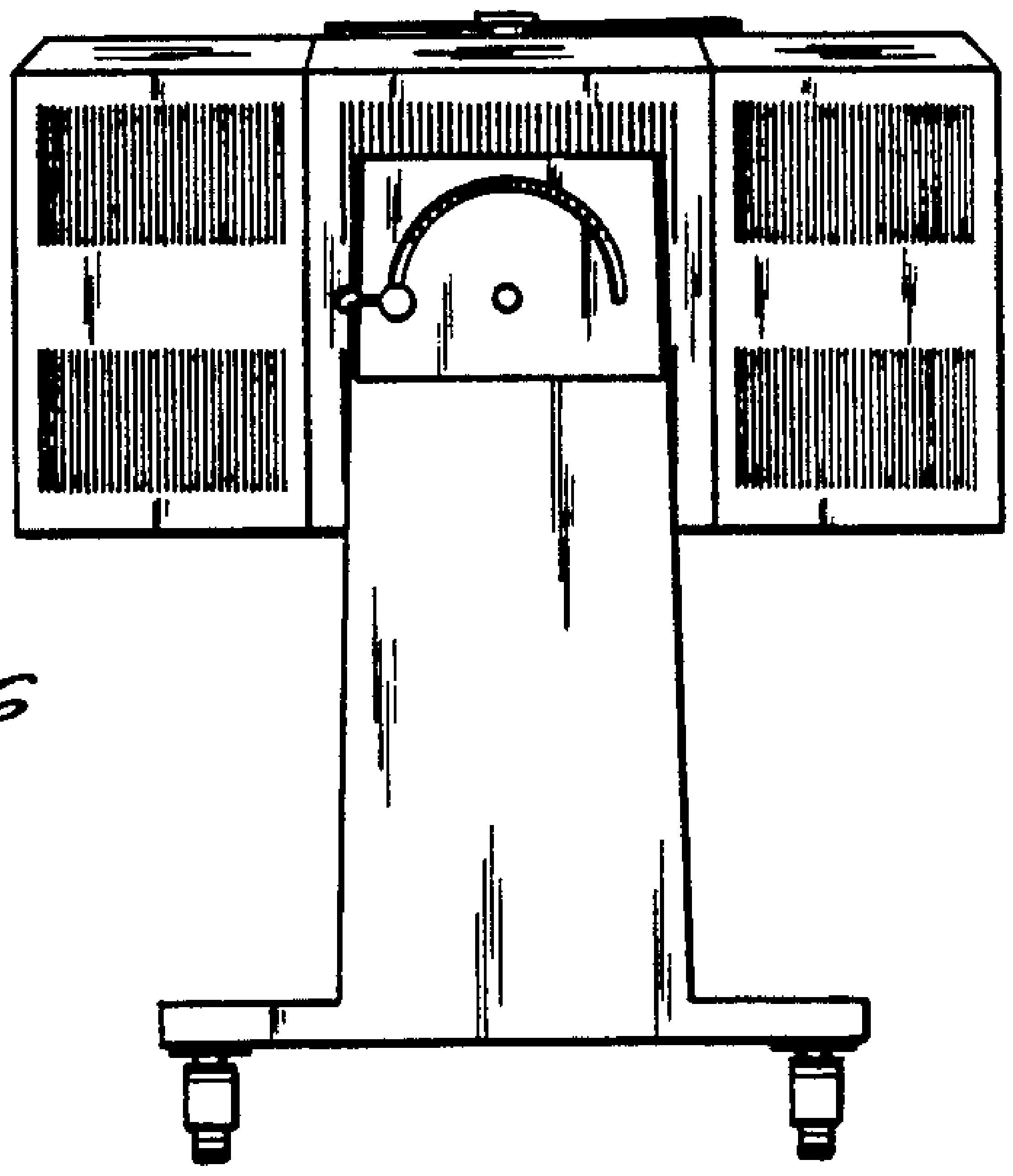


Fig. 16

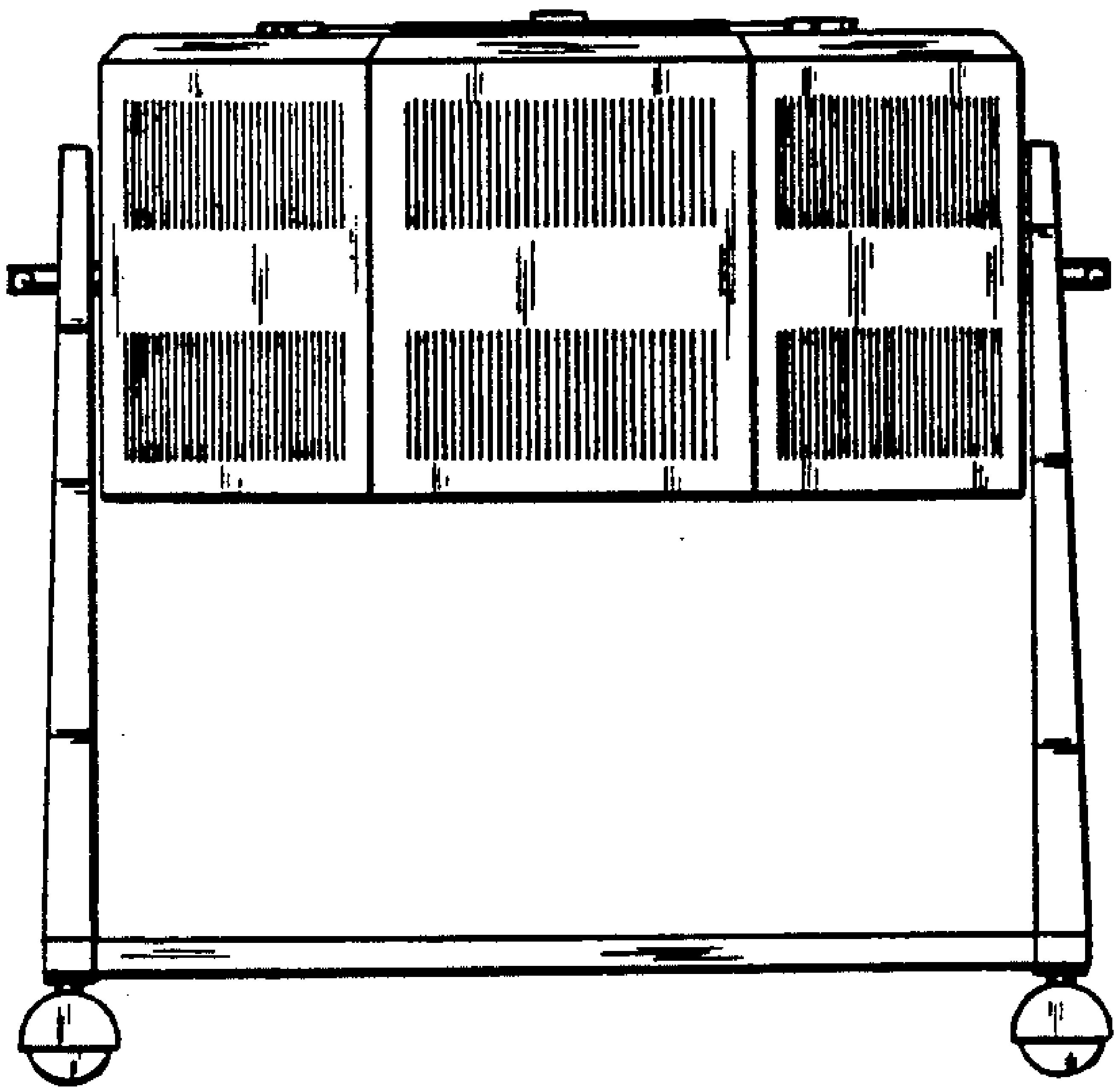


Fig. 17

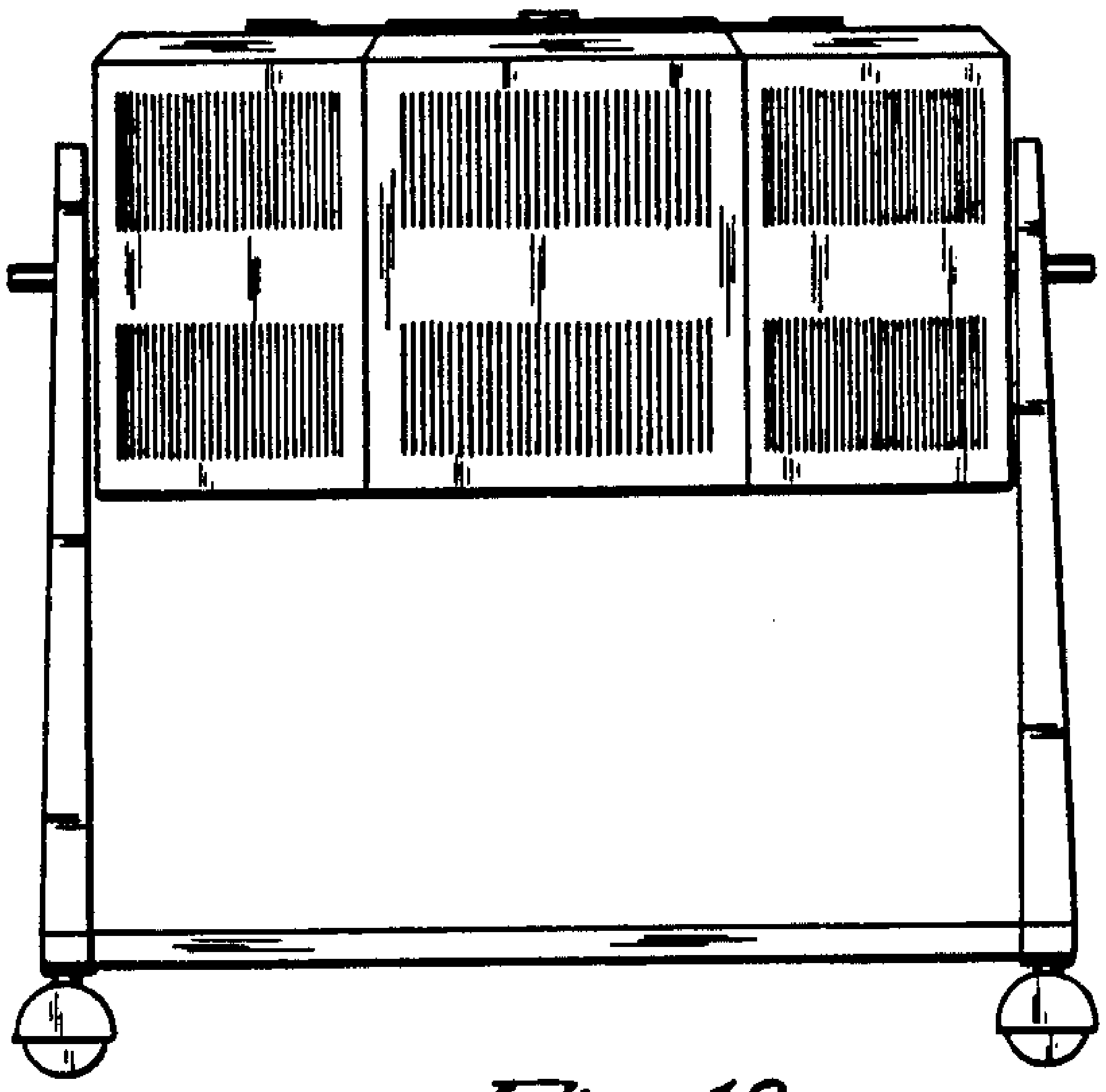


Fig. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : Des. 320,755

DATED : October 15, 1991

INVENTOR(S) : Dahlberg, et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in item [54] and in col. 1, line 2, change "INTERGRATED" to --INTEGRATED--; and

In item [57] Claim, change "a intergrated" to --an integrated--.

In the Description for FIG. 1, change "an intergrated" to --an integrated--.

Signed and Sealed this

Thirteenth Day of April, 1993

Attest:

STEPHEN G. KUNIN

Attesting Officer

Acting Commissioner of Patents and Trademarks