

[54] SEMI-CONDUCTOR MOUNTING  
SUBSTRATE

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[73] Assignee: Ibiden Co., Ltd., Ogaki, Japan

[ \* ] Notice: The portion of the term of this patent  
subsequent to Oct. 24, 2003 has been  
disclaimed.

[\*\*] Term: 14 Years

[21] Appl. No.: 181,252

[22] Filed: Apr. 13, 1988

[52] U.S. Cl. .... D13/182

[58] Field of Search ..... D13/12, 20, 99;  
361/401, 403, 404, 405; 357/70, 72, 74, 80;  
174/52.4; 437/209

[56] References Cited

U.S. PATENT DOCUMENTS

4,288,841	9/1981	Gogal .....	357/74
4,338,621	7/1982	Braun .....	357/80 X
4,437,141	3/1984	Prokop .....	357/74
4,458,291	7/1984	Yanagisawa et al. ....	361/212
4,513,355	4/1985	Shroeder et al. ....	174/52.4
4,677,526	6/1987	Muehling .....	357/70
4,698,663	10/1987	Sugimoto et al. ....	357/81

FOREIGN PATENT DOCUMENTS

0232827	8/1987	European Pat. Off. ....	357/74
0048945	3/1983	Japan .	
644662	2/1985	Japan .	
647072	3/1985	Japan .	
647074	3/1985	Japan .	

647078	3/1985	Japan .	
673983-1	3/1986	Japan .	
673983	3/1986	Japan .	
673984	3/1986	Japan .	
150353	7/1986	Japan .	
0271863	12/1986	Japan .	
0035653	2/1987	Japan .....	357/74

OTHER PUBLICATIONS

*Electronics*, p. 7, Feb. 24, 1986 by Fujitsu Microelec-  
tronics, Inc.

*Electronic Design*, p. 7, dtd 10-16-86, NRC 1C package  
pictured thereon.

*Electronic Design*, p. 190, dtd 10-16-86, Disc Controll  
pictured thereon.

*Electronics*, p. 131, dtd 8-7-86, CMOS chip pictured  
thereon.

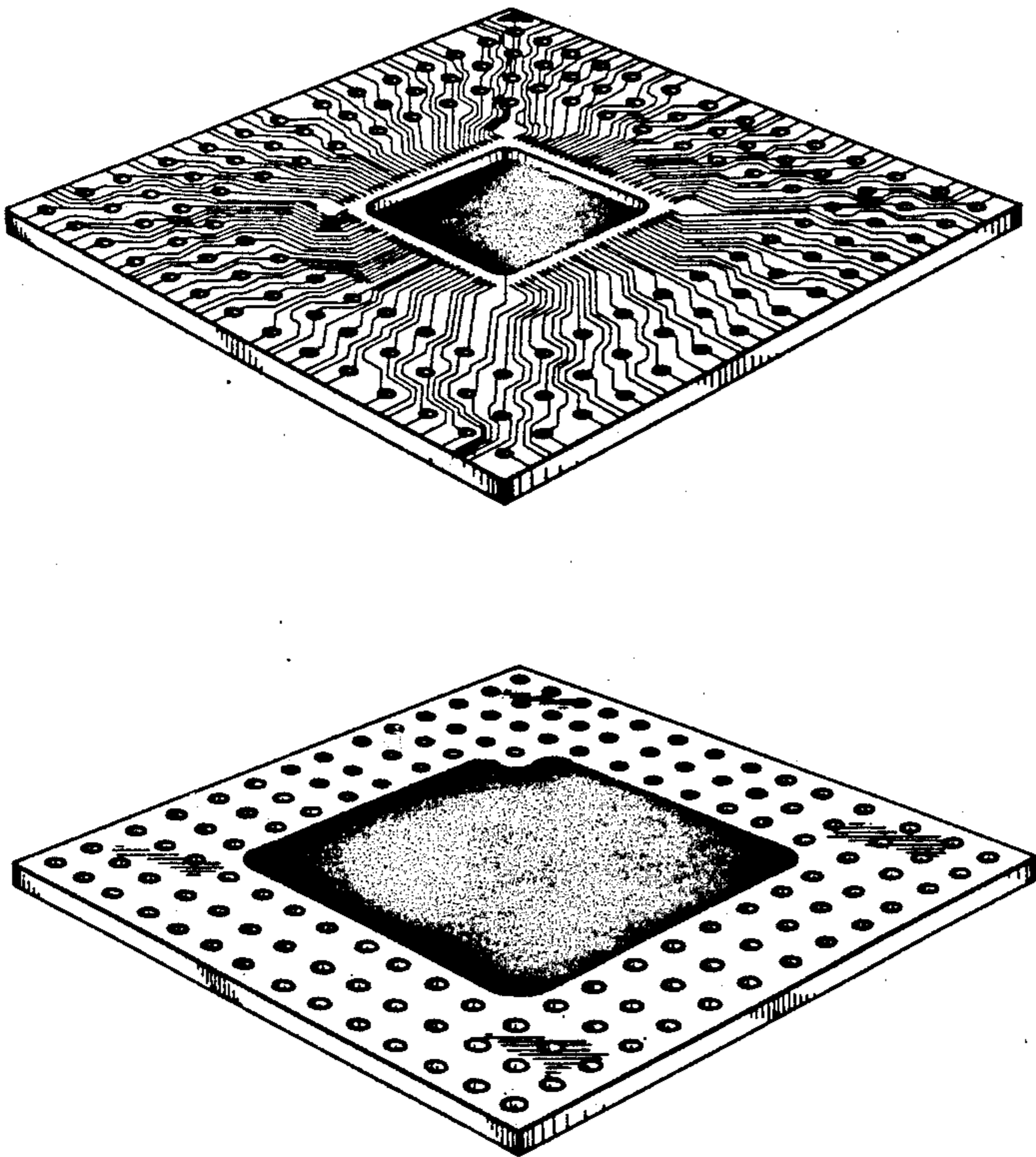
Primary Examiner—Susan J. Lucas  
Assistant Examiner—Joel Sincavage  
Attorney, Agent, or Firm—Lorusso & Loud

[57] CLAIM

The ornamental design for a semi-conductor mounting  
substrate, as shown.

DESCRIPTION

FIG. 1 is a top perspective view of a semi-conductor  
mounting substrate showing our new design;  
FIG. 2 is a bottom perspective view thereof;  
FIG. 3 is a right side elevational view thereof;  
FIG. 4 is a left side elevational view thereof;  
FIG. 5 is a rear elevational view thereof;  
FIG. 6 is a front elevational view thereof;  
FIG. 7 is a top plan view thereof; and  
FIG. 8 is a bottom plan view thereof.



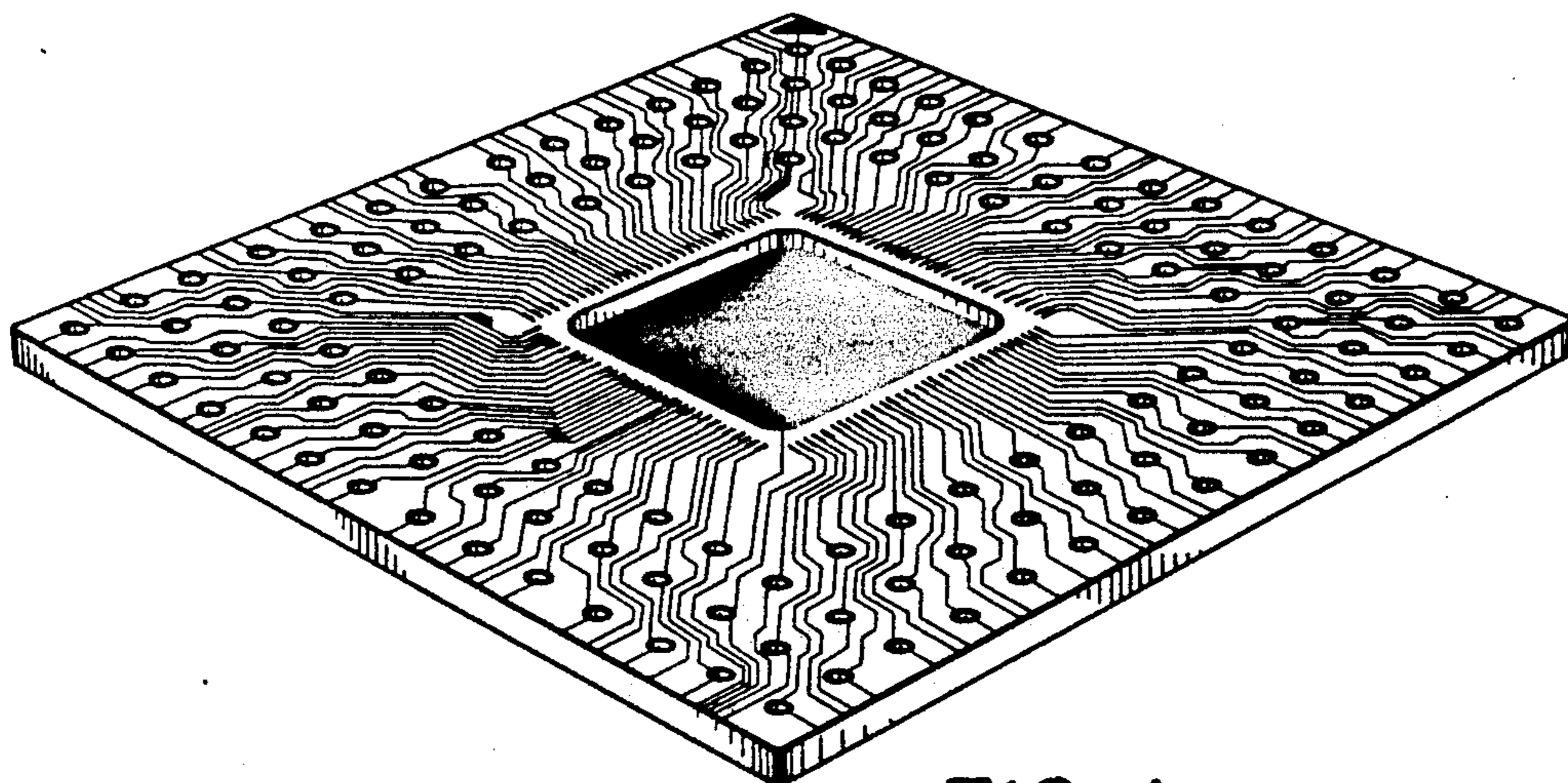


FIG. 1

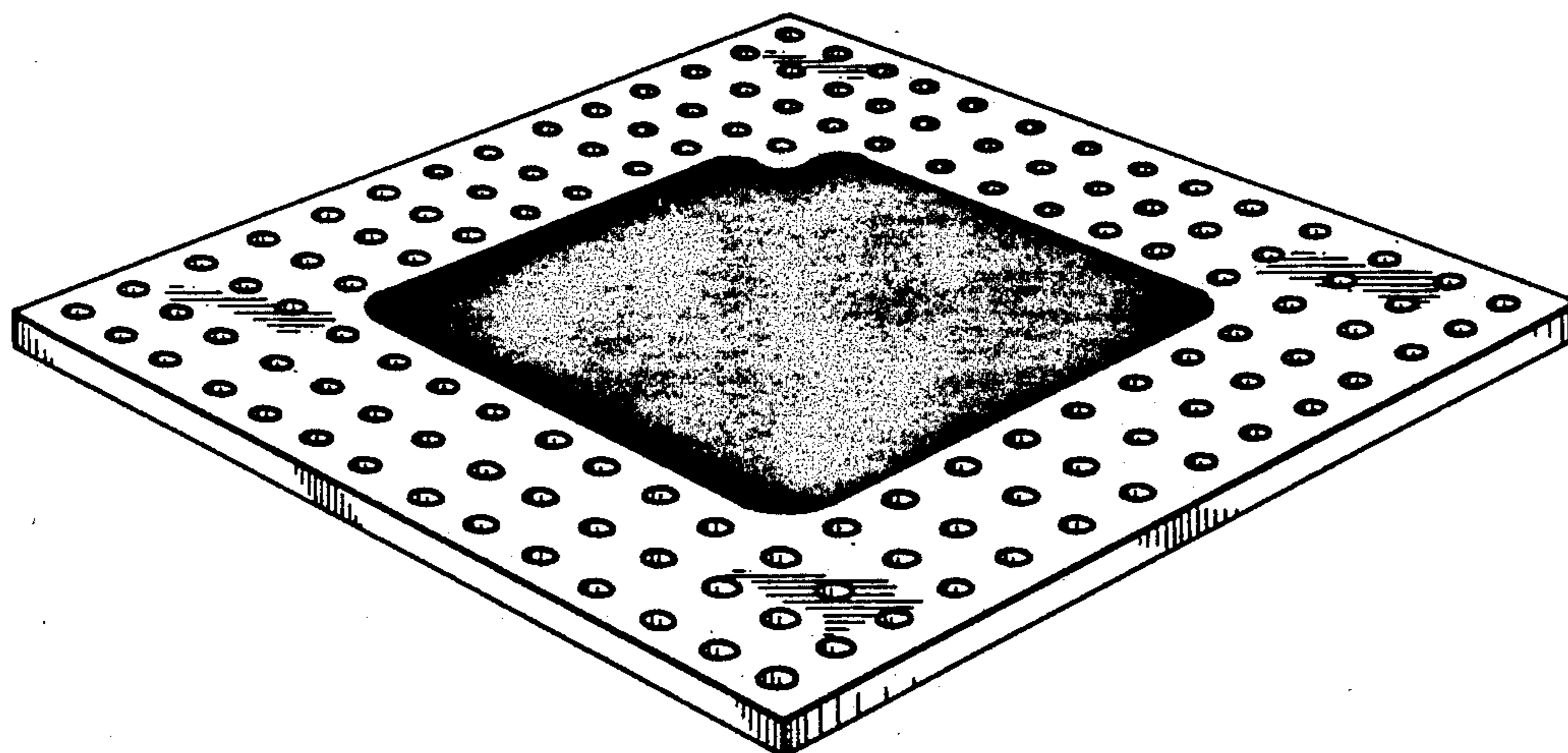


FIG. 2



*FIG. 3*



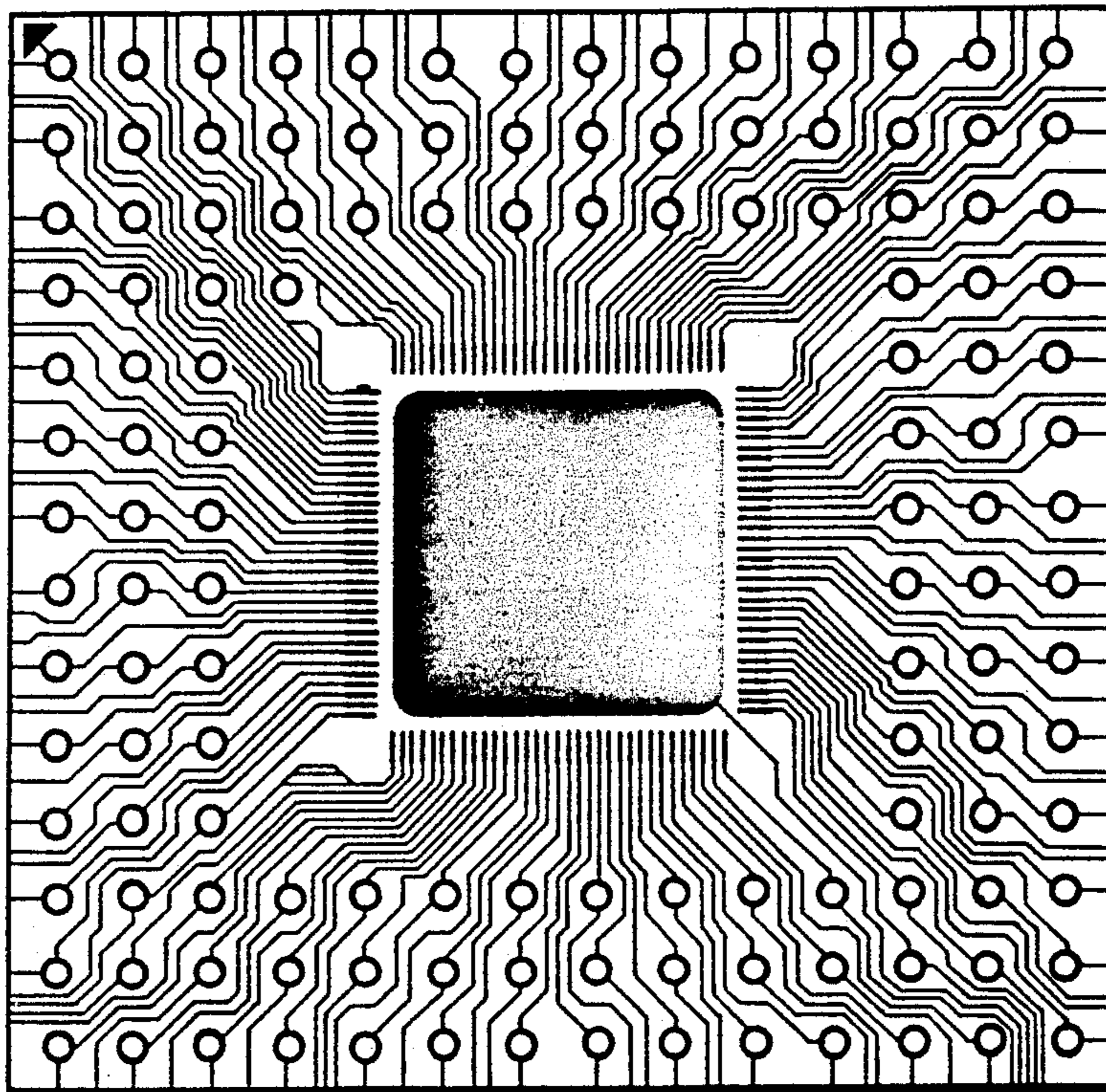
*FIG. 4*



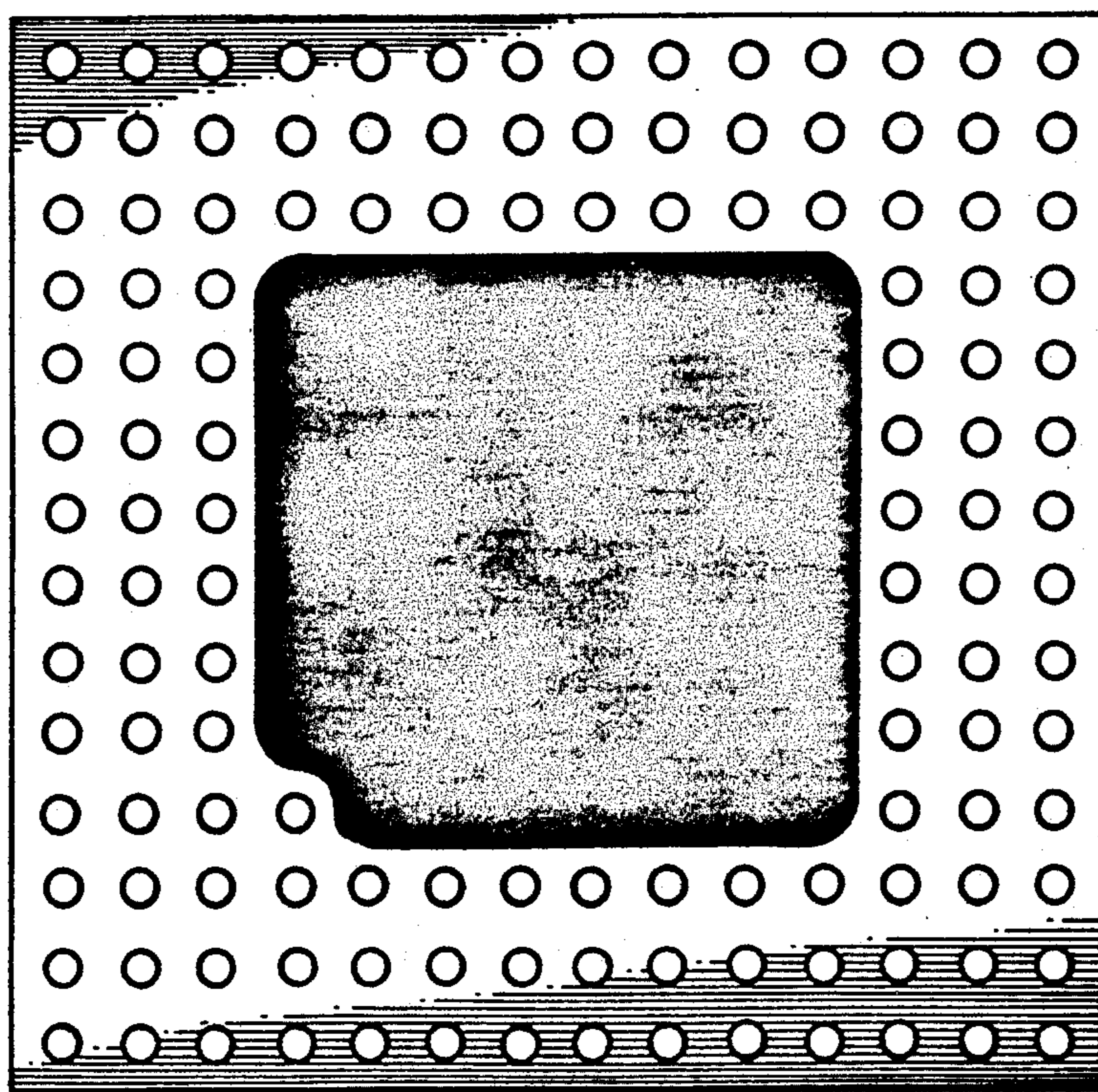
*FIG. 5*



*FIG. 6*



*FIG. 7*



*FIG. 8*

UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. : Des. 318,461

DATED : July 23, 1991

INVENTOR(S) : Hasegawa et al.

It is certified that error appears in the above—identified patent and that said Letters Patent is hereby corrected as shown below:

In Col. 1, line 6, the "[\*] Notice:" section should be delete in its entirety.

Signed and Sealed this  
Fifteenth Day of June, 1993

Attest:



MICHAEL K. KIRK

Attesting Officer

Acting Commissioner of Patents and Trademarks