

[54] MOUNTING SUBSTRATE FOR SEMICONDUCTORS

[76] Inventors: Terutomi Hasegawa, 2-40 Nakagawa-Cho, Ogaki-City, Gifu Pref.; Nobumichi Goto, 291, Kami-Shirokane, Seki City Gifu Pref., both of Japan

[**] Term: 14 Years

[21] Appl. No.: 140,434

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[30] Foreign Application Priority Data

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Jul. 4, 1987 [JP] Japan 62-27280

[52] U.S. Cl. D13/82

[58] Field of Search D13/12, 20, 99; 361/401, 403, 404, 405; 357/70, 72, 74, 80; 174/52.4; 437/209

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Disc Controller pictured on p. 190, Electronic Design, 10-16-86.
NCR IC Package pictured on p. 7, Electronic Design, 10-16-86.
CMOS Chip pictured on p. 131, Electronics, 8-7-86.

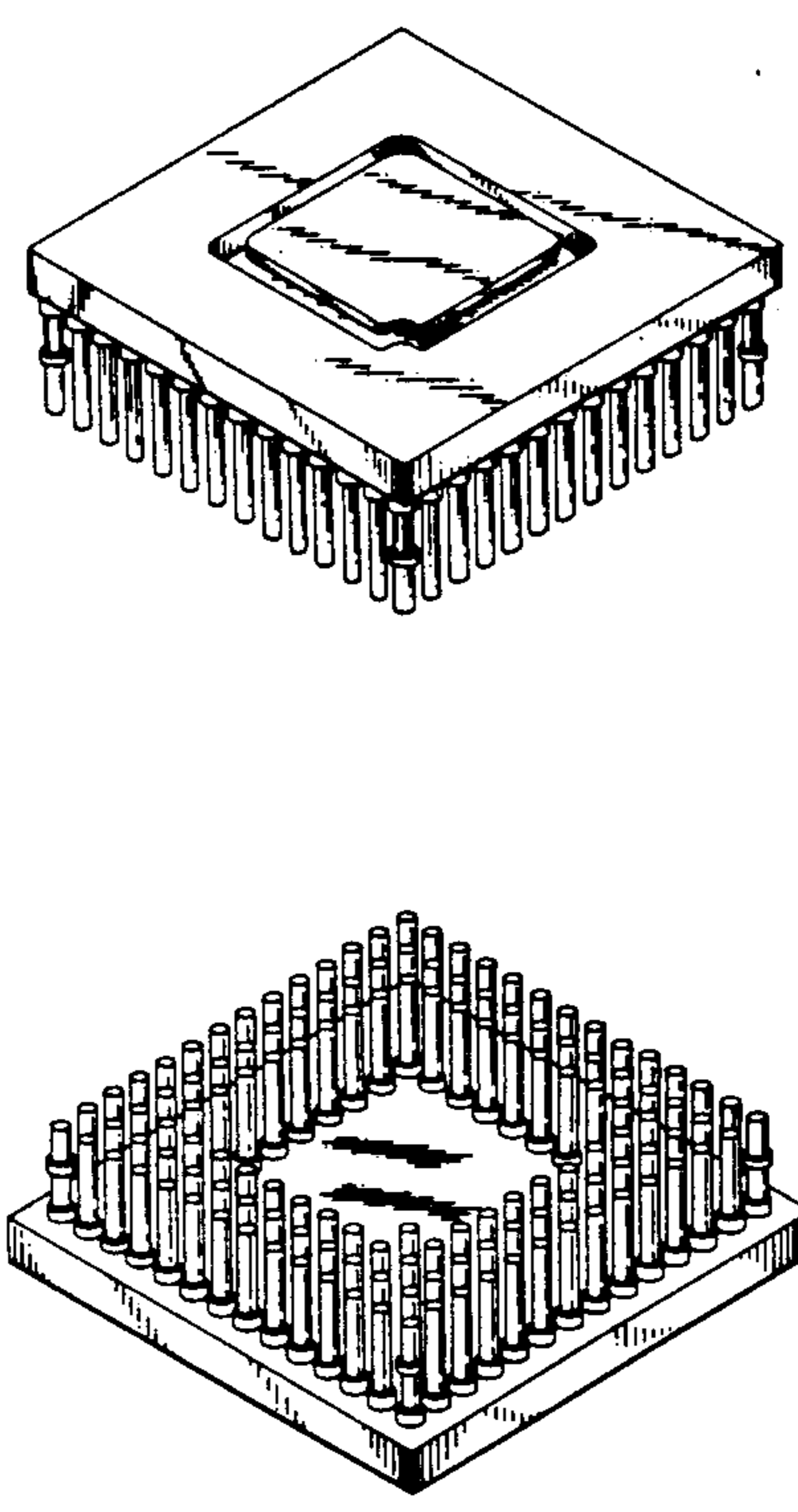
Primary Examiner—Susan J. Lucas
Assistant Examiner—Joel Sincavage
Attorney, Agent, or Firm—Lorruso & Loud

[57] CLAIM

The ornamental design for a mounting substrate for semi-conductors, as shown.

DESCRIPTION

FIG. 1 is a top perspective view of a mounting substrate for semi-conductors showing our new design; FIG. 2 is a bottom perspective view thereof; FIG. 3 is a right side elevational view thereof; FIG. 4 is a left side elevational view thereof; FIG. 5 is a rear elevational view thereof; and FIG. 6 is a front elevational view thereof.



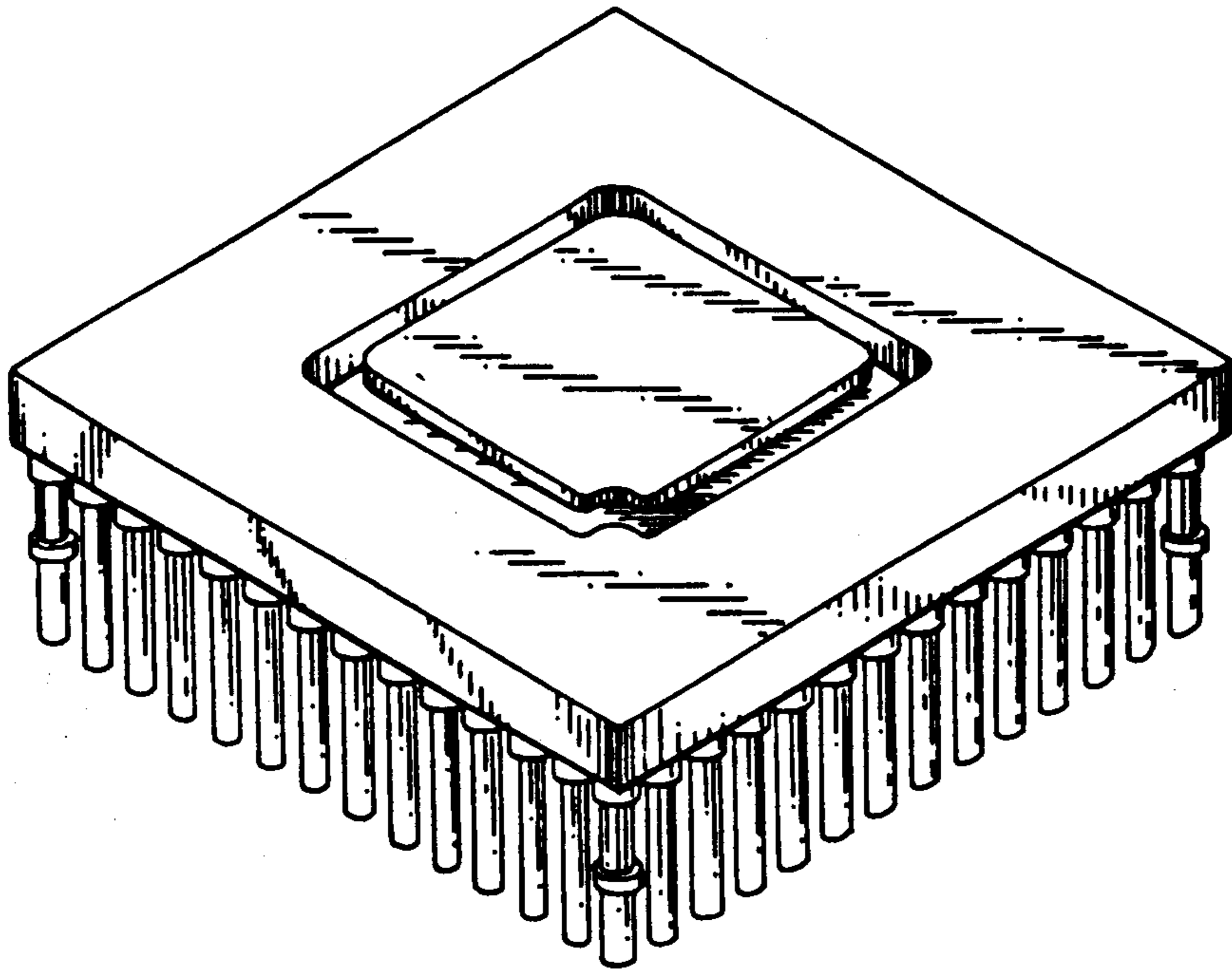


FIG. 1

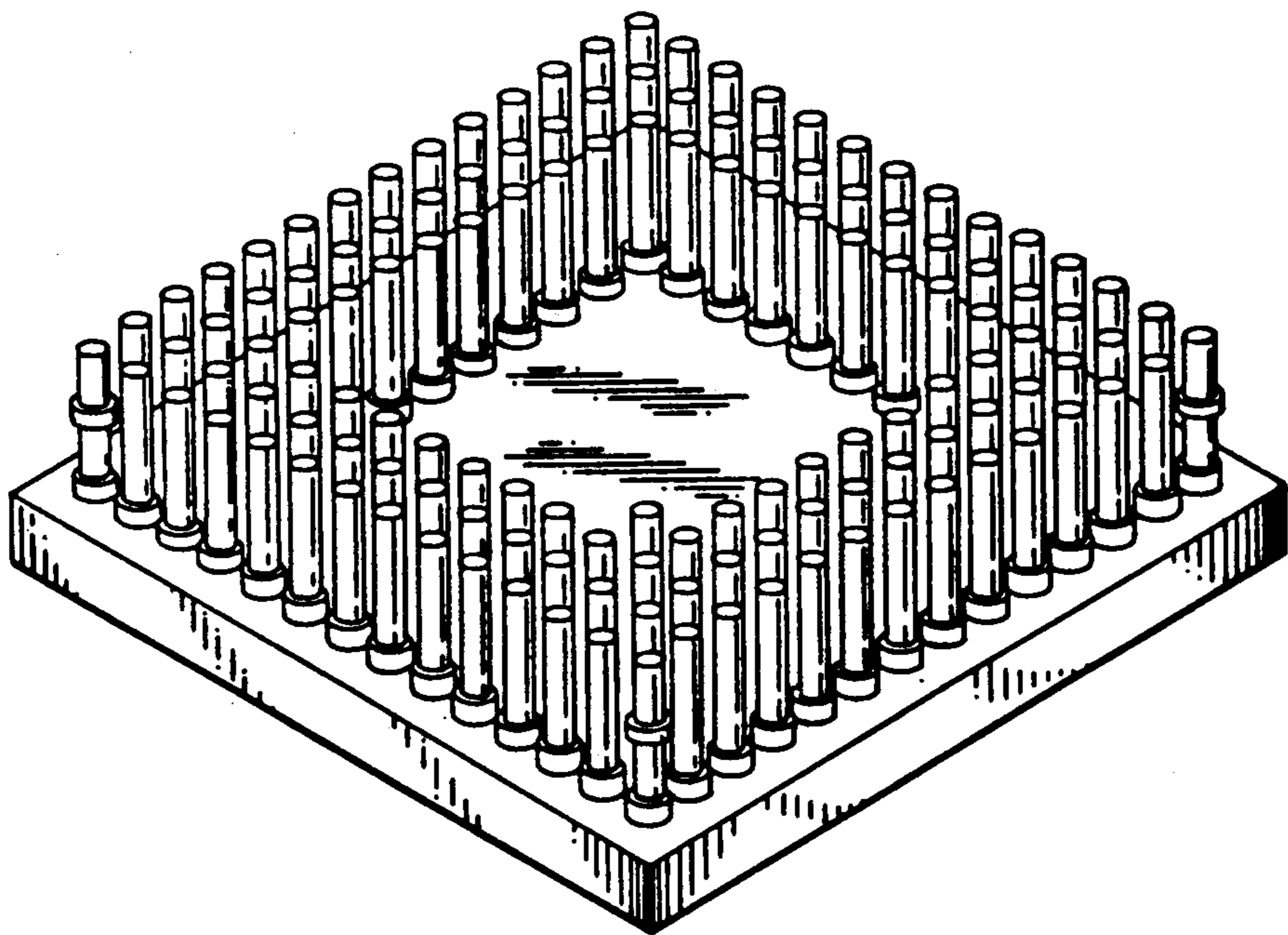


FIG. 2

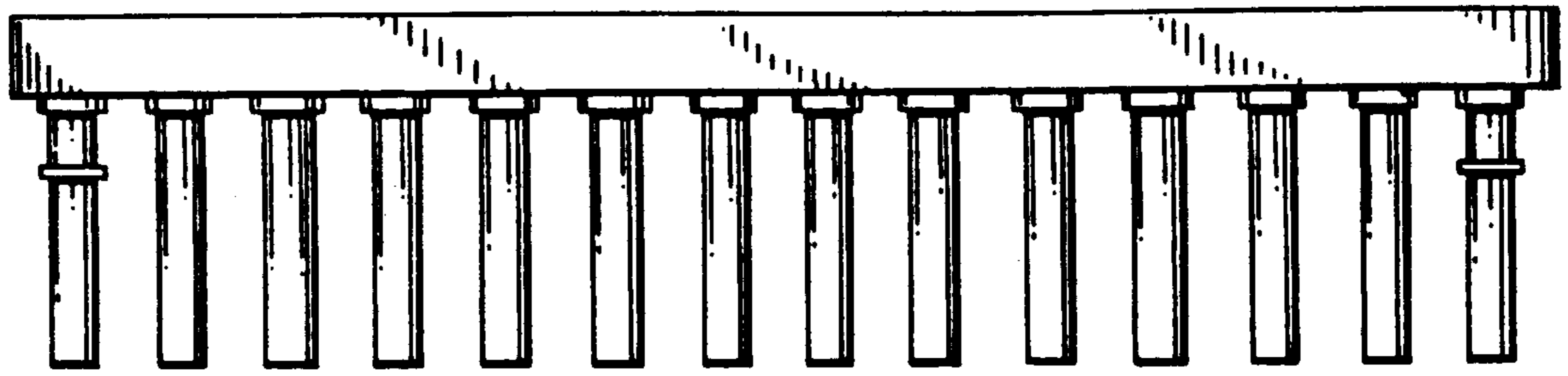


FIG. 3

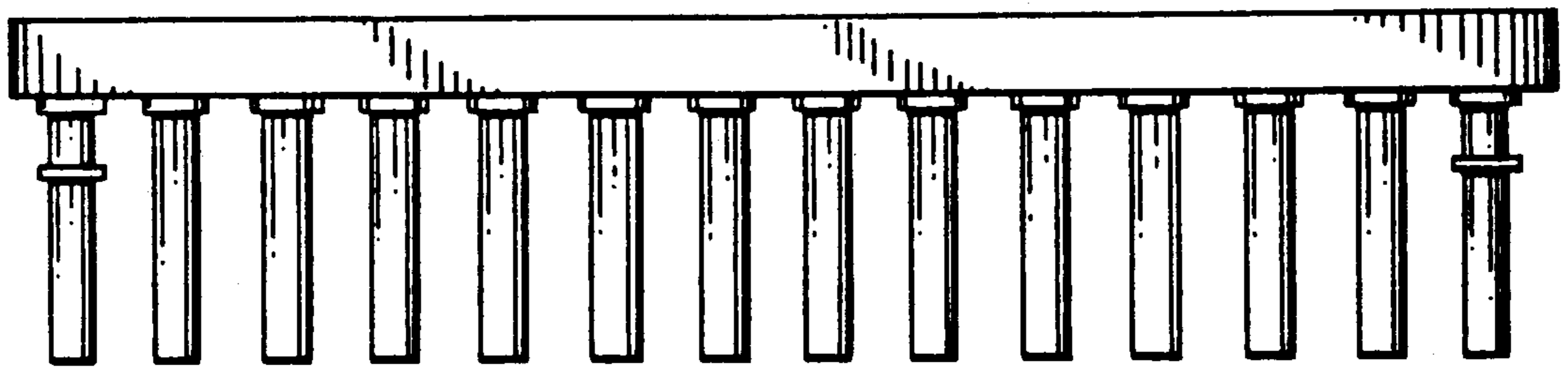


FIG. 4

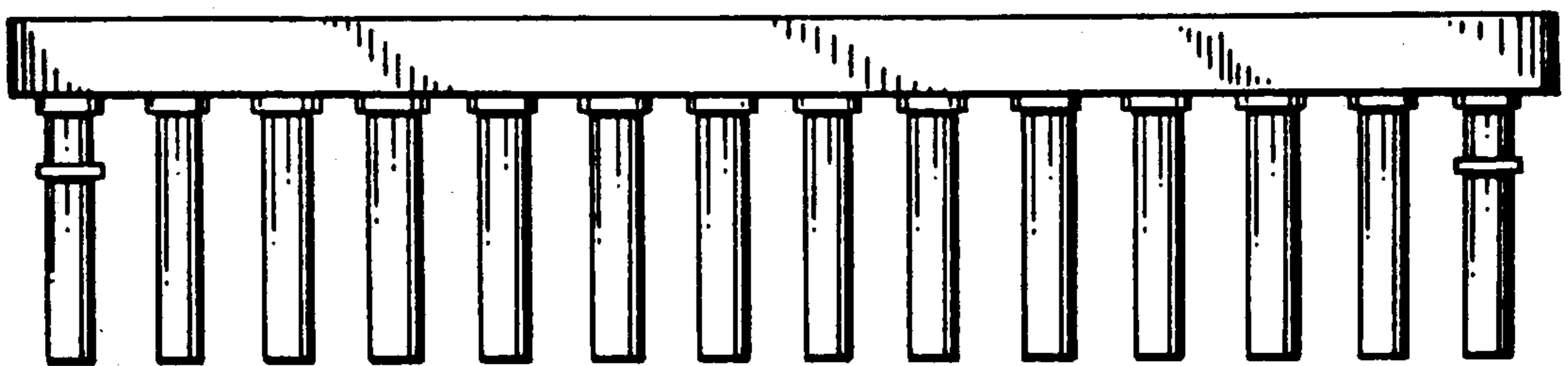


FIG. 5

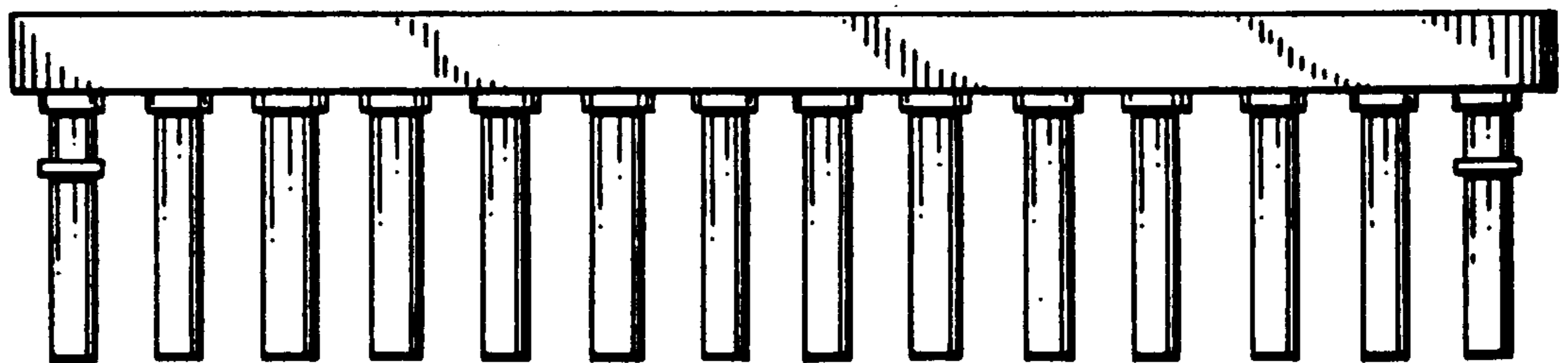


FIG. 6

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : Des. 316,848
DATED : May 14, 1991
INVENTOR(S) : Hasegawa et al.

It is certified that error appears in the above—identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:

Under the heading "FOREIGN PATENT DOCUMENTS", please insert the following:

--673983	11/1985	Japan
673983-1	11/1985	Japan
673984	11/1985	Japan --

Signed and Sealed this
Third Day of August, 1993

Attest:



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