

[54] IN-LINE SEMICONDUCTOR PACKAGE

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[\*\*] Term: 14 Years

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[52] U.S. Cl. .... D13/182

[58] Field of Search ..... D13/182, 147; 361/403, 361/404, 405; 174/52.2, 52.4; 357/70, 72; 437/209

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Primary Examiner—Susan J. Lucas  
Assistant Examiner—Joel Sincavage

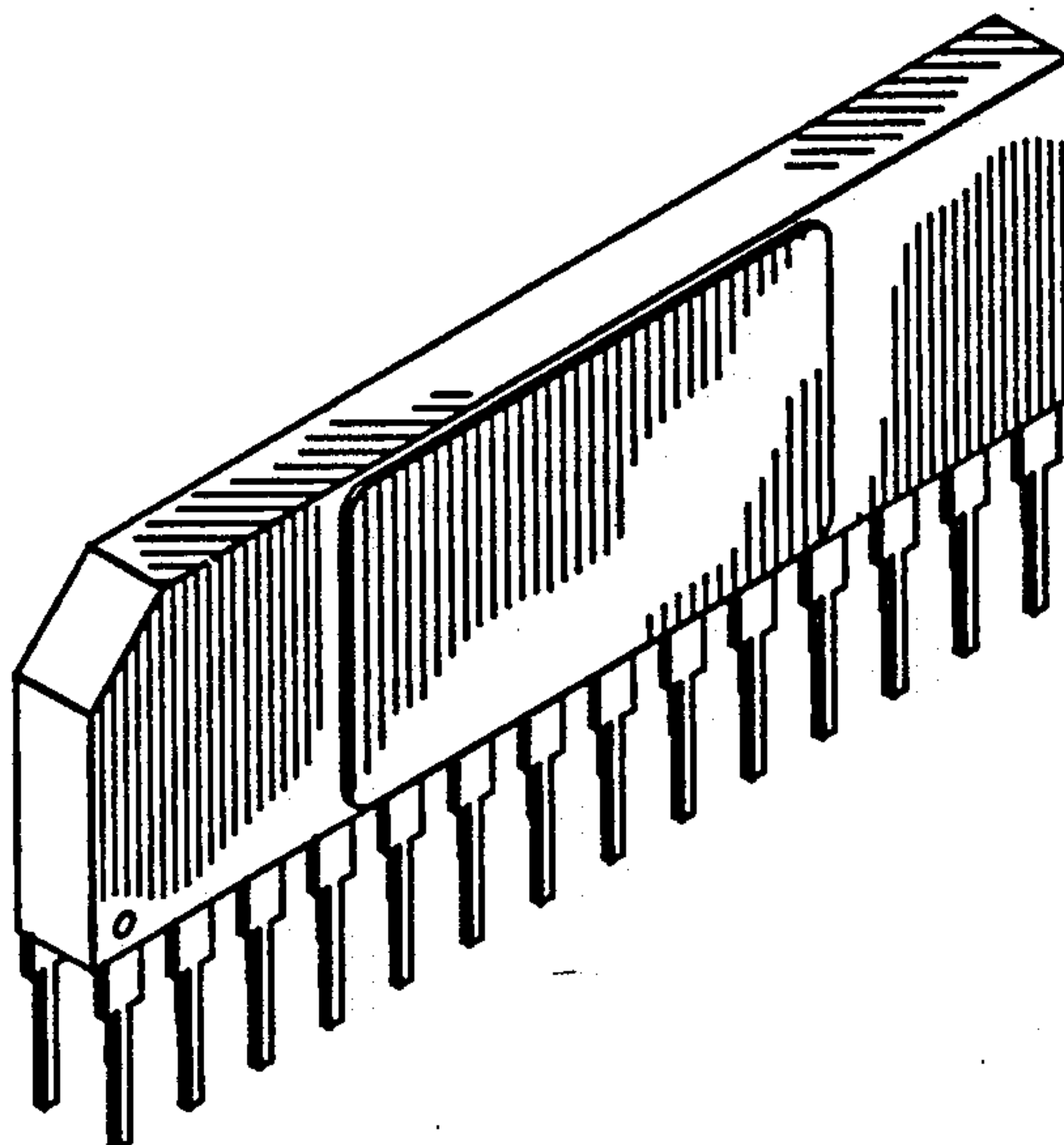
Attorney, Agent, or Firm—Knobbe, Martens, Olson & Bear

[57] CLAIM

The ornamental design for a in-line semiconductor package, as shown and described.

DESCRIPTION

FIG. 1 is a top, front and left side perspective view of an in-line semiconductor package showing my new design; FIG. 2 is a top plan view thereof; FIG. 3 is a front elevational view thereof; FIG. 4 is a bottom plan view thereof; FIG. 5 is a rear elevational view thereof; FIG. 6 is a left side elevational view thereof; FIG. 7 is a right side elevational view thereof; FIG. 8 is a top, front and left side perspective view of an in-line semiconductor package showing a second embodiment of my new design; FIG. 9 is a top plan view thereof; FIG. 10 is a front elevational view thereof; FIG. 11 is a bottom plan view thereof; FIG. 12 is a rear elevational view thereof; FIG. 13 is a right side elevational view thereof, the left side being a mirror image; FIG. 14 is a top, front and left side perspective view of an in-line semiconductor package showing a third embodiment of my new design; FIG. 15 is a bottom, left and rear perspective view thereof; FIG. 16 is a top, front and left side perspective view of an in-line semiconductor package showing a fourth embodiment of my new design; FIG. 17 is a bottom, left and rear perspective view thereof; FIG. 18 is a top, front and left side perspective view of an in-line semiconductor package showing a fifth embodiment of my new design; FIG. 19 is a bottom, left and rear perspective view thereof; FIG. 20 is a right side elevational view of the third, fourth and fifth embodiments of my new design.



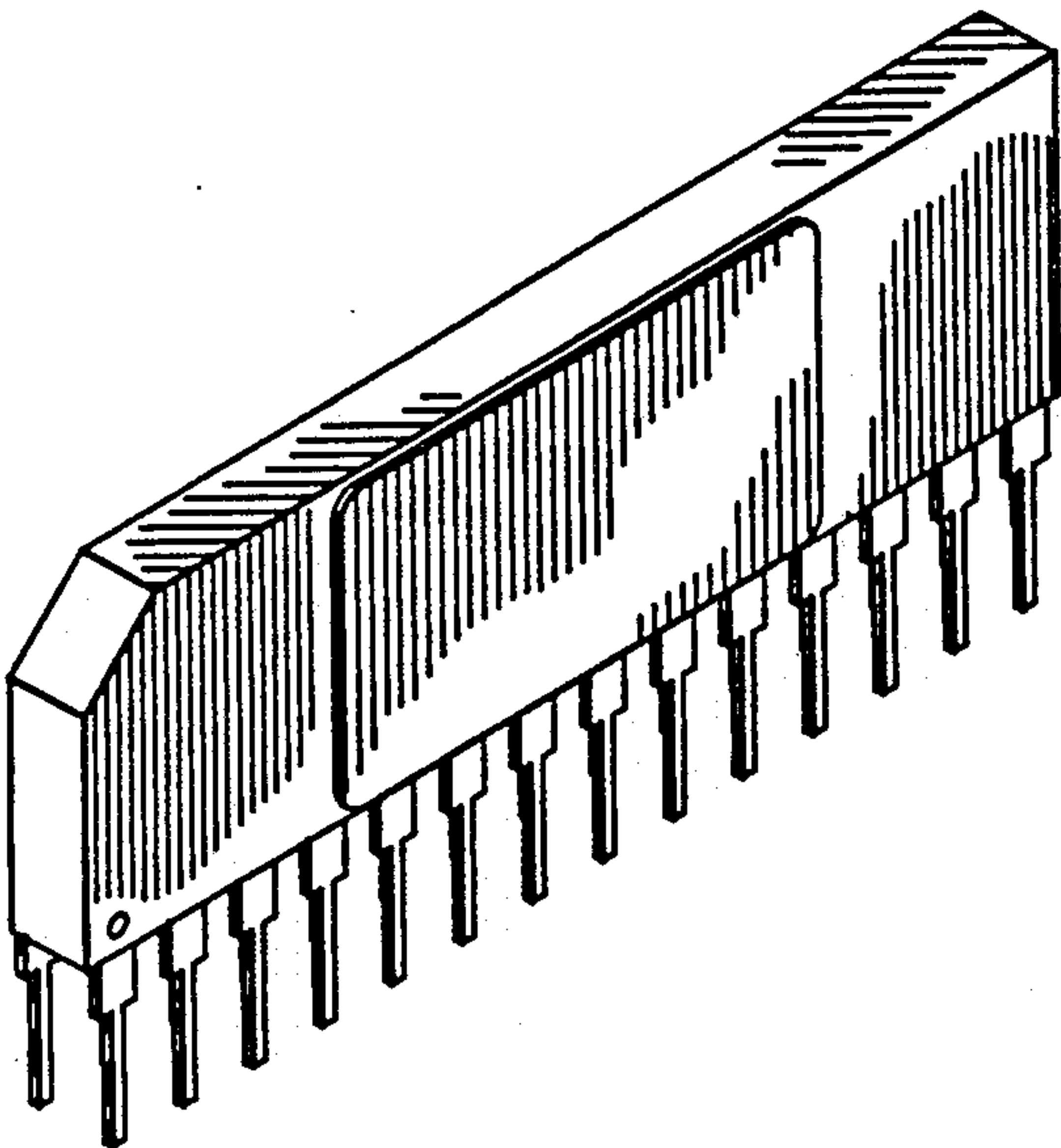


FIG. 1



FIG. 2



FIG. 6

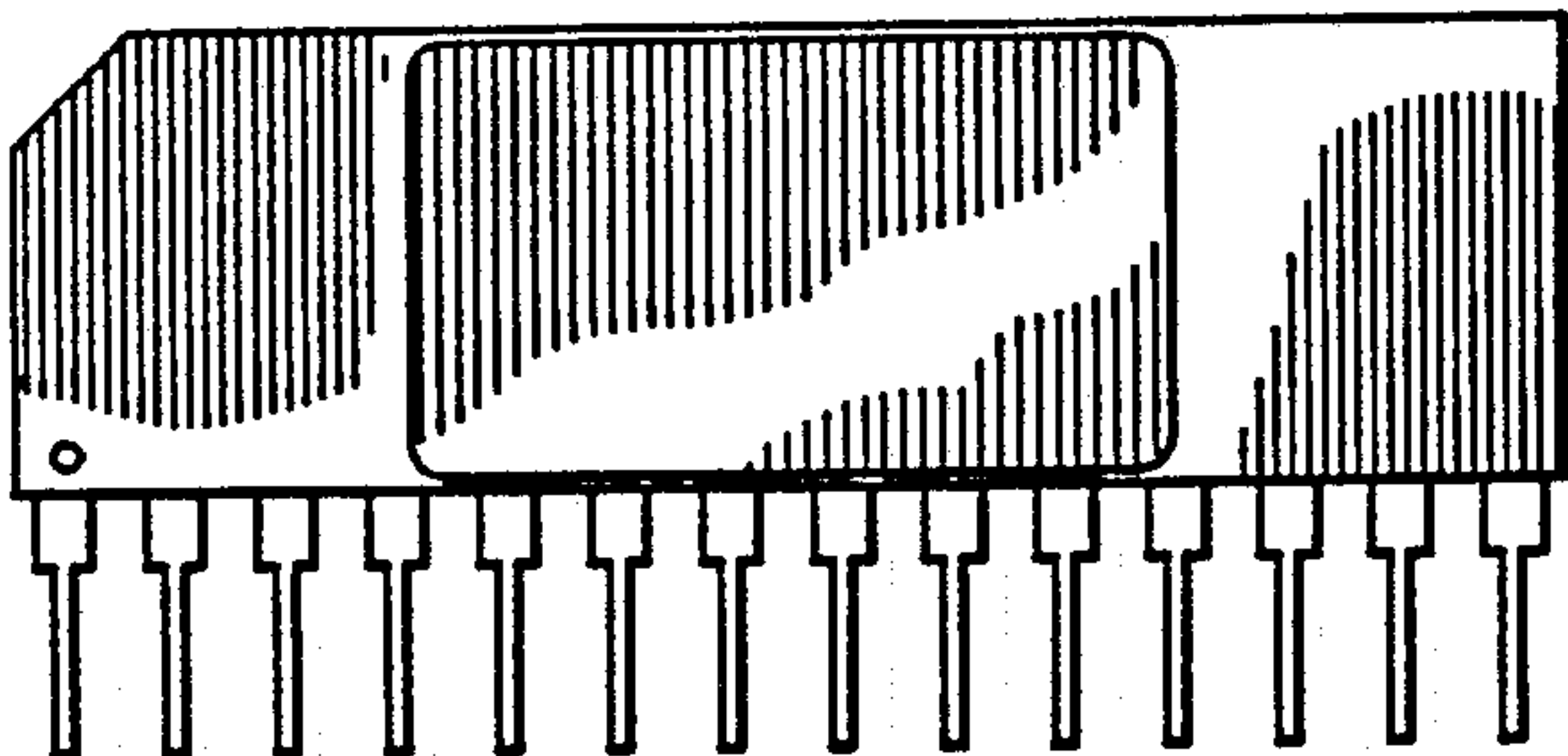


FIG. 3



FIG. 7



FIG. 4

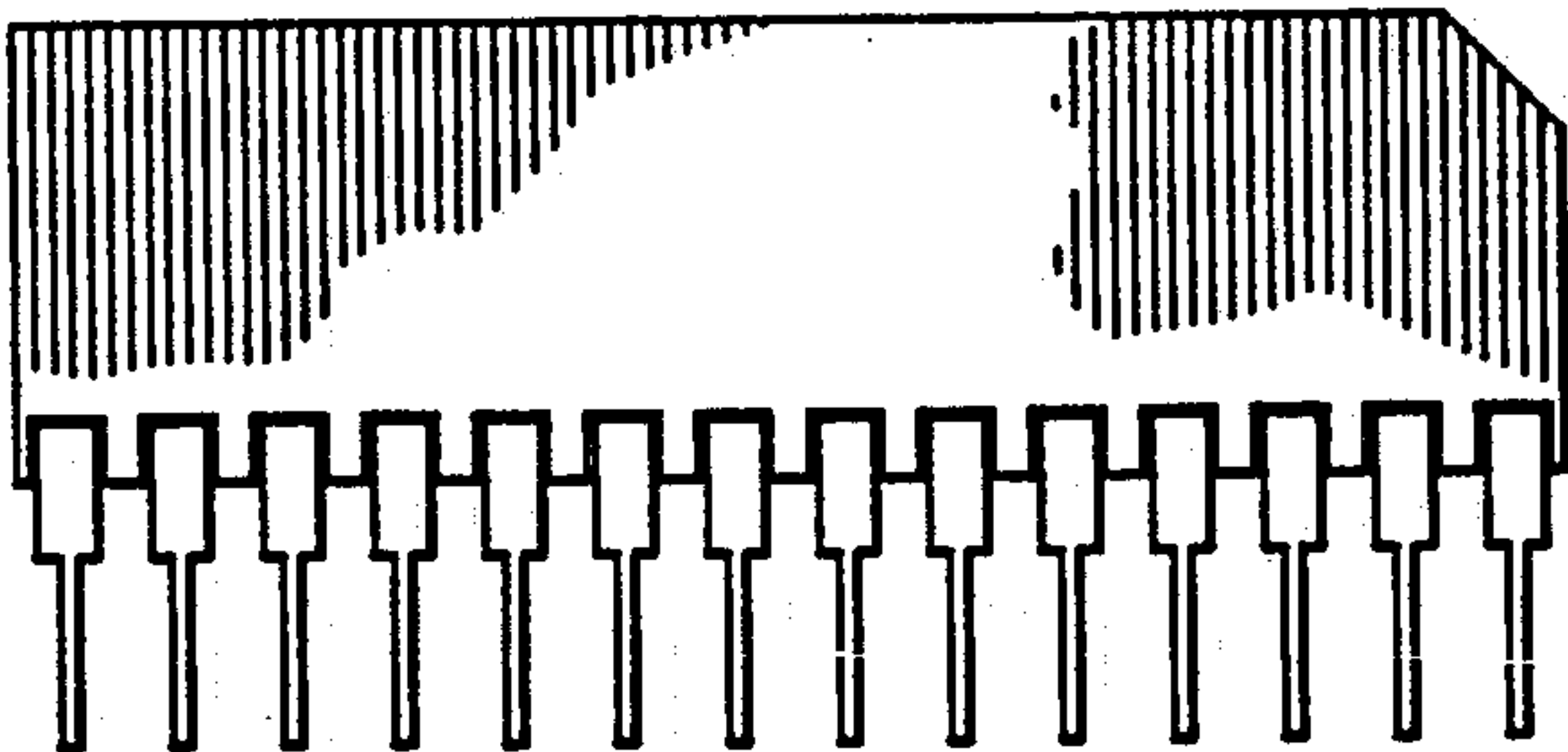


FIG. 5

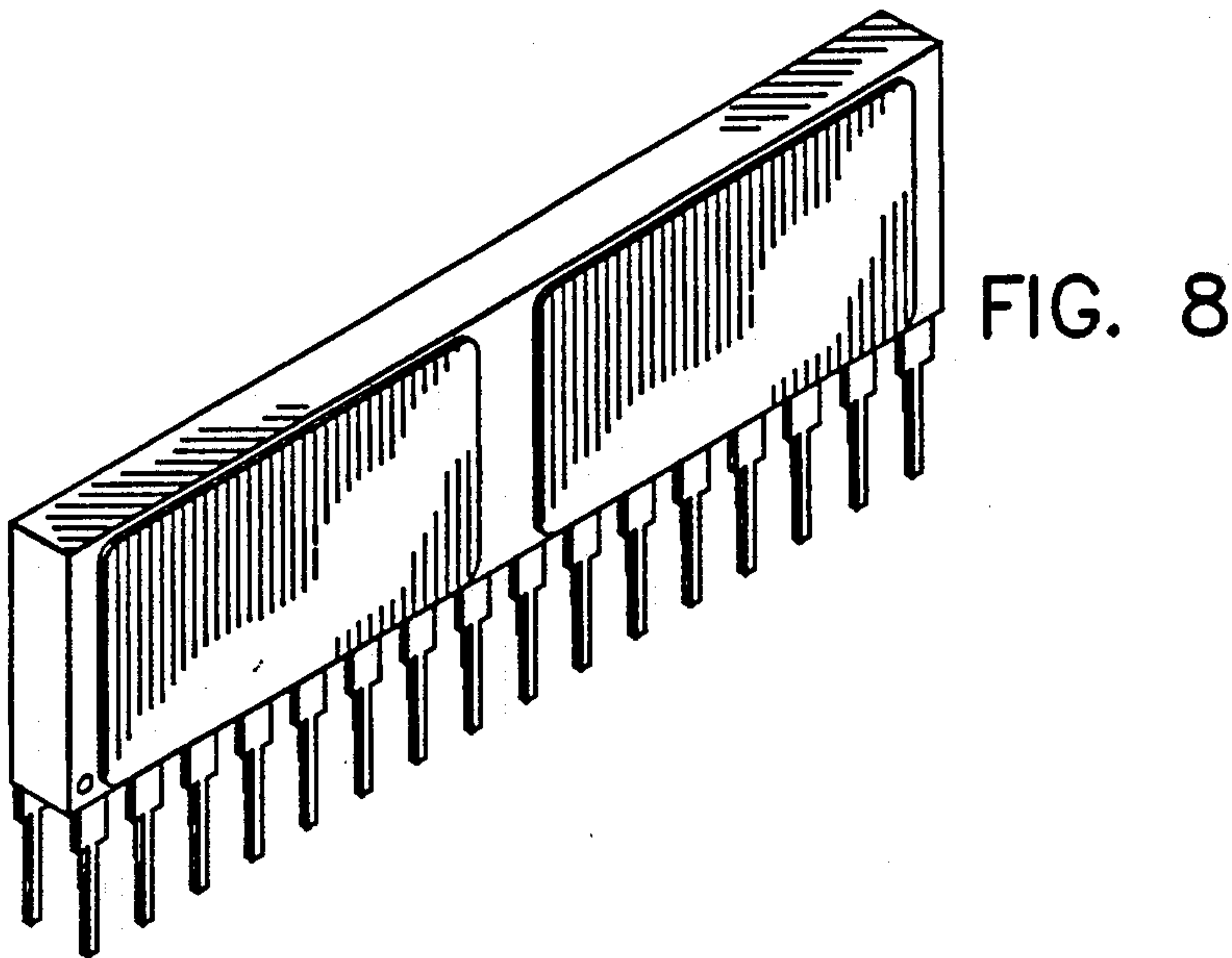


FIG. 8



FIG. 9

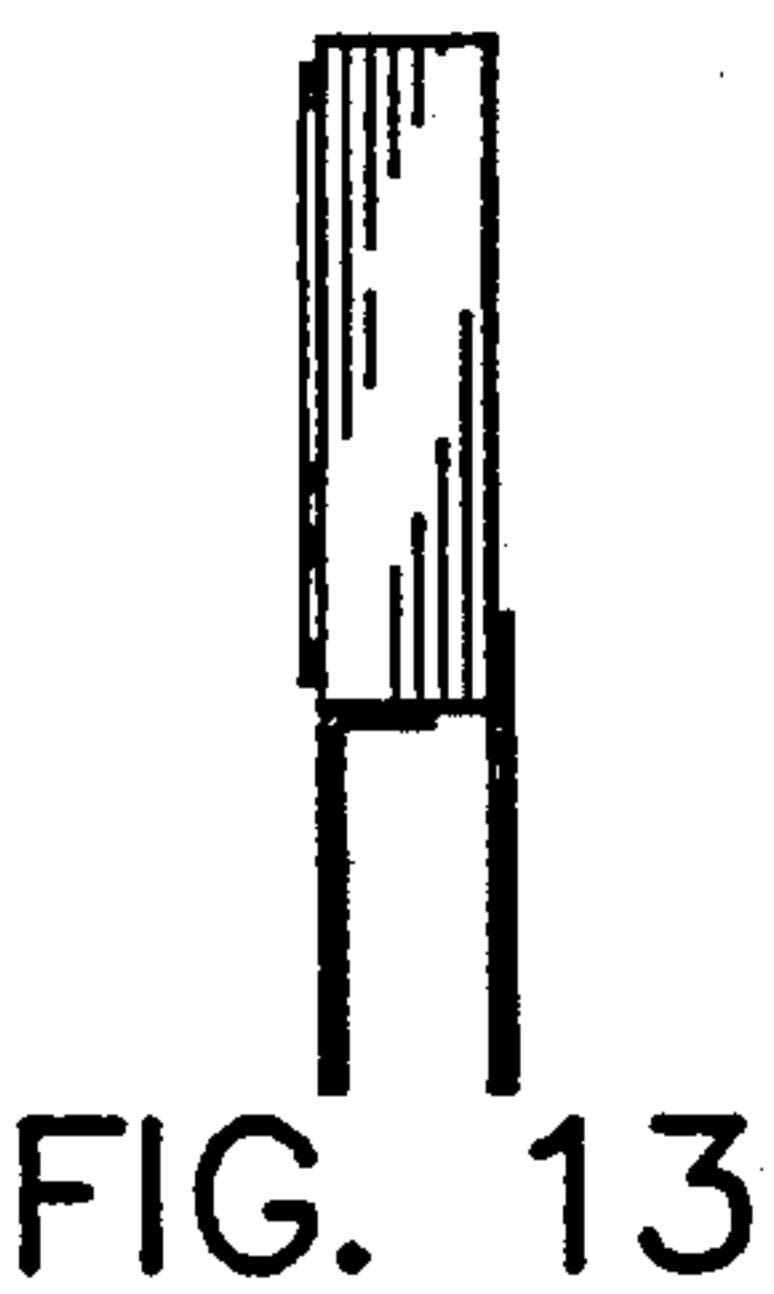


FIG. 13

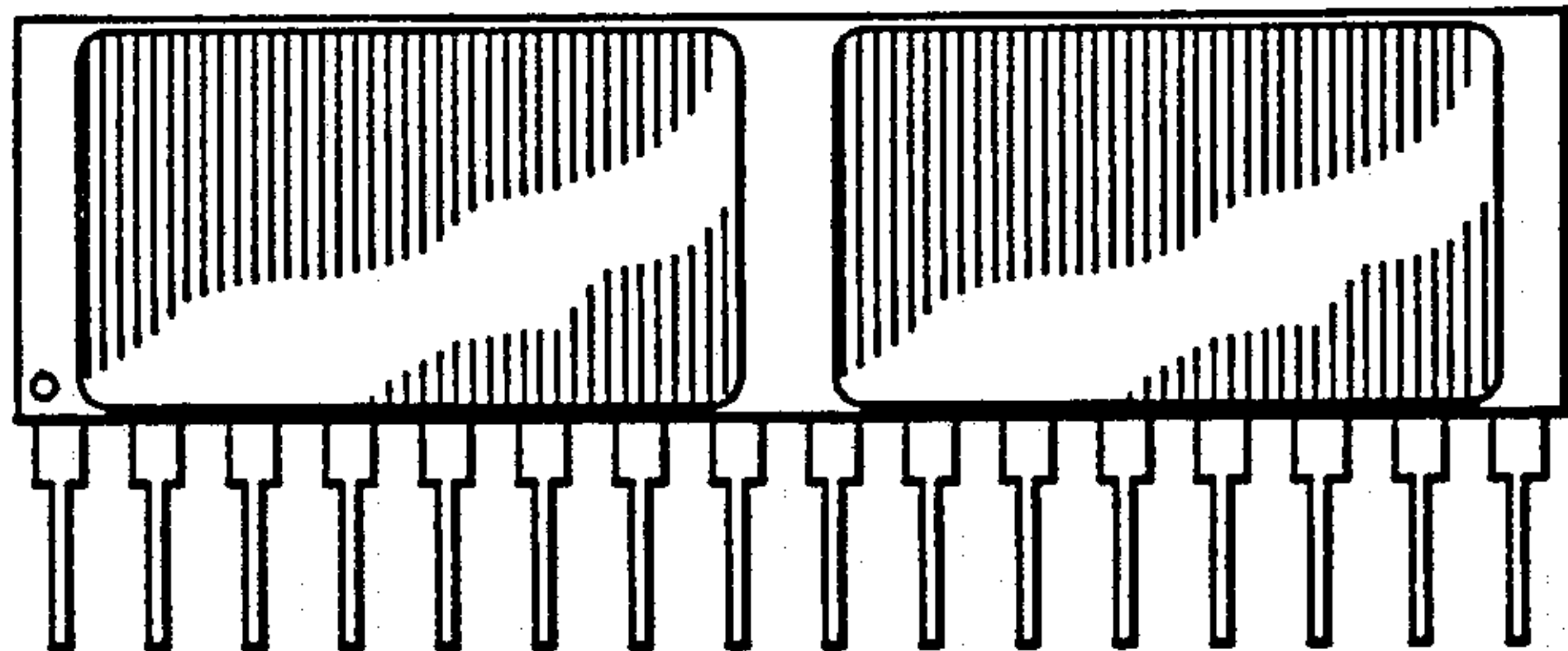


FIG. 10



FIG. 11

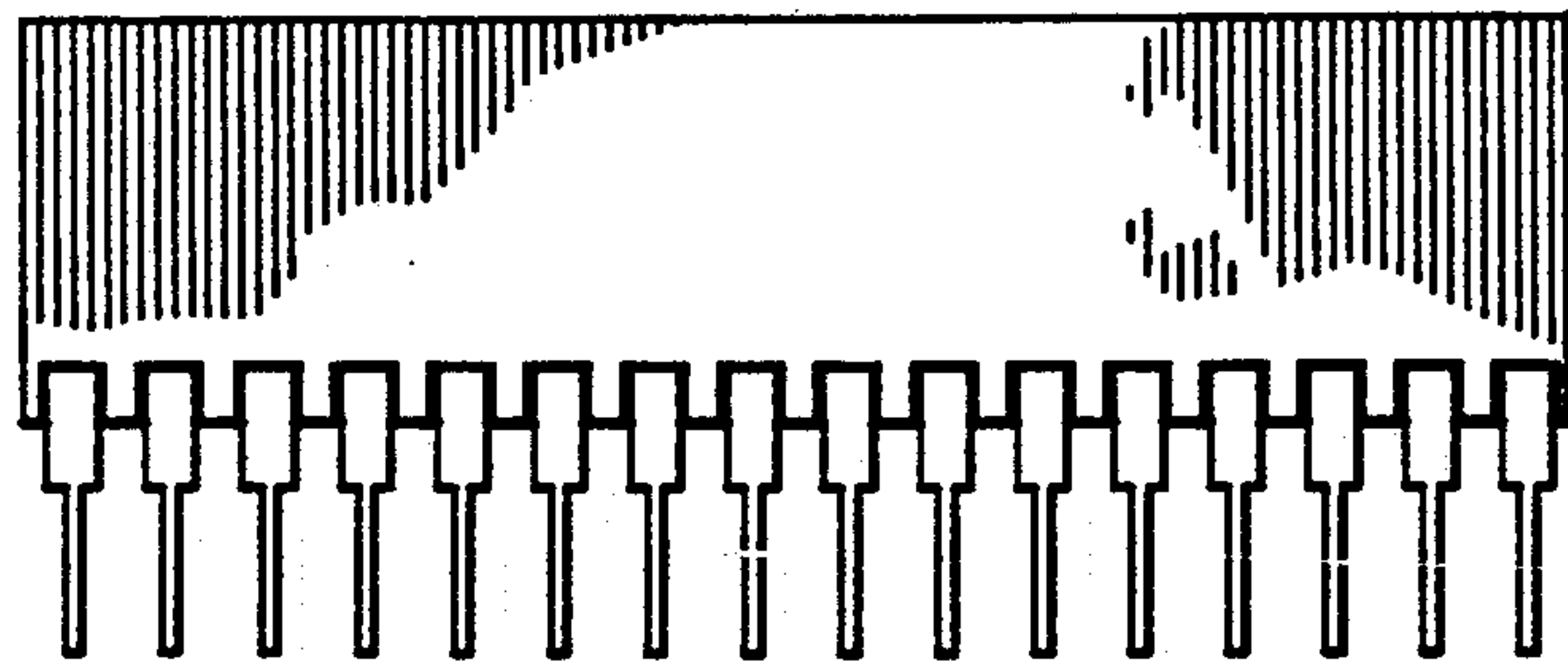


FIG. 12



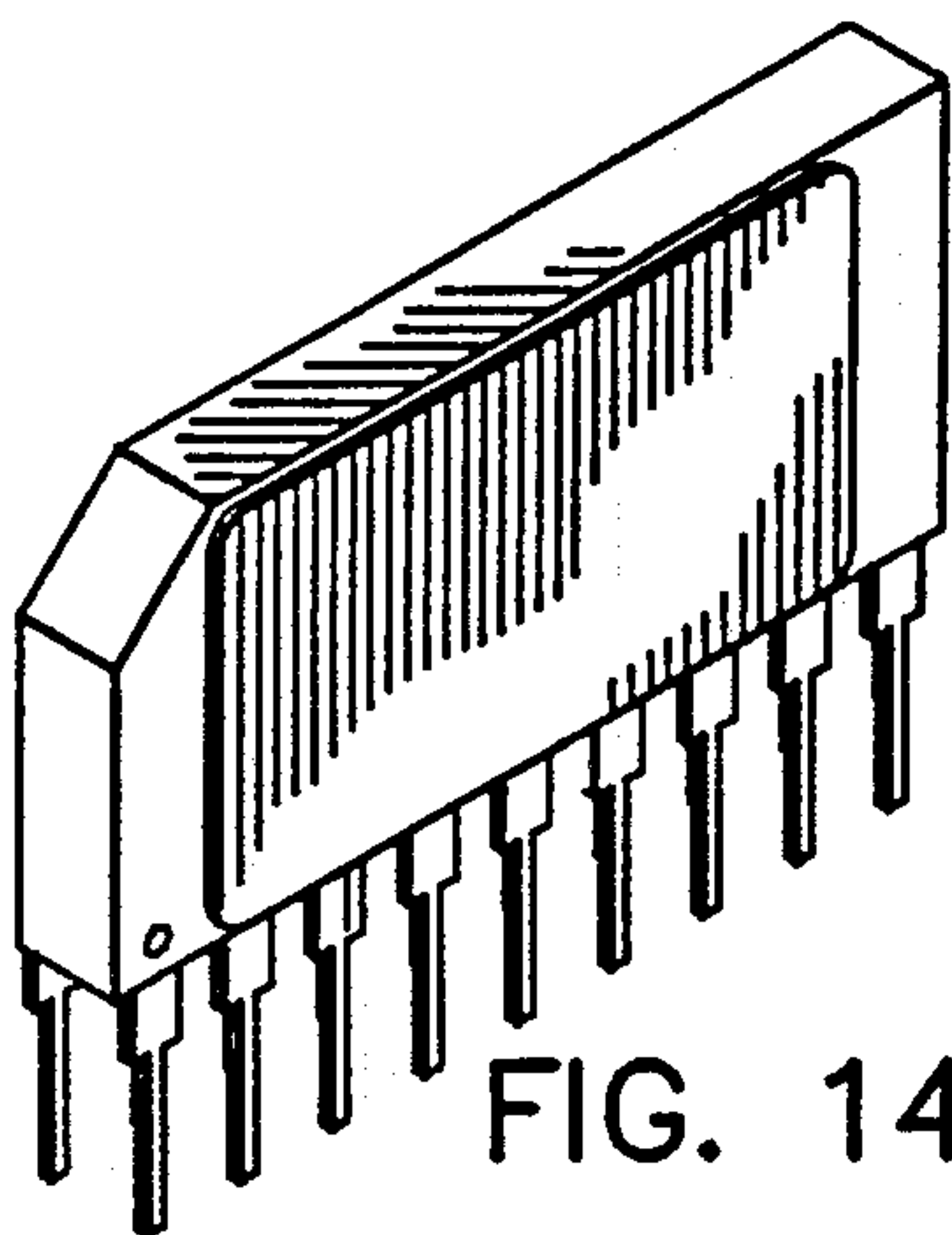


FIG. 14

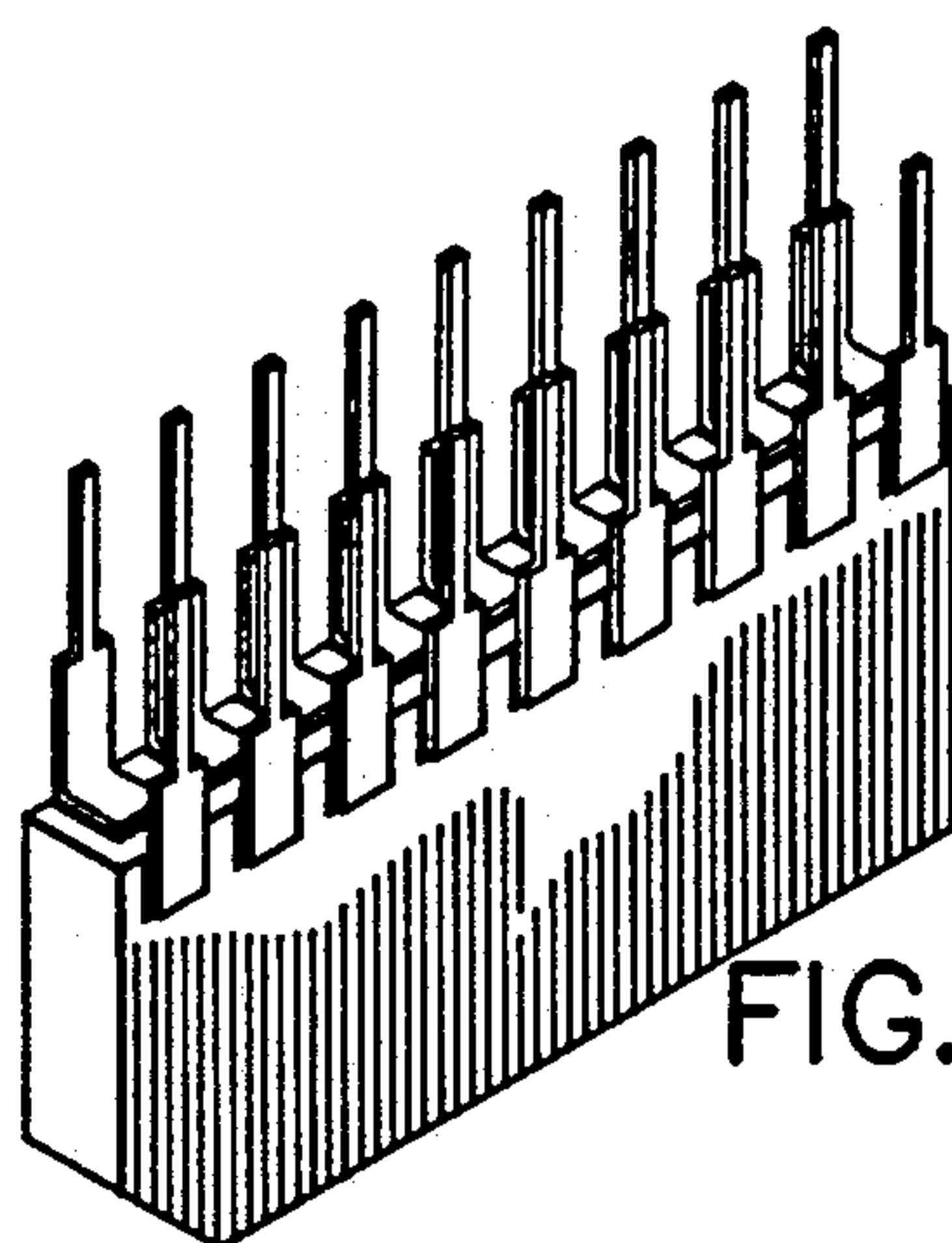


FIG. 15

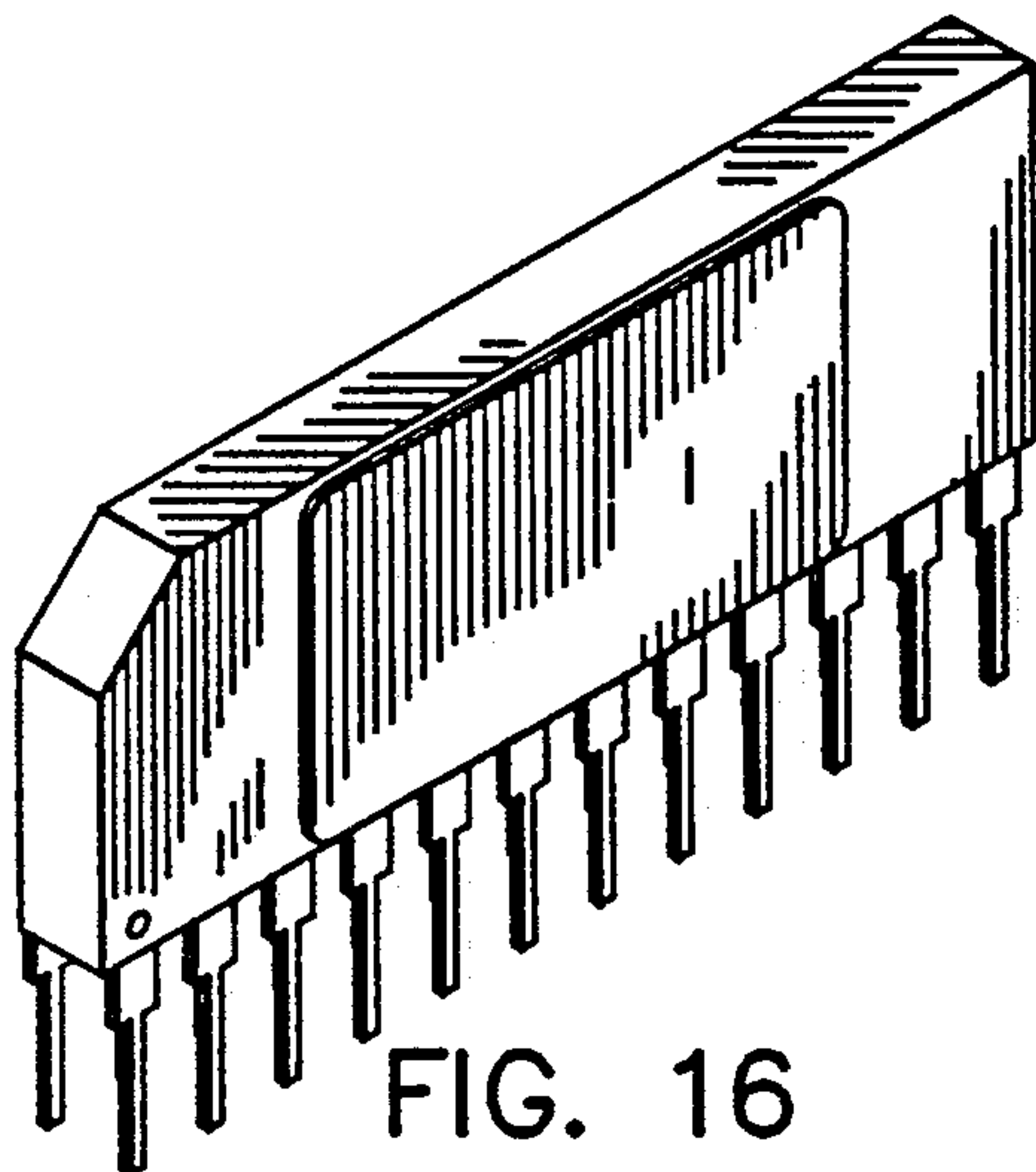


FIG. 16

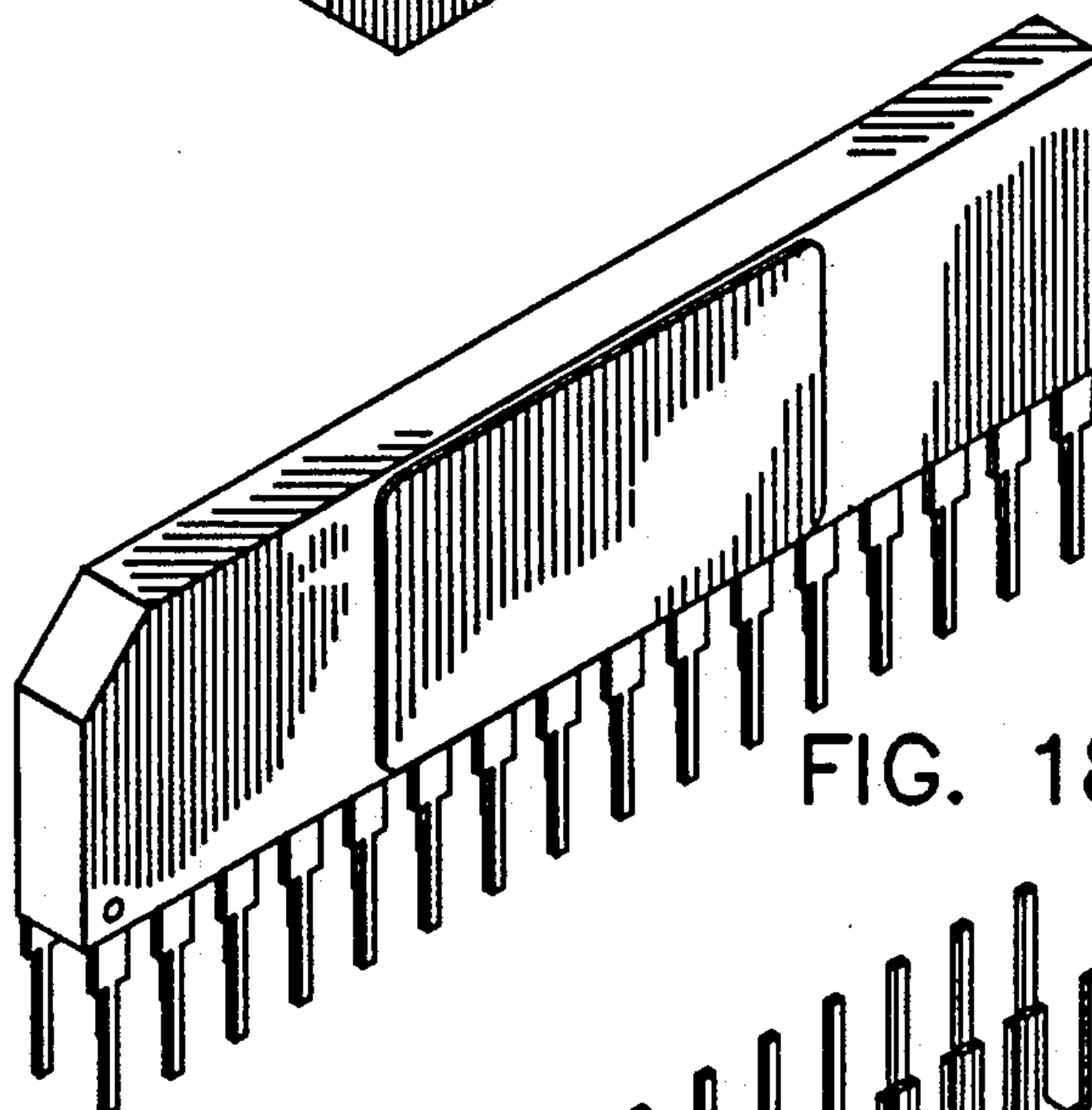


FIG. 18

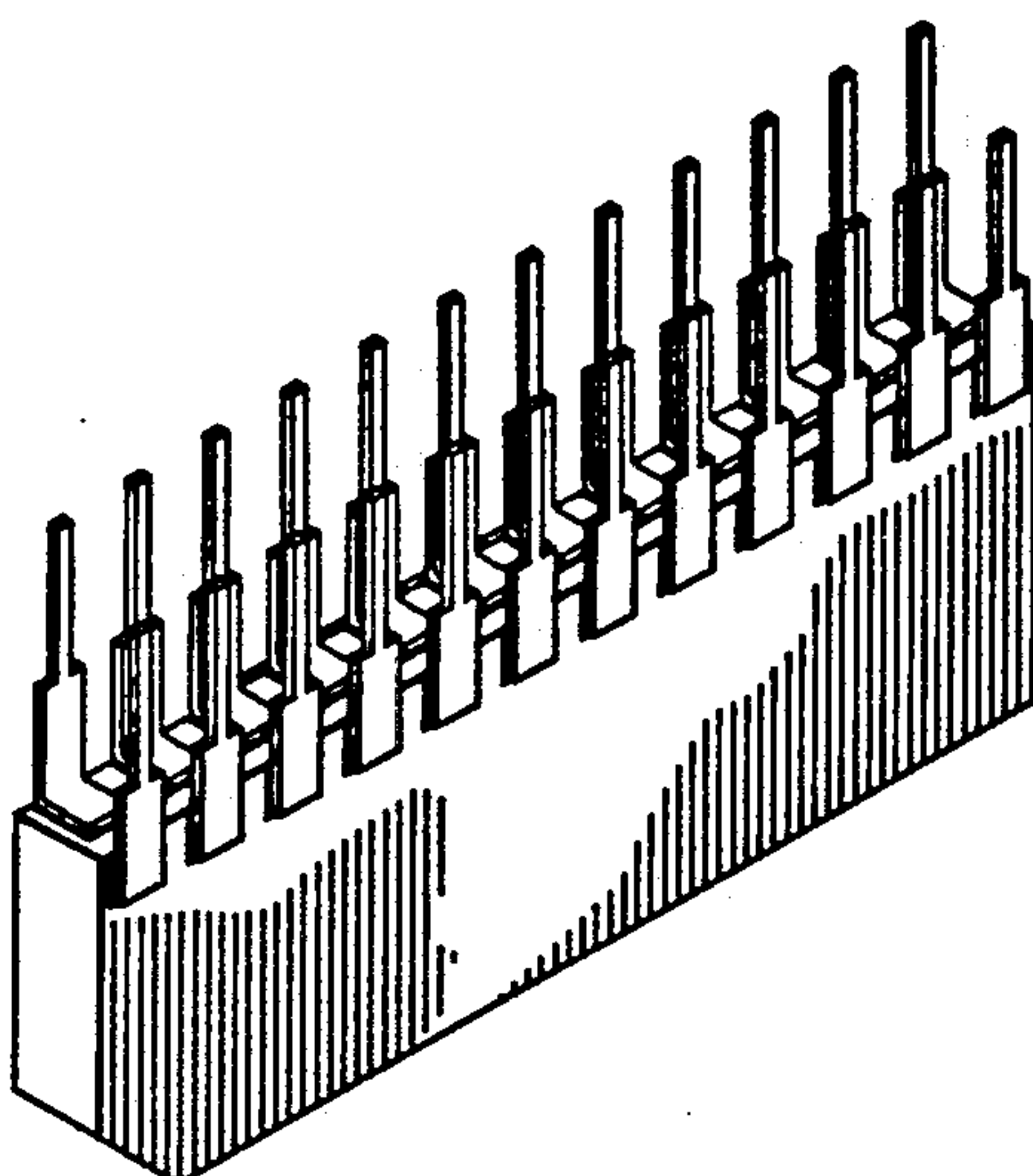


FIG. 17

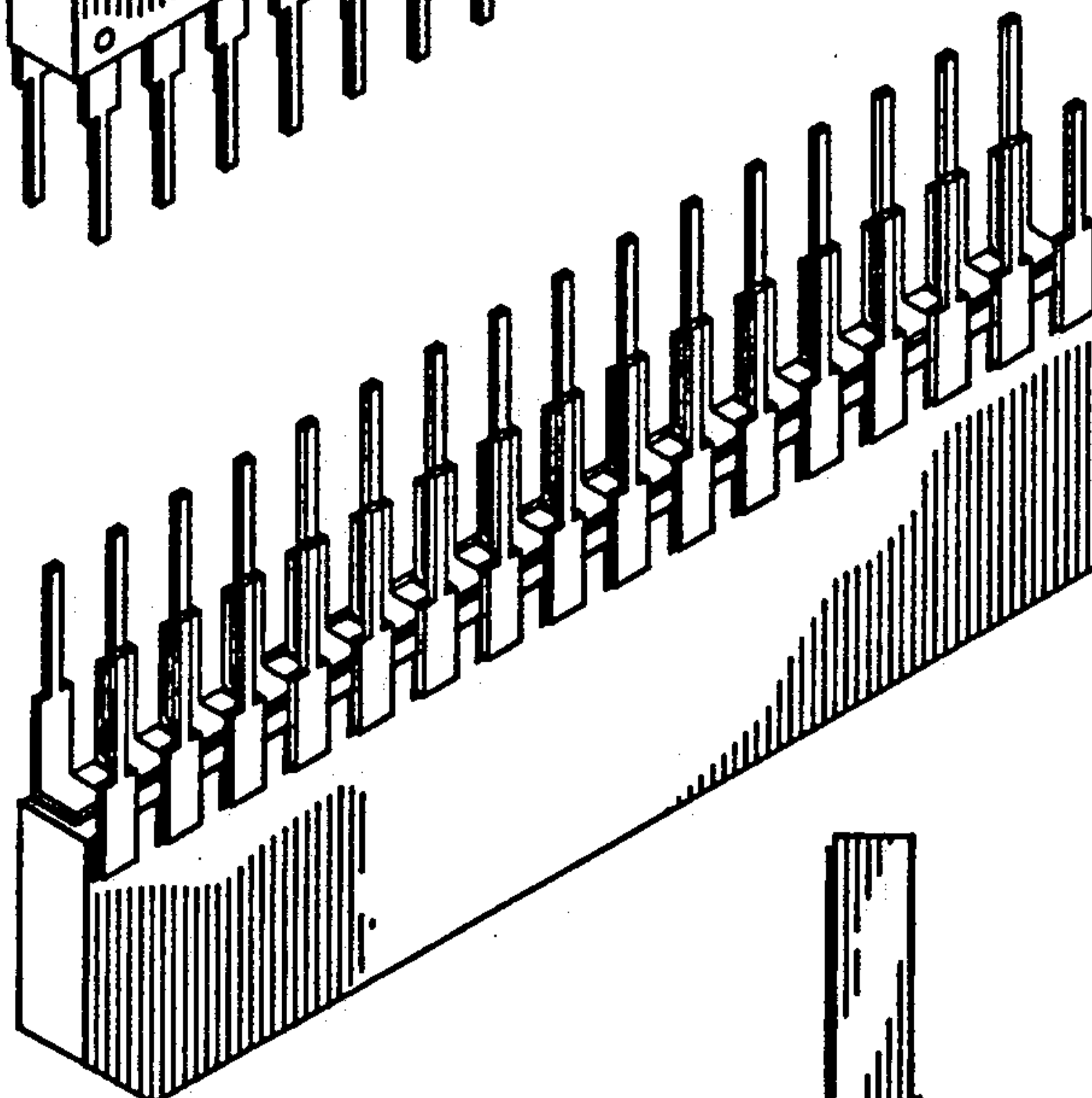


FIG. 19



FIG. 20