

United States Patent [19]

Imamura et al.

[11] Patent Number: **Des. 316,084**

[45] Date of Patent: **** Apr. 9, 1991**

[54] **ARITHMETIC PROCESSOR FOR USE IN ELECTRONIC COMPUTERS**

[75] Inventors: **Tetsuya Imamura; Benito Mishiro**, both of Osaka; **Yoshihiko Sugiyama**, Nara, all of Japan

[73] Assignees: **Matsushita Electric Industrial Co., Ltd.**, Japan; **Solutions Are Everything, Inc.**, Colo.

[**] Term: **14 Years**

[21] Appl. No.: **179,127**

[22] Filed: **Apr. 8, 1988**

[30] **Foreign Application Priority Data**

Dec. 15, 1987 [JP] Japan 62-51131

[52] U.S. Cl. **D14/102**

[58] Field of Search D14/102, 100, 109; 361/390-395

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 169,684 5/1953 Kress et al. D14/109
D. 245,159 7/1977 Hardy D14/102
D. 247,810 5/1978 Moeckl D14/102

D. 250,019 10/1978 Pycha et al. D14/102
D. 293,111 12/1987 Nezu D14/102
D. 303,375 9/1989 Sellars, Jr. et al. D14/102

Primary Examiner—Carmen H. Vales-Lado
Attorney, Agent, or Firm—Stevens, Davis, Miller & Mosher

[57] CLAIM

The ornamental design for an arithmetic processor for use in electronic computers, as shown and described.

DESCRIPTION

FIG. 1 is a front elevational view of an arithmetic processor for use in electronic computers showing our new design;

FIG. 2 is a top plan view;

FIG. 3 is a rear elevational view;

FIG. 4 is a bottom view;

FIG. 5 is a right side elevational view;

FIG. 6 is a front, top and right side perspective view;

FIG. 7 is a sectional view taken along line 7—7 of FIG. 1; and

FIG. 8 is a sectional view taken along line 8—8 of FIG. 1.

The internal mechanism removed in FIGS. 7 and 8 for convenience of illustration.

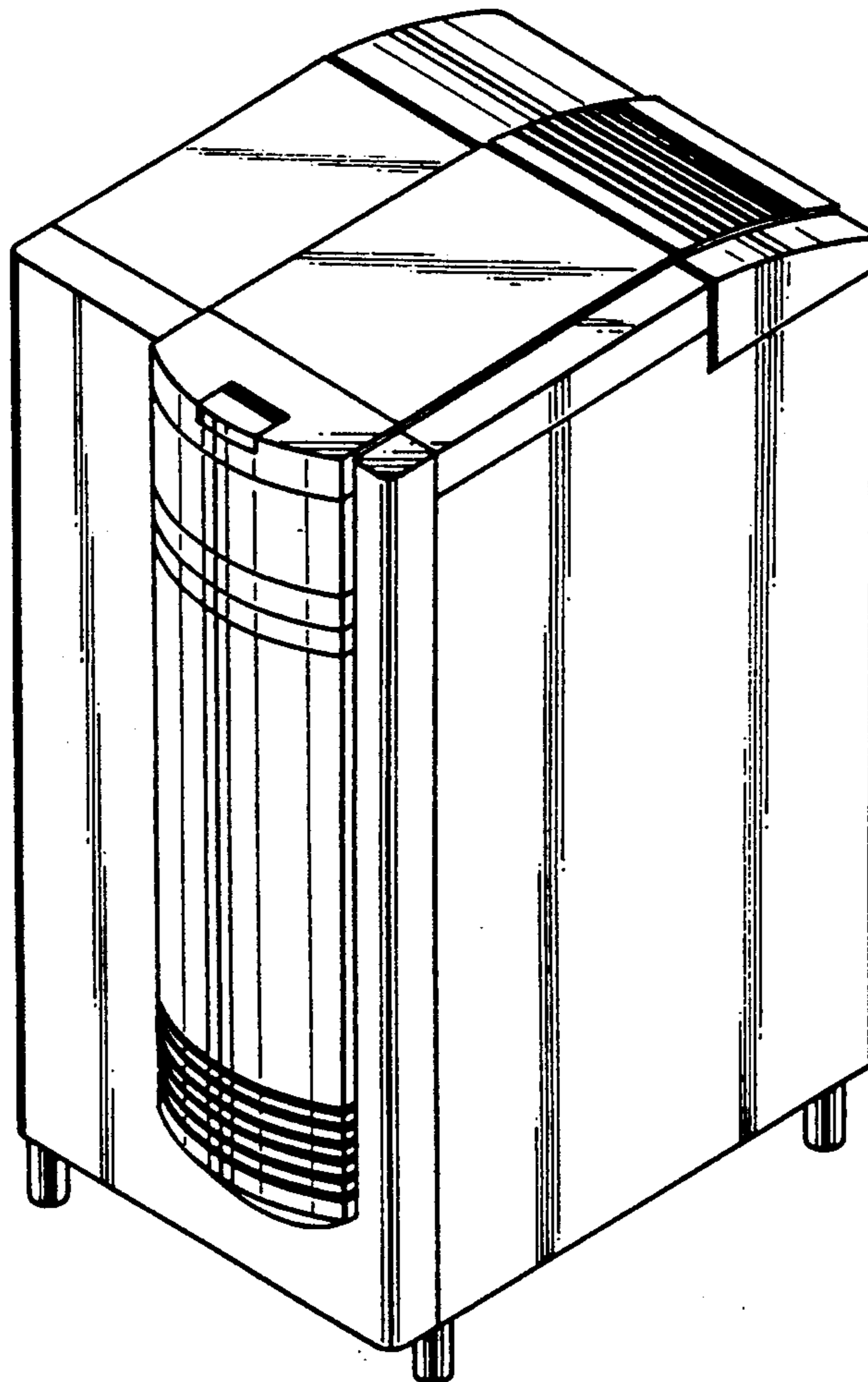


FIG. 1

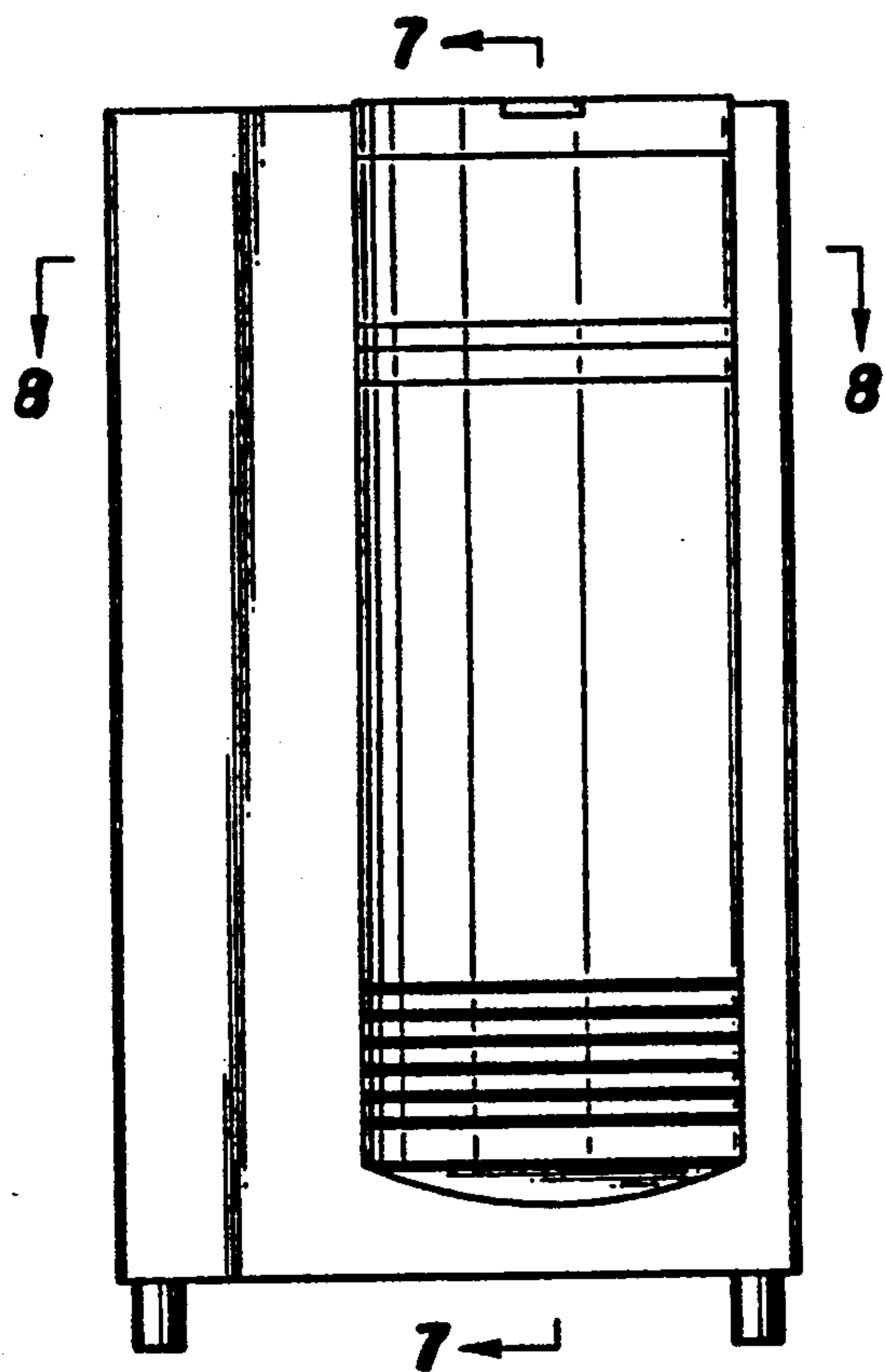


FIG. 2

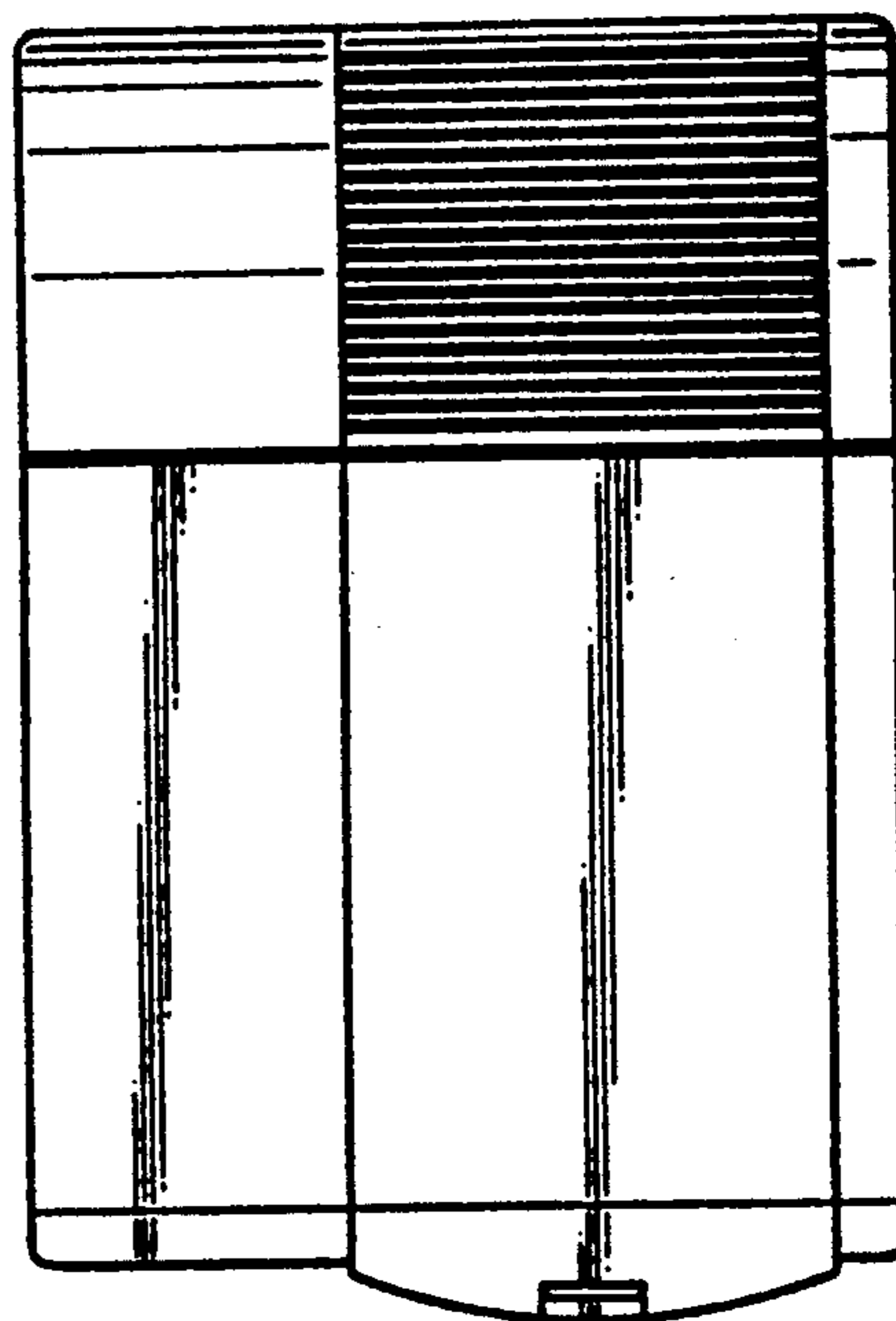


FIG. 3

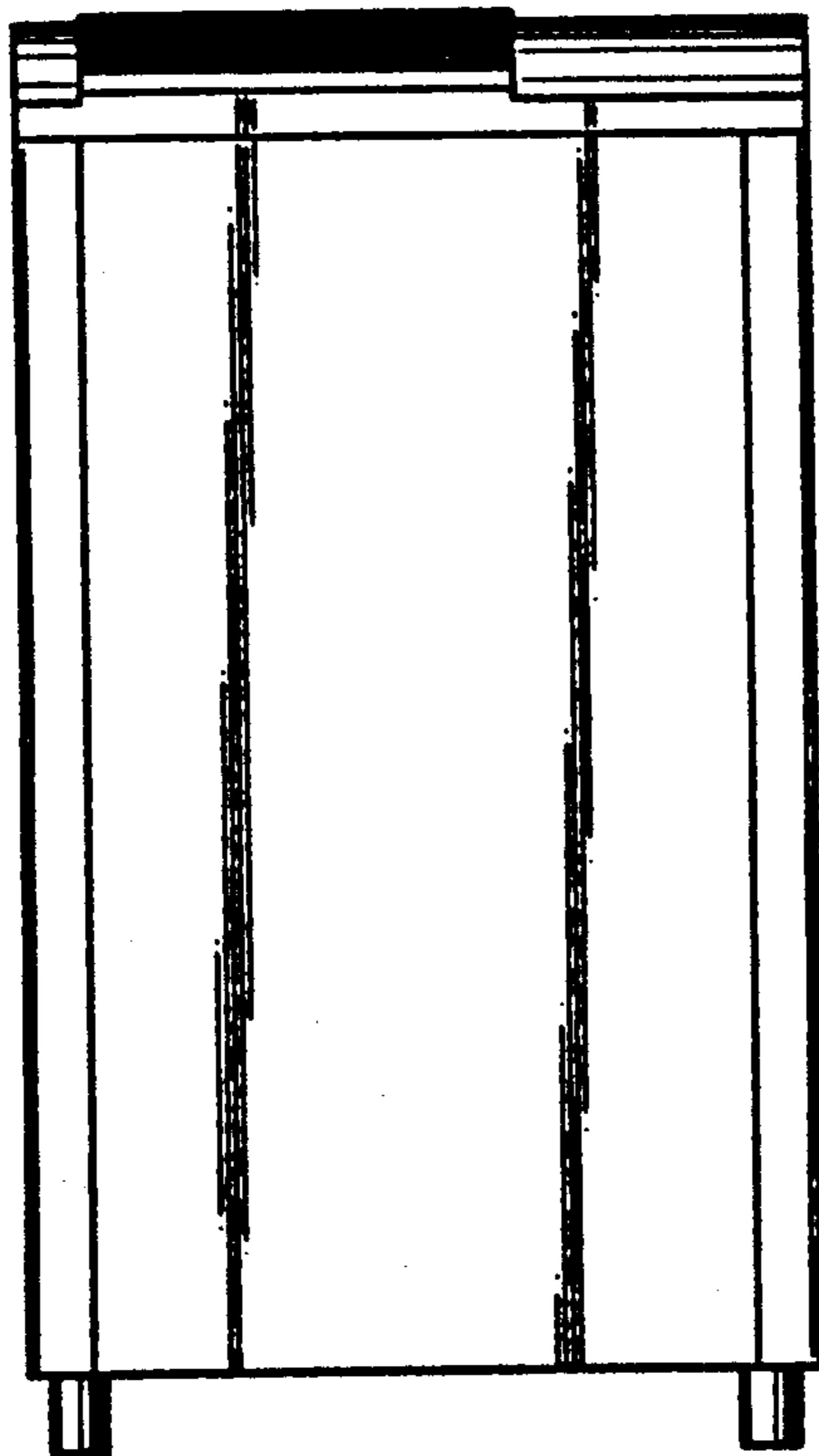


FIG. 4

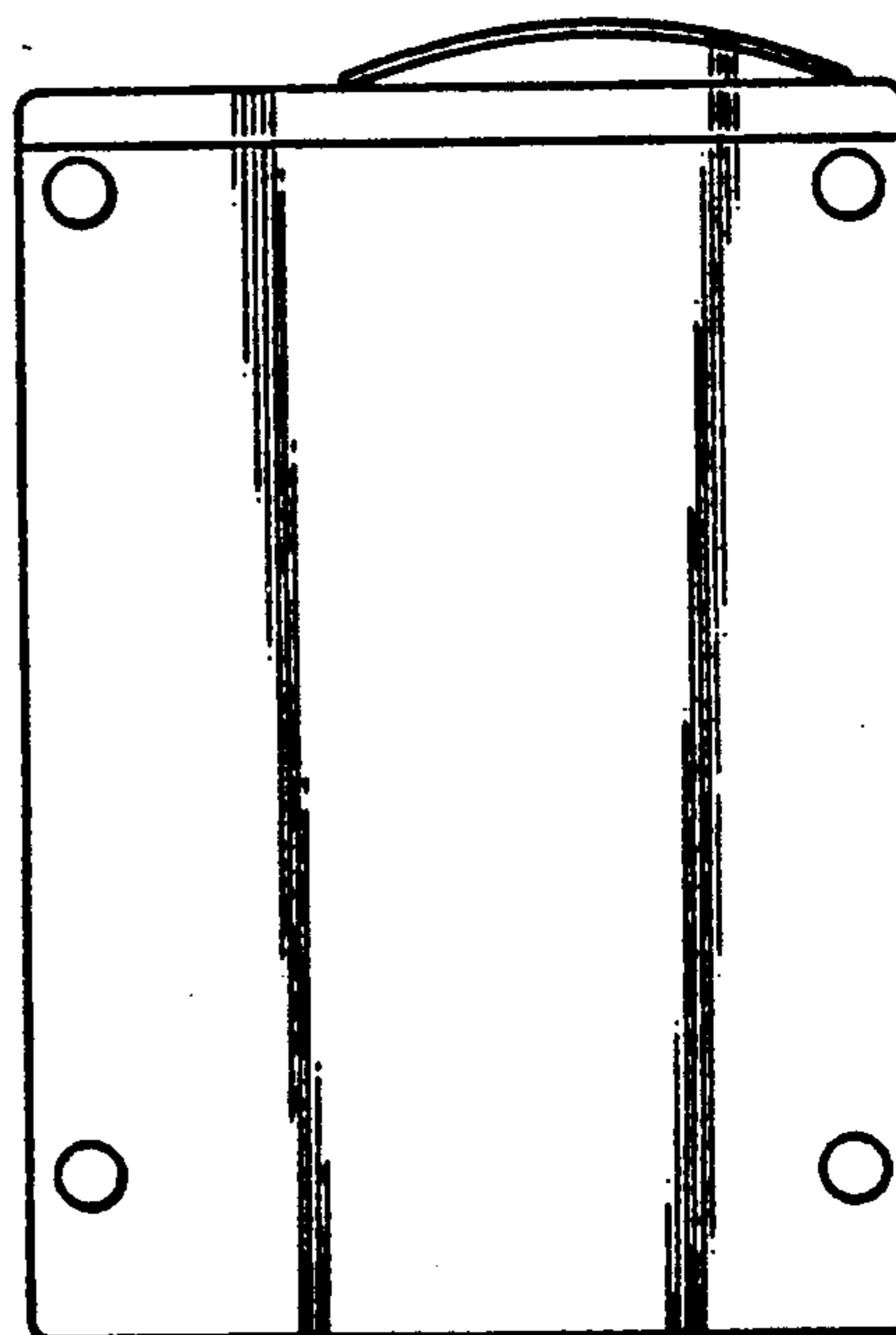


FIG. 6

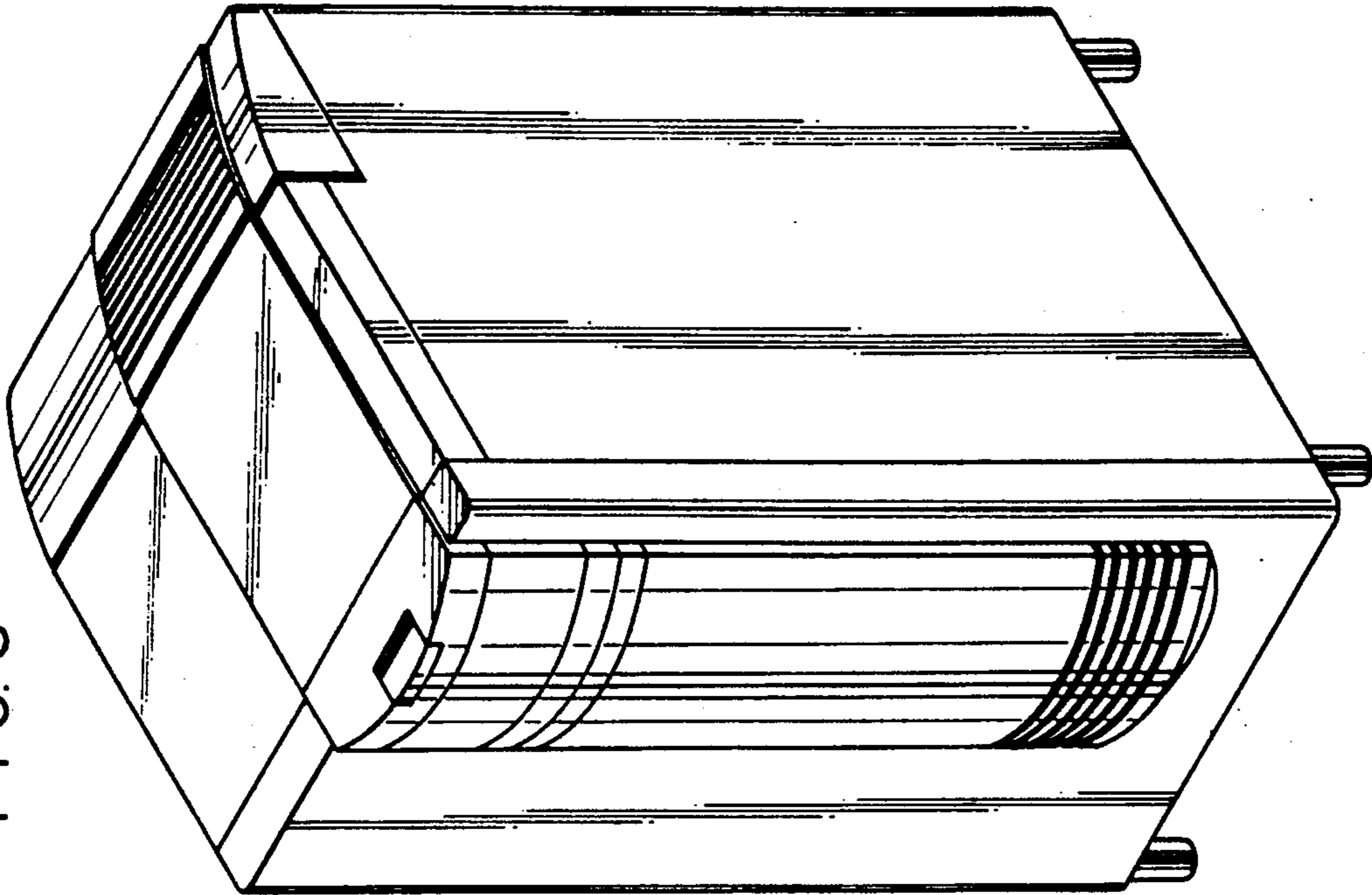


FIG. 5

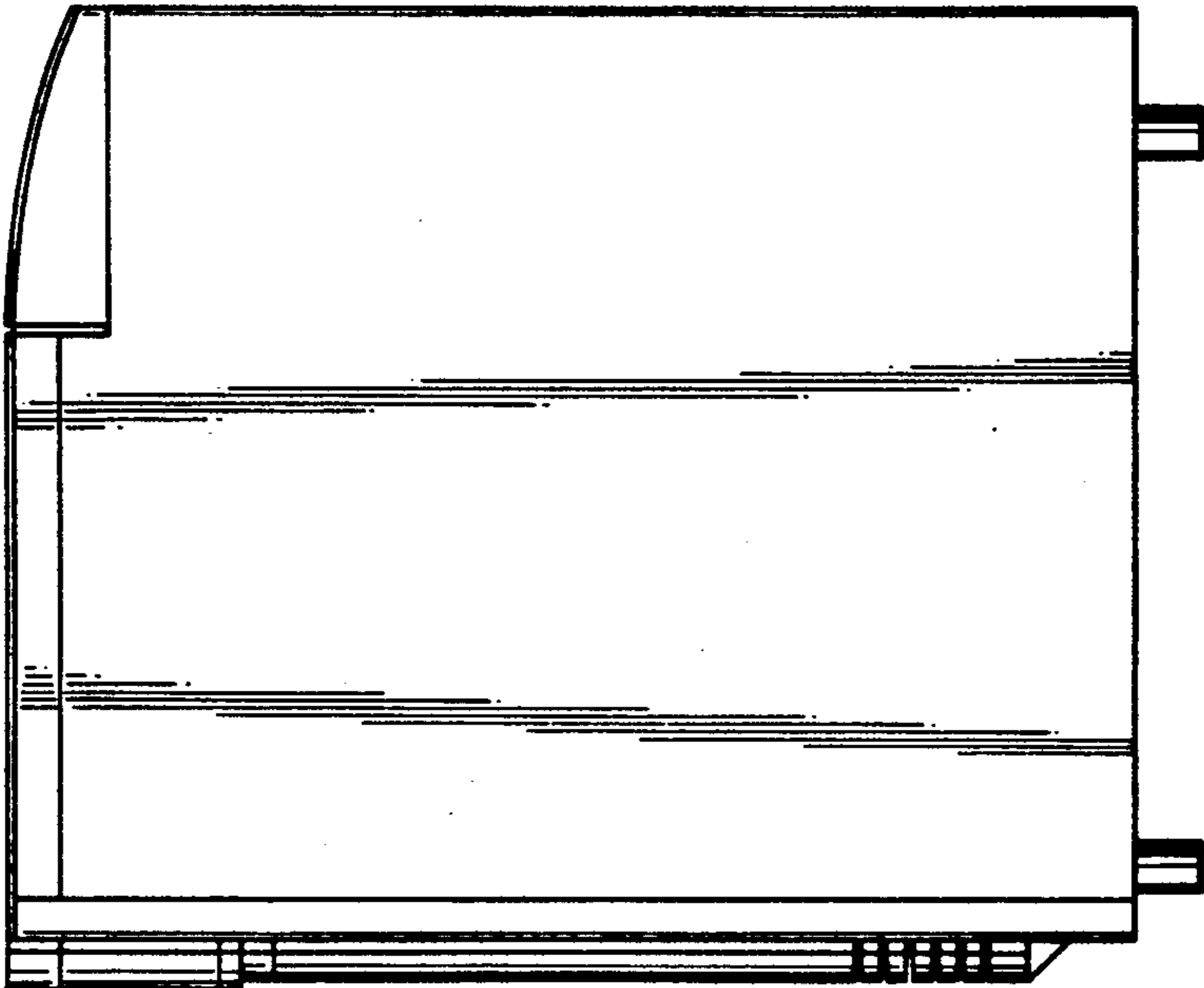


FIG. 7

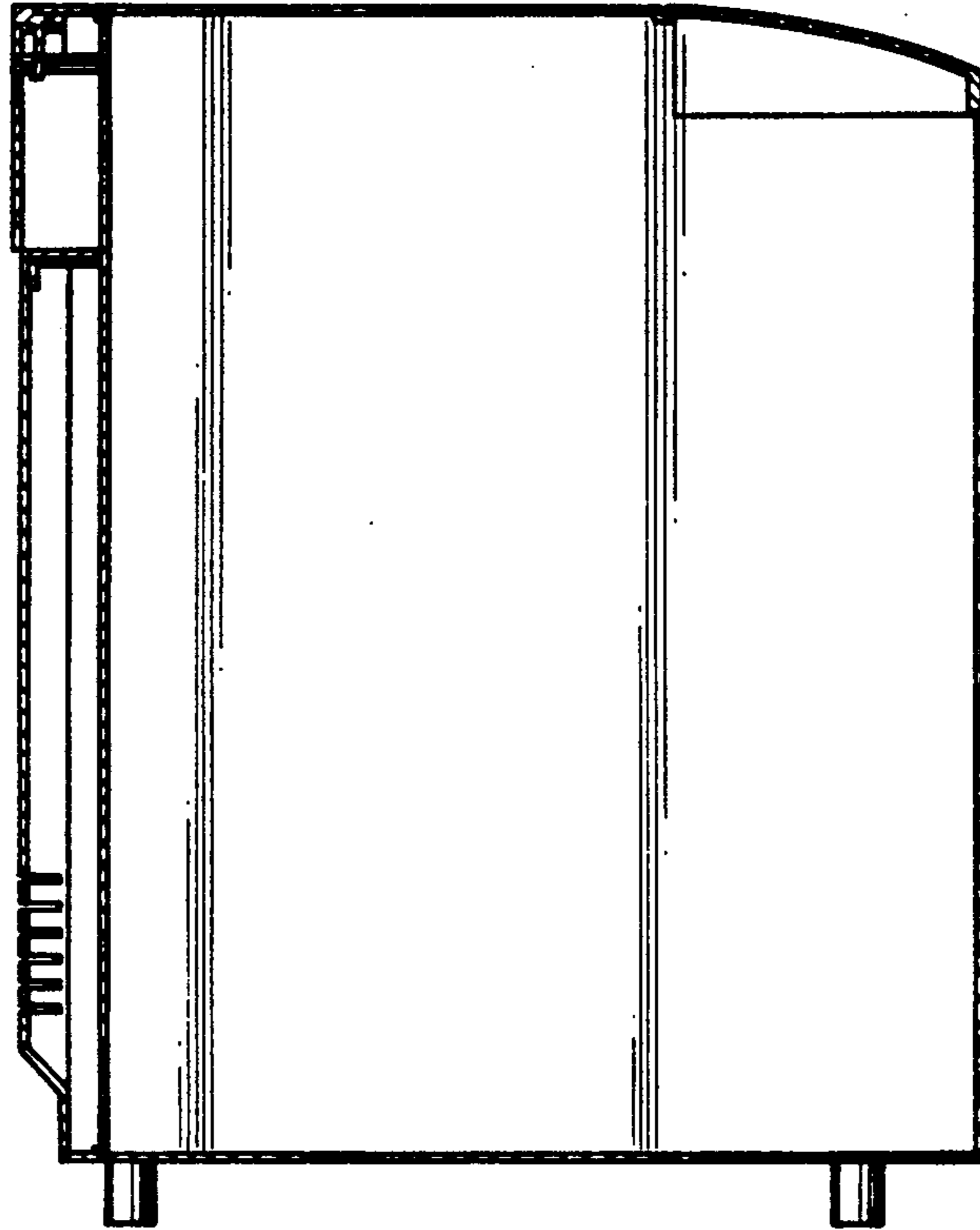


FIG. 8

