# United States Patent [19]

## Fitzpatrick et al.

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### LATCHING/EJECTING LEVERS FOR ELECTRONIC CIRCUIT BOARD

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14 Years Term:

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U.S. Cl. ...... D13/99

[58] D13/20, 23-31, 99; D8/382, 395; 248/74.5; 339/17 LC, 45 R, 45 M; 361/415, 399; 211/41

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[57] **CLAIM** 

The ornamental design for a latching/ejecting lever for

electronic circuit board, substantially as shown and described.

#### DESCRIPTION

FIG. 1 is a front perspective view of a first embodiment of a latching ejecting lever for an electronic circuit board showing our new design, the circuit board being fragmentarily shown in broken lines for illustrative purposes only;

FIG. 2 is a bottom plan view thereof on an enlarged scale;

FIG. 3 is a top plan view thereof on an enlarged scale; FIG. 4 is a right side elevational view thereof on an enlarged scale;

FIG. 5 is a front elevational view thereof on an enlarged scale;

FIG. 6 is a left side elevational view thereof on an enlarged scale;

FIG. 7 is a rear elevational view thereof on an enlarged scale;

FIG. 8 is a front perspective view of a second embodiment of our new design, the circuit board being fragmentarily shown in broken lines for illustrative purposes only;

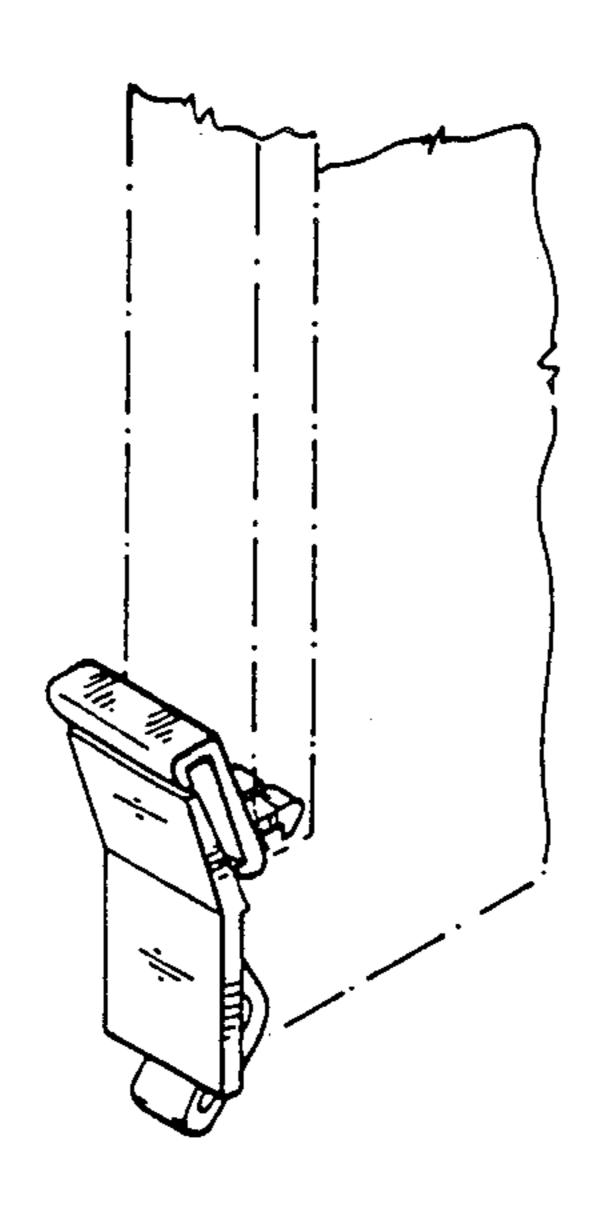
FIG. 9 is a top plan view thereof on an enlarged scale; FIG. 10 is a bottom plan view thereof on an enlarged scale;

FIG. 11 is an inverted left side elevational view thereof on an enlarged scale;

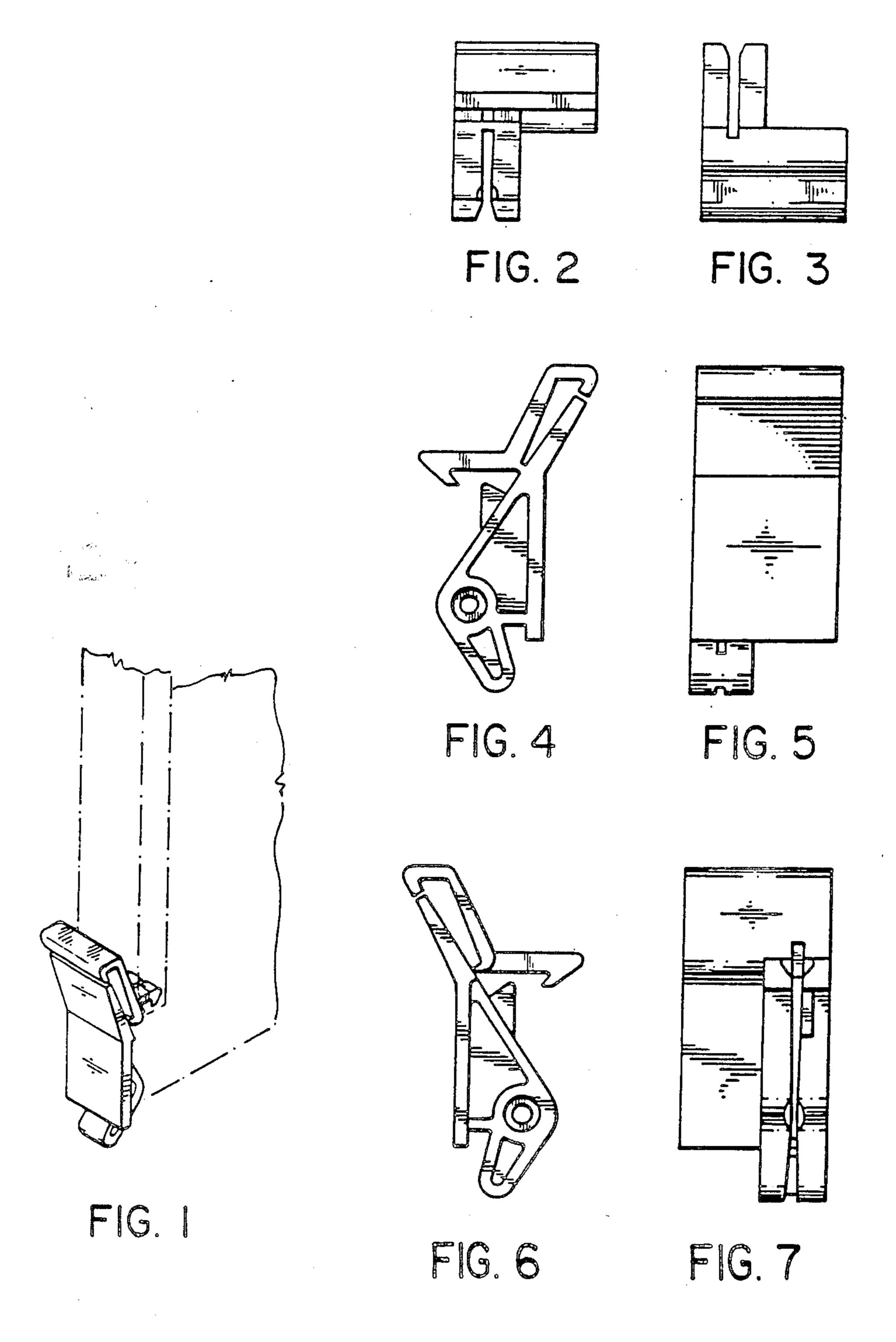
FIG. 12 is an inverted front elevational view thereof on an enlarged scale;

FIG. 13 is an inverted right side elevational view thereof on an enlarged scale;

FIG. 14 is an inverted rear elevational view thereof on an enlarges scale.



Apr. 26, 1988



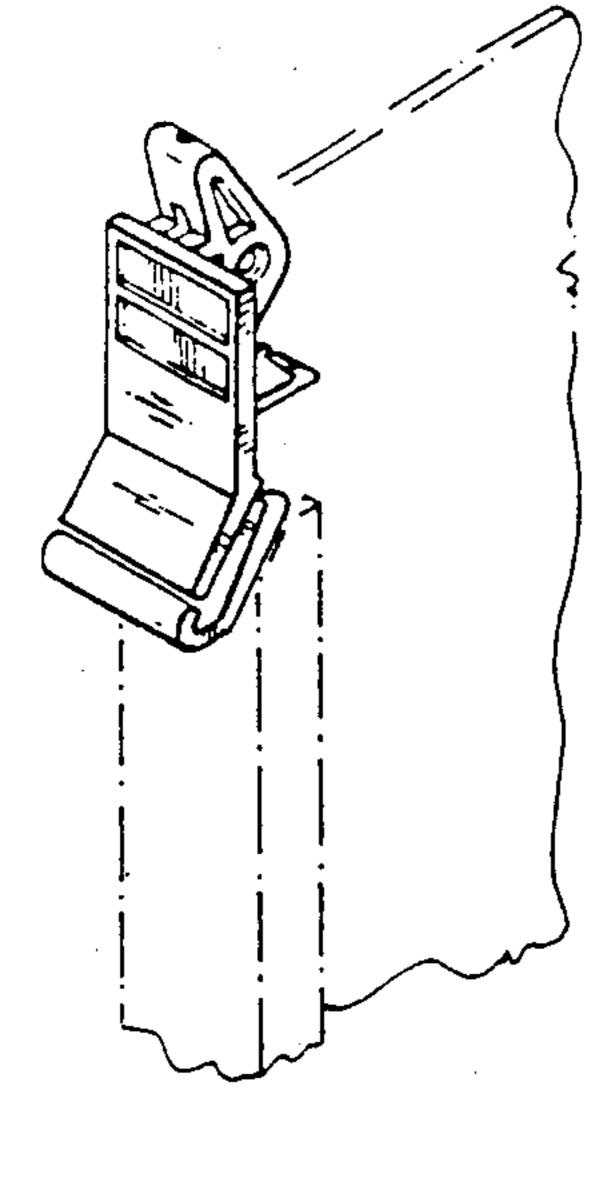


FIG.8

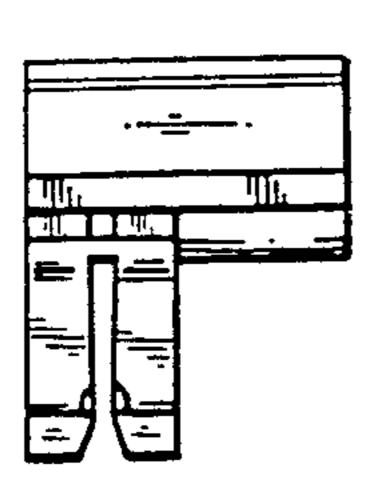


FIG.9

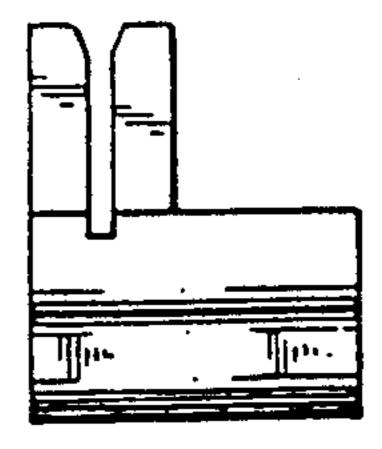


FIG.10

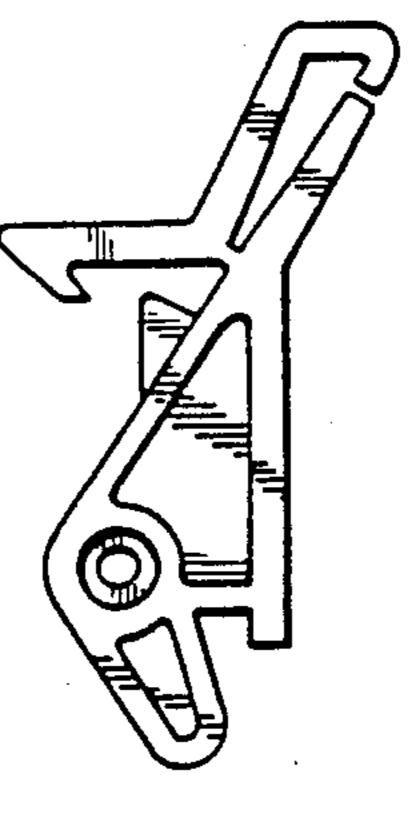
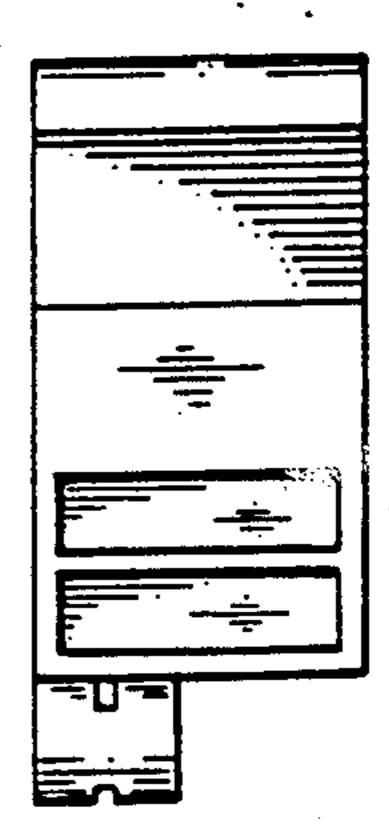
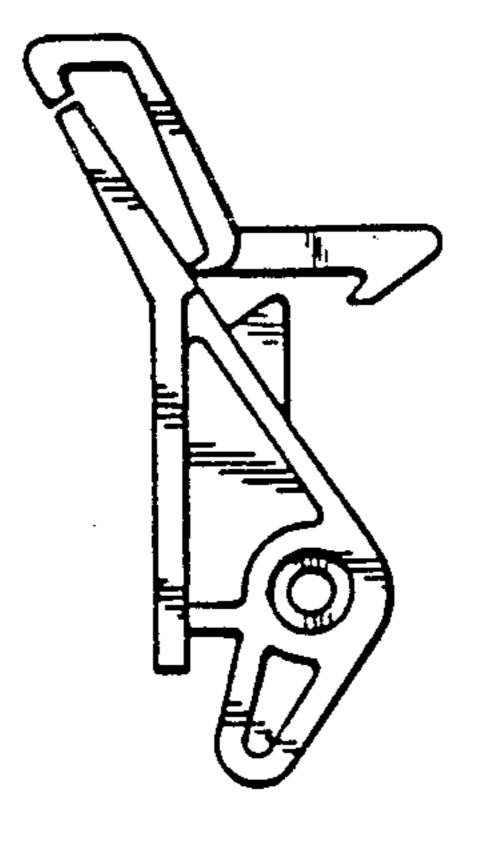


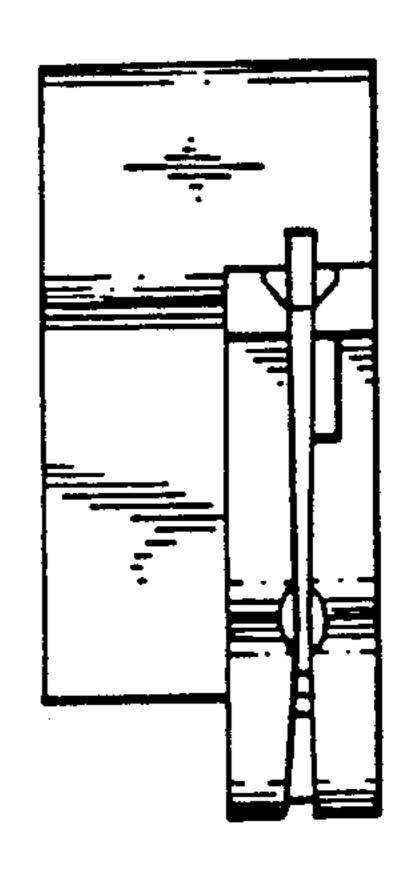
FIG. 11



F1G.12



F1G.13



F1G.14