United States Patent [19]

Chow

[11] **Patent Number: Des. 292,979**

[45] **Date of Patent: ** Dec. 1, 1987**

[54] **AUTOMATIC SEMICONDUCTOR WAFER TESTER**

[75] Inventor: **Marland Chow**, San Jose, Calif.

[73] Assignee: **Prometrix Corporation**, Santa Clara, Calif.

[**] Term: **14 Years**

[21] Appl. No.: **727,417**

[22] Filed: **Apr. 26, 1985**

[52] **U.S. Cl.** **D10/75**; D10/46

[58] **Field of Search** ..... D10/46, 75, 77, 78, D10/81, 102; 324/73 R, 73 AT, 73 PC, 158 F

[56] **References Cited**

U.S. PATENT DOCUMENTS

D. 173,618	12/1954	Hose	D10/78
D. 215,120	9/1969	Estes	D10/75 X
D. 276,315	11/1984	Collister	D10/46
D. 282,724	2/1986	Collister	D10/46
D. 283,107	3/1986	Collister	D10/46
4,348,636	9/1982	Doundoulakis	324/73 R
4,520,931	6/1985	Evain	324/73 AT X

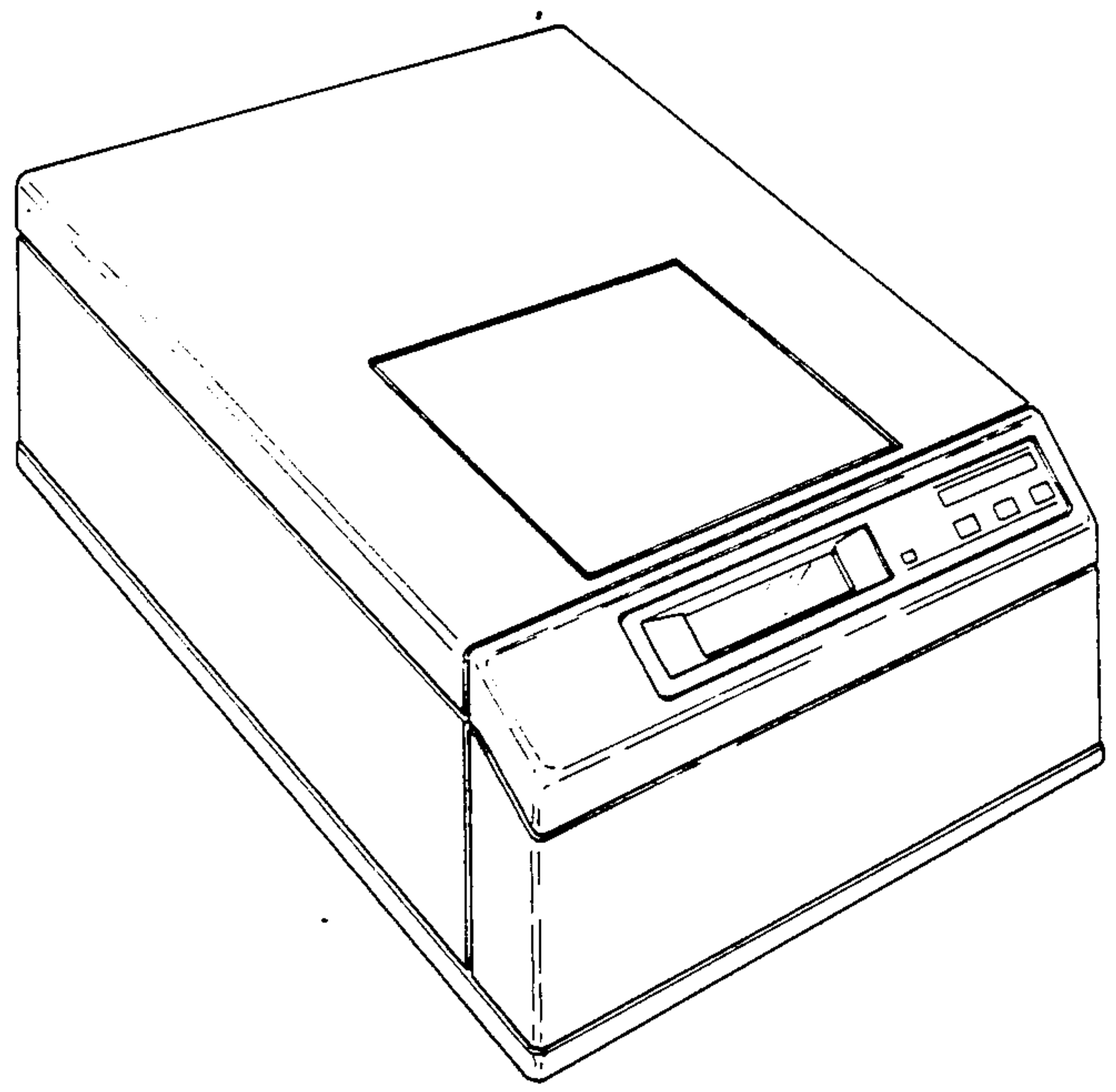
Primary Examiner—Nelson C. Holtje
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **CLAIM**

The ornamental design for an automatic semiconductor wafer tester, as shown.

DESCRIPTION

FIG. **1** is a top and left front perspective view of an automatic semiconductor wafer tester showing my new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a front elevational view thereof;
FIG. **4** is a rear elevational view thereof;
FIG. **5** is a left side elevational view thereof;
FIG. **6** is a right side elevational view thereof.



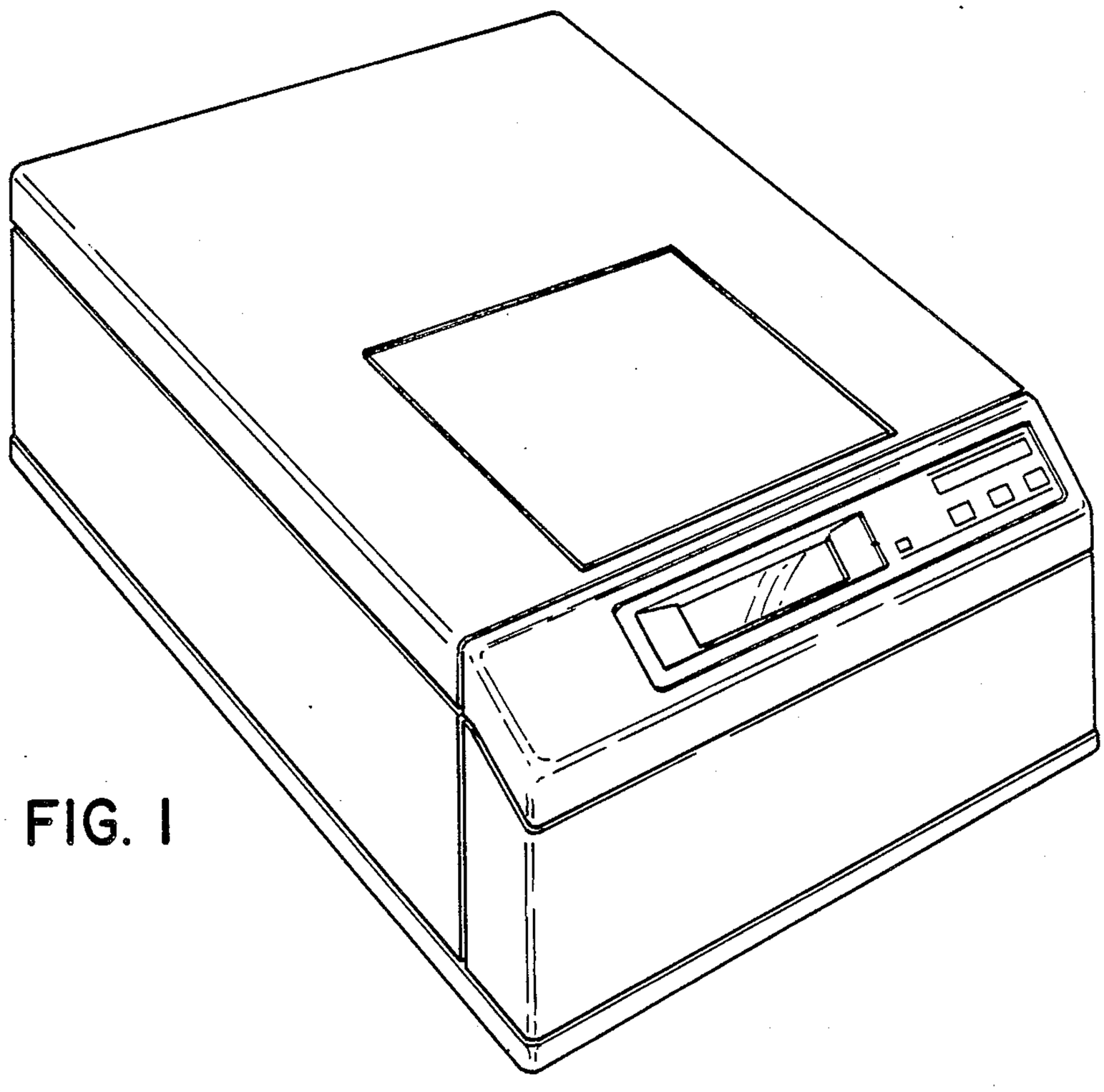


FIG. 1

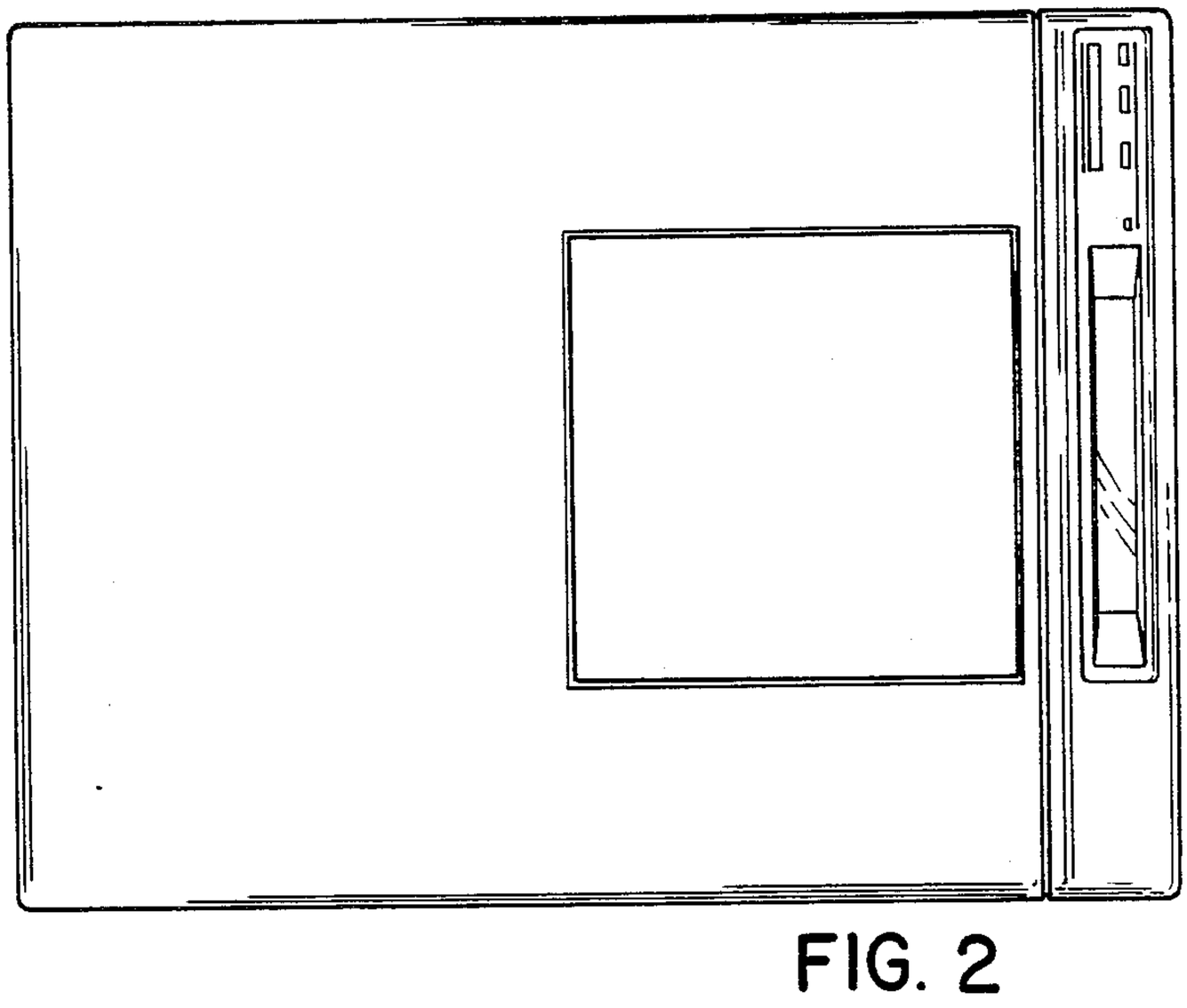


FIG. 2

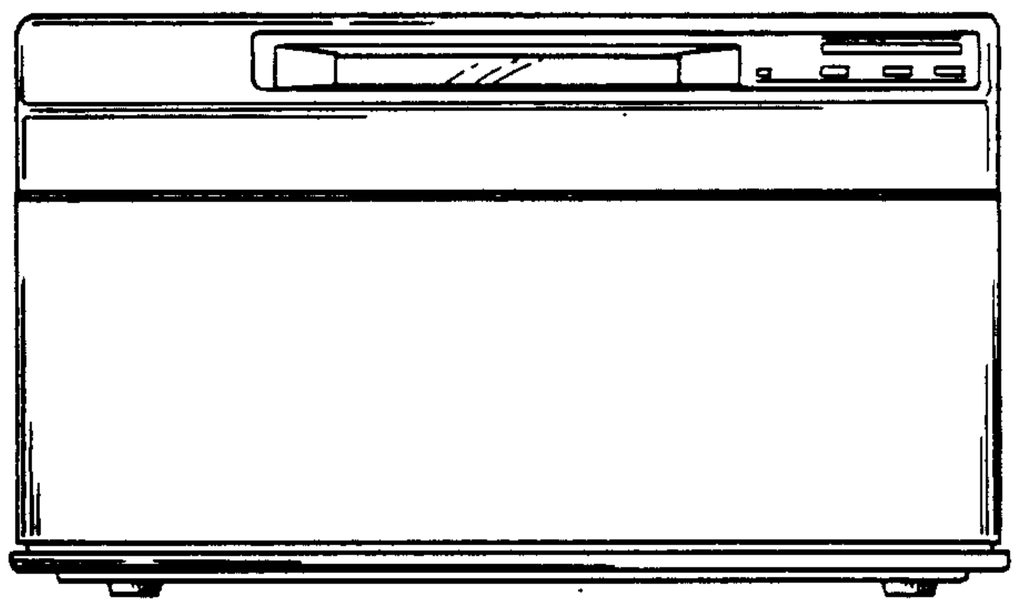


FIG. 3

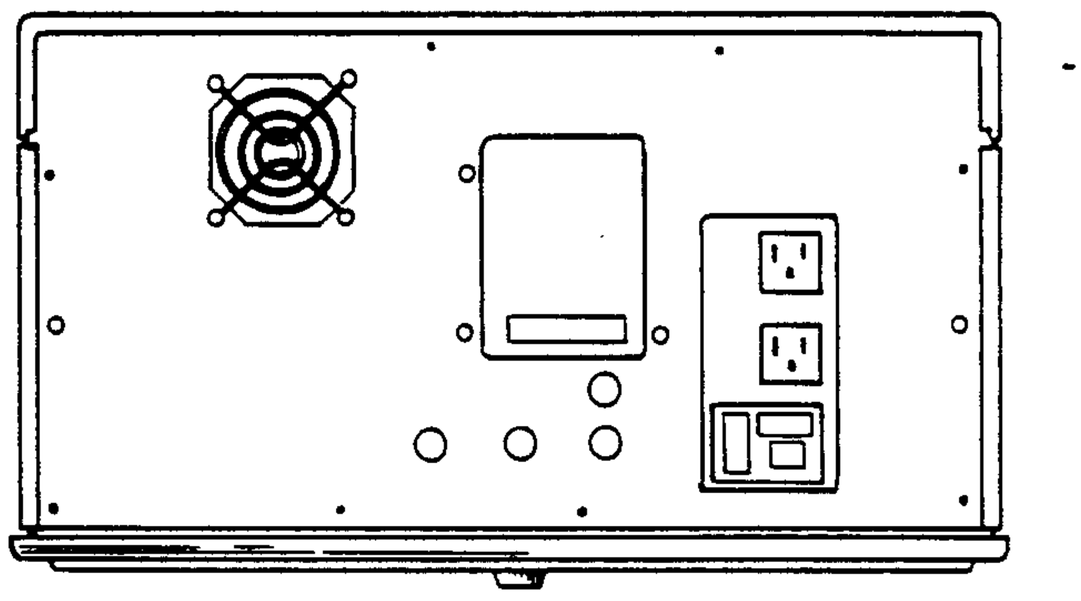


FIG. 4

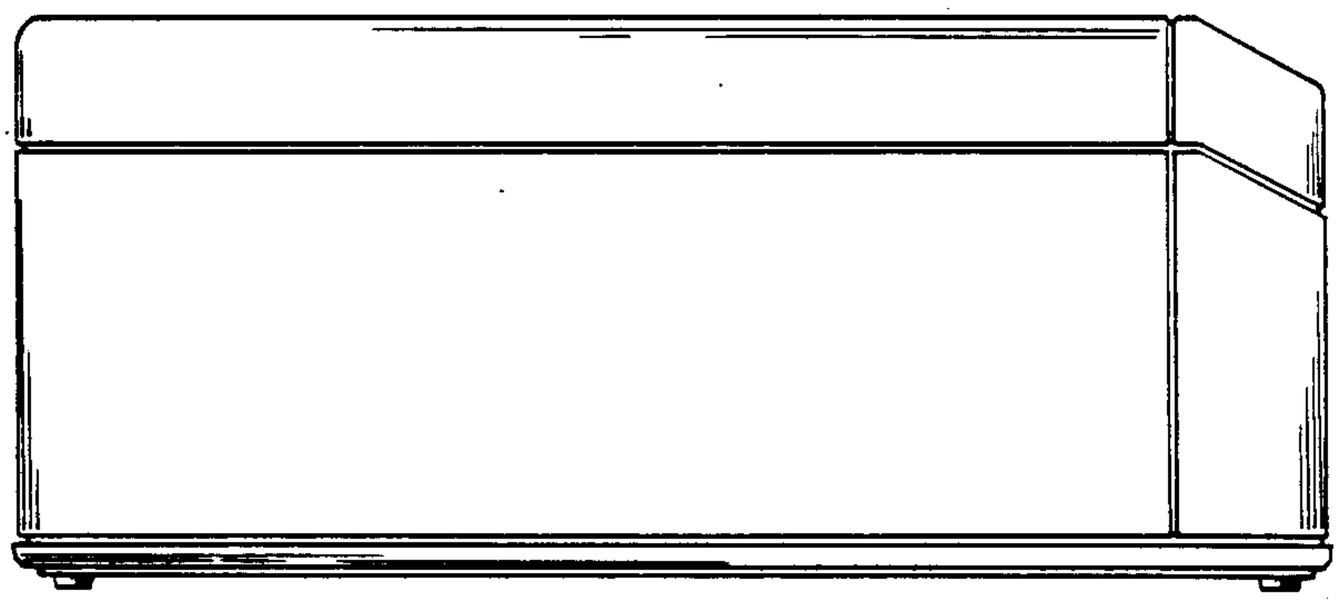


FIG. 5

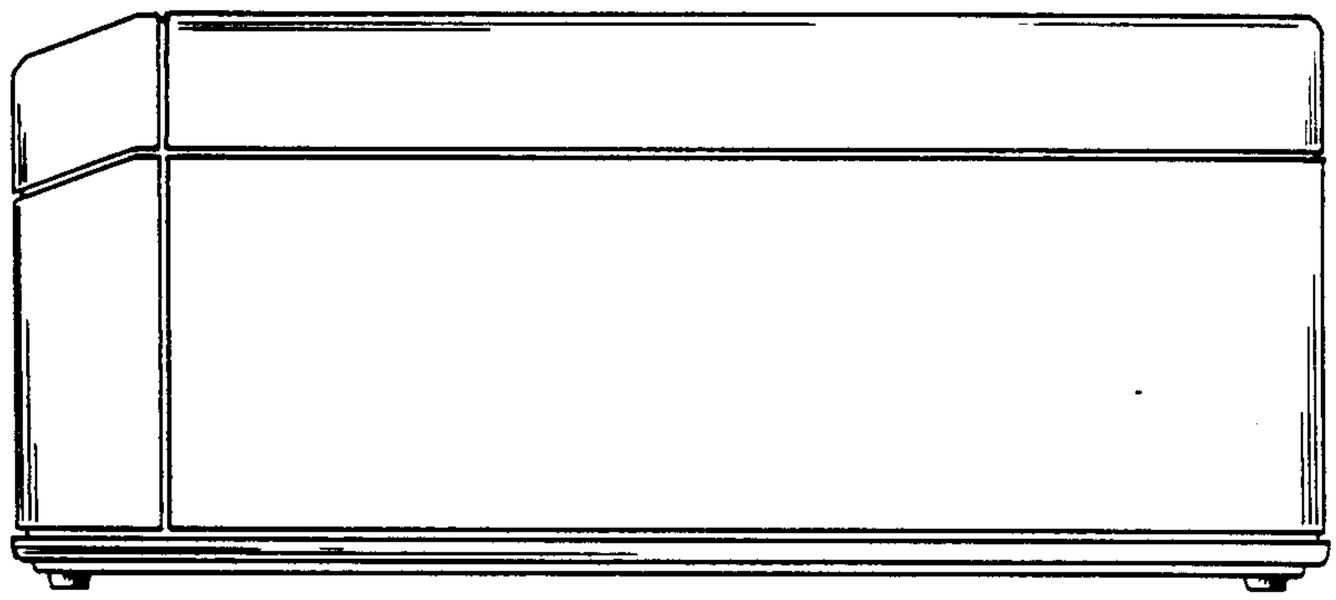


FIG. 6