United States Patent [19]

Dlugos

[11] **Des. 261,760**

[45] ** **Nov. 10, 1981**

[54] **ELECTRONIC POSTAL RATE MEMORY**

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[73] Assignee: **Pitney Bowes Inc.,** Stamford, Conn.

[**] Term: **14 Years**

[21] Appl. No.: **972,583**

[22] Filed: **Dec. 22, 1978**

[51] **Int. Cl.** ..... **D14—02;** D13—99

[52] **U.S. Cl.** **D14/114;** D13/99

[58] **Field of Search** ..... 339/17 R, 17 L, 45 R, 339/45 M; 361/399, 415; D13/99; D14/40

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,017,232	1/1962	Schwab et al.	339/45 M
3,798,507	3/1974	Damon et al.	361/415
3,952,232	4/1976	Coules	361/415

OTHER PUBLICATIONS

Electronics, 2-17-77, p. 22-Circuit Board with Ejector Handle.

Electronics, 4-28-77, p. 99, top right, Memory Board.

Vero Bulletin, 6-71, Card Ejector.

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[57] **CLAIM**

The ornamental design for an electronic postal rate memory, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of an electronic postal rate memory showing my new design;

FIG. **2** is a front elevational view thereof on a reduced scale;

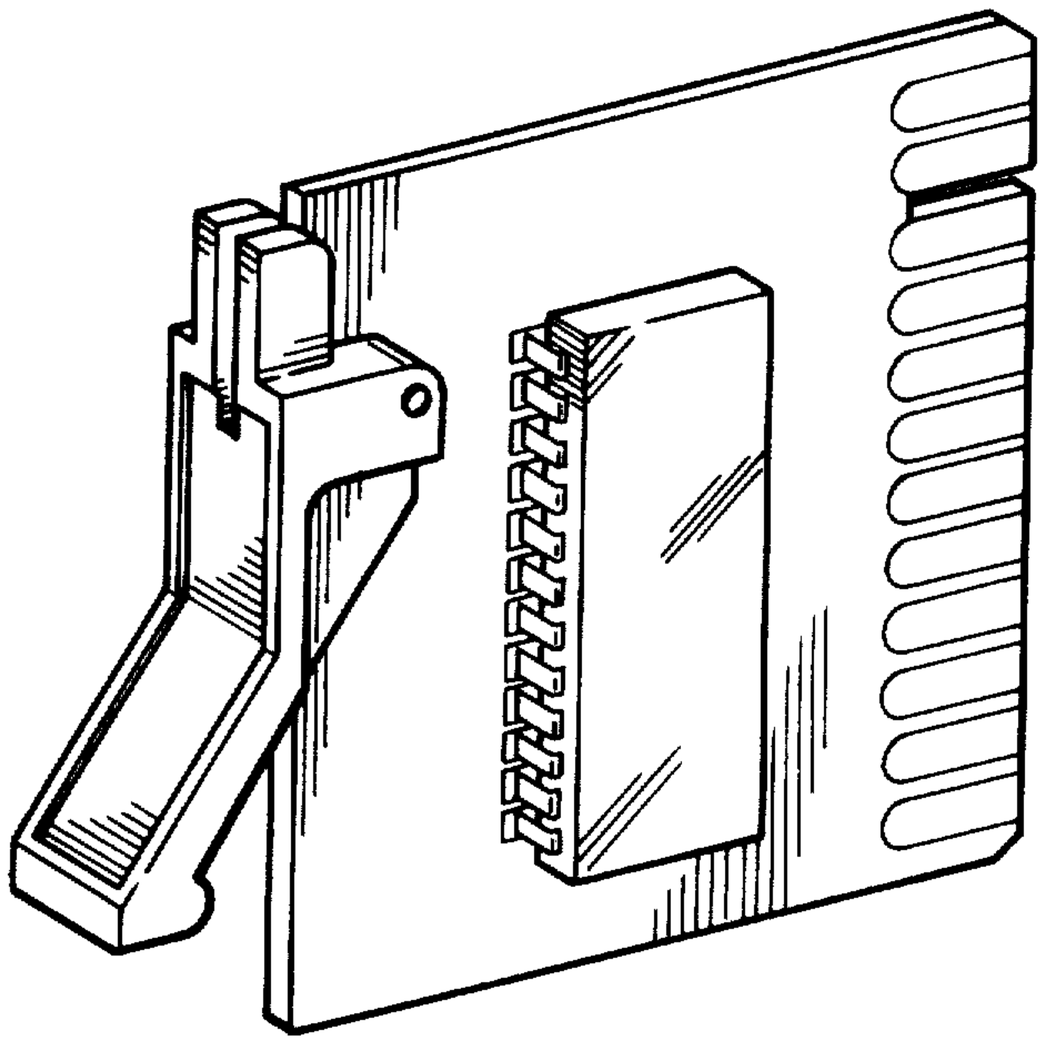
FIG. **3** is a top plan view thereof on a reduced scale;

FIG. **4** is a bottom view thereof on a reduced scale;

FIG. **5** is a rear elevatioal view thereof on a reduced scale;

FIG. **6** is a left side elevational view thereof on a reduced scale;

FIG. **7** is a right side elevational view thereof on a reduced scale.



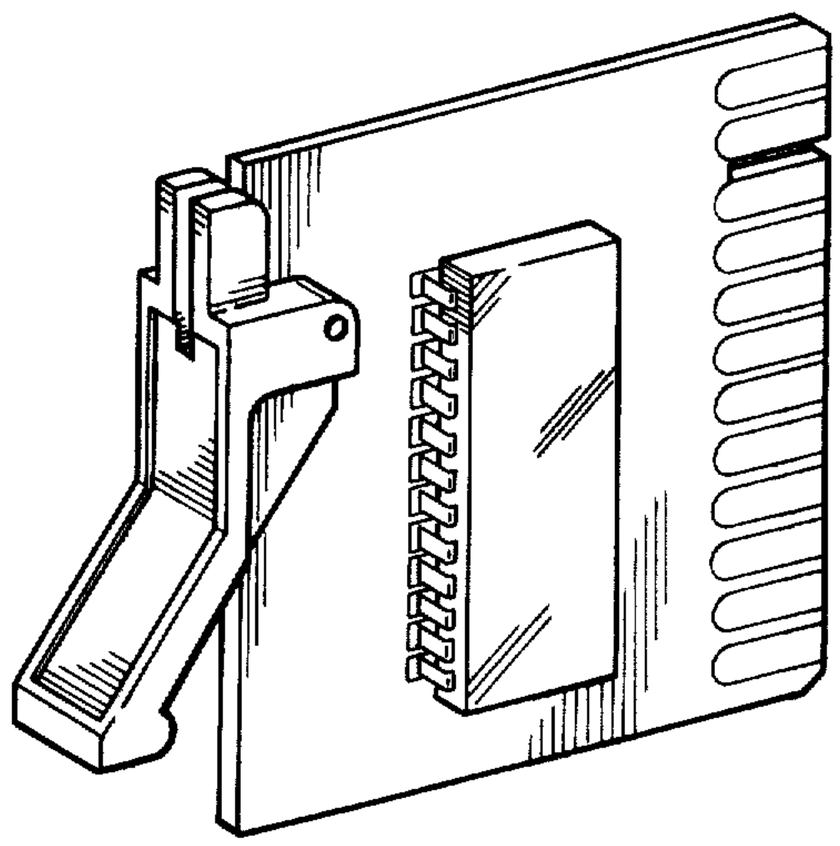


Fig. 1

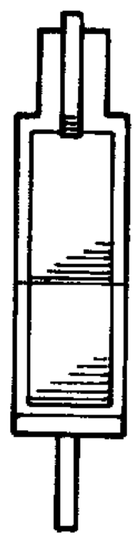


Fig. 6

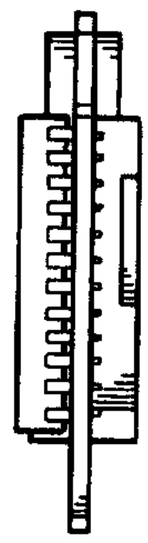


Fig. 7

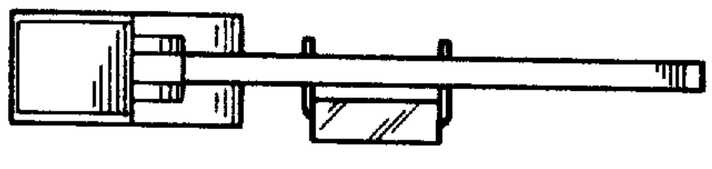


Fig. 3

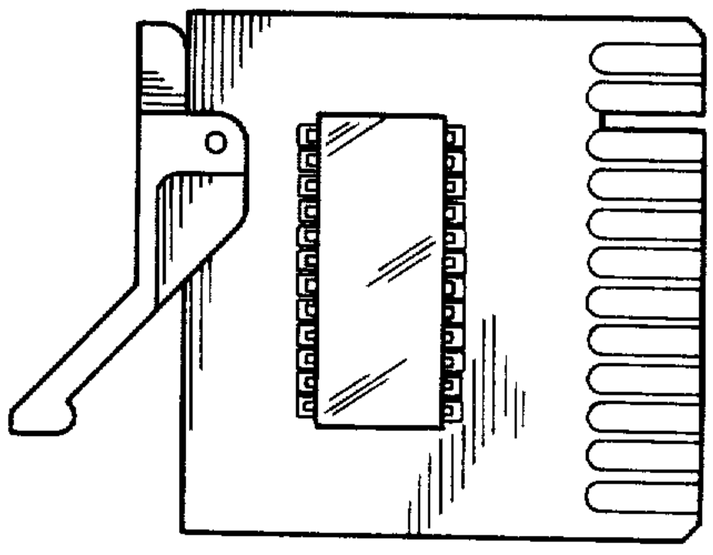


Fig. 2

Fig. 4

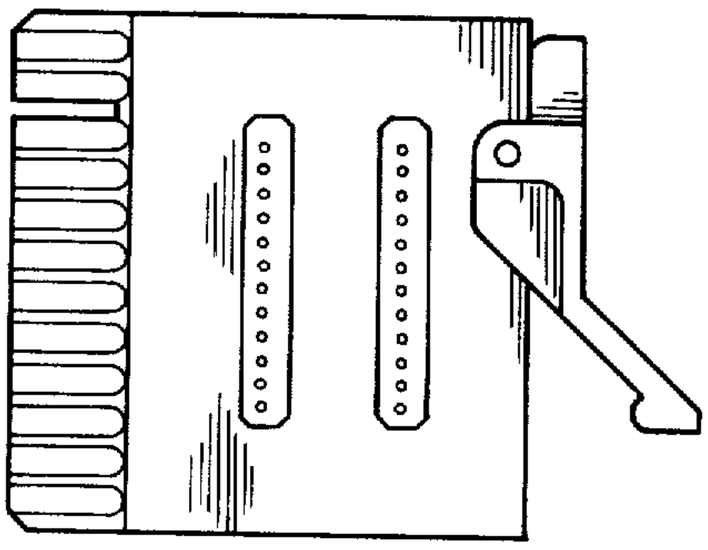


Fig. 5