United States Patent [19]
Mochizuki et al.

[11] **Des. 260,091**
[45] ** **Aug. 4, 1981**

[54] **SEMICONDUCTOR**

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[73] Assignee: **Hitachi, Ltd.,** Tokyo, Japan

[**] Term: **14 Years**

[21] Appl. No.: **15,216**

[22] Filed: **Feb. 26, 1979**

[30] **Foreign Application Priority Data**

Aug. 25, 1978	[JP]	Japan	53-35723
Aug. 25, 1978	[JP]	Japan	53-35730
Aug. 25, 1978	[JP]	Japan	53-35734
Aug. 25, 1978	[JP]	Japan	53-35738

[51] **Int. Cl.** .... **D13—03**
[52] **U.S. Cl.** **D13/99**
[58] **Field of Search** .... D13/12, 99, 40, 41; 174/52 R, 52 PE, 52 S, 52 FP, 50.5, 50.52, 50.56; 357/70, 73, 74, 80

[56] **References Cited**

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Electronics, 10-27-1977, p. 9, Integrated Circuit Package (square).
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Primary Examiner—Susan J. Lucas
Attorney, Agent, or Firm—Craig & Antonelli

[57] **CLAIM**

The ornamental design for a semiconductor, as shown and described.

DESCRIPTION

FIG. **1** is a right side, top and front perspective view of a semiconductor showing our new design;
FIG. **2** is a rear elevational view thereof;
FIG. **3** is a left side view thereof;
FIG. **4** is a bottom view thereof;
FIG. **5** is a right side, top and front perspective view of a semiconductor showing another embodiment of our new design;
FIG. **6** is a bottom view thereof;
FIG. **7** is a right side, top and front perspective view of a semiconductor showing another embodiment of our new design;
FIG. **8** is a bottom view thereof;
FIG. **9** is a right side, top and front perspective view of a semiconductor showing another embodiment of our new design;
FIG. **10** is a bottom view thereof.

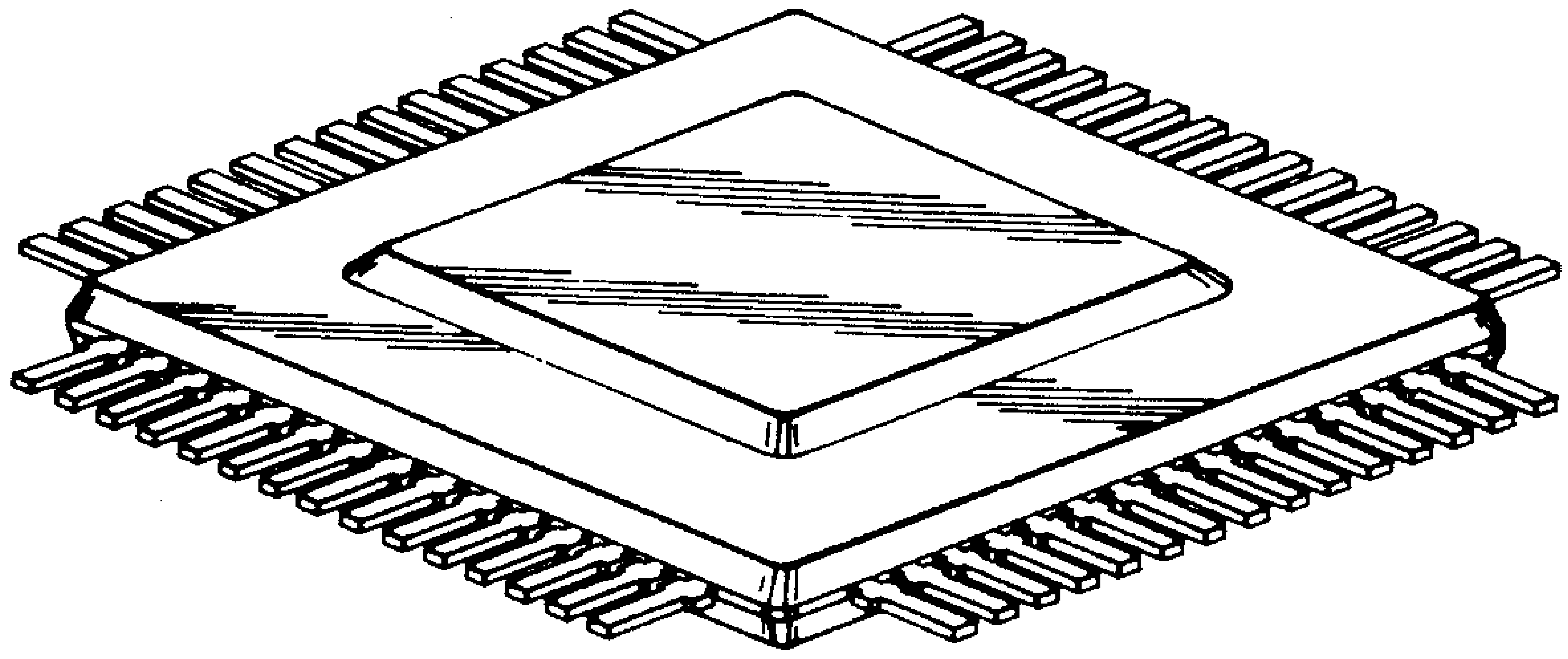


FIG. 1

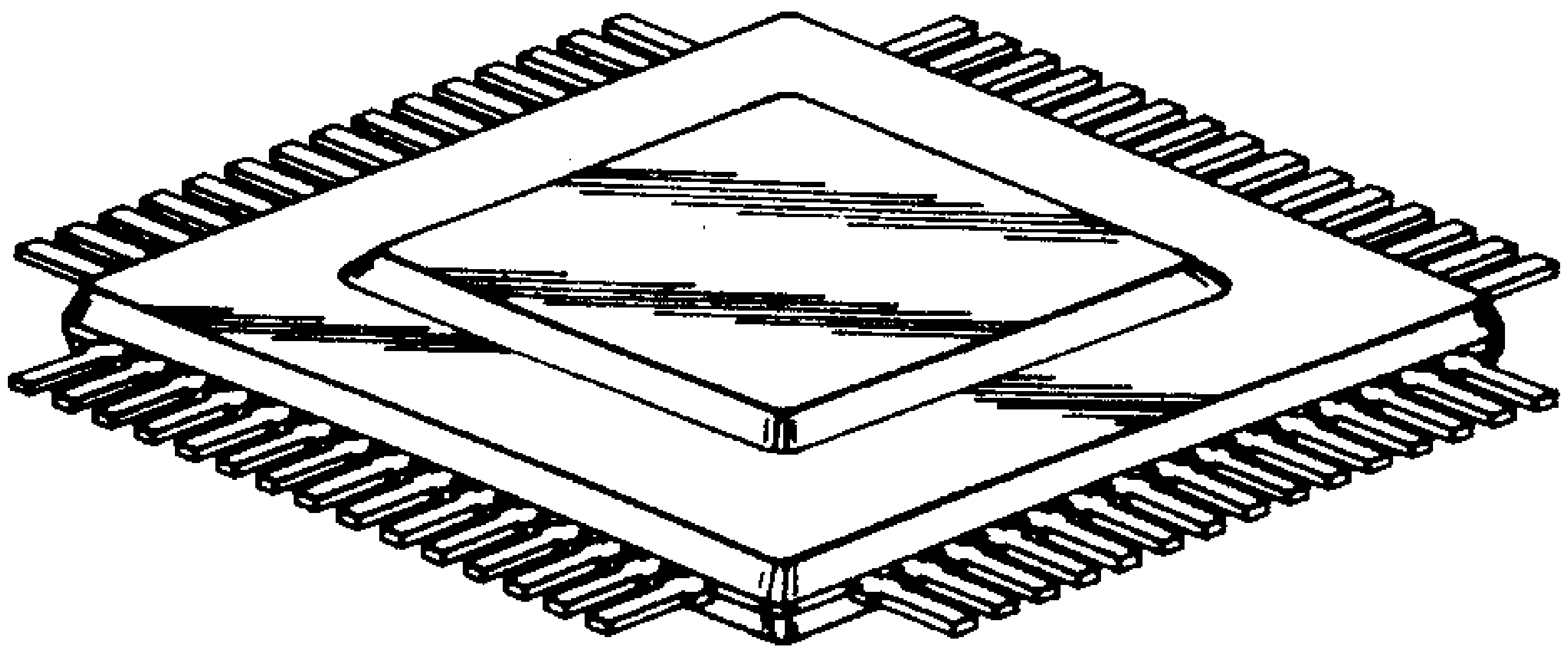


FIG. 2

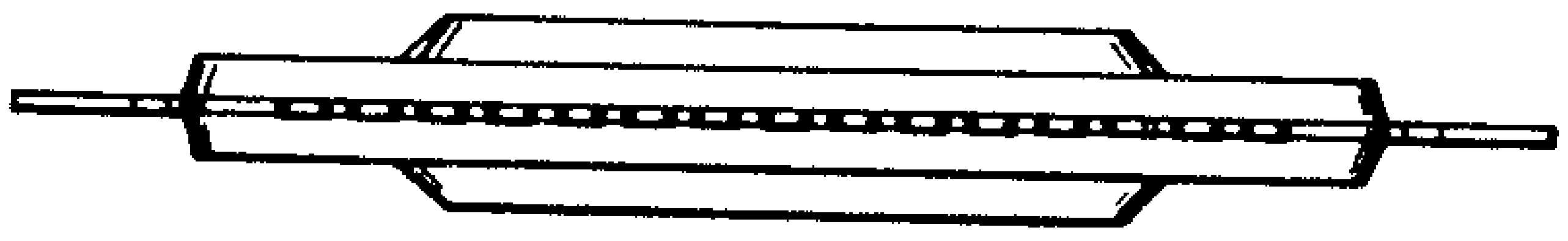


FIG. 3

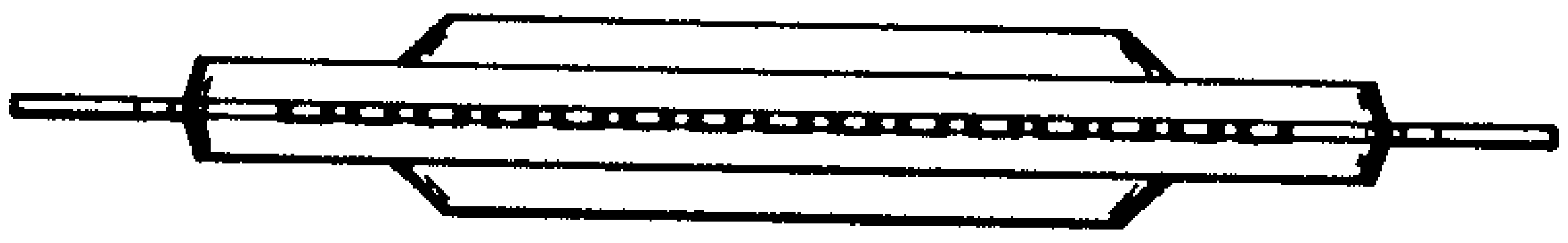
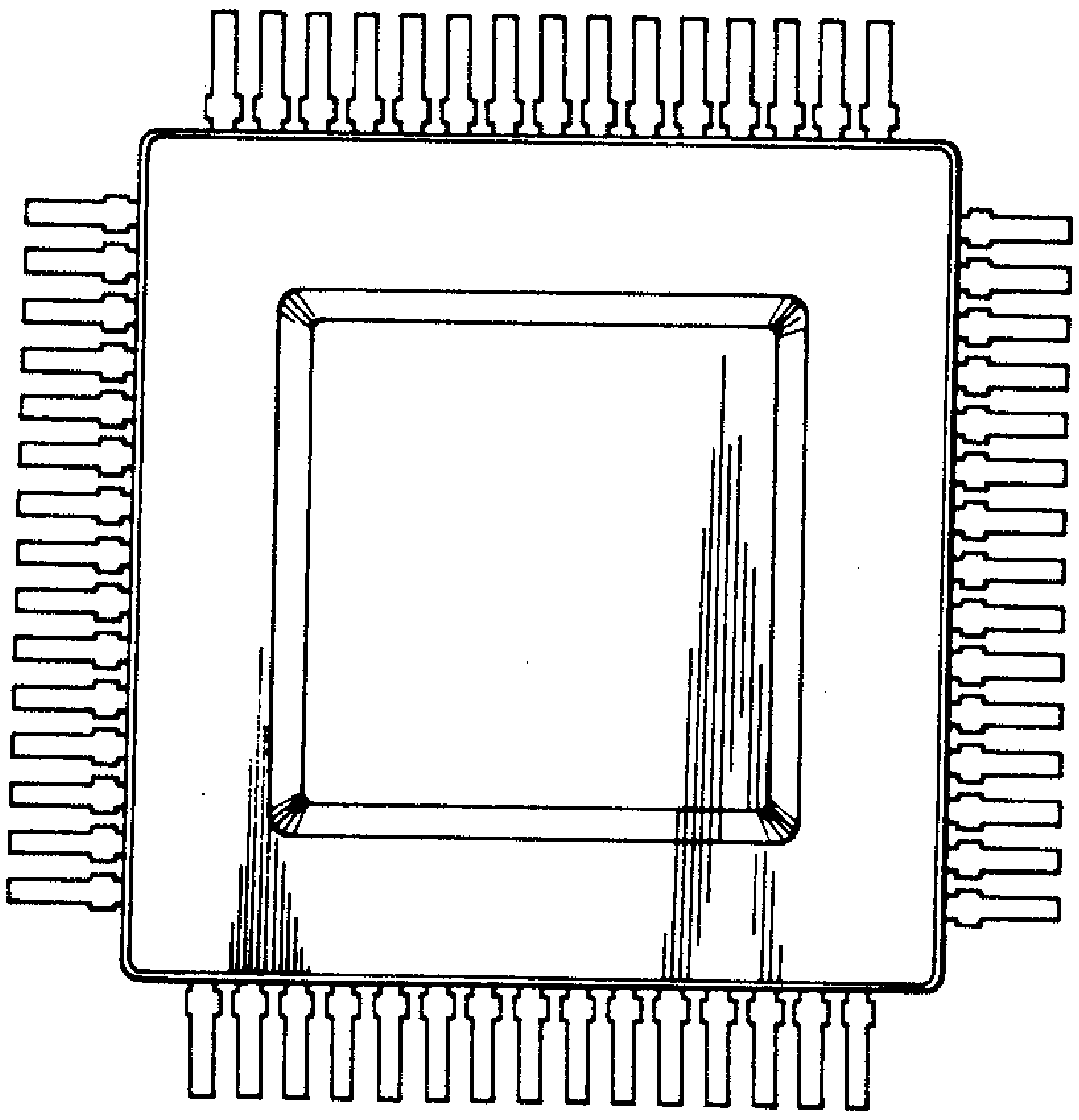


FIG. 4



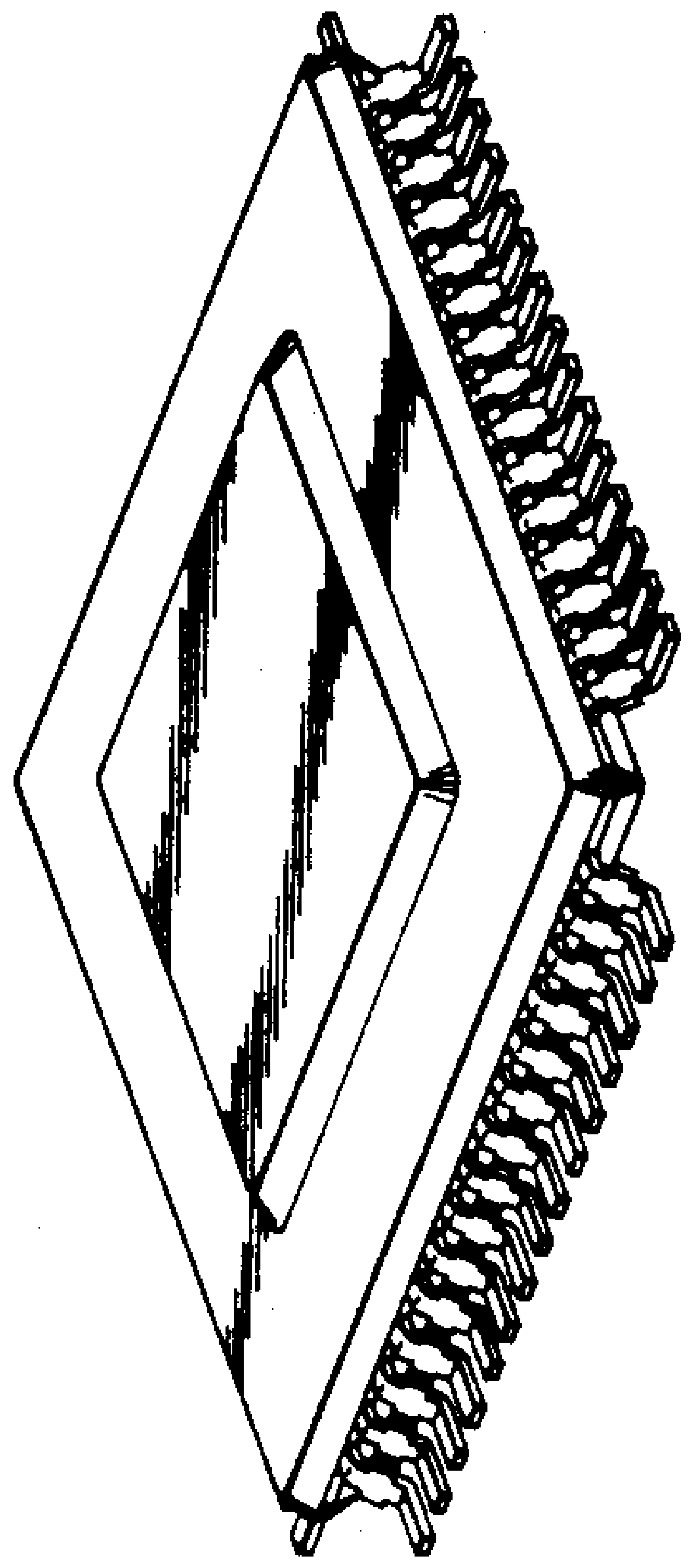


FIG. 5

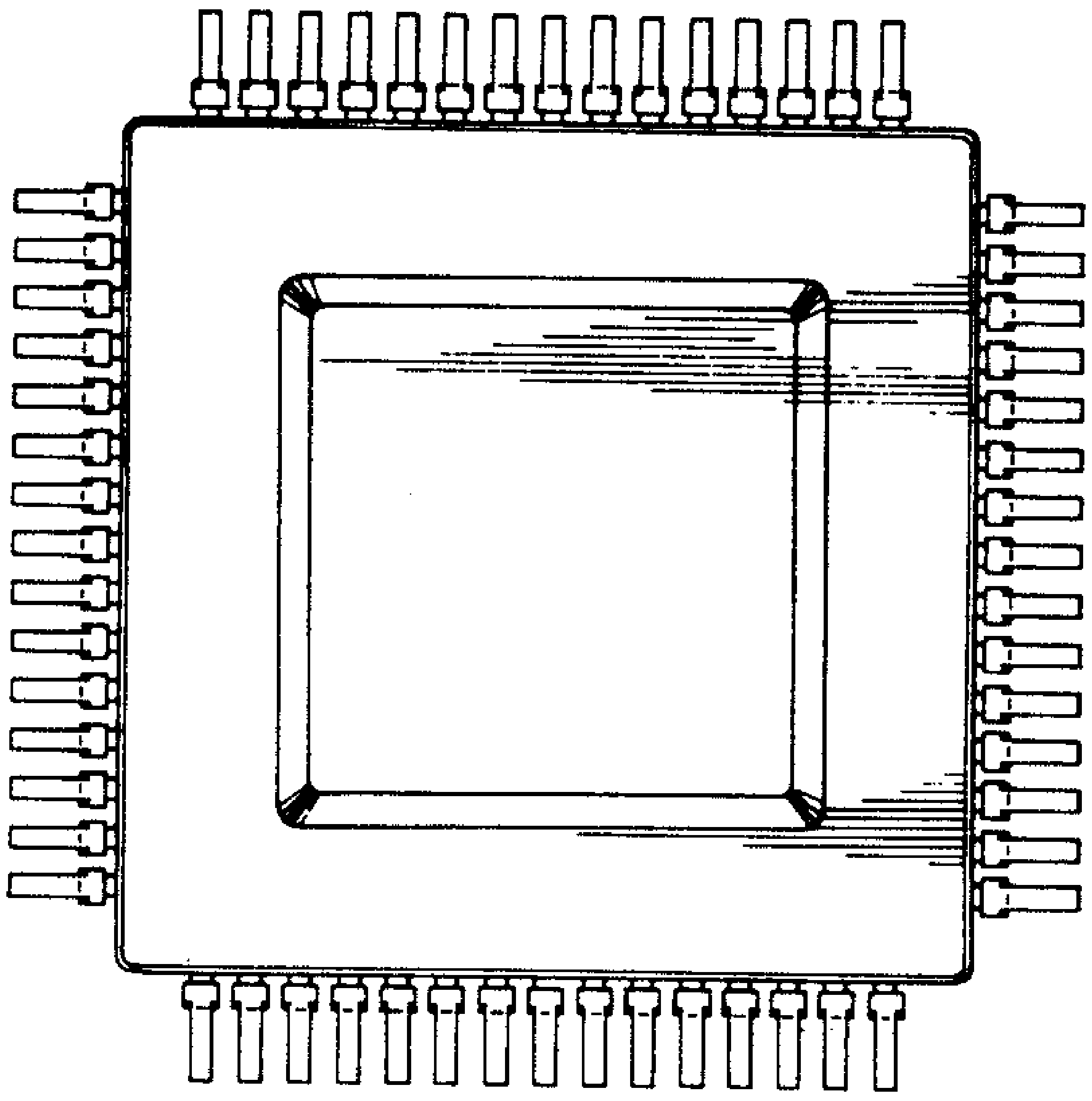


FIG. 6

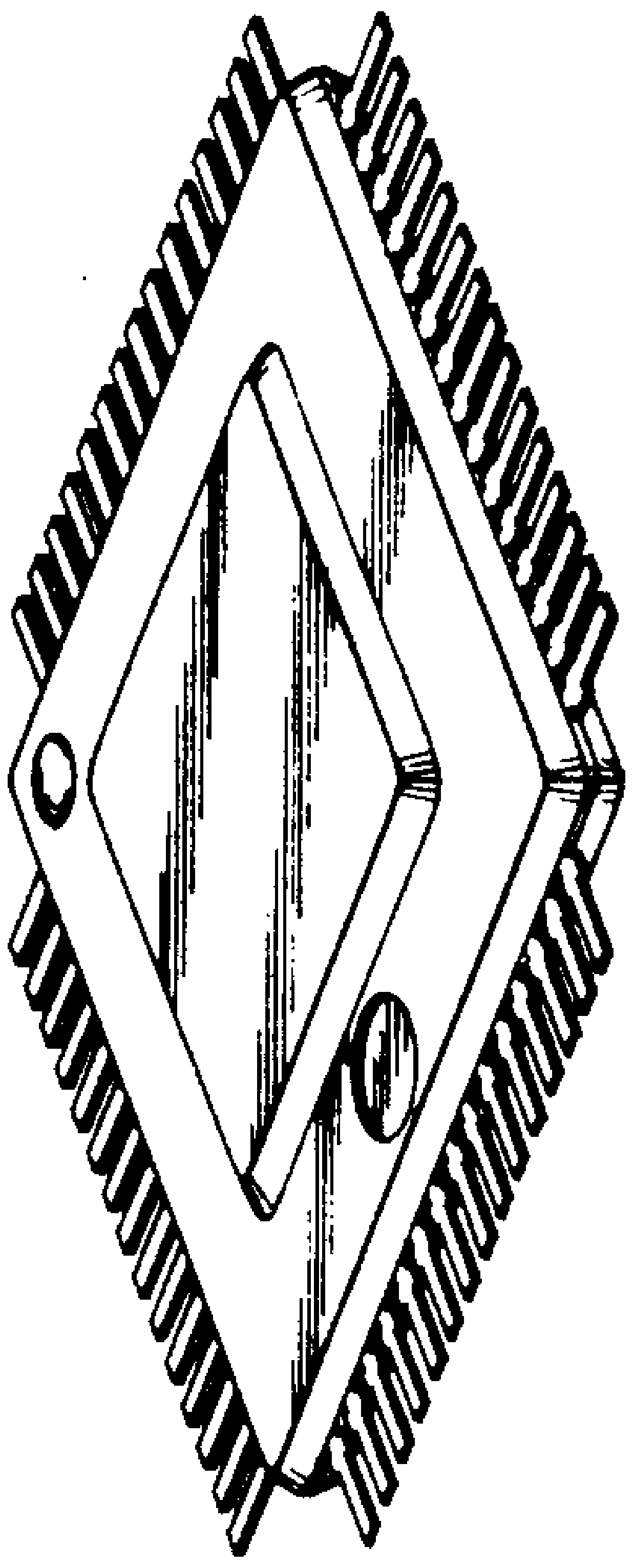


FIG. 7

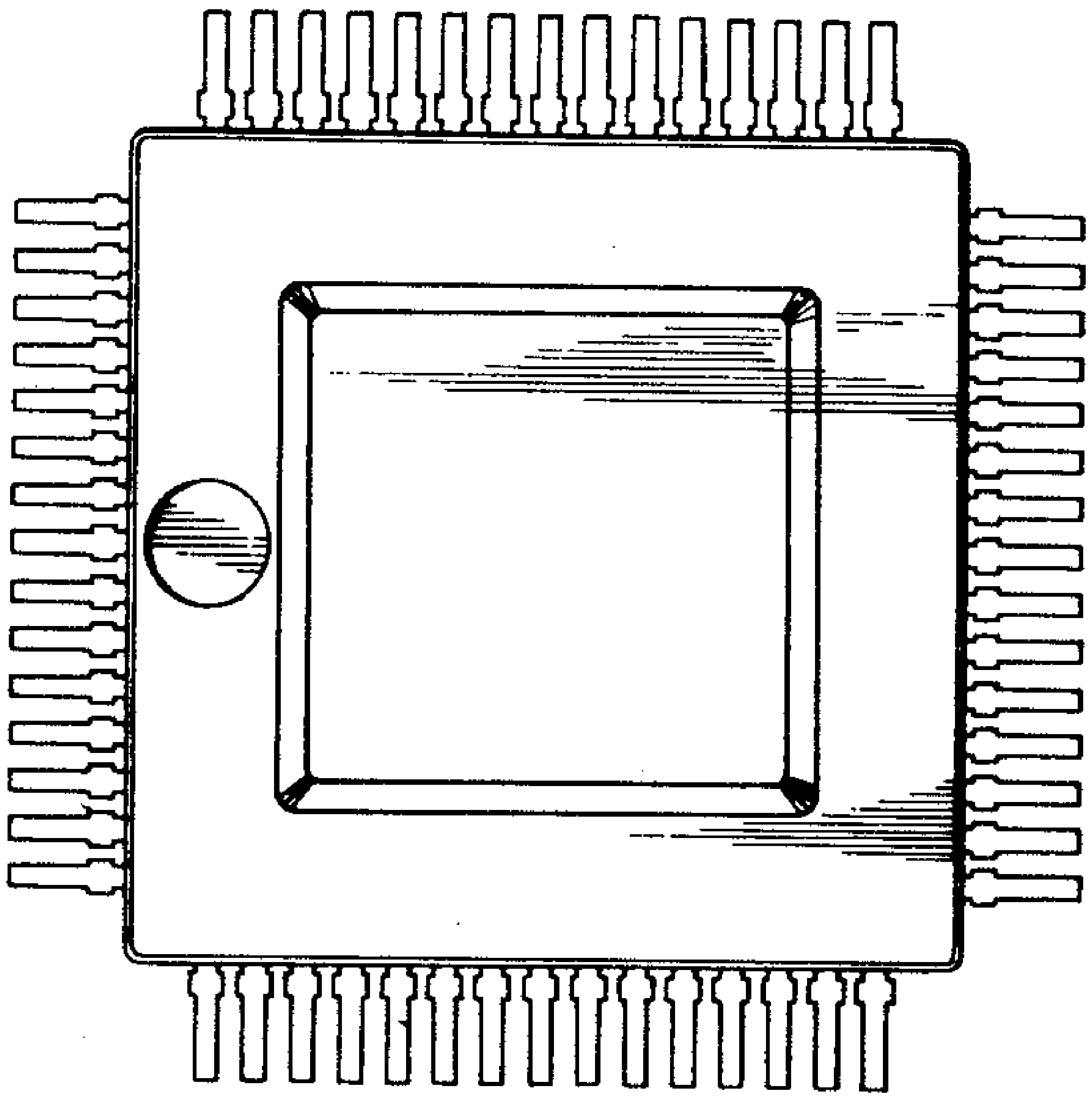


FIG. 8

FIG. 9

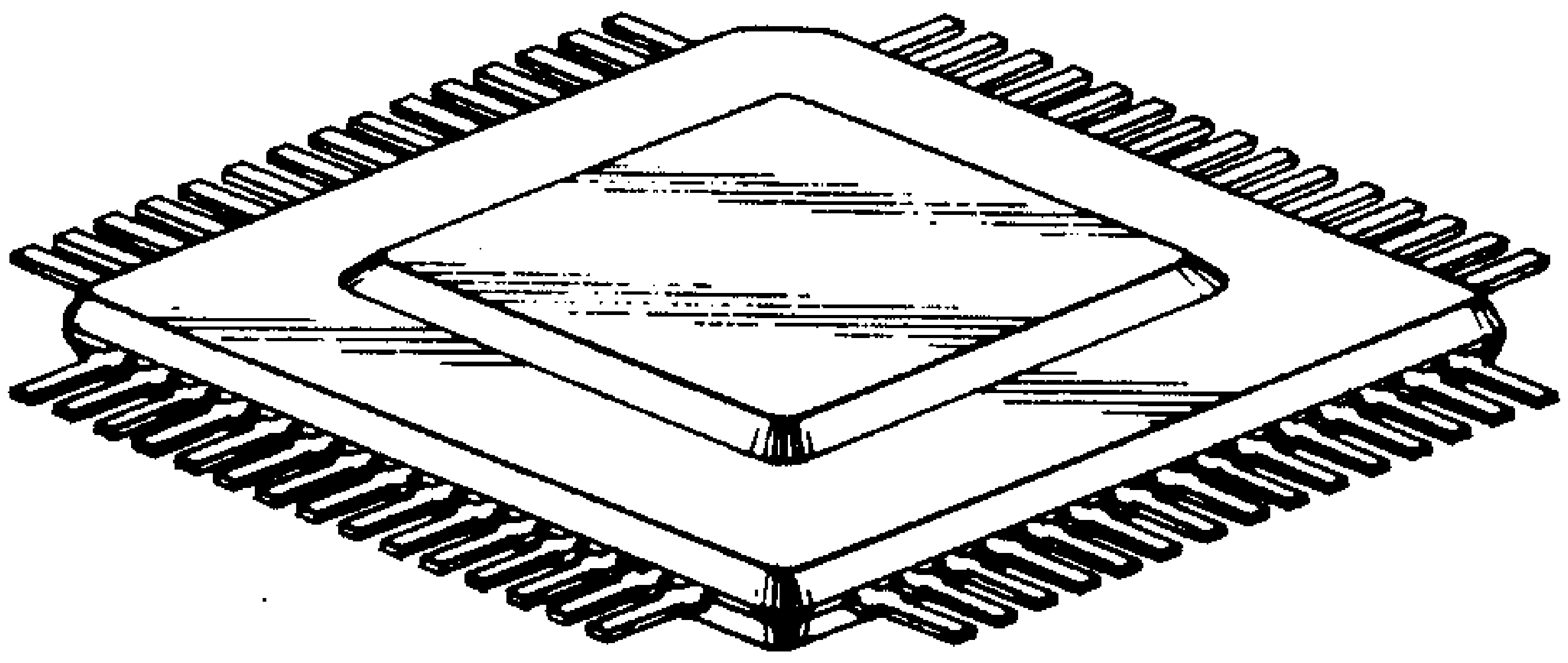


FIG. 10