United States Patent [19]

Mochizuki et al.

[11] **Des. 259,559**

[45] ** **Jun. 16, 1981**

[54] **SEMICONDUCTOR**

[75] Inventors: **Hidetoshi Mochizuki**, Fuchu; **Keizo Otsuki**, Higashiyamato; **Hideki Kosaka**, Kodaira; **Gen Murakami**, Machida, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[**] Term: **14 Years**

[21] Appl. No.: **6,199**

[22] Filed: **Jan. 24, 1979**

[30] **Foreign Application Priority Data**

Jul. 28, 1978 [JP] Japan 53-31692

[51] **Int. Cl.** .... **D13—03**
[52] **U.S. Cl.** **D13/99**
[58] **Field of Search** .... D13/12, 99, 40, 41; 174/52 R, 52 PE, 52 S, 52 FP, 50.5, 50.52, 50.56; 357/70, 73, 74, 80

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,208,892	9/1965	Miller et al.	174/52 FP X
3,436,451	4/1969	Wasser	174/52 FP X
4,012,766	3/1977	Phillips et al.	174/52 FP X

OTHER PUBLICATIONS

Electronics, 3-17-1977, p. 89, LSI package, leaded type B.

Electronics, 11-24-1977, p. 145, integrated circuit housing.

Primary Examiner—Susan J. Lucas
Attorney, Agent, or Firm—Craig and Antonelli

[57] **CLAIM**

The ornamental design for a semiconductor, as shown.

DESCRIPTION

FIG. **1** is a right side, top and front perspective view of a semiconductor showing our new design.
FIG. **2** is a rear elevational view thereof;
FIG. **3** is a left side view thereof;
FIG. **4** is a bottom view thereof.

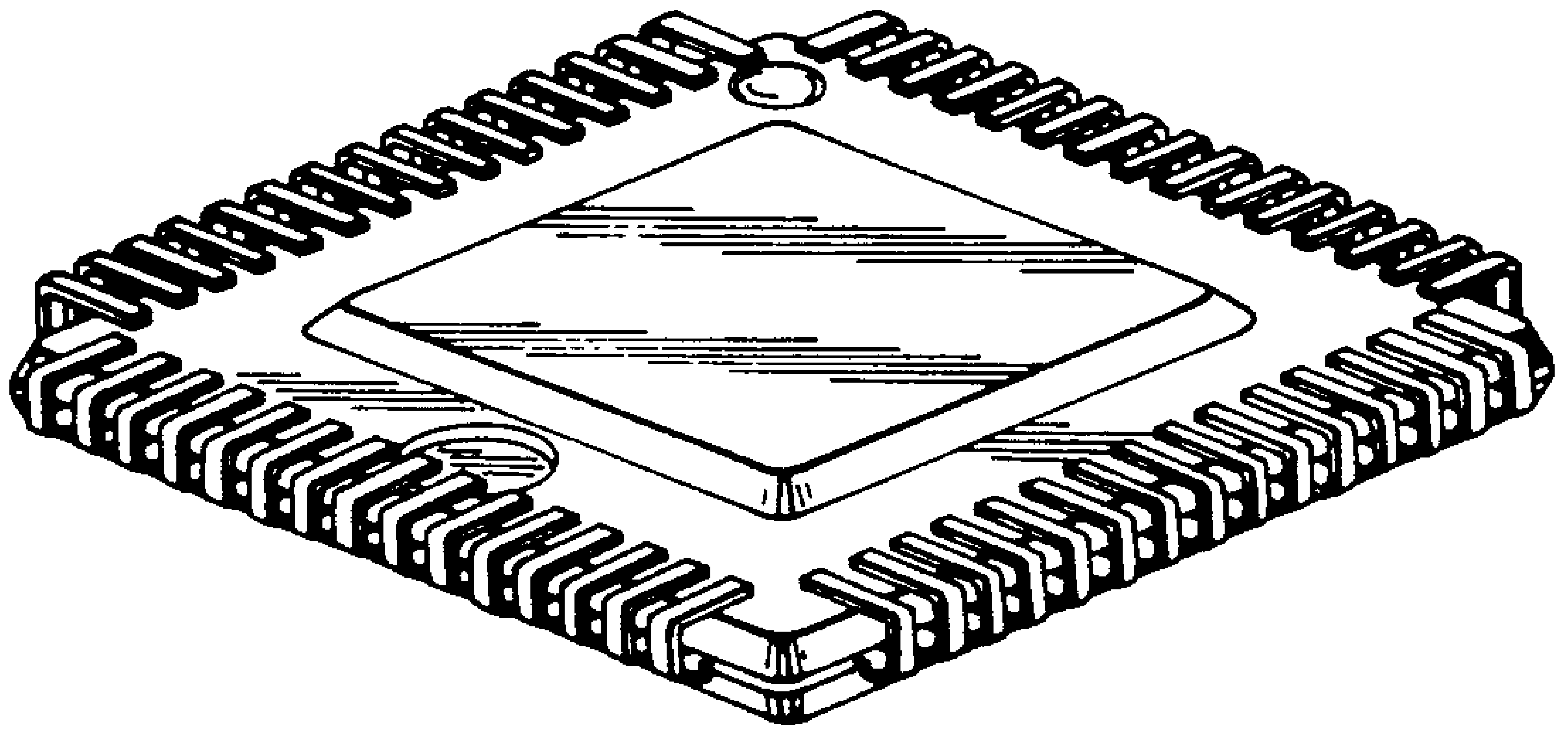

FIG. 1

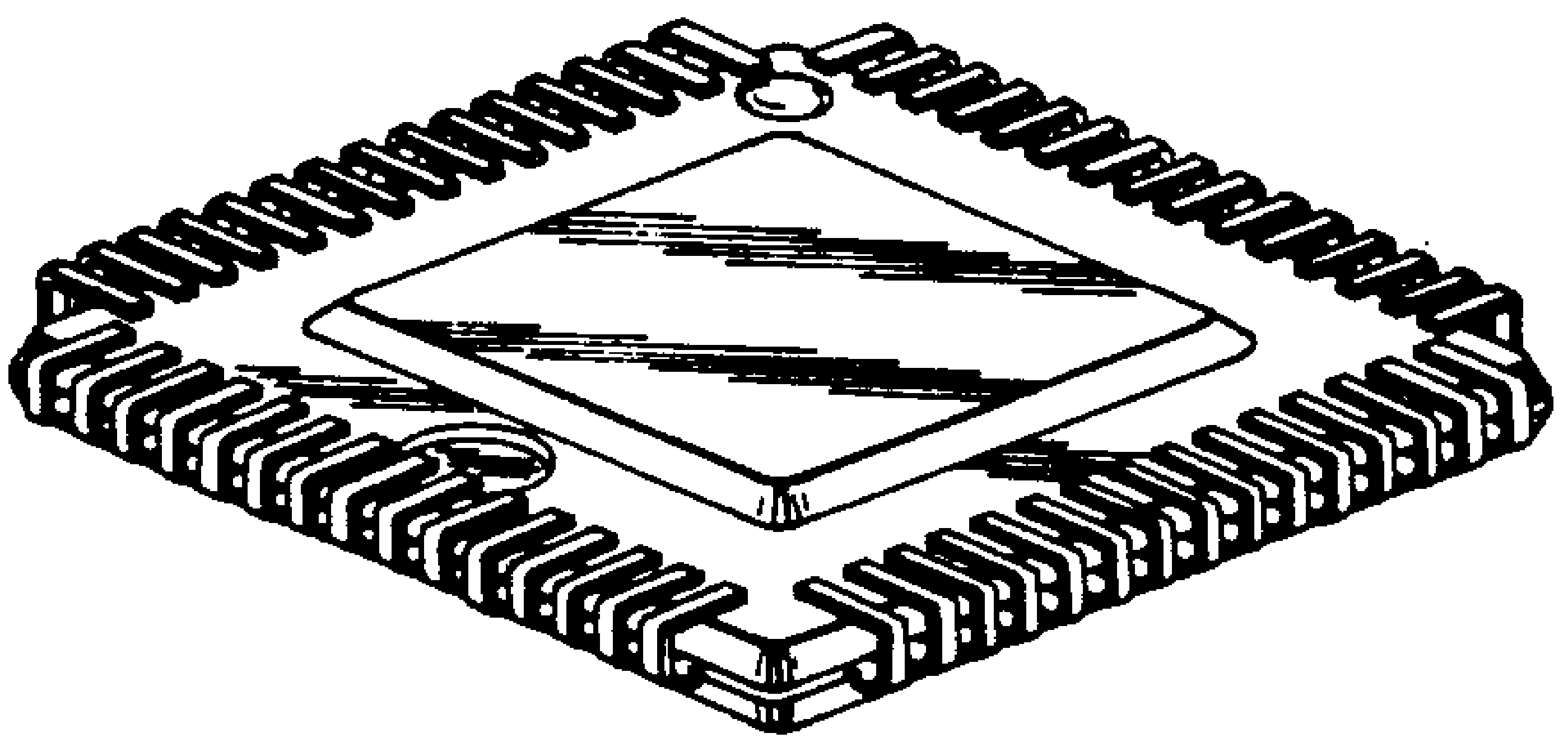

FIG. 2

FIG. 3

FIG. 4