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Treibergs et al.

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(54) COMPLIANT GROUND BLOCK AND TESTING SYSTEM FOR TESTING INTEGRATED CIRCUITS

8,460,010 B2 6/2013 Kimura et al.
D691,101 S * 10/2013 Ishizawa D13/182
D695,231 S * 12/2013 Shen D13/160
D742,338 S * 11/2015 Akana D13/182
(Continued)

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FOREIGN PATENT DOCUMENTS

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KR 102121754 B1 6/2020
TW D205153 6/2020
(Continued)

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OTHER PUBLICATIONS

(**) Term: 15 Years

LGA Sockets, Land Gris Array Sockts—Te.com, No Announcement
Date [online], retrieved on Aug. 3, 2023, retrieved from internet,
<https://www.te.com/usa-en/products/connectors/sockets/ic-sockets/lga-sockets.html?tab=pgp-story> (Year: 2023).*
(Continued)

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USPC D13/182

(58) Field of Classification Search
USPC D13/117, 121, 133, 164, 173, 182, 184,
D13/199
CPC H05K 3/36; H05K 3/361; H05K 3/363;
H05K 3/365; H05K 3/40; H05K 3/4007;
H05K 4/4015
See application file for complete search history.

(57) CLAIM
The ornamental design for a compliant ground block and testing system for testing integrated circuits, as shown and described.

DESCRIPTION

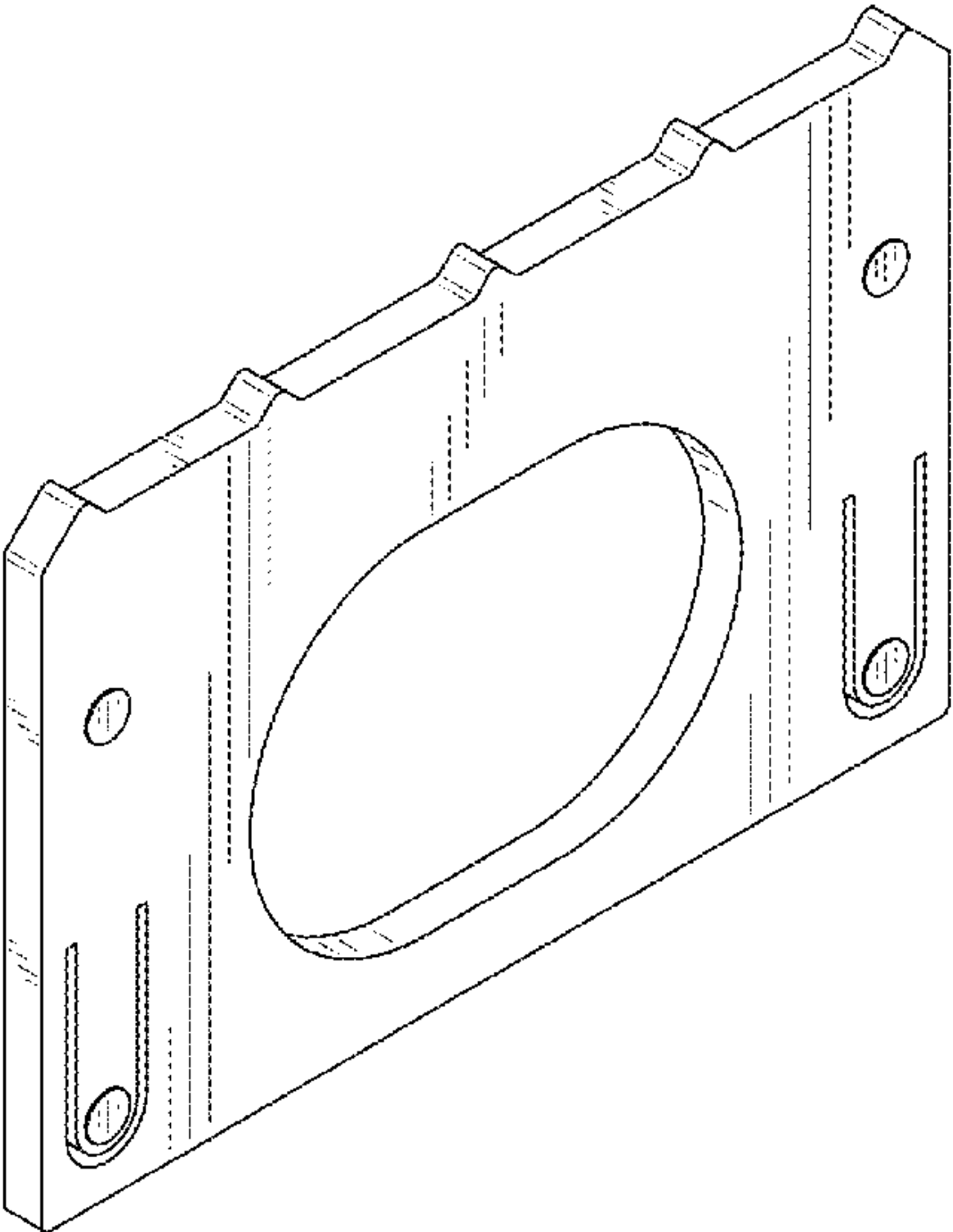
(56) References Cited

U.S. PATENT DOCUMENTS

6,299,459 B1 10/2001 Botka et al.
6,861,667 B2 3/2005 Gilk et al.
6,979,595 B1 * 12/2005 James H01L 23/3107
438/118
7,074,049 B2 7/2006 O’Sullivan
D548,201 S * 8/2007 Jones D13/182
7,255,576 B2 8/2007 O’Sullivan
D605,613 S * 12/2009 Carter D13/182
7,862,391 B2 1/2011 Johnston et al.

FIG. 1 is a Top Perspective view of a compliant ground block and testing system for testing integrated circuits showing the new design;
FIG. 2 is a Bottom Perspective view thereof;
FIG. 3 is a Front view thereof;
FIG. 4 is a Back view thereof;
FIG. 5 is a Left view thereof;
FIG. 6 is a Right view thereof;
FIG. 7 is a Top view thereof; and,
FIG. 8 is a Bottom view thereof.

1 Claim, 5 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

D757,666 S * 5/2016 Yokoo D13/182
9,476,936 B1 * 10/2016 Johnson G01R 31/2874
D773,404 S * 12/2016 Li D13/160
9,606,143 B1 * 3/2017 Sherry G01R 1/067
D879,787 S * 3/2020 Luo D13/182
D880,484 S * 4/2020 Li D13/182
11,293,968 B2 * 4/2022 Sherry G01R 31/31905
2003/0232516 A1 12/2003 Bedell et al.
2008/0297142 A1 12/2008 Alladio et al.
2022/0107359 A1 * 4/2022 Treibergs G01R 1/0466
2023/0056822 A1 * 2/2023 Tadele H05K 1/141

FOREIGN PATENT DOCUMENTS

TW 223374-0001 * 2/2023
TW 223708-0001 * 2/2023
TW 224736-0001 * 4/2023

OTHER PUBLICATIONS

Products—Johnstech.com, No Announcement Date [online], retrieved on Aug. 3, 2023, retrieved from internet, <https://www.johnstech.com/products/> (Year: 2023).*

Office Action issued in Taiwan Design Patent Application No. 110303723, Apr. 11, 2022, with summary translation (4 pages).

* cited by examiner

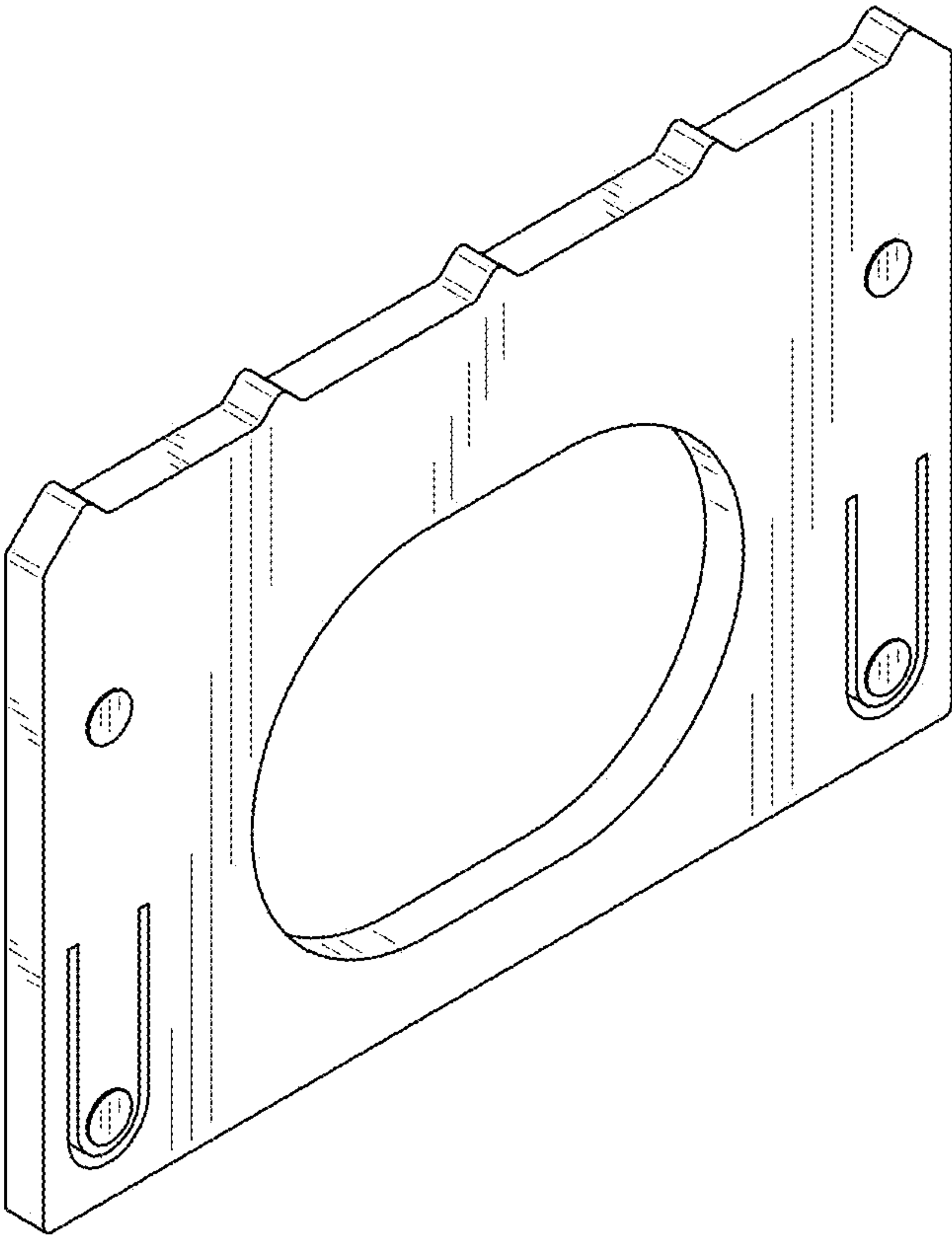


FIG. 1

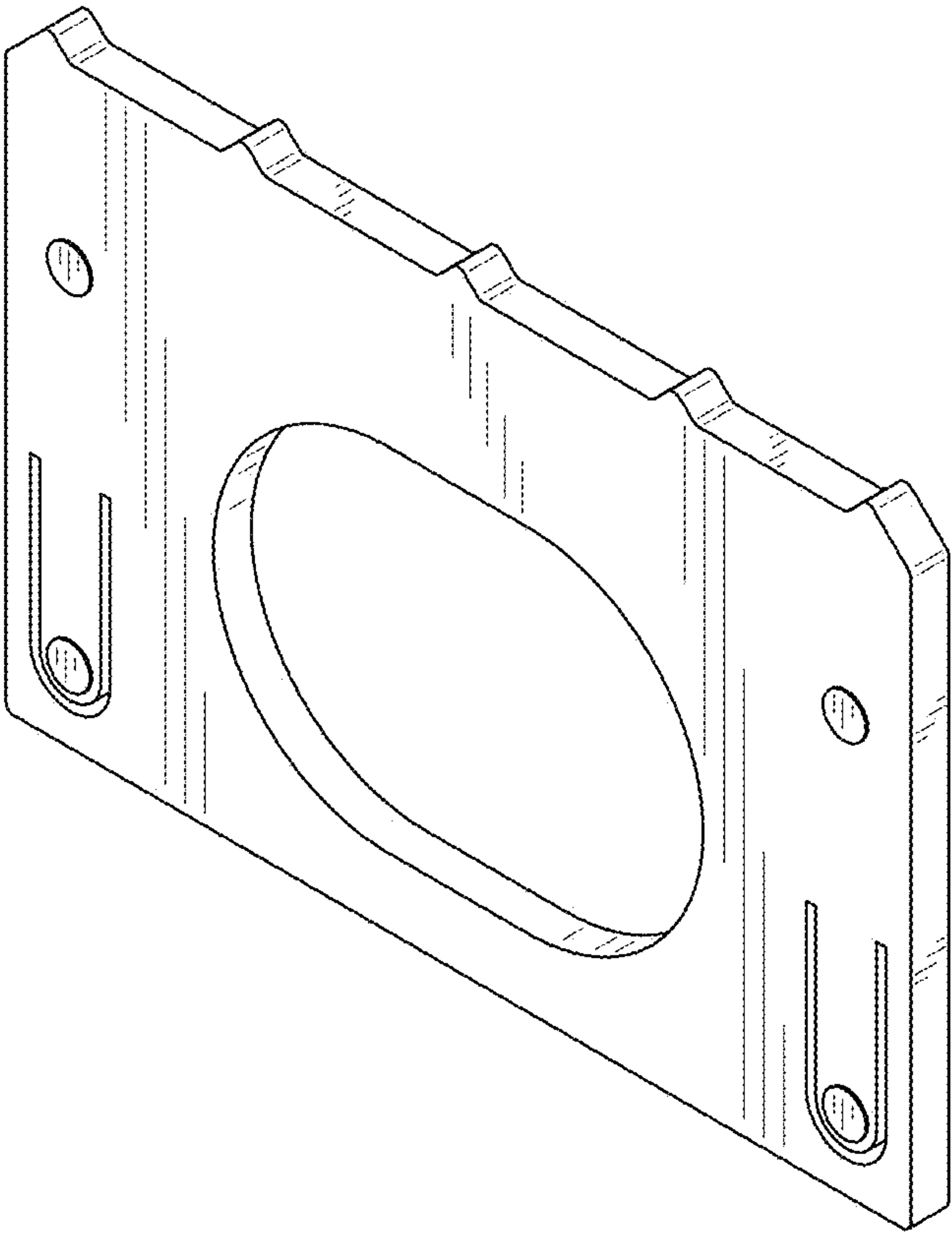


FIG. 2

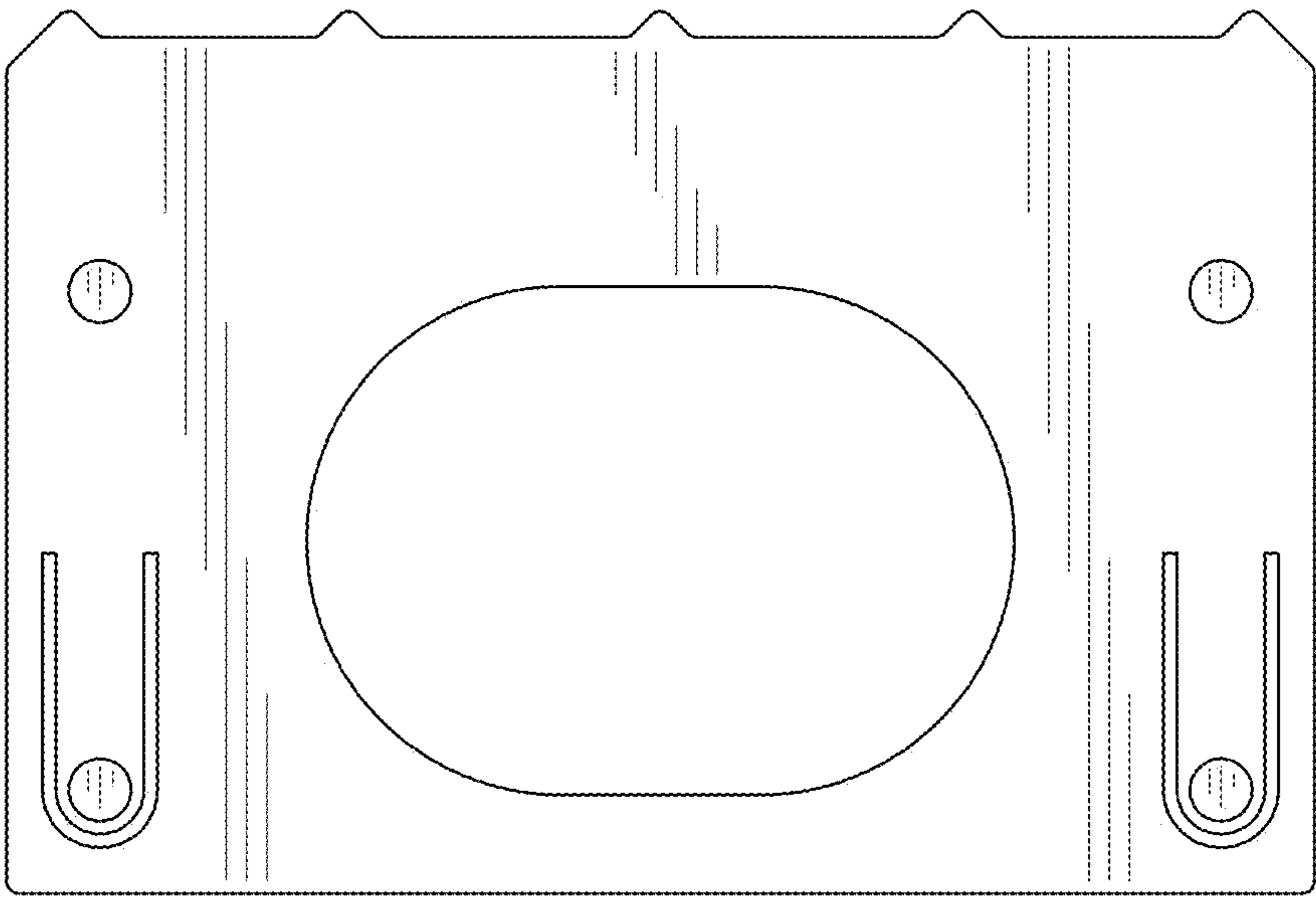


FIG. 3

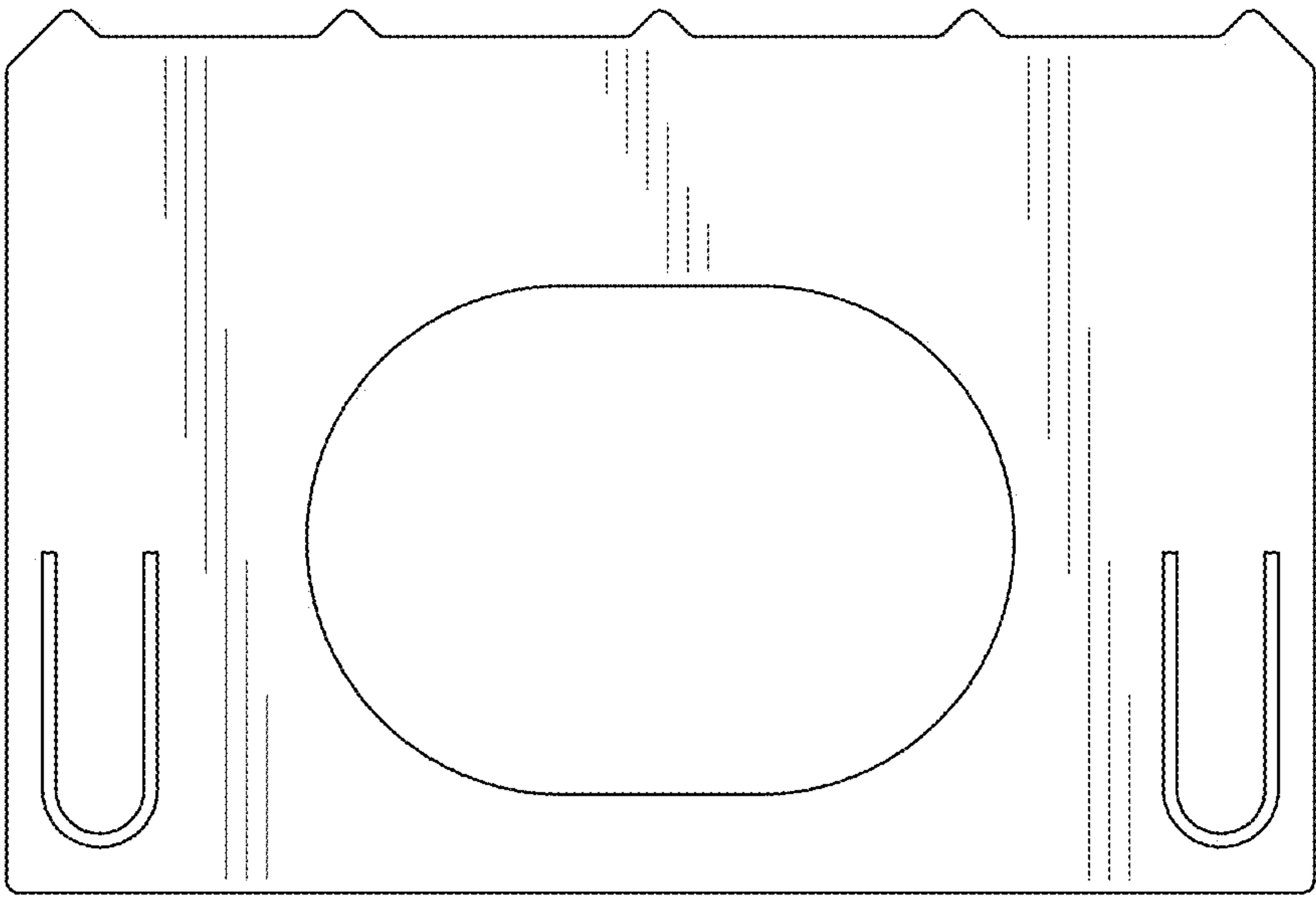


FIG. 4



FIG. 5



FIG. 6



FIG. 7



FIG. 8