US009899467B2

(12) United States Patent
Chiou et al.

(10) **Patent No.: US 9,899,467 B2**

(45) **Date of Patent: Feb. 20, 2018**

(54) **SEMICONDUCTOR DEVICES, METHODS OF MANUFACTURE THEREOF, AND CAPACITORS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 114 days.

(21) Appl. No.: **14/102,268**

(22) Filed: **Dec. 10, 2013**

(65) **Prior Publication Data**

US 2015/0162397 A1 Jun. 11, 2015

(51) **Int. Cl.**

H01L 49/02	(2006.01)
H01L 23/522	(2006.01)
H01L 23/532	(2006.01)
H01L 23/525	(2006.01)
H01L 27/08	(2006.01)
H01L 27/02	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 28/40*** (2013.01); ***H01L 23/5223*** (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 23/5256*** (2013.01); ***H01L 23/53295*** (2013.01); ***H01L 27/0248*** (2013.01); ***H01L 27/0805*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC . H01L 28/40; H01L 23/5256; H01L 23/5226; H01L 23/5223; H01L 23/53295; H01L 27/0805

See application file for complete search history.

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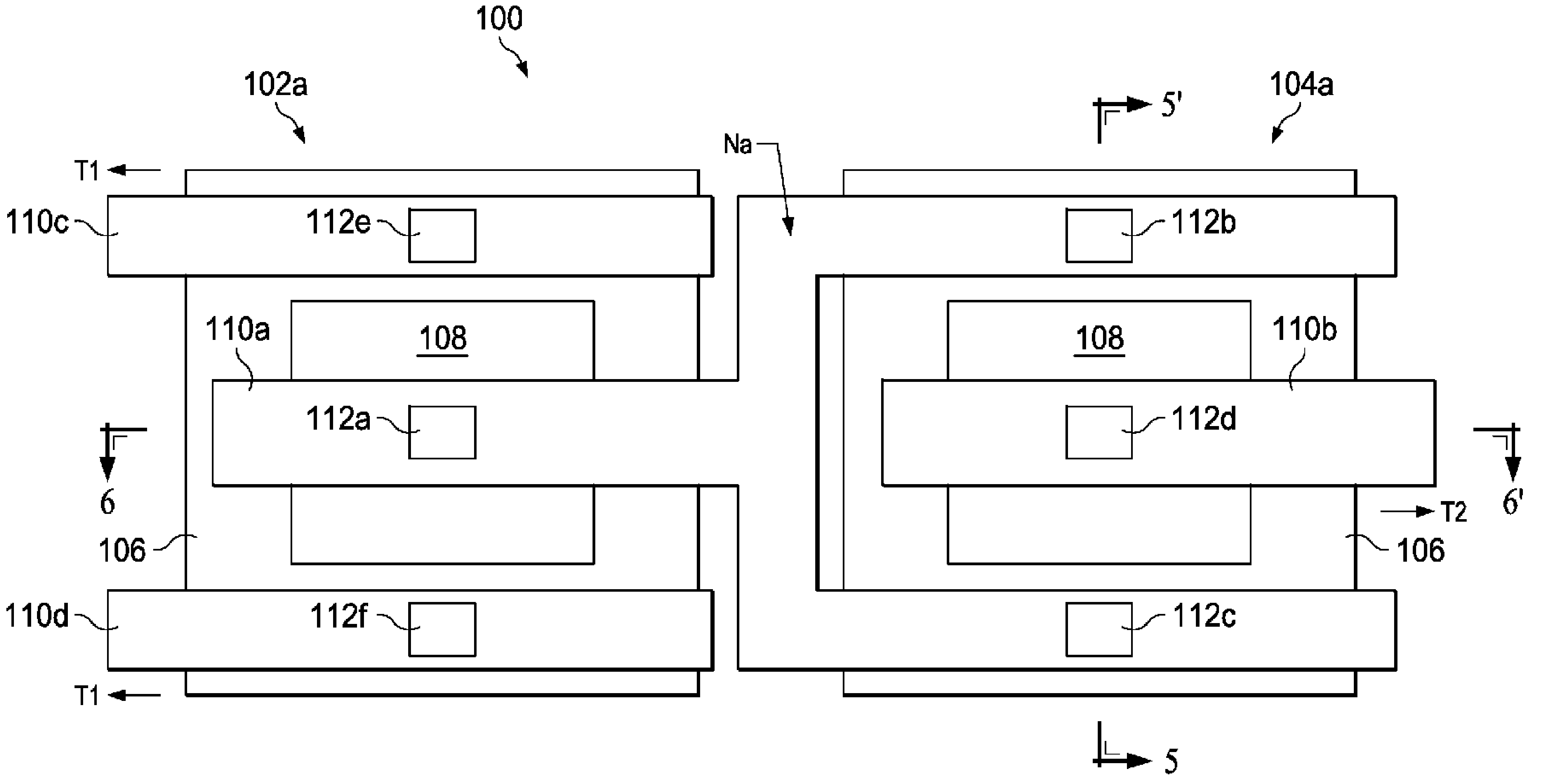
(57) **ABSTRACT**

Semiconductor devices, methods of manufacture thereof, and capacitors are disclosed. In some embodiments, a semiconductor device includes a first capacitor and a protection device coupled in series with the first capacitor. A second capacitor is coupled in parallel with the first capacitor and the protection device.

19 Claims, 8 Drawing Sheets



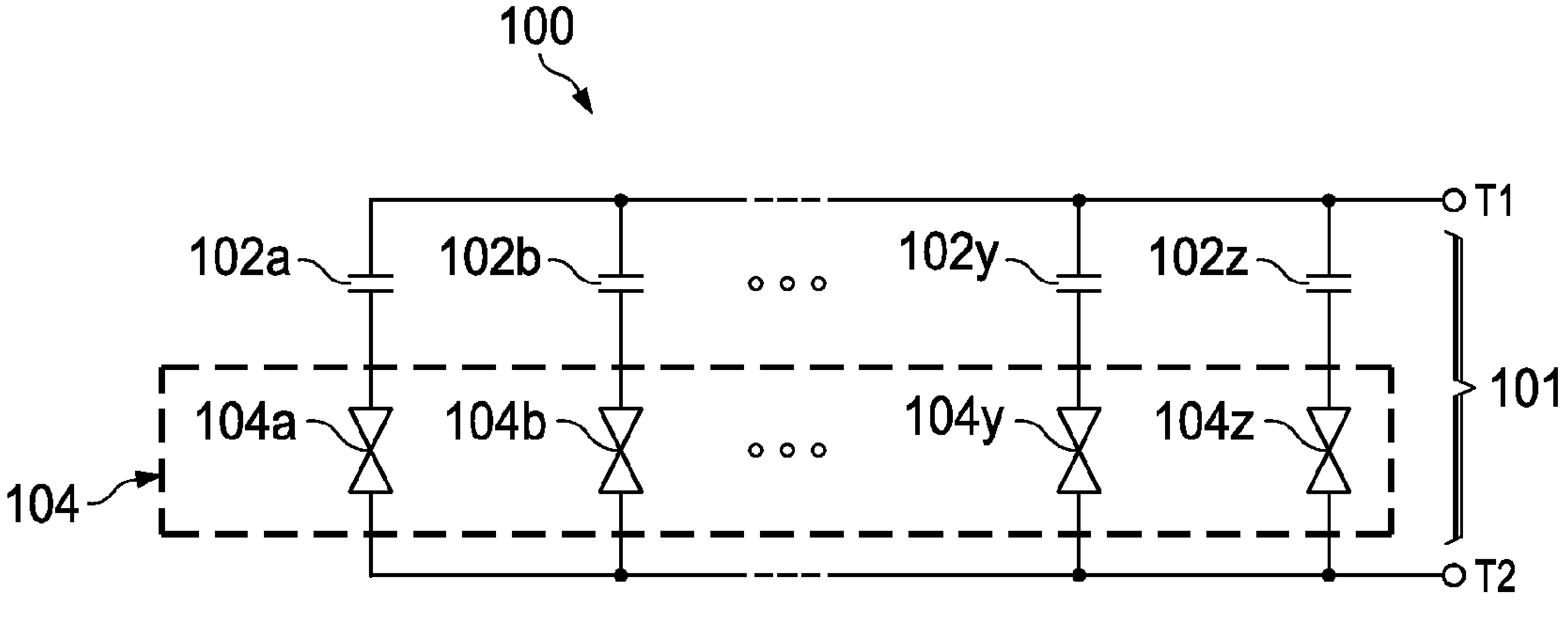


FIG. 1

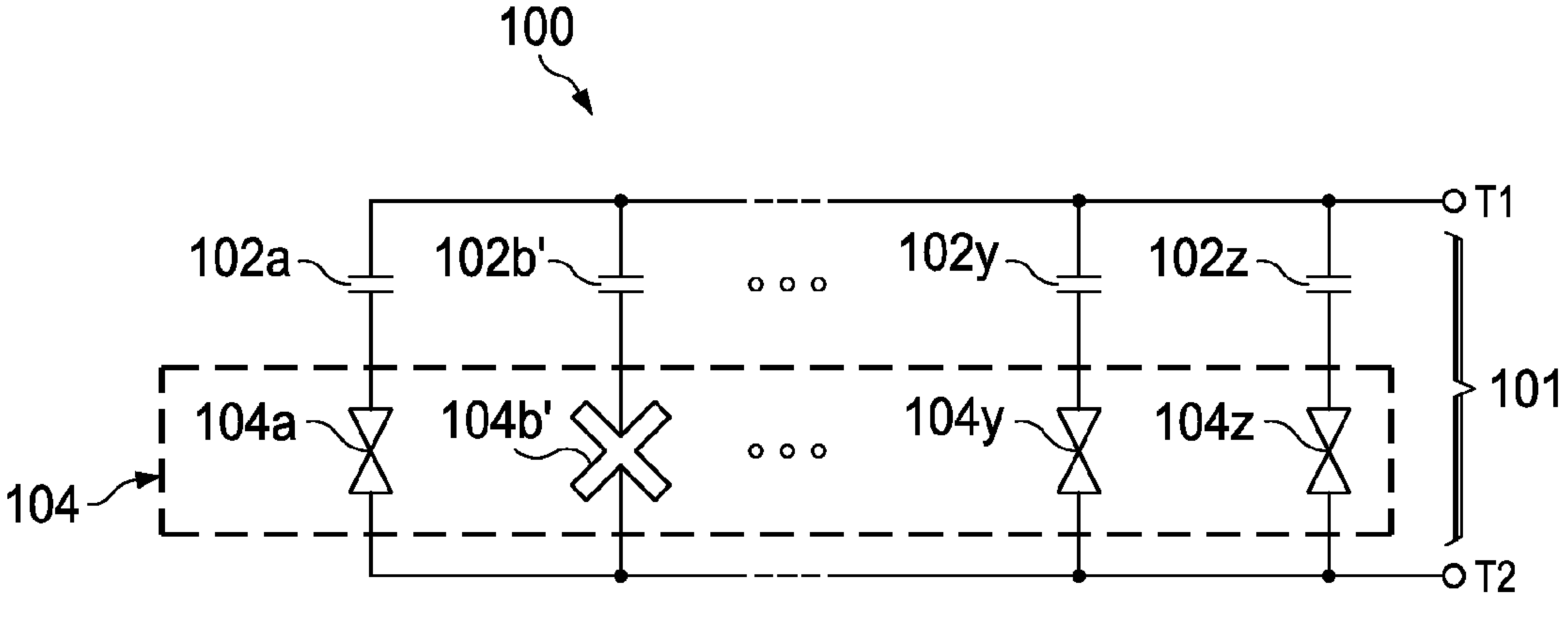


FIG. 2

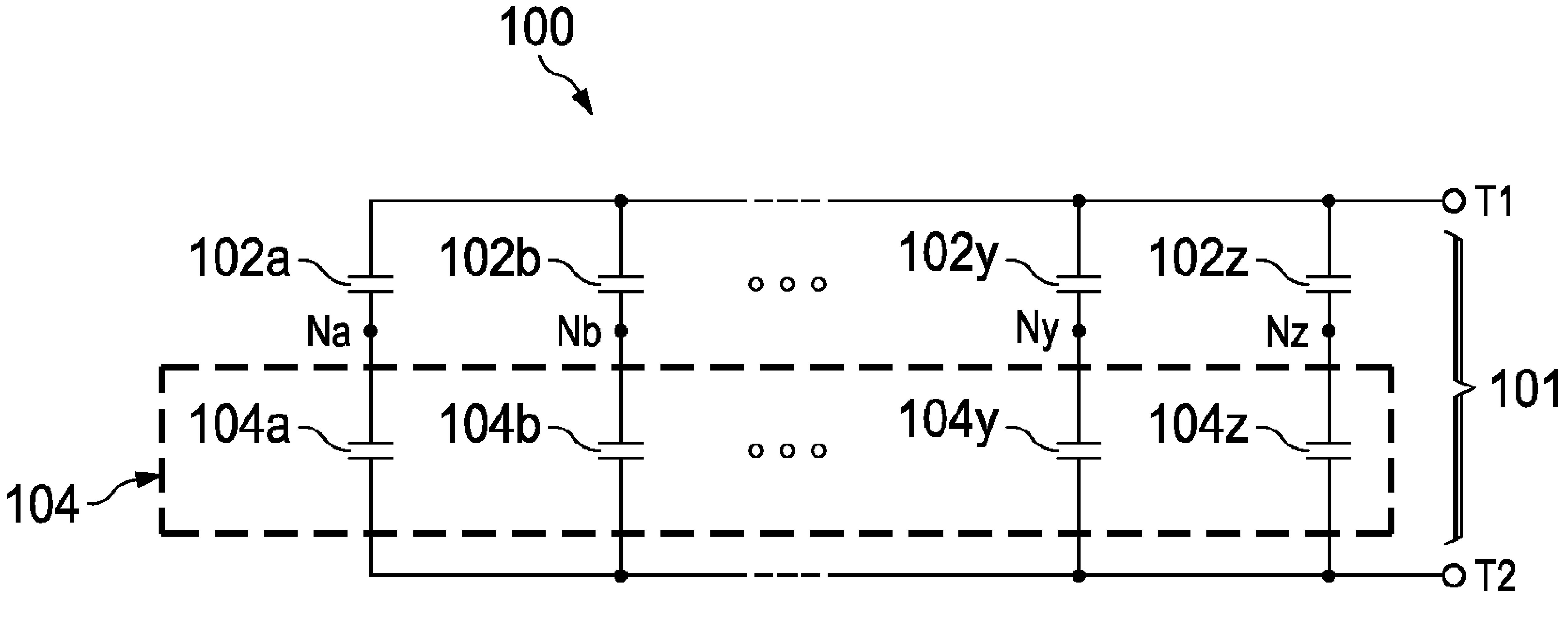


FIG. 3

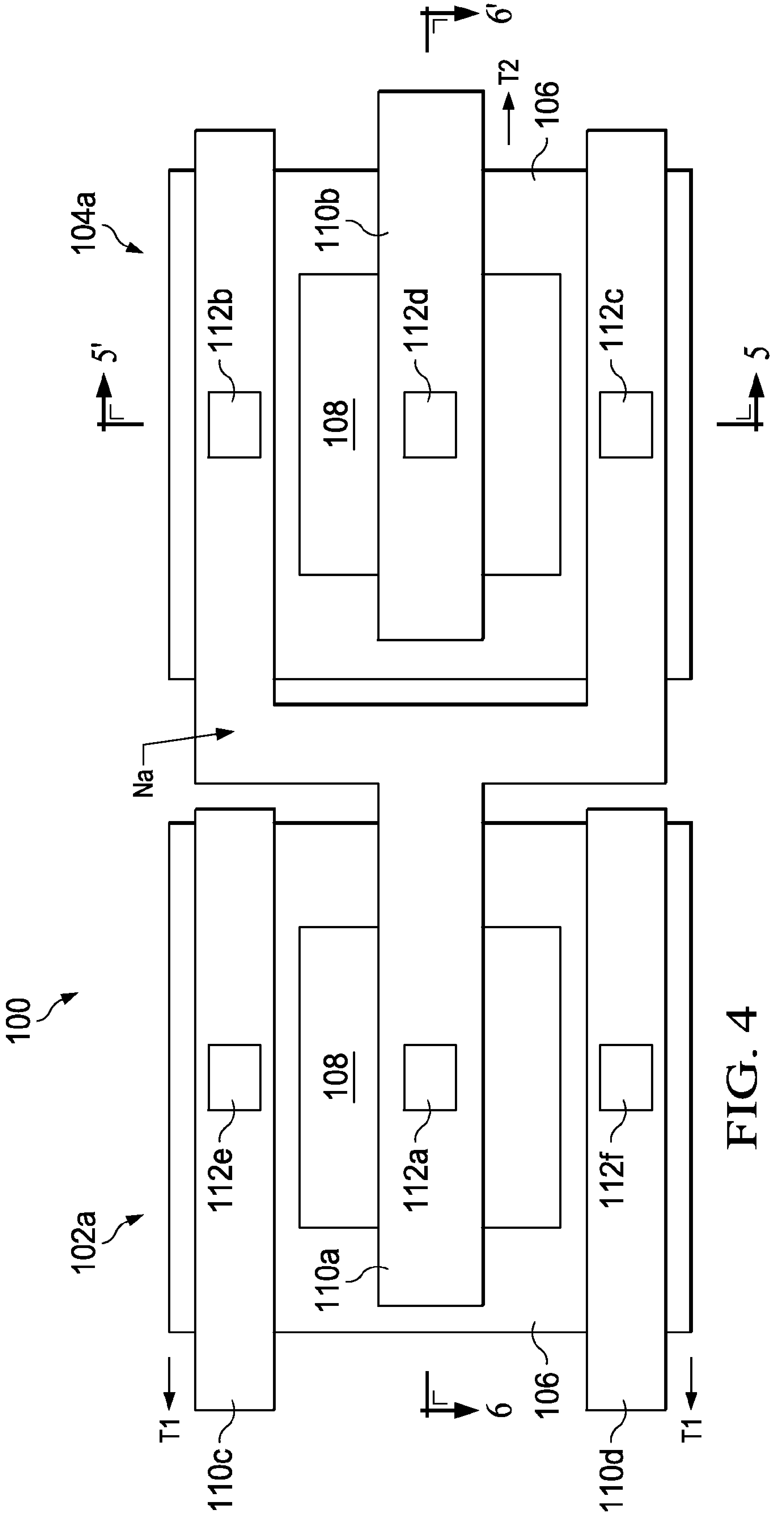

6'
T2
106
104a
110b
112b
112d
112c
5'
5
108
Na
100
108
112e
112a
112f
102a
110a
106
T1
6
106
T1
110c
110d

FIG. 4

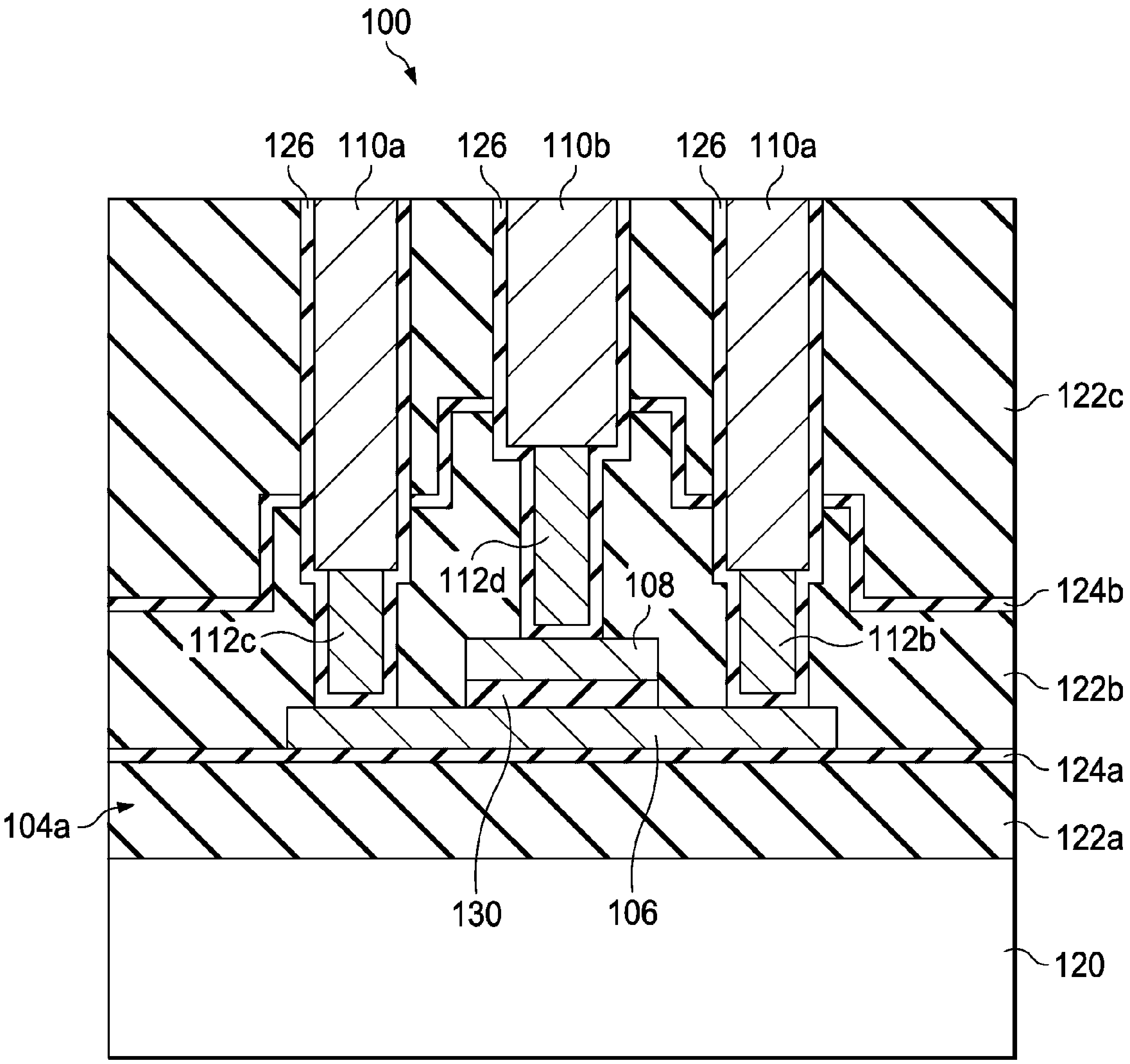

100
126
110a
126
110b
126
110a
122c
124b
112d
108
112c
112b
122b
124a
104a
122a
130
106
120

FIG. 5

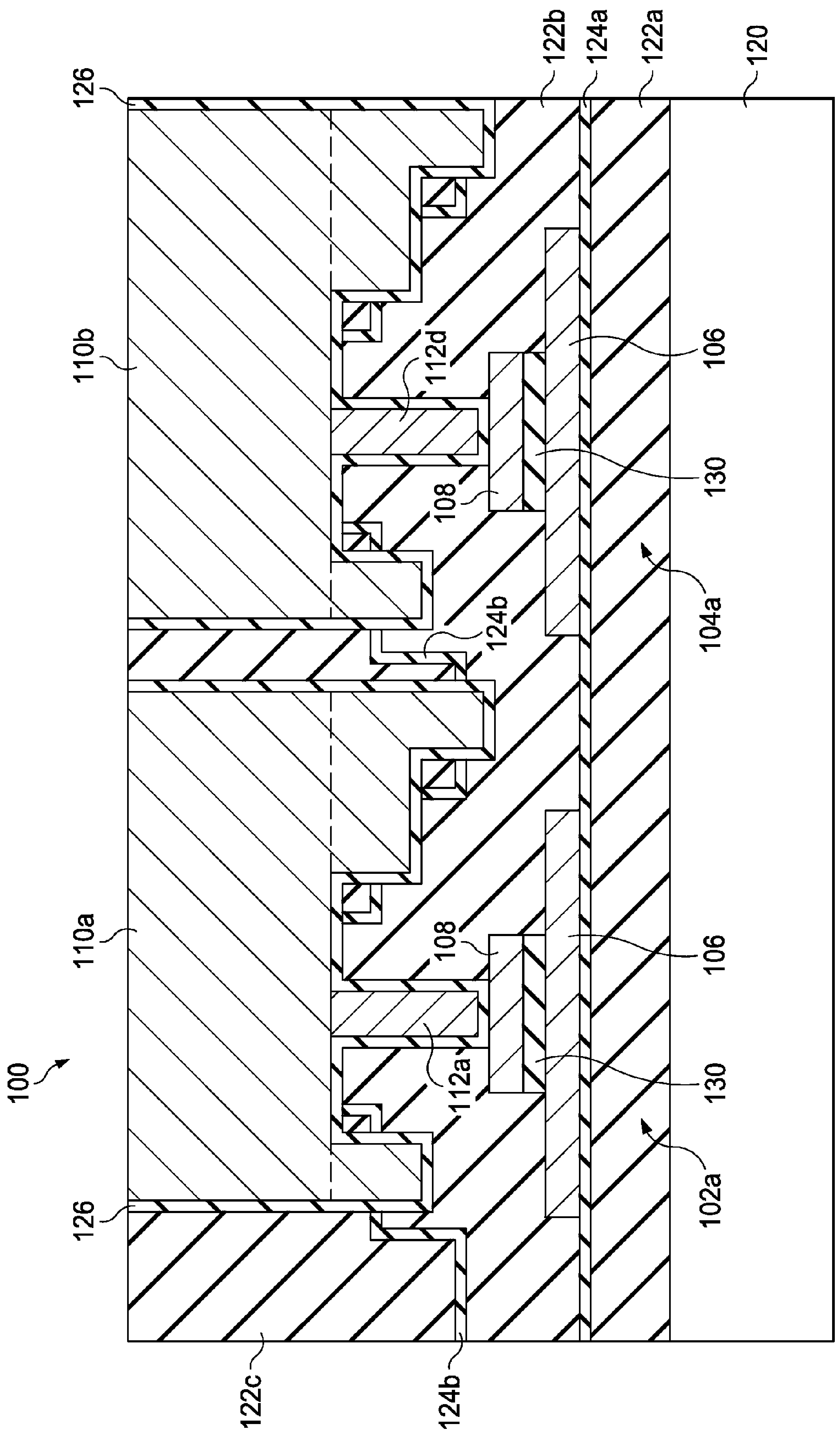

100
126
110a
110b
126
122b
124a
122a
120
112d
106
130
108
104a
124b
108
106
130
112a
102a
122c
124b

FIG. 6

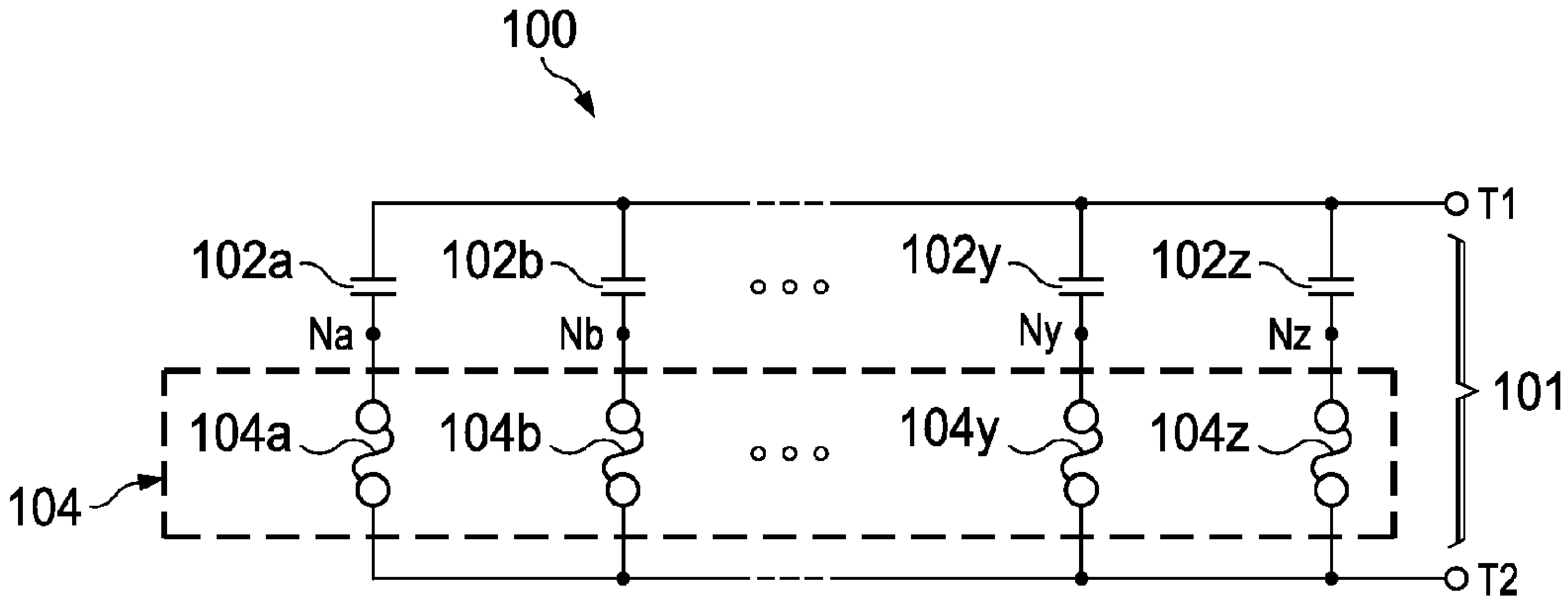

100
T1
102a
102b
102y
102z
Na
Nb
Ny
Nz
101
104a
104b
104y
104z
104
T2

FIG. 7

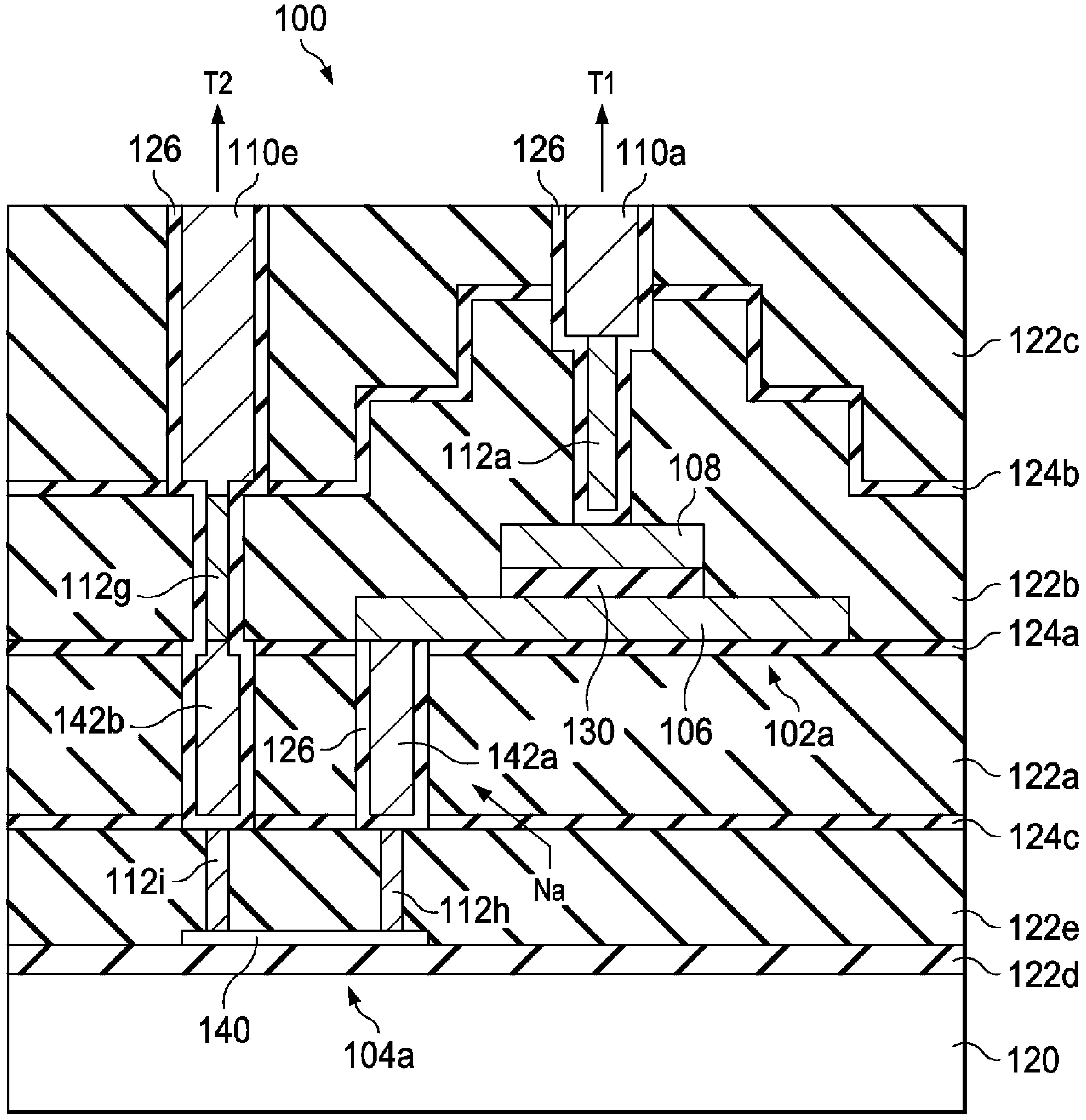

100
T2
126
110e
T1
126
110a
122c
112a
108
124b
112g
122b
124a
142b
126
142a
130
106
102a
122a
124c
112i
Na
112h
122e
122d
140
104a
120

FIG. 8

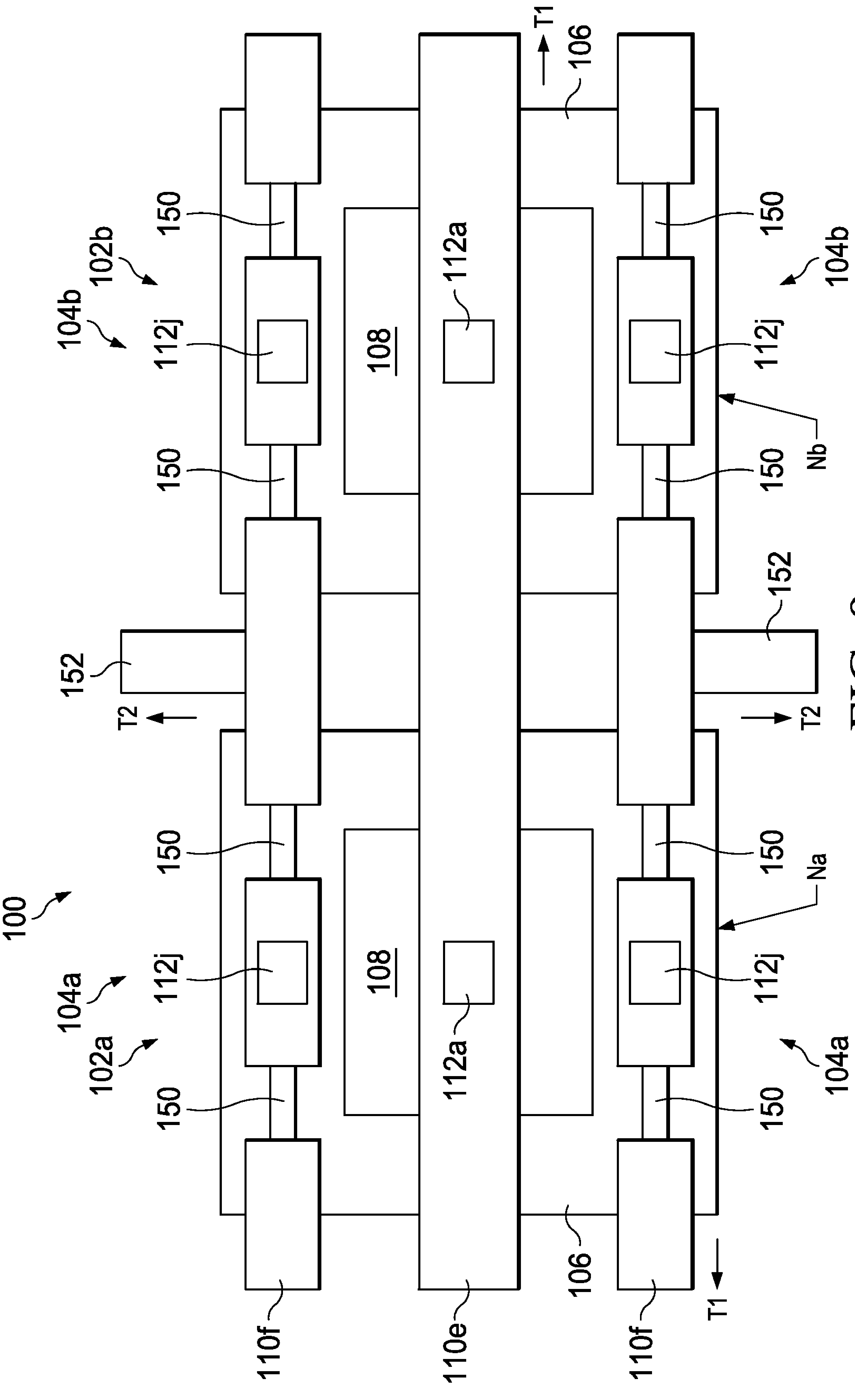

100
102a
102b
104a
104b
106
108
110e
110f
112a
112j
150
152
Na
Nb
T1
T2

FIG. 9

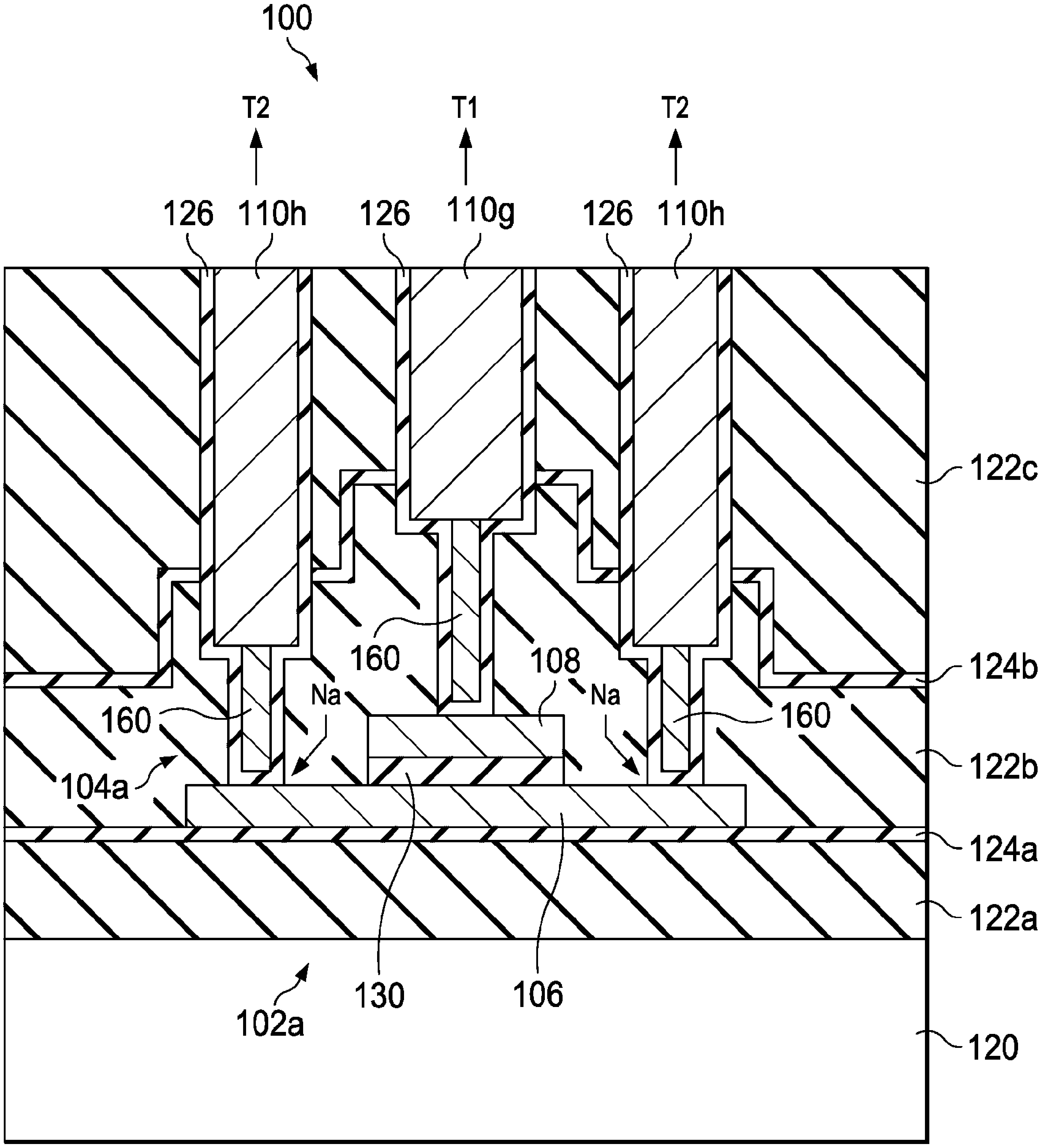

100
T2
T1
T2
126
110h
126
110g
126
110h
122c
160
160
108
Na
Na
160
124b
104a
122b
124a
122a
102a
130
106
120

FIG. 10

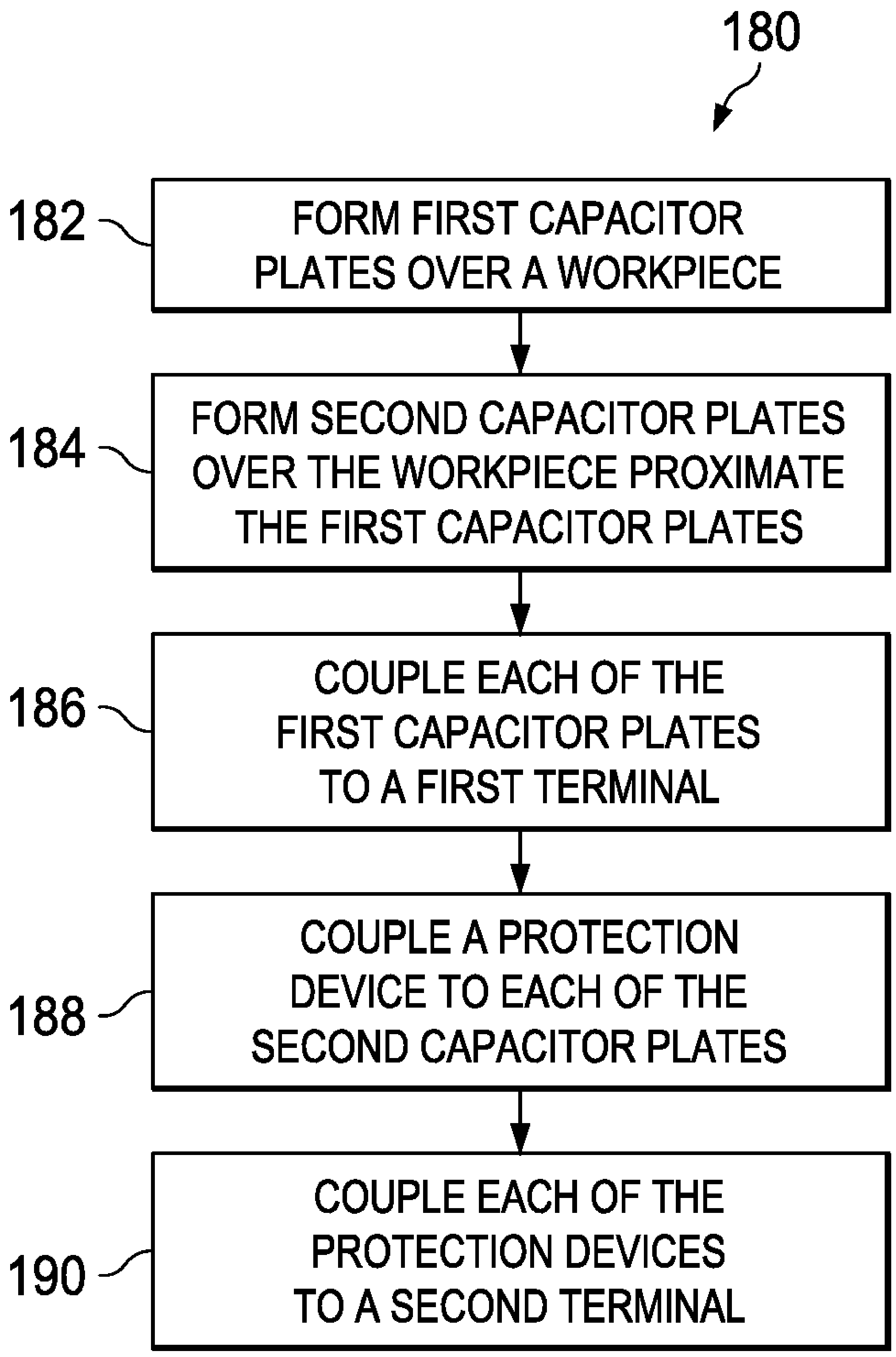

180
182
FORM FIRST CAPACITOR PLATES OVER A WORKPIECE
184
FORM SECOND CAPACITOR PLATES OVER THE WORKPIECE PROXIMATE THE FIRST CAPACITOR PLATES
186
COUPLE EACH OF THE FIRST CAPACITOR PLATES TO A FIRST TERMINAL
188
COUPLE A PROTECTION DEVICE TO EACH OF THE SECOND CAPACITOR PLATES
190
COUPLE EACH OF THE PROTECTION DEVICES TO A SECOND TERMINAL

FIG. 11

SEMICONDUCTOR DEVICES, METHODS OF MANUFACTURE THEREOF, AND CAPACITORS

BACKGROUND

Semiconductor devices are used in a variety of electronic applications, such as personal computers, cell phones, digital cameras, and other electronic equipment, as examples. Semiconductor devices are typically fabricated by sequentially depositing insulating or dielectric layers, conductive layers, and semiconductive layers of material over a semiconductor substrate, and patterning the various material layers using lithography to form circuit components and elements thereon.

Capacitors are elements that are used extensively in semiconductor devices for storing an electrical charge. Capacitors essentially comprise two conductive plates separated by an insulating or dielectric material. Capacitors are used in applications such as electronic filters, analog-to-digital converters, memory devices, control applications, and many other types of semiconductor device applications.

In some semiconductor devices, power lines and ground lines are routed to logic gates and other devices in integrated circuits. The current from a power supply flows through the power lines, logic gates, and finally to ground. During switching of the logic gates, a large amount of change in the current occurs within a short period of time. Decoupling capacitors are used to absorb these glitches during current switching. Decoupling capacitors are also used to maintain a constant voltage between the supply voltage and ground. The decoupling capacitors act as charge reservoirs that additionally supply current to circuits when required, to prevent momentary drops in the supplied voltage.

One type of decoupling capacitor used is referred to as a metal-insulator-metal (MIM) capacitor. A MIM capacitor has two metal layers and a dielectric insulator layer between the two metal layers. A capacitance is formed between the two metal layers. MIM capacitors are often fabricated in interconnect layers of a semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** is a schematic of a semiconductor device that includes a protection structure that comprises a plurality of protection devices for capacitors in accordance with some embodiments of the present disclosure;

FIG. **2** illustrates the schematic of FIG. **1** after one of the capacitors has failed in accordance with some embodiments;

FIG. **3** is a schematic of a semiconductor device wherein the protection devices comprise redundant capacitors in accordance with some embodiments;

FIG. **4** is a top view of a semiconductor device illustrating a configuration for a protection device comprising a redundant capacitor and a capacitor coupled to the protection device in accordance with some embodiments;

FIG. **5** is a cross-sectional view of the semiconductor device shown in FIG. **4** at view **5-5'**;

FIG. **6** is a cross-sectional view of the semiconductor device shown in FIG. **4** at view **6-6'**;

FIG. **7** is a schematic of a semiconductor device wherein the protection devices comprise fuses in accordance with some embodiments;

FIG. **8** is a cross-sectional view of a semiconductor device wherein a protection device comprising a fuse comprises a segment of semiconductive material in accordance with some embodiments;

FIG. **9** is a top view of a semiconductor device wherein a protection device comprising a fuse comprises a portion of a conductive line in accordance with some embodiments;

FIG. **10** is a cross-sectional view of a semiconductor device wherein a protection device comprising a fuse comprises a conductive via in accordance with some embodiments; and

FIG. **11** is a flow chart of a method of manufacturing a semiconductor device in accordance with some embodiments.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of some of the embodiments of the present disclosure are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosure, and do not limit the scope of the disclosure.

Some embodiments of the present disclosure are related to semiconductor devices that include large-area capacitors and methods of manufacture thereof. Novel large-area capacitors that include protection structures and devices will be described herein.

FIG. **1** is a schematic of a semiconductor device **100** that includes a large-area capacitor **101** that includes a plurality of capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* and a protection structure **104** in accordance with some embodiments. The protection structure **104** includes a plurality of protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* for the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* in accordance with some embodiments of the present disclosure. Each of the plurality of protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* is coupled in series with one of the plurality of capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* in accordance with some embodiments, e.g., between a first terminal T**1** and a second terminal T**2**. The protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* of the protection structure **104** comprise redundant capacitors or fuses in some embodiments, which will be described further herein.

The large-area capacitor **101** of the semiconductor device **100** in some embodiments has an overall width and/or length in a top view of about a few hundred micrometers (μm) to about several centimeters (cm) in some embodiments. The large-area capacitor **101** includes about 1,000 or more of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* and protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* in some embodiments. Alternatively, the large-area capacitor **101** may comprise other dimensions and may include fewer than 1,000 of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* and protection devices **104***a*, **104***b* . . . **104***y*, and **104***z*. The large-area capacitor **101** comprises a metal-insulator-metal (MIM) capacitor in some embodiments. The large-area capacitor **101** may be formed in a plurality of metallization layers of the semiconductor device **100**, for example. The large-area capacitor **101** may comprise a decoupling capacitor in some applications. Alternatively, the large-area capacitor **101** may comprise other functions. The protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* prevent failure of the large-area capacitor **101**, to be described further herein.

A plurality of the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* is shown in FIG. **1**; however, in accordance with some embodiments, only one protection device **104***a* is coupled to a single capacitor **102***a* in series between the two terminals T**1** and T**2**. At least one of the other capacitors **102***b* . . . **102***y*, and **102***z* does not include a protection device **104***b* . . . **104***y*, and **104***z* coupled in series (not shown), in some embodiments. For example, in some embodiments, a semiconductor device **100** comprises a first capacitor **102***a* shown in FIG. **1**, and a protection device **104***a* is coupled in series with the first capacitor **102***a*. A second capacitor **102***b* is coupled in parallel with the first capacitor **102***a* and the protection device **104***a* (e.g., the protection device **104***b* is not included, and the bottom plate of the second capacitor **102***b* is coupled to the second terminal T**2**). In embodiments wherein the protection device **104***a* comprises a redundant capacitor, the protection device **104***a* comprises a third capacitor, for example.

In other embodiments, a second protection device **104***b* is coupled in series with the second capacitor **102***b* as shown in FIG. **1**, and the second capacitor **102***b* and the second protection device **104***b* are coupled in parallel with the first capacitor **102***a* and the first protection device **104***a*, also shown in FIG. **1**.

In some embodiments, the large-area capacitor **101** comprises a capacitor having a plurality of first plates and a plurality of second plates. For example, in FIG. **1**, each of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* includes a top plate which is also referred to herein as a first plate. The first plate of each of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* is coupled to the first terminal T**1**. Each of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* also includes a bottom plate which is also referred to herein as a second plate. Each of the plurality of second plates is coupled to the second terminal T**2** (e.g., by a protection device **104***a*, **104***b* . . . **104***y*, and **104***z*). Each of the second plates is disposed proximate one of the first plates. The first plates and the second plates may be separated from one another by a capacitor dielectric in some embodiments (see capacitor dielectric **130** shown in FIG. **5**). A protection device **104***a*, **104***b* . . . **104***y*, and/or **104***z* is coupled between one of the second plates and the second terminal T**2**, wherein the protection device **104***a*, **104***b* . . . **104***y*, and/or **104***z* comprises a redundant capacitor or a fuse, in some embodiments.

FIG. **2** illustrates the schematic of FIG. **1** after one of the capacitors **102***b*' has a failure in accordance with some embodiments. The protection device **104***b*' coupled in series with the failed capacitor **102***b*' advantageously prevents the failure of the overall large-area capacitor **101**. For example, in an event that the failed capacitor **102***b*' has an early failure caused by process defects such as particle or pinholes on a capacitor dielectric of the capacitor **102***b*', a reliability failure during a service life of the semiconductor device **100** in a field application, or other types of failures, a short may form in the failed capacitor **102***b*'. In some embodiments wherein the protection device **104***b*' comprises a redundant capacitor, the associated redundant capacitor remains connected and functional in the circuit, protecting the overall large-area capacitor **101** from a catastrophic failure. In embodiments wherein the protection device **104***b*' comprises a fuse, the fuse is “blown” and turns into an open circuit which also protects the large-area capacitor **101** from a catastrophic failure, because the other capacitors **102***a* . . . **102***y*, and **102***z* are isolated from the failed capacitor **102***b*' and remain intact and functional.

FIG. **3** is a schematic of a semiconductor device **100** wherein the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* of the protection structure **104** comprise redundant capacitors. The top plates of the redundant capacitors of the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are coupled to the bottom plates of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* at nodes Na, Nb . . . Ny, and Nz, respectively. The bottom plates of the redundant capacitors of the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are coupled to the second terminal T**2**.

FIG. **4** is a top view of a semiconductor device **100** illustrating a configuration for a protection device **104***a* comprising a redundant capacitor and a capacitor **102***a* coupled to the protection device **104***a* in accordance with some embodiments. FIG. **5** is a cross-sectional view of the semiconductor device **100** shown in FIG. **4** at view **5**-**5**', and FIG. **6** is a cross-sectional view of the semiconductor device **100** shown in FIG. **4** at view **6**-**6**'. A portion of the large-area capacitor **101** shown in the schematic of FIG. **3** is shown in FIGS. **4**, **5**, and **6**.

The protection device **104***a* may be formed in the same metallization layers that the capacitor **102***a* is formed in, as shown in FIG. **6**. The protection device **104***a* may be positioned adjacent, e.g., along-side and/or proximate the capacitor **102***a* in some embodiments, as shown in FIGS. **4** and **6**. Alternatively, the protection device **104***a* may not be formed in the same metallization layers that the capacitor **102***a* is formed in, and protection device **104***a* may be spaced apart from the capacitor **102***a* in other embodiments, not shown.

The capacitor **102***a* and protection device **104***a* comprising the redundant capacitor both include a bottom plate **106**, a capacitor dielectric **130** disposed over the bottom plate **106**, and a top plate **108** disposed over the capacitor dielectric **130**. In some embodiments, the bottom plate **106** and the top plate **108** comprise MIM electrodes, for example. In some embodiments, the bottom plate **106** is larger than the top plate **108** to permit landing of conductive vias on the bottom plate **106** to make electrical connection to the bottom plate **106**. For example, conductive vias **112***b* and **112***c* are coupled to the bottom plate **106** of the protection device **104***b* (see FIGS. **4** and **5**), and conductive vias **112***e* and **112***f* are coupled to the bottom plate of the capacitor **102***a* (see FIG. **4**).

The capacitor **102***a* and the protection device **104***a* comprising the redundant capacitor may be coupled together using a conductive line **110***a* in some embodiments, as shown in FIGS. **4** and **5**. The conductive line **110***a* comprises node Na shown in FIG. **3**, for example. The conductive line **110***a* comprises a pronged shape in the top view in some embodiments. Alternatively, the conductive line **110***a* may comprise other shapes, and the capacitor **102***a* and protection device **104***a* can be coupled together in other configurations and methods. The conductive line **110***a* is coupled to the top plate **108** of the capacitor **102***a* by a conductive via **112***a* and to the bottom plate **106** of the protection device **104***b* comprising the redundant capacitor by conductive vias **112***b* and **112***c*.

The top plate **108** of the protection device **104***b* is coupled to a conductive line **110***b* by a conductive via **112***d*. The conductive line **110***b* is coupled elsewhere on the semiconductor device **100** to the second terminal T**2**. The bottom plate **106** of the capacitor **102***a* is coupled to conductive lines **110***c* and **110***d* by conductive vias **112***e* and **112***f*, respectively. The conductive lines **110***c* and **110***d* are coupled elsewhere on the semiconductor device **100** to the first terminal T**1**.

In some embodiments, the overall high-area capacitor **101** comprises a high-value capacitor having a capacitance of on the order of hundreds of nano-farads that is comprised of thousands of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* that comprise smaller-area MIM units, for example.

The cross-sectional views shown in FIGS. **5** and **6** illustrate various other material layers and components of the semiconductor device **100** in accordance with some embodiments. To manufacture the semiconductor device **100**, first, a workpiece **120** is provided. The workpiece **120** may include a semiconductor substrate comprising silicon or other semiconductor materials and may be covered by an insulating layer, for example. The workpiece **120** may also include other active components or circuits, not shown. The workpiece **120** may comprise silicon oxide over single-crystal silicon, for example. The workpiece **120** may include conductive layers or elements, e.g., transistors, diodes, resistors, inductors, etc., not shown. Compound semiconductors, GaAs, InP, Si/Ge, or SiC, as examples, may be used in place of silicon. The workpiece **120** may comprise a silicon-on-insulator (SOI) or a germanium-on-insulator (GOI) substrate, as examples.

In some embodiments, the workpiece **120** comprises a silicon interposer that is adapted to be used for packaging one or more integrated circuit dies in a 2.5 dimensional (D) or 3D packaging scheme, for example. The workpiece **120** may include wiring and redistribution layers (RDLs), not shown, that are adapted to provide electrical connections between multiple integrated circuit dies coupled to the workpiece **120**.

An insulating material layer **122***a* is formed over the workpiece **120** using a deposition process, and an etch stop layer **124***a* is formed over the insulating material layer **122***a*, in some embodiments. The insulating material layer **122***a* may comprise silicon dioxide, silicon oxynitride, carbon-doped silicon oxide, a spin-on glass, a spin-on polymer, or other insulators, and the etch stop layer **124***a* may comprise silicon nitride, silicon oxynitride, silicon carbide, oxygen-doped silicon carbide, nitrogen-doped silicon carbide, or other insulators having an etch selectivity to the insulating material layer **122***a*, as examples. The insulating material layer **122***a* may comprise a thickness of about 10 nm to about 1,000 nm, and the etch stop layer **124***a* may comprise a thickness of about 10 nm to about 100 nm, as examples. Alternatively, the insulating material layer **122***a* and the etch stop layer **124***a* may comprise other materials and dimensions.

A conductive material such as copper, a copper alloy, or other conductors is formed over the etch stop layer **124***a*. The conductive material is patterned using a lithography process and etch process to form the bottom plates **106** of the capacitor **102***a* and the protection device **104***a* in some embodiments. Alternatively, the bottom plates **106** may be formed using a damascene and/or plating process, by forming an insulating material (e.g., a portion of insulating material layer **122***b*) over the etch stop layer **124***a*, patterning the insulating material, and filling the patterned insulating material with a conductive material to form the bottom plates **106**. Excess conductive material may be removed from over a top surface of the insulating material using a chemical-mechanical polishing (CMP) process and/or etch process. Each of the bottom plates **106** may comprise a thickness of about 100 nm to about 2,000 nm and a width of about 10 μm to about 500 μm, as examples. Alternatively, the bottom plates **106** may comprise other dimensions.

A capacitor dielectric **130** is formed over the bottom plates **106**. The capacitor dielectric **130** may comprise an insulator such as silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, a metal oxide, a polymer, a laminate of a plurality of different dielectric films, or other dielectric materials. The capacitor dielectric **130** may comprise a thickness of about 5 nm to about 50 nm, for example. Alternatively, the capacitor dielectric **130** may comprise other materials and dimensions.

A conductive material comprising similar materials as described for the conductive material of the bottom plates **106** in some embodiments is formed over the capacitor dielectric **130**. The conductive material is patterned using lithography to form the top plates **108** of the capacitor **102***a* and the protection device **104***a* comprising the redundant capacitor. The capacitor dielectric **130** is also patterned during the etching process used to form the top plates **108** in some embodiments. Alternatively, the capacitor dielectric **130** may be patterned using a separate lithography and etch step, in other embodiments. Each of the top plates **108** may comprise a thickness of about 100 nm to about 2,000 nm and a width of about 10 μm to about 500 μm, as examples. Alternatively, the top plates **108** may comprise other dimensions.

An insulating material layer **122***b* is formed over the top plates **108**, exposed portions of the bottom plates **106**, and exposed portions of the etch stop layer **124***a*. The insulating material layer **122***b* comprises similar materials and dimensions as described for insulating material layer **122***a* in some embodiments. The insulating material layer **122***b* conforms to the shape of the underlying capacitor **102***a* or protection device **104***a* in some embodiments, as shown in FIGS. **5** and **6**. In other embodiments, the insulating material layer **122***b* may have a flat top surface or the insulating material layer **122***b* may be planarized so that it has a flat top surface, not shown.

An etch stop layer **124***b* comprising similar materials and dimensions as described for etch stop layer **124***a* is formed over the insulating material layer **122***b*. An insulating material layer **122***c* comprising similar materials and dimensions as described for insulating material layers **122***a* and **122***b* is formed over the etch stop layer **124***b*.

The conductive lines **110***a*, **110***b*, **110***c*, and **110***d* and conductive vias **112***a*, **112***b*, **112***c*, **112***d*, **112***e*, and **112***f* (which are not all shown in FIGS. **5** and **6**; see FIG. **4**) are formed in the insulating material layer **122***c*, the etch stop layer **124***b*, and the insulating material layer **122***b* using a damascene process which may comprise a single damascene or dual damascene process in some embodiments. For example, the insulating material layer **122***c*, etch stop layer **124***b*, and insulating material layer **122***b* are patterned using a lithography and etch process, and the patterns in the insulating material layer **122***c*, etch stop layer **124***b*, and insulating material layer **122***b* are filled with a conductive material to form the conductive lines **110***a*, **110***b*, **110***c*, and **110***d* and conductive vias **112***a*, **112***b*, **112***c*, **112***d*, **112***e*, and **112***f*. The conductive lines **110***a*, **110***b*, **110***c*, and **110***d* and conductive vias **112***a*, **112***b*, **112***c*, **112***d*, **112***e*, and **112***f* may include a liner **126** and a conductive material such as copper or a copper alloy formed over the liner **126**, in some embodiments. The liner **126** may comprise a barrier layer and/or seed layer, as examples. In some embodiments, the liner **126** is not included. In some embodiments, the conductive lines **110**_a_, **110**_b_, **110**_c_, and **110**_d_ and conductive vias **112**_a_, **112**_b_, **112**_c_, **112**_d_, **112**_e_, and **112**_f_ may be formed using subtractive etch processes.

In some embodiments, the conductive lines **110**_a_ and **110**_b_ (and also the other conductive lines) may include downwardly-extending portions, as shown in FIG. **6**, for example, in embodiments wherein the top surface of insulating material layer **122**_b_ is not planar. The conductive lines **110**_a_, **110**_b_, **110**_c_, and **110**_d_ may comprise a width in a top view of about 0.1 μm to about 10 μm, and the conductive vias **112**_a_, **112**_b_, **112**_c_, **112**_d_, **112**_e_, and **112**_f_ may comprise a width in a cross-sectional view of about 0.01 μm to about 1 μm, as examples. In other embodiments, the conductive lines **110**_a_ and **110**_b_ may not include downwardly-extending portions, e.g., wherein the top surface of insulating material layer **122**_b_ comprises a flat surface.

The materials and dimensions described for the workpiece **102**, insulating materials **122**_a_, **122**_b_, and **122**_c_, etch stop layers **124**_a_ and **124**_b_, bottom and top plates **106** and **108**, capacitor dielectric **130**, liner **126**, and conductive lines **110**_a_, **110**_b_, **110**_c_, and **110**_d_ and conductive vias **112**_a_, **112**_b_, **112**_c_, **112**_d_, **112**_e_, and **112**_f_ may alternatively comprise other materials and dimensions, in accordance with embodiments of the present disclosure. Likewise, other methods may be used to form the novel large-area capacitor **101** that includes the capacitors **102**_a_ and protection devices **104**_a_.

FIG. **7** is a schematic of a semiconductor device **100** wherein the protection devices **104**_a_, **104**_b_ . . . **104**_y_, and **104**_z_ of the protection structure **104** of the large-area capacitor **101** comprise fuses in accordance with some embodiments. The fuses may comprise a semiconductive material as shown in FIG. **8**, a conductive line as shown in FIG. **9**, or a conductive via as shown in FIG. **10**, in accordance with some embodiments of the present disclosure. The fuses have a higher resistance than the conductive material of the adjacent elements they are connected to, in some embodiments. The fuses will burn out to form an open circuit if a current higher than a predetermined limit or amount is forced through or passed through them. As a result, if the corresponding capacitor **102**_a_ that the fuse protects fails, the failed capacitor **102**_a_ is electrically isolated and therefore the overall large-area capacitor **101** continues to perform its intended function.

For example, FIG. **8** is a cross-sectional view of a semiconductor device **100** wherein a protection device **104**_a_ comprising a fuse comprises a segment of semiconductive material **140** in accordance with some embodiments. The fuse may be formed in some embodiments by forming an insulating material layer **122**_d_ over the workpiece **120**, and forming a layer of polysilicon or other type of semiconductive material over the insulating material layer **122**_d_. The layer of semiconductive material is patterned using a lithography process and etch process to form the segment which comprises the semiconductive material. The segment of semiconductive material **140** may comprise width of about 1 nm to about 100 nm, a thickness of about 1 nm to about 50 nm, and a width in a top view (not shown) of about 1 nm to about 100 nm in some embodiments. Alternatively, the segment of semiconductive material **140** may comprise other dimensions. In some embodiments, the dimensions of the fuse comprising the segment of semiconductive material **140** are of a sufficient size so that if the capacitor **102**_a_ fails and is electrically shorted, the fuse is 'blown' and is changed to an open position, isolating the failed capacitor **102**_a_ from the other capacitors **102**_b_ . . . **102**_y_, and **102**_z_ of the capacitor

101. Before the capacitor **102**_a_ fails, the fuse is in a closed position wherein current may flow through the fuse, for example.

One end of the protection device **104**_a_ comprising the segment of semiconductive material **140** is coupled to the bottom plate **106** of the capacitor **102**_a_ by a conductive via **112**_h_ formed in insulating material layer **122**_e_ and a conductive plug **142**_a_ which is formed in etch stop layer **124**_c_ and insulating material layer **122**_a_. The other opposing end of the segment of semiconductive material **140** is coupled to terminal T2 by a conductive via **112**_i_ formed in insulating material layer **122**_e_, a conductive plug **142**_b_ formed in etch stop layer **124**_c_, insulating material layer **122**_a_, and etch stop layer **124**_a_, a conductive via **122**_g_ formed in insulating material layer **122**_b_, and a conductive plug **110**_e_ formed in etch stop layer **124**_b_ and insulating material layer **122**_c_. In some embodiments, the segment of semiconductive material **140** is disposed between neighboring capacitor electrodes (e.g., the plates **106** and/or **108**), for example.

FIG. **9** shows a top view of a semiconductor device **100** wherein protection device **104**_a_ comprise fuses that comprise a portion **150** of a conductive line **110**_f_ in accordance with some embodiments. The portions **150** of the conductive lines **110**_f_ have a higher resistance than the other portions of the conductive lines **110**_f_ because of their decreased width, for example. The portions **150** of the conductive lines **110**_f_ have a higher electrical resistance, due to a reduction of the conductive line **110**_f_ cross-section, in some embodiments. The conductive lines **110**_f_ are coupled to the bottom plates **106** by conductive vias **112**_j_ in the embodiments shown. If the capacitor **102**_a_ fails, one or more of the portions **150** of the conductive lines **110**_f_ will burn out to isolate the faulty capacitor **102**_a_, so that the overall capacitor **101** survives.

Two capacitors **102**_a_ and **102**_b_ are shown in FIG. **9**. Capacitor **102**_a_ includes four portions **150** of conductive lines **110**_f_ coupled thereto that function as fuses because of their decreased width. The length of the portions **150** in the top view may comprise about 100 nm to about 10 μm in some embodiments. The width of the portions **150** in the top view may comprise about 10 nm to about 1 μm in some embodiments. The thickness of the portions **150** of the conductive lines **110**_f_ is substantially the same as the thickness of the conductive lines **110**_f_, which may be about 100 nm to about 2,000 nm in some embodiments, for example. Alternatively, the portions **150** of the conductive lines **110**_f_ may comprise other dimensions.

Capacitor **102**_b_ also includes four portions **150** of conductive lines **110**_f_ coupled thereto that function as a fuse protection device **104**_b_ in FIG. **9**. Alternatively, the protection devices **104**_a_ and **104**_b_ may include other numbers of portions **150** of conductive lines; e.g., only one portion **150**, or two or more portions **150** of conductive lines may be used as a fuse type of protection device **104**_a_ or **104**_b_ coupled to a capacitor **102**_a_, **102**_b_ . . . **102**_y_, and **102**_z_ in accordance with some embodiments. FIG. **9** also illustrates a portion **152** of the conductive lines **110**_f_ that may be coupled to terminal T2 in some embodiments. In some embodiments, the narrowed portions **150** of conductive lines **110**_f_ with higher resistance are disposed between neighboring capacitor electrodes, for example.

FIG. **10** is a cross-sectional view of a semiconductor device **100** wherein a protection device **104**_a_ comprising a fuse comprises one or more conductive vias **160** in accordance with some embodiments. The conductive vias **160** are coupled to the bottom plate **106** and/or top plate **108** of the capacitor **102**_a_ and have a higher resistance than the plates **106** and **108** and conductive plugs **110**_g_ and **110**_h_, for example. The conductive via or vias **160** are formed within insulating material layer **122**b. Three conductive vias **160** are shown in FIG. **10**; two coupled to the bottom plate **106** of the capacitor **102**a and one coupled to the top plate **108**. The two conductive vias **160** coupled to the bottom plate **106** are coupled to terminal T**2** by conductive plugs **110**h formed within insulating material layer **122**c, etch stop layer **124**b, and insulating material layer **122**b. Note that the conductive via **160** coupled to the top plate **108** is coupled to terminal T**1** rather than to terminal T**2** and is not shown in the schematic of FIG. **7**. The conductive via **160** coupled to the top plate **108** is coupled to terminal T**1** by a conductive plug **110**g formed within insulating material layer **122**c, etch stop layer **124**b, and insulating material layer **122**b.

Only one conductive via **160** may be included in the capacitor **101** as a fuse type of protection device **104**a in accordance with some embodiments, coupled either to the top plate **108** or the bottom plate **106**. Alternatively, the protection device **104**a may comprise two or more of the conductive vias **160** that function as fuses. The length of the conductive vias **160** may comprise about 10 nm to about 1,000 nm in some embodiments. The width of the conductive vias **160** may comprise about 0.01 μm to about 1 μm in some embodiments. Alternatively, the conductive vias **160** may comprise other dimensions.

The conductive vias **160** may include a liner **126** and may be formed during the formation of conductive plugs **110**g and **110**h using a dual damascene process. The conductive vias **160** comprise the same material as the conductive plugs **110**g and **110**h in these embodiments. Alternatively, the conductive vias **160** may not include a liner **126**. In some embodiments, the conductive vias **160** may be formed in a single damascene process, and may comprise a different material or the same material as the conductive plugs **110**g and **110**h. In some embodiments, the conductive vias **160** may comprise a material that is less conductive and has a higher resistance than the material of the conductive lines **110**g and **110**h, such as tungsten, aluminum, titanium, tantalum, tantalum nitride, titanium nitride, or other conductors, which is advantageous in that the conductive vias **160** comprising the fuses may more easily "blow" if the capacitor **102**a fails.

In some embodiments, if the capacitor **102**a fails, an electrical current forced through one of the conductive vias **160** leads to local burn-out of the conductive via **160** due to Joule's heating, thus causing an open circuit of the conductive via **160**, for example.

In some embodiments wherein the conductive vias **160** include a liner **126**, the liner **126** may include a barrier layer and/or a seed layer. The barrier layer may comprise a metal and the seed layer may comprise copper in some embodiments, as examples. In some embodiments, a pinch-off may be formed near the end of the formation of a portion of the liner **126** (e.g., comprising the barrier liner and/or seed layer) to form higher electrical resistance conductive vias **160**, e.g., due to a decrease of an amount of the barrier layer and/or seed layer in the conductive via **160** which is caused by the pinch-off process. For example, the barrier layer and/or seed layer formation process may have different step coverage capabilities by tuning the process parameters thereof. For a dual damascene structure, the conductive via **160** openings may be closed up (i.e., pinched off) by the barrier layer at the end of barrier layer formation process or by the seed layer at the beginning of seed layer formation process, e.g., so that the seed layer will not be deposited inside the trenches for the conductive vias **160**, but will be deposited only inside the trenches for the conductive plugs **110**g and **110**h. As a result, in a subsequent electroplating process or other process used to fill the trenches for the conductive vias **160** and the conductive plugs **110**g and **110**h, the conductive fill material (i.e., comprising Cu or other type of conductive material) will be deposited only inside the trenches for the conductive plugs **110**g and **110**h, but not inside the trenches for the conductive vias **160**, therefore forming conductive vias **160** that comprise high-resistance via fuses.

The embodiments shown in FIGS. **9** and **10** are particularly advantageous in some applications, because a minimal manufacturing process flow and/or design change is required to implement the protection devices **104**a and **104**b. For example, in FIG. **9**, a change in the design of the conductive lines **110**f to include the portions **150** that have a smaller width than the remainder of the conductive lines **110**f is all that is required. Similarly, in FIG. **10**, a change in the design of conductive vias that would ordinarily be coupled to the bottom plate **106** or top plate **108** (e.g., see conductive vias **112**b, **112**c, and **112**d in FIG. **5**) is all that is required, to decrease the width or diameter of the conductive vias **160** or alter the liner **126** or prohibit or limit the formation of the liner **126** so that the vias function as fuses.

Note that in the embodiments shown in FIGS. **7** through **10**, the insulating material layers **122**d and **122**e may comprise similar materials and dimensions as described for insulating material layers **122**a, **122**b, and **122**c shown in FIGS. **5** and **6**. Likewise, the etch stop layer **124**c may comprise similar materials and dimensions as described for etch stop layers **124**a and **124**b shown in FIGS. **5** and **6**.

FIG. **11** is a flow chart **180** of a method of manufacturing a semiconductor device **100** in accordance with some embodiments. In step **182**, first capacitor plates **106** are formed over a workpiece **120** (see also FIG. **6** and FIG. **1**; the first capacitor plates comprise the top plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z). In step **184**, second capacitor plates **108** (e.g., comprising the bottom plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z in FIG. **1**) are formed over the workpiece **120** proximate the first capacitor plates **106**. In step **186**, each of the first capacitor plates is coupled to a first terminal T**1** (see also FIG. **1**). In step **188**, a protection device **104**a, **104**b . . . **104**y, and **104**z is coupled to each of the second capacitor plates (e.g., comprising the bottom plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z in FIG. **1**). In step **190**, each of the protection devices **104**a, **104**b . . . **104**y, and **104**z is coupled to a second terminal T2.

The order in which the various steps **182**, **184**, **186**, **188**, and **190** are performed is not limited to the order illustrated in the flow chart **180** shown in FIG. **11**. For example, in some embodiments, i.e., in the embodiments shown in FIGS. **3** through **6**, the protection devices **104**a, **104**b . . . **104**y, and **104**z are formed simultaneously with the formation of the capacitor plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z. For example, step **188** is formed simultaneously with steps **182** and **184** in some embodiments. In other embodiments, i.e., in the embodiments shown in FIGS. **7** and **8**, the protection devices **104**a, **104**b . . . **104**y, and **104**z comprising a polysilicon fuse **140** are formed before the formation of the capacitor plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z. For example, step **188** is formed before steps **182** and **184** in some embodiments. In other embodiments, i.e., in the embodiments shown in FIGS. **7** and **10**, the protection devices **104**a, **104**b . . . **104**y, and **104**z comprising via fuses are formed simultaneously with the coupling of the capacitor plates of the capacitors **102**a, **102**b . . . **102**y, and **102**z. For example, step **188** is formed simultaneously with step **186** and also step **190** in some embodiments. Alternatively, the various steps **182**, **184**, **186**, **188**, and **190** of the flow chart **180** may be performed before, after, or simultaneously with other steps **182**, **184**, **186**, **188**, and **190** and/or other manufacturing process steps of the semiconductor device **100**.

Coupling the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* comprises coupling a redundant capacitor or a fuse in some embodiments. The plurality of first capacitor plates and the plurality of second capacitor plates comprise a plurality of capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* coupled together in parallel, and a protection device **104***a*, **104***b* . . . **104***y*, and **104***z* is coupled in series with each of the plurality of capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*, in some embodiments.

In some embodiments, the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are coupled below the plurality of second capacitor plates (e.g., below the bottom plates **106** of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*), e.g., in the embodiments shown in FIGS. **7** and **8**). In other embodiments, the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are coupled or formed in material layers that the plurality of first capacitor plates and the plurality of second capacitor plates of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* are formed in, e.g., in the embodiments shown in FIGS. **4** through **6**. In other embodiments, the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are coupled above the plurality of second capacitor plates of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*, e.g., in the embodiments shown in FIGS. **9** and **10**.

In some embodiments, pairs of the first plates and second plates comprise a plurality of capacitive units (e.g., comprising the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*), and the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* are adapted to self-diagnose and isolate a defaulted one of the plurality of capacitive units.

Some embodiments of the present disclosure include methods of manufacturing semiconductor devices **100**, and also include semiconductor devices **100** manufactured using the methods described herein. Some embodiments of the present disclosure also include capacitors **101** that include the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* and protection structures **104** described herein.

Advantages of some embodiments of the present disclosure include providing novel capacitors **101** that include the protection structures **104** described herein. The protection structures **104** include one or more protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* that comprise redundant capacitors or fuses that are placed in series with the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* of the overall capacitor **101**. The protection structures **104** advantageously provide self-diagnosis and isolation of faulty capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* and prevent catastrophic failure of the capacitor **101**.

In embodiments wherein the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* comprise redundant capacitors, if one of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* fails and a short-circuit is formed through the failed capacitor, the redundant capacitor remains connected in parallel with the functioning capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* so that the capacitor **101** continues to function. In embodiments wherein the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* comprise fuses, the fuse structures turn into open circuits in an event of a failure so that the capacitor **101** continues to function.

In some embodiments, a failure of certain capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* actually results in an increase in the overall capacitance of the capacitor **101**, e.g., in embodiments wherein the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* comprise redundant capacitors. In other embodiments, a failure of certain capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* may result in a slight but substantially negligible decrease in the overall capacitance of the capacitor **101**, e.g., in embodiments wherein the protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* comprise fuses.

In some embodiments, the large-area capacitors **101** can be implemented in semiconductor devices that comprise interposer packages for integrated circuits, and the capacitors **101** comprise a high-value decoupling capacitance, e.g., on the order of hundreds of nano-farads, which effectively attenuates voltage fluctuations that may occur due to simultaneous switching of various circuits, for example. The high capacitance value is achieved by coupling together many of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* together in parallel. The novel protection devices **104***a*, **104***b* . . . **104***y*, and **104***z* provide protection from a complete failure of the large-area capacitor **101** due to a failure of one of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*. If one or more of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* fails, the capacitor **101** continues to function and serve the decoupling purpose.

The protection structure **104** provides a self-protection function for each of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* that can be triggered either by a burn-in screening test in a foundry or in a field application. In an event of a failure of one of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z*, the capacitor **101** survives with nearly zero loss of capacitance, (e.g., substantially negligible) due to the large number of the capacitors **102***a*, **102***b* . . . **102***y*, and **102***z* in the capacitor **101**. In embodiments wherein the protection structure **104** comprises fuses, the integration of the protection structure **104** does not degrade capacitance density of the capacitor **101**, for example.

Although some embodiments of the present disclosure are particularly advantageous when implemented in large-area capacitors that are used for decoupling, the various embodiments disclosed herein also have application in smaller capacitors, capacitors that are not MIM capacitors, and capacitors that are used for other functions than decoupling, as examples.

Implementing the novel protection structures **104** in capacitors **101** of semiconductor devices **100** results in increased manufacturing yields and longer service life in some applications, by preventing or reducing failures of the capacitors **101**. Furthermore, the novel capacitor **101** structures and designs are easily implementable in manufacturing process flows. In some embodiments, no process modifications are needed to implement the protection structure **104**, for example.

In accordance with some embodiments of the present disclosure, a semiconductor device includes a first capacitor and a protection device coupled in series with the first capacitor. A second capacitor is coupled in parallel with the first capacitor and the protection device.

In accordance with other embodiments, a capacitor includes a plurality of first plates, each of the plurality of first plates being coupled to a first terminal. The capacitor includes a plurality of second plates. Each of the plurality of second plates is coupled to a second terminal, and each of the second plates is disposed proximate one of the plurality of first plates. A protection device is coupled between one of the plurality of second plates and the second terminal. The protection device comprises a redundant capacitor or a fuse.

In accordance with other embodiments, a method of manufacturing a semiconductor device includes forming a plurality of first capacitor plates over a workpiece, forming a plurality of second capacitor plates over the workpiece proximate the plurality of first capacitor plates, and coupling each of the plurality of first capacitor plates to a first terminal. A protection device is coupled to each of the plurality of second capacitor plates. Each of the protection devices is coupled to a second terminal.

Although some embodiments of the present disclosure and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present disclosure. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A semiconductor device, comprising:

- a first capacitor, the first capacitor including a bottom capacitor plate formed in a first metallization layer and a top capacitor plate formed in a second metallization layer, the second metallization layer being above the first metallization layer, the bottom capacitor plate and top capacitor plate each having a major surface extending along a first plane;
- a protection device coupled in series with the first capacitor by an electrical connection, the electrical connection including at least one conductive element having an elongated axis that is perpendicular to the first plane;
- a second capacitor coupled in parallel with the first capacitor and the protection device; and
- a dielectric layer over and extending along sidewalls of the first capacitor; and
- an insulating etch-stop layer over and forming a first interface with a first top surface of the dielectric layer and a second interface with a second top surface of the dielectric layer, the second interface being higher than the first interface in a cross-sectional view, the insulating etch-stop layer extending continuously from the first top surface of the dielectric layer to the second top surface of the dielectric layer.

2. The semiconductor device according to claim **1**, wherein the protection device comprises a third capacitor comprising a second bottom capacitor plate formed in the first metallization layer and a second top capacitor plate formed in the second metallization layer.

3. The semiconductor device according to claim **1**, wherein the protection device comprises a fuse.

4. The semiconductor device according to claim **3**, wherein the fuse comprises a first conductive line, wherein the first conductive line is disposed between a second conductive line and a third conductive line along a first line, wherein the first conductive line has a first dimension measured along a second line perpendicular to the first line, wherein the second conductive line has a second dimension measured along the second line, and wherein the first dimension is smaller than the second dimension.

5. The semiconductor device according to claim **3**, wherein the fuse comprises a conductive via having a higher resistance than the top capacitor plate.

6. The semiconductor device according to claim **3**, wherein the fuse comprises a semiconductive material disposed below the first capacitor.

7. The semiconductor device according to claim **1**, wherein the protection device comprises a first protection device, further comprising a second protection device coupled in series with the second capacitor, and wherein the second capacitor and the second protection device are coupled in parallel with the first capacitor and the first protection device.

8. A semiconductor device, comprising:

- a capacitor comprising:
  - a plurality of first plates, each of the plurality of first plates being coupled to a first terminal and each of the plurality of first plates being located in a common first metallization layer on a common first plane;
  - a plurality of second plates, each of the plurality of second plates being coupled to a second terminal, each of the second plates being disposed opposed to a respective one of the plurality of first plates and each of the plurality of second plates being located in a common second metallization layer on a common second plane;
  - a protection device coupled between one of the plurality of second plates and the second terminal, wherein the protection device comprises a redundant capacitor or a fuse;
  - an electrical connector connecting the one of the plurality of second plates to the protection device, the electrical connector including (a) a conductive element located in a third metallization layer different than the first and second metallization layers, the third metallization layer on a third plane different than the first and second planes, and (b) an electrically conductive via extending from the second plane to the third plane, wherein the conductive element is wider than the conductive via in a cross-sectional view;
- a dielectric layer over and extending along sidewalls of the capacitor; and
- an insulating etch-stop layer over and in direct contact with the dielectric layer, the insulating etch-stop layer being made of a different material than the dielectric layer, wherein the conductive element of the electrical connector extends through the insulating etch-stop layer.

9. The semiconductor device according to claim **8**, wherein the protection device comprises a fuse, and wherein the fuse comprises a portion of a conductive line, a conductive via, or a segment comprising a semiconductive material.

10. The semiconductor device according to claim **8**, wherein the capacitor comprises a metal-insulator-metal (MIM) capacitor, and wherein the capacitor is formed in a plurality of metallization layers of the semiconductor device.

11. The semiconductor device according to claim **8**, the capacitor having an overall length or width in a top view of at least three hundred μm, and wherein the protection device prevents failure of the capacitor.

12. The semiconductor device according to claim **8**, wherein the capacitor includes about 1,000 or more of the plurality of first plates or the plurality of second plates.

13. The semiconductor device according to claim **8**, wherein the capacitor comprises a decoupling capacitor.

14. The semiconductor device according to claim **8**, wherein pairs of the plurality of first plates and the plurality of second plates comprise a plurality of capacitive units, and wherein the protection device is adapted to self-diagnose and isolate a defaulted one of the plurality of capacitive units.

15. A semiconductor device, comprising:

a plurality of first capacitor plates over a workpiece, each of the plurality of first capacitor plates being coupled to a first terminal and each of the plurality of first capacitor plates being in a common plane;

a plurality of second capacitor plates over the workpiece and parallel to the plurality of first capacitor plates, each of the plurality of second capacitor plates being in a common second plane different than the common plane; and

a plurality of protection devices connected to a second terminal through a plurality of conductive elements each extending in a direction perpendicular to the common second plane, the plurality of protection devices being coupled to at least one of the second capacitor plates by one or more electrical connectors, wherein the one or more electrical connectors comprises a conductive line extending along a first side and a second side of the at least one second capacitor plate in a top down view of the semiconductor device, and wherein the first side and the second side are directly adjoined at a corner of the at least one second capacitor plate, wherein the plurality of protection devices comprises:

a plurality of third capacitor plates disposed in the common plane; and

a plurality of fourth capacitor plates disposed in the common second plane.

16. The semiconductor device according to claim **15**, wherein the plurality of first capacitor plates and the plurality of second capacitor plates comprise a plurality of capacitors coupled together in parallel, and wherein one of the plurality of protection devices is coupled in series with each of the plurality of second capacitor plates.

17. The semiconductor device according to claim **15**, wherein the plurality of first capacitor plates and the plurality of second capacitor plates are formed in material layers, and wherein the plurality of protection devices are coupled in the material layers.

18. The semiconductor device according to claim **15**, wherein the plurality of protection devices are coupled above the plurality of second capacitor plates.

19. The semiconductor device according to claim **15**, wherein the one or more electrical connectors further comprises:

a first conductive via extending from the conductive line to one of the first capacitor plates; and

a second conductive via extending from the conductive line to one of the fourth capacitor plates.

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