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(54) **SCHOTTKY BARRIER DIODE**

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(58) **Field of Classification Search**
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See application file for complete search history.

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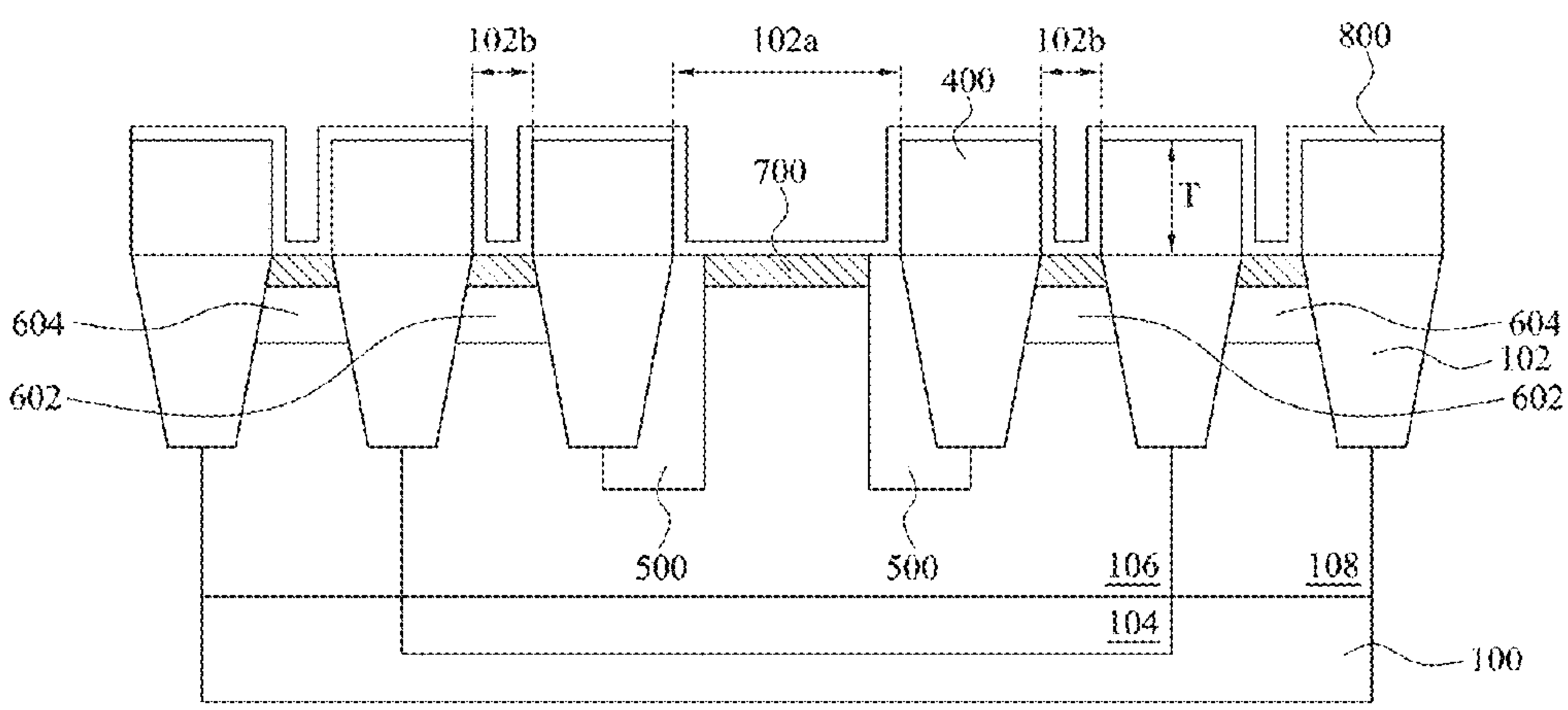
(57) **ABSTRACT**

A Schottky barrier diode is provided, which includes a semiconductor substrate, a first well region, an isolation region, a silicide layer and a silicon oxide-containing layer. The first well region of a first conductivity type is in the semiconductor substrate. The isolation region is in the first well region. The silicide layer is laterally adjacent to the isolation region, and over and in contact with the first well region. The silicon oxide-containing layer is over and in contact with the isolation region.

20 Claims, 7 Drawing Sheets



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H01L 21/285	(2006.01)
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H01L 29/06	(2006.01)
H01L 29/66	(2006.01)
H01L 21/3115	(2006.01)

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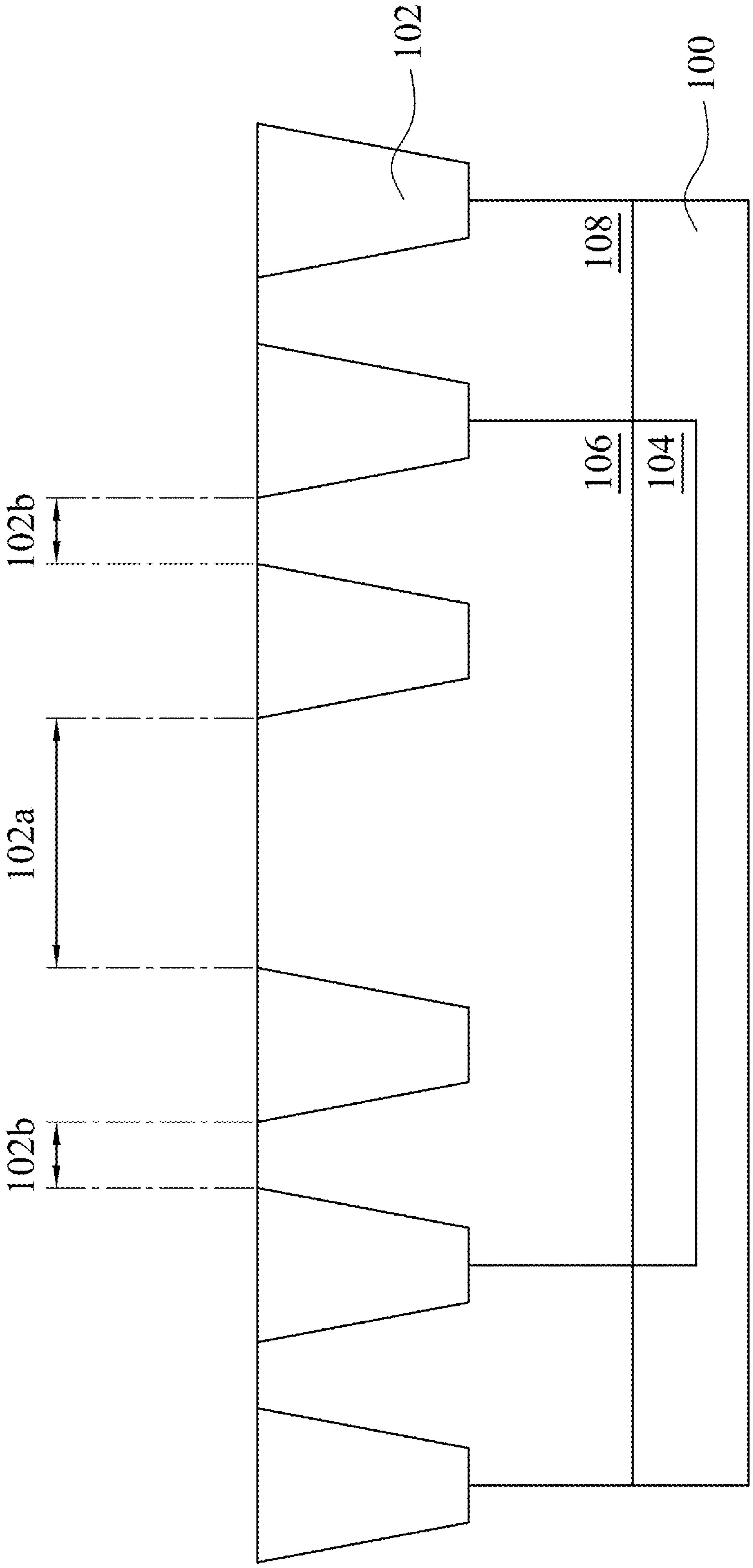

Fig. 1A

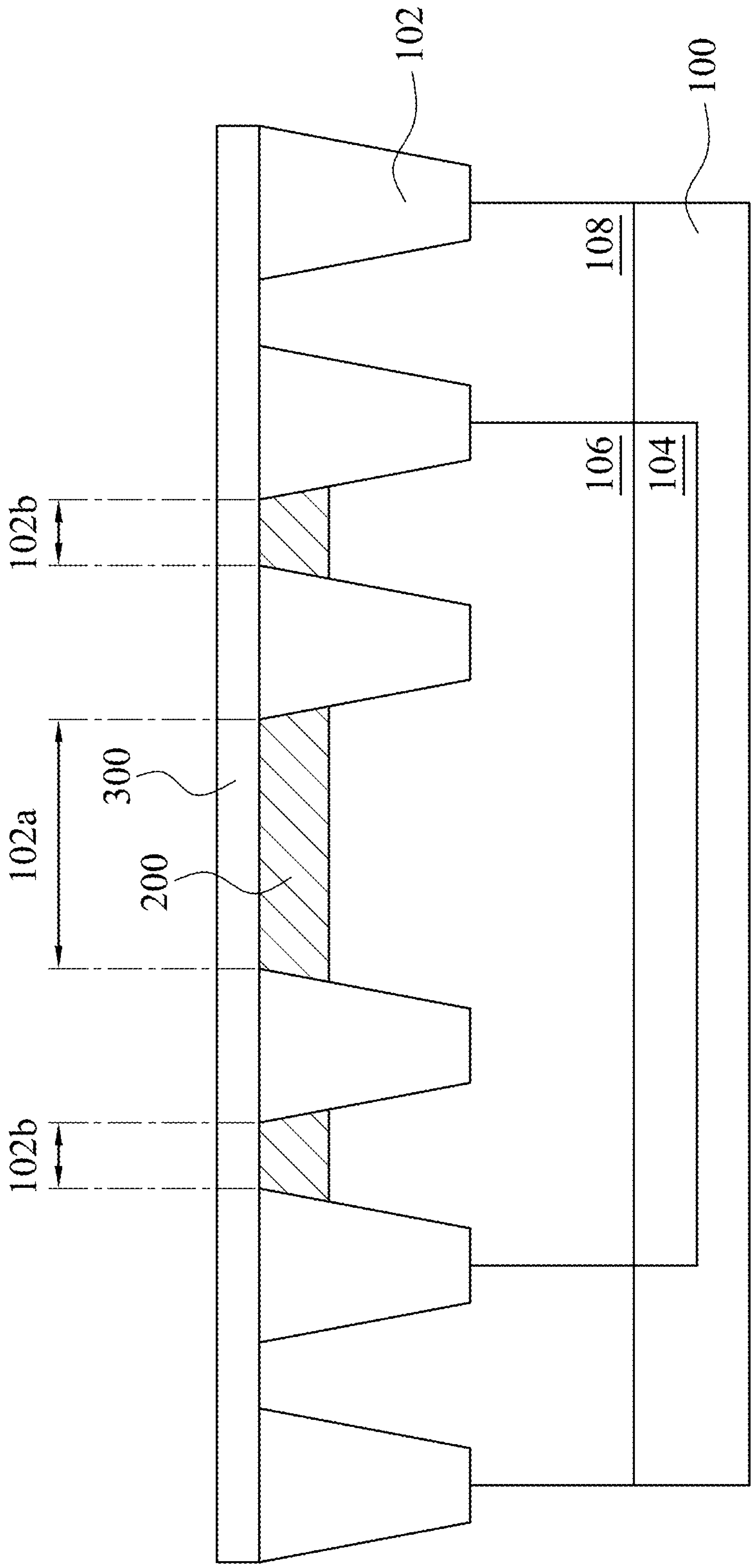

Fig. 1B

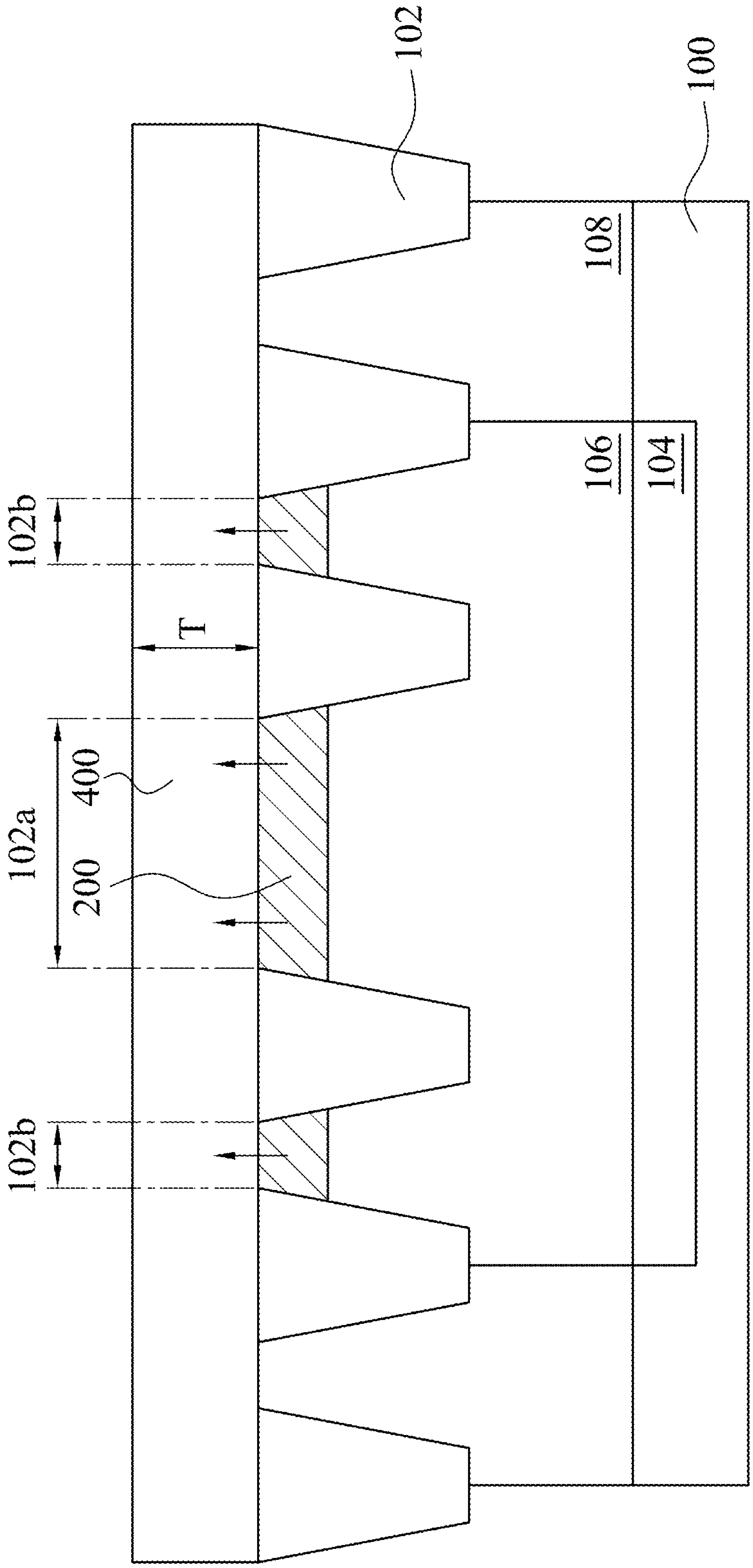

Fig. 1C

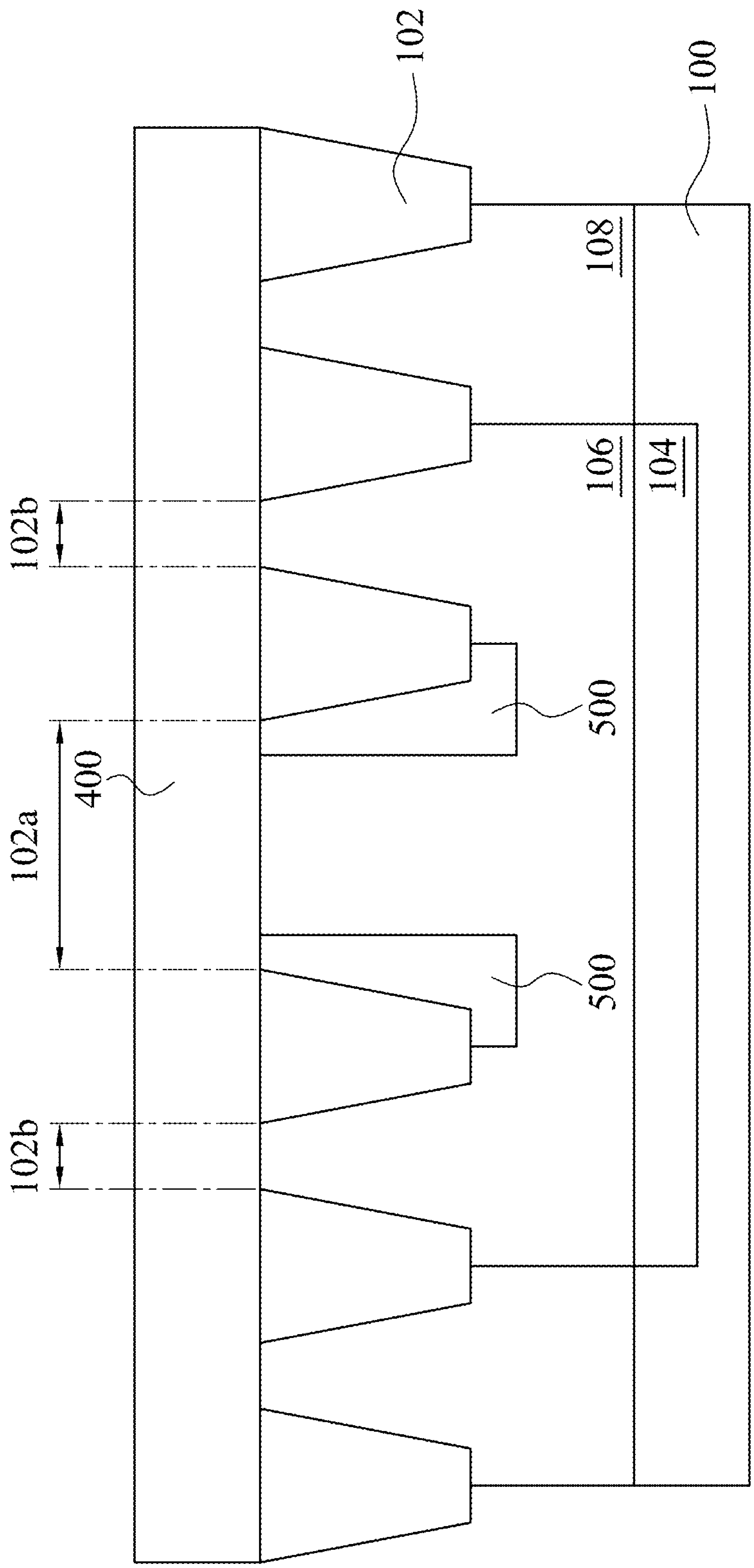

Fig. 1D

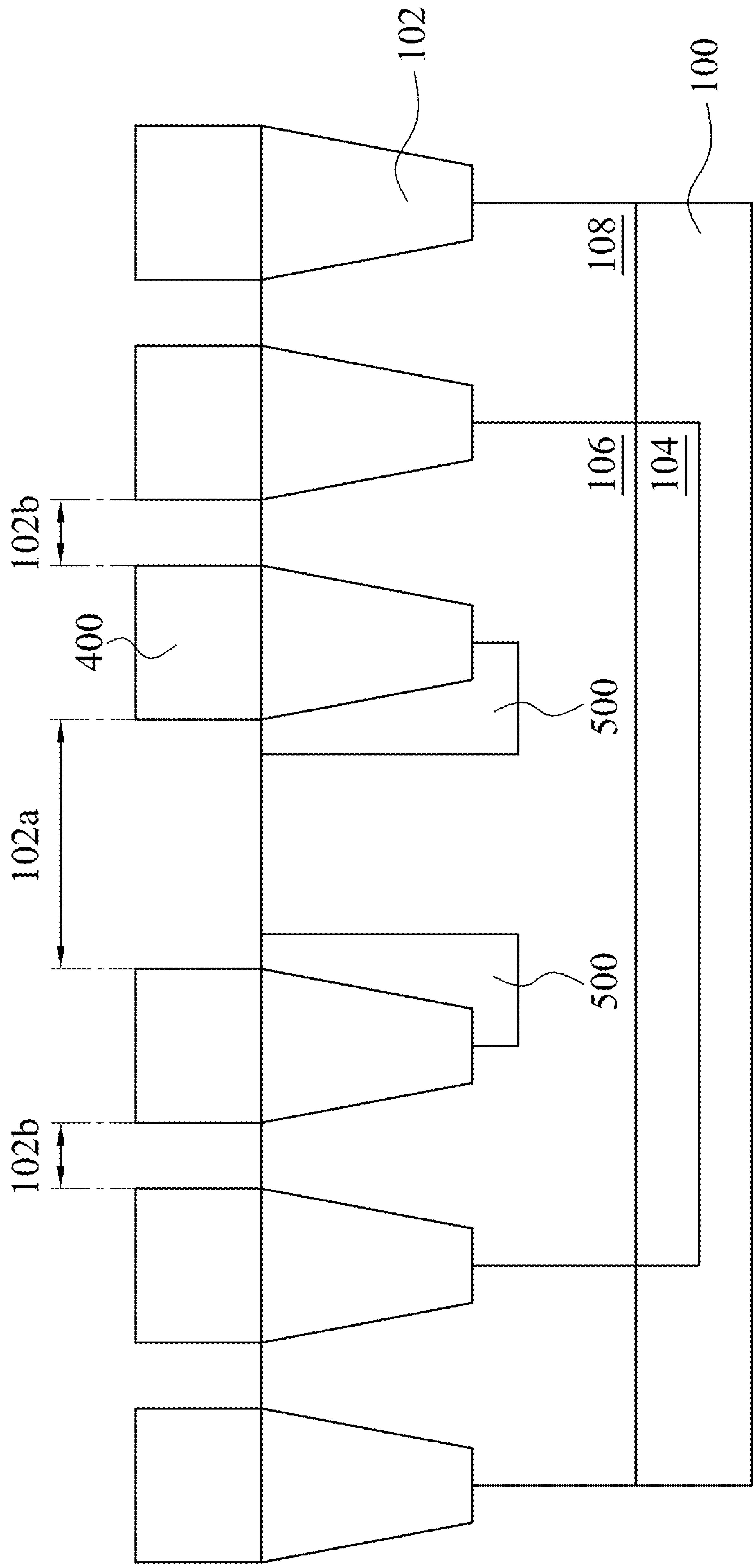

Fig. 1E

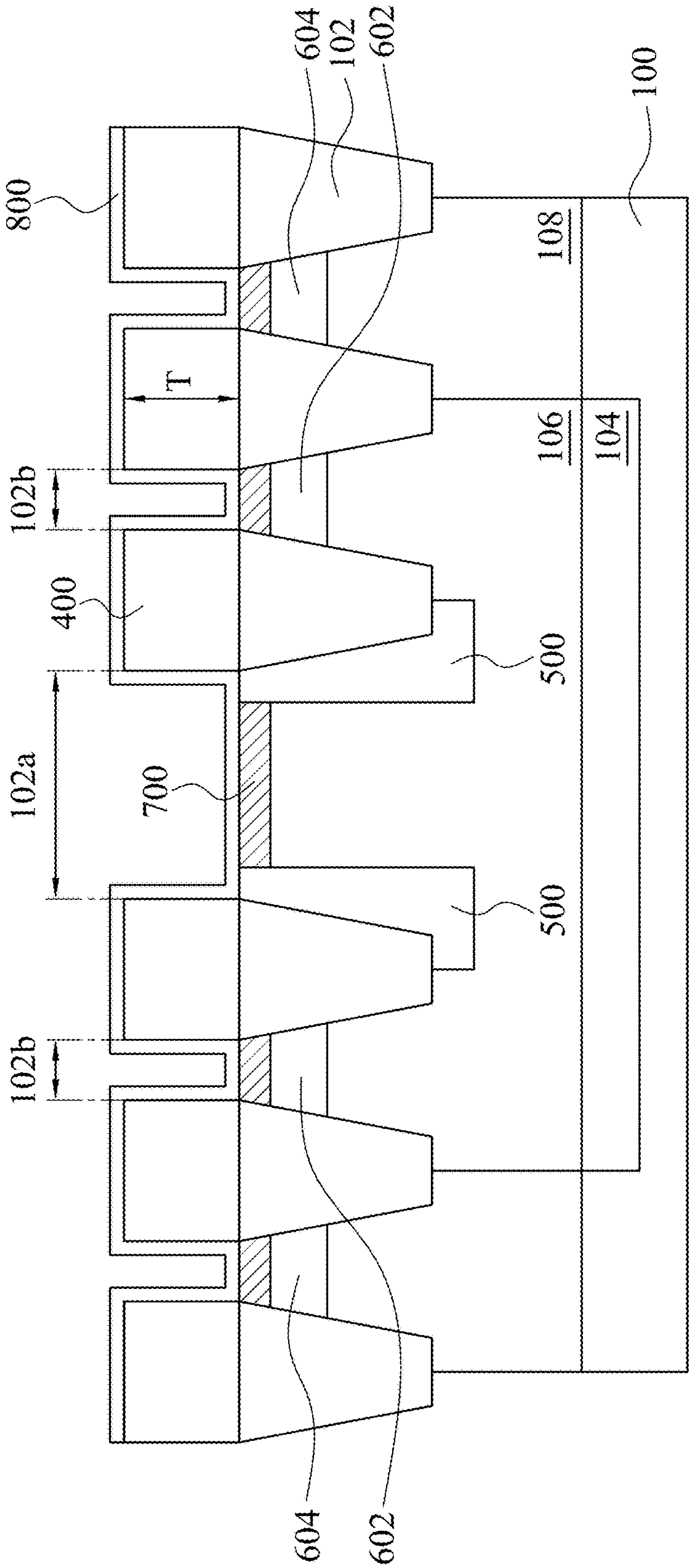
800
604
102
602
100
108
T
106
104
102b
400
500
102a
700
500
102b
604
602

Fig. 1F

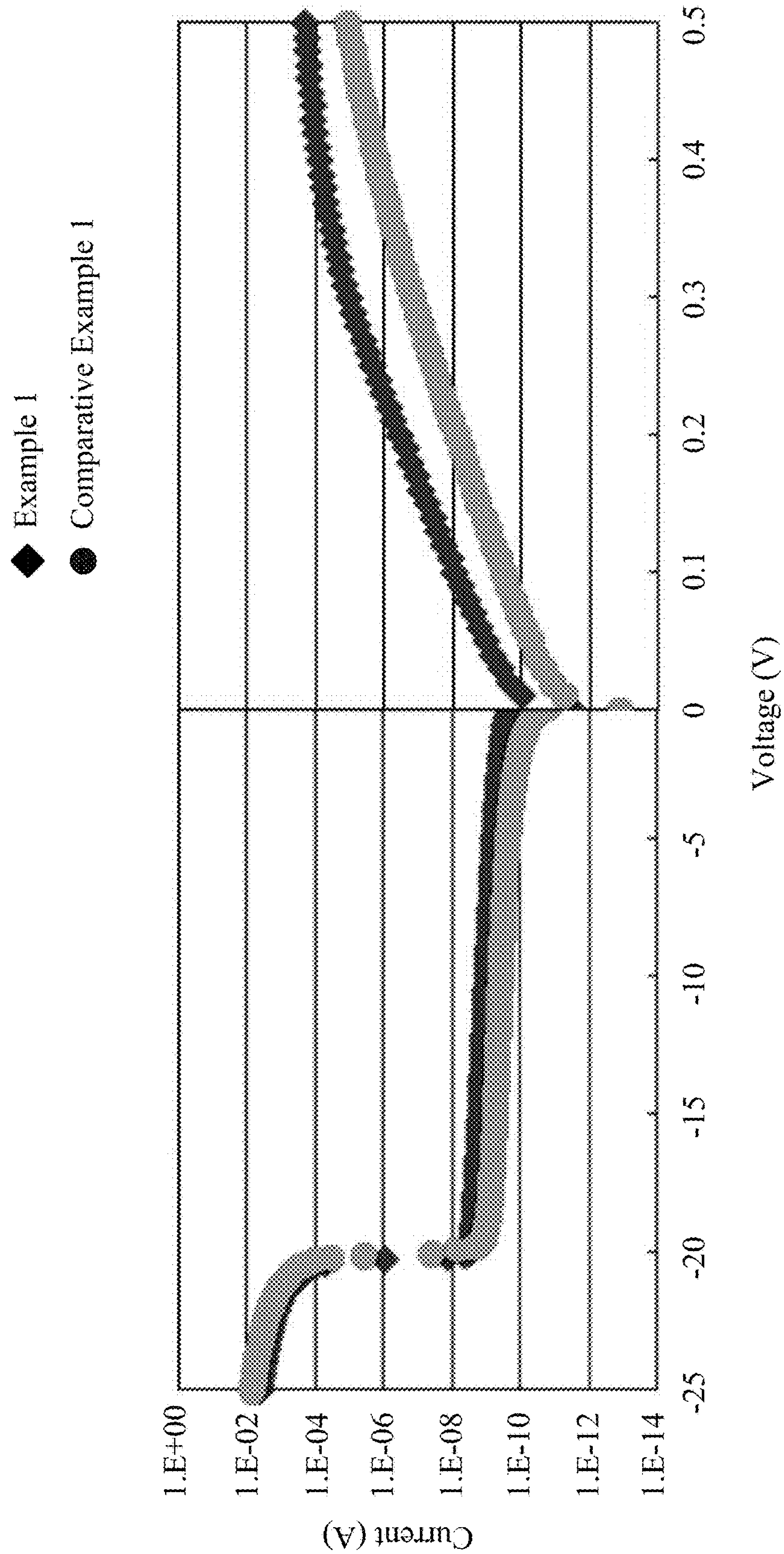
Example 1
Comparative Example 1
Current (A)
1.E+00
1.E-02
1.E-04
1.E-06
1.E-08
1.E-10
1.E-12
1.E-14
-25
-20
-15
-10
-5
0
0.1
0.2
0.3
0.4
0.5
Voltage (V)

Fig. 2

SCHOTTKY BARRIER DIODE

RELATED APPLICATIONS

The present application is a Divisional Application of the application Ser. No. 14/690,209, filed Apr. 17, 2015.

BACKGROUND

Schottky barrier diode has superior characteristics of low turn-on voltage, low power loss, fast recovery time and low junction capacitance compared to a PN junction diode, and thus has been widely used in power and high voltage (HV) technology. Typically, the Schottky barrier diode includes a metal layer and a doped semiconductor layer, and the Schottky barrier is formed at the juncture of the metal layer and the semiconductor layer. Breakdown voltage is improved by placing a guard ring in a semiconductor substrate around the Schottky barrier. Nevertheless, an existing Schottky barrier diode exhibits low forward current. Therefore, how to improve the forward current of the existing Schottky barrier diode becomes an important issue in this field.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. **1A-1**F are cross-sectional views at various stages of manufacturing a Schottky barrier diode in accordance with some embodiments of the present disclosure.

FIG. **2** is a current-voltage diagram of a Schottky barrier diode with a surface-doped modulation (redistribution) process (i.e., Example 1) and a Schottky barrier diode without a surface-doped modulation (redistribution) process (i.e., Comparative Example 1).

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

As mentioned above, the existing Schottky barrier diode exhibits low forward current. For instance, the process of forming the Schottky barrier diode may be combined with other processes, such as the process of forming NMOS transistor and/or PMOS transistor. One or more layers for specific applications unrelated to the Schottky barrier diode may be added to the Schottky barrier diode. However, the added layer(s) may deteriorate the forward current of the Schottky barrier diode. For a specific example, a surface-doped semiconductor layer is formed in a channel region of a NMOS transistor or PMOS transistor to tune threshold voltage (Vt) thereof. The surface-doped semiconductor layer also formed in the Schottky barrier diode, such as formed between a doped well region and a metal layer of the Schottky barrier diode, may result in low forward current of the Schottky barrier diode. The surface-doped semiconductor layer may not be formed in the Schottky barrier diode, such as between the doped well region and the metal layer, by using an extra mask, but the extra mask is too costly.

In view of the foregoing, the present disclosure provides a method of manufacturing a Schottky barrier diode without a surface-doped semiconductor layer to solve the issue of low forward current mentioned above. In this method, the surface-doped semiconductor layer is formed without using any extra mask, and then completely moved in a specific material using one or more thermal treatments. The thermal treatment may be extra added or included in follow-up processing steps for forming other elements. The thermal treatment included in the follow-up processing steps does not generate extra costs and is fully compatible to the process of manufacturing the existing Schottky barrier diode having the surface-doped semiconductor layer and the NMOS and/or PMOS transistor. In addition, it is noteworthy that, the Schottky barrier diode manufactured using the method of the present disclosure not only exhibits much higher forward current but also does not affect reverse characteristics compared to the existing Schottky barrier diode having the surface-doped semiconductor layer. Embodiments of the method of manufacturing the Schottky barrier diode without the surface-doped semiconductor layer and the Schottky barrier diode will be sequentially described below in detail.

FIGS. **1A-1**F are cross-sectional views at various stages of manufacturing a Schottky barrier diode in accordance with some embodiments of the present disclosure. Referring to FIG. **1**A, a semiconductor substrate **100** is provided. In some embodiments, the semiconductor substrate **100** includes an elementary semiconductor including silicon or germanium in crystal, polycrystalline, and/or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; any other suitable material; and/or a combination thereof. In some embodiments, the semiconductor substrate **100** is a p-type semiconductor substrate.

The semiconductor substrate **100** includes a first well region **106** of a first conductivity type in the semiconductor substrate **100**. In some embodiments, the first well region **106** is an n-well (NW). In some embodiments, the dopant concentration of the first well region **106** is ranging from about 10^{11} ions/cm^3 to about 10^{14} ions/cm^3, although a higher dopant concentration is also applicable. In some embodiments, the first well region **106** is formed by implanting n-type impurities into the semiconductor substrate **100**, such as phosphorus, arsenic, antimony, bismuth, selenium, or tellurium, or another suitable n-type dopant. Alternatively, in some embodiments, the first well region **106** is formed by epitaxially growing a semiconductor layer on the semiconductor substrate **100**, and then performing an n-type impurity implantation.

In some embodiments, the semiconductor substrate **100** further includes a deep well region **104** of the first conductivity type beneath the first well region **106**. In some embodiments, the deep well region **104** is a deep n-type well (DNW) region. The deep well region **104** may be omitted in some embodiments. In some embodiments, the deep well region **104** is formed by implanting n-type impurities into the semiconductor substrate **100**, such as phosphorus, arsenic, antimony, bismuth, selenium, or tellurium, or another suitable n-type dopant. Alternatively, in some embodiments, the deep well region **104** is formed by epitaxially growing a semiconductor layer on the semiconductor substrate **100**, and then performing an n-type impurity implantation.

In some embodiments, the semiconductor substrate **100** further includes a third well region **108** of a second conductivity type opposite to the first conductivity type in the semiconductor substrate **100**. In some embodiments, the third well region **108** is a p-well (PW). In some embodiments, the dopant concentration of the third well region **108** is ranging from about 10^{11} ions/cm^3 to about 10^{14} ions/cm^3, although a higher dopant concentration is also applicable. In some embodiments, the third well region **108** is formed by implanting p-type impurities into the semiconductor substrate **100**, such as boron, boron difluoride or another suitable p-type dopant. Alternatively, in some embodiments, the third well region **108** is formed by epitaxially growing a semiconductor layer on the semiconductor substrate **100**, and then performing a p-type impurity implantation.

In some embodiments, the semiconductor substrate **100** further includes an isolation region **102** in the first well region **106**. In some embodiments, the semiconductor substrate **100** further includes a plurality of isolation regions **102** in the first well region **106**, the third well region **108** or between the first well region **106** and the third well region **108**. In some embodiments, the isolation portion **102** is a shallow trench isolation (STI). In some embodiments, the isolation portion **102** includes silicon oxide, silicon nitride, silicon oxynitride, a low-k dielectric material, and/or a combination thereof. In some embodiments, the isolation portion **102** includes silicon oxide. In some embodiments, the isolation region **102** is formed by selective oxidation. In some embodiments, the isolation region **102** is firstly formed, and the deep well region **104**, the first well region **106** and the third well region **108** are then sequentially formed. The formation order of the isolation region **102**, the deep well region **104**, the first well region **106** and the third well region **108** may be appropriately changed and not limited to the embodiments mentioned above.

The formed isolation region **102** is configured to define a diode area **102***a* of the first well region **106** and a contact area **102***b* of the first well region **106** separated from each other by the isolation region **102**. As shown in FIG. **1**A, the diode area **102***a* is between two contact area **102***b*; however, in some embodiments, in top view, the diode area **102***a* is surrounded by a contact area **102***b*. In some embodiments, the exposed area (not marked) of the third well region **108** is another contact area.

Referring to FIG. **1**B, a surface-doped layer **200** having a dopant of the second conductivity type is formed in the first well region **106**. Specifically, the surface-doped layer **200** is formed in the diode area **102***a* of the first well region **106**. In some embodiments, the surface-doped layer **200** is further formed in the contact area **102***b* of the first well region **106**. In some embodiments, the surface-doped layer **200** includes a p-type dopant, such as boron, boron difluoride or another suitable p-type dopant.

It is noteworthy that in some embodiments, the surface-doped layer **200** is used to form in a channel region (not shown) of the NMOS transistor or PMOS transistor, and thus to tune threshold voltage (Vt) thereof. In some embodiments, the surface-doped layer **200** having the p-type dopant is used to form in a n-channel region of the PMOS transistor, and thus to tune threshold voltage (Vt) thereof. In some embodiments, the surface-doped layer **200** is formed in both the first well region **106** and the channel region. In some embodiments, the surface-doped layer **200** is formed into the first n-well region **106** and the n-channel region of the PMOS transistor by implanting p-type impurities without using any mask.

However, the surface-doped layer **200** formed in the first well region **106** will deteriorate forward current of the Schottky barrier diode. Accordingly, as shown in FIG. **1**C, a dielectric layer **400** is formed in contact with the surface-doped layer **200** to receive or absorb the dopant of the surface-doped layer **200**. In some embodiments, the dielectric layer **400** is formed over the first well region **106**. In some embodiments, the dielectric layer **400** is formed over the entire first well region **106** and the third well region **108**. In some embodiments, the dielectric layer **400** is formed using a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process (e.g., plasma enhanced CVD (PECVD), low pressure CVD (LPCVD) or atmosphere pressure CVD (APCVD)), a spin-on coating process, a thermal grown (e.g., a thermal dry oxidation or a thermal wet oxidation) or another formation process. In some embodiments, the dielectric layer **400** is formed using thermal oxidation. In some embodiments, the dielectric layer **400** includes silicon oxide. In some embodiments, the dielectric layer **400** excludes silicon nitride since the dopant of the surface-doped layer **200** cannot be driven into a silicon nitride layer. In some embodiments, a portion (not shown) of the dielectric layer **400** is acted as a gate dielectric layer of the NMOS transistor and/or PMOS transistor. In some embodiments, the dielectric layer **400** has a thickness T in a range of 200 Å to 3000 Å, although a greater or smaller thicknesses are also applicable.

In some embodiments, referring to FIGS. **1**B and **1**C, a silicon nitride-containing layer **300** is formed over the surface-doped layer **200** after forming the surface-doped layer **200** and before forming the dielectric layer **400**. In some embodiments, the silicon nitride-containing layer **300** is acted as an etch stop layer and will then be removed in follow-up processing steps. In some embodiments, the silicon nitride-containing layer **300** is made of silicon nitride. However, based on the above, the dopant of the surface-doped layer **200** fails to be driven into a silicon nitride-containing layer; therefore, the silicon nitride-containing layer **300** should be removed before forming the dielectric layer **400** to avoid blocking of the dopant of the surface-doped layer **200** when the dopant of the surface-doped layer **200** is driven.

Continuously referring to FIG. **1**C, after the dielectric layer **400** is formed, a thermal treatment is performed on the surface-doped layer **200** to move the dopant of the surface-doped layer **200** in the dielectric layer **400**. In some embodiments, when the dielectric layer **400** is formed using thermal oxidation, a thermal treatment is accompanied with the thermal oxidation and can help drive the dopant of the surface-doped layer **200** into the dielectric layer **400** without generating extra manufacturing costs. In other words, performing the thermal treatment on the surface-doped layer **200** to move the dopant of the surface-doped layer **200** in the dielectric layer **400** is included in forming the dielectric layer **400**. Alternatively, the thermal treatment is extra added in some embodiments. In some embodiments, the extra added thermal treatment or the thermal treatment included in forming the dielectric layer **400** is greater than or equal to 400° C. In some embodiments, the extra added thermal treatment or the thermal treatment included in forming the dielectric layer **400** is lower than or equal to 1200° C., although a higher temperature is also applicable.

Referring to FIG. **1**D, the method further includes forming a second well region **500** of the second conductivity type in the first well region **106** after forming the dielectric layer **400**. In some embodiments, in top view, the second well region **500** is ring-shaped and surrounds the diode area **102***a* of the first well region **106**. The second well region **500** is configured to surround a silicide layer (not shown in FIG. **1**D but shown in FIG. **1**F) formed over the diode area **102***a* of the first well region **106** in follow-up processing steps to improve breakdown voltage. In some embodiments, the dopant concentration of the second well region **500** is ranging from about 10^{11} ions/cm^3 to about 10^{14} ions/cm^3, although a higher dopant concentration is also applicable.

In some embodiments, the second well region **500** is formed by implanting a dopant of the second conductivity type into a specific region of the first well region **106** and performing an annealing process, such as a rapid thermal annealing process (RTA). The annealing process can also help drive the dopant of the surface-doped layer **200** of FIG. **1**C into the dielectric layer **400**. In other words, performing the thermal treatment on the surface-doped layer **200** to move the dopant of the surface-doped layer **200** in the dielectric layer **400** is included in forming the second well region **500**. The annealing process included in forming the second well region **500** can help effectively remove the surface-doped layer **200** in the first n-well region **106** without generating extra manufacturing costs. In some embodiments, the thermal treatment (i.e., the annealing process) included in forming the second well region **500** is greater than or equal to 400° C. In some embodiments, the thermal treatment included in forming the second well region **500** is lower than or equal to 1200° C., although higher temperature is also applicable.

Referring to FIGS. **1**D and **1**E, the dielectric layer **400** over the diode area **102***a* is removed to expose the diode area **102***a* of the first well region **106**. Specifically, the dielectric layer **400** is patterned to expose the diode area **102***a* of the first well region **106**. In some embodiments, the dielectric layer **400** is patterned to further expose the contact area **102***b* of the first well region **106**. In some embodiments, the dielectric layer **400** is patterned to further expose the contact area (not marked) of the third well region **108**. In some embodiments, the dielectric layer **400** is patterned using a photolithography/etching process, a laser drilling process or another suitable material removal process.

It is noted that, if the second well region **500** is formed after the dielectric layer **400** is removed or patterned, some residual dopant of the surface-doped layer **200** in the first well region **106** cannot be completely removed in some embodiments. Therefore, in some embodiments, to completely remove the dopant of the surface-doped layer **200** in the first well region **106**, forming the second well region **500** is before removing or patterning the dielectric layer **400**. In addition, before the dielectric layer **400** is removed or patterned, other processing steps for forming other elements including thermal treatments can also help drive the residual dopant of the surface-doped layer **200** into the dielectric layer **400**.

Referring to FIGS. **1**E and **1**F, a silicide layer **700** is formed in contact with the exposed first well region **106** of FIG. **1**E. Specifically, the silicide layer **700** is formed in contact with the exposed diode area **102***a* of the first well region **106**. In some embodiments, the silicide layer **700** is formed in contact with the diode area **102***a*, the contact area **102***b* and the contact area (not marked) of the third well region **108**. In some embodiments, the silicide layer **700** is formed by forming a metal-containing layer (not shown) and then performing an annealing process on the metal-containing layer. In some embodiments, the metal-containing layer includes cobalt, titanium, tungsten, nickel or a combination thereof. In some embodiments, the silicide layer **700** includes a material selected from the group consisting of cobalt silicide, titanium silicide, tungsten silicide, nickel silicide and a combination thereof.

In some embodiments, the method further includes forming a heavily doped layer **602** of the first conductivity type in the contact area **102***b* of the first well region **106**. In some embodiments, forming the heavily doped layer **602** is before forming the silicide layer **700**. In some embodiments, a portion (not shown) of the heavily doped layer **602** is acted as a source region or a drain region of the NMOS transistor and/or PMOS transistor. In some embodiments, two portions (not shown) of the heavily n-doped layer **602** are respectively acted as source and drain regions of the NMOS transistor.

In some embodiments, the method further includes forming another heavily doped layer **604** of the second conductivity type in the contact area (not marked) of the third well region **108**. In some embodiments, forming the heavily doped layer **604** is before forming the silicide layer **700**. In some embodiments, a portion (not shown) of the heavily doped layer **604** (not shown) is acted as a source region or a drain region of the NMOS transistor and/or PMOS transistor. In some embodiments, two portions (not shown) of the heavily p-doped layer **604** are respectively acted as source and drain regions of the PMOS transistor.

In some embodiments, patterning the dielectric layer **400** further includes to remain the dielectric layer **400** over the isolation region **102**. In some embodiments, the dielectric layer **400** and the isolation layer **102** include silicon oxide. In some embodiments, the dielectric layer **400** and the isolation layer **102** exclude silicon nitride.

In some embodiments, the method further includes forming a contact etch stop layer (CESL) **800** over the dielectric layer **400** and the silicide layer **700**. In some embodiments, the contact etch stop layer **800** is formed of silicon nitride, silicon oxynitride, silicon carbon nitride, any other suitable insulating material or a combination thereof. In some embodiments, the contact etch stop layer **800** is formed using a PVD process, a CVD process, a spin-on coating process, a thermal grown or another formation process.

In some embodiments, the method further includes forming an inter-layer dielectric (ILD) (not shown) over the contact etch stop layer **800**. In some embodiments, the inter-layer dielectric includes silicon oxide, silicon nitride, silicon oxynitride, any other suitable insulating material or a combination thereof. In some embodiments, the ILD is formed using a PVD process, a CVD process, a spin-on coating process, a thermal grown or another formation process.

The present disclosure further provides a Schottky barrier diode, which includes a semiconductor substrate **100**, a first well region **106**, an isolation region **102**, a silicide layer **700** and a silicon oxide-containing layer **400**, as shown in FIG. **1**F.

The semiconductor substrate **100** includes an elementary semiconductor including silicon or germanium in crystal, polycrystalline, and/or an amorphous structure; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; any other suitable material; and/or a combination thereof. In some embodiments, the semiconductor substrate **100** is a p-type semiconductor substrate.

The first well region **106** of a first conductivity type is in the semiconductor substrate **100**. In some embodiments, the first well region **106** is an n-well (NW). In some embodiments, the dopant concentration of the first well region **106** is ranging from about 10^{11} ions/cm^3 to about 10^{14} ions/cm^3.

The isolation region **102** is in the first well region **106** to define a diode area **102**_a_ of the first well region **106** and a contact area **102**_b_ of the first well region **106** separated from each other by the isolation region **102**. In some embodiments, the isolation portion **102** is a shallow trench isolation (STI). In some embodiments, the isolation portion **102** includes silicon oxide, silicon nitride, silicon oxynitride, a low-k dielectric material, and/or a combination thereof.

In some embodiments, the Schottky barrier diode further includes a deep well region **104** of the first conductivity type beneath the first well region **106**. In some embodiments, the deep well region **104** is a deep n-type well (DNW) region. The deep well region **104** may be omitted in some embodiments.

In some embodiments, the Schottky barrier diode further includes a third well region **108** of a second conductivity type opposite to the first conductivity type in the semiconductor substrate **100**. In some embodiments, the third well region **108** is a p-well (PW). In some embodiments, the dopant concentration of the third well region **108** is ranging from about 10^{11} ions/cm^3 to about 10^{14} ions/cm^3.

The silicide layer **700** is laterally adjacent to the isolation region **102**, and over and in contact with the first well region **106**. In some embodiments, the silicide layer **700** includes cobalt silicide, titanium silicide, tungsten silicide, nickel silicide and a combination thereof. In some embodiments, the silicide layer **700** is not in contact with the isolation region **102**. In some embodiments, the silicide layer **700** is not in contact with the silicon-containing layer **400**.

The silicon oxide-containing layer **400** is over and in contact with the isolation region **102**. In some embodiments, the silicon oxide-containing layer **400** is substantially aligned with the isolation layer **102**. The term "substantially aligned" refers to aligned with some acceptable deviation and does not require exact alignment. In some embodiments, an edge of the silicon oxide-containing layer **400** is aligned with an edge of the isolation **102**, as shown in FIG. **1**F. In some embodiments, an edge of the silicon oxide-containing layer touches an upper surface of a second well region. In some embodiments, an edge of the silicon oxide-containing layer touches an upper surface of the isolation region **102**. In some embodiments, the silicon oxide-containing layer **400** has a thickness T in a range of 200 Å to 3000 Å. In some embodiments, the silicon oxide-containing layer **400** excludes silicon nitride.

In some embodiments, the Schottky barrier diode further includes a second well region **500** of the second conductivity type surrounding the silicide layer **700** to improve breakdown voltage of the Schottky barrier diode. In some embodiments, the second well region **500** is between the silicide layer **700** and the isolation region **102**.

In some embodiments, the Schottky barrier diode further includes a heavily doped layer **602** of the first conductivity type in the contact area **102**_b_ of the first well region **106**. In some embodiments, the Schottky barrier diode further includes a heavily doped layer **604** of the second conductivity type in a contact area (not marked) of the third well region **108**.

In some embodiments, the Schottky barrier diode further includes a contact etch stop layer **800** over the silicon oxide-containing layer **400** and the silicide layer **700**. In some embodiments, the contact etch stop layer **800** is formed of silicon nitride, silicon oxynitride, silicon carbon nitride, any other suitable insulating material or a combination thereof.

In some embodiments, the Schottky barrier diode further includes an inter-layer dielectric (not shown) over the contact etch stop layer **800**. In some embodiments, the inter-layer dielectric includes silicon oxide, silicon nitride, silicon oxynitride, any other suitable insulating material or a combination thereof.

FIG. **2** is a current-voltage diagram of a Schottky barrier diode with a surface-doped modulation (redistribution) process (i.e., Example 1) and a Schottky barrier diode without a surface-doped modulation (redistribution) process (i.e., Comparative Example 1). The Schottky barrier diode of Example 1 has a structure of FIG. **1**F, and the Schottky barrier diode of Comparative Example 1 has a structure of FIG. **1**F and an additional surface-doped layer (not shown in FIG. **1**F) beneath and in contact with the silicide layer **700**. In the Schottky barrier diodes of Example 1 and Comparative Example 1, the heavily doped layer **602** is acted as a cathode, and the silicide layer **700** is acted as an anode. As shown in FIG. **2**, the forward current of Example 1 is significantly higher than that of Comparative Example 1, and the reverse current of Example 1 is similar to that of Comparative Example 1. Therefore, the Schottky barrier diode of the present disclosure can indeed effectively solve the issue of low forward current and does not affect reverse characteristics.

According to some embodiments, a Schottky barrier diode includes a semiconductor substrate, a first well region, an isolation region, a silicide layer and a silicon oxide-containing layer. The first well region of a first conductivity type is in the semiconductor substrate. The isolation region is in the first well region. The silicide layer is laterally adjacent to the isolation region, and over and in contact with the first well region. The silicon oxide-containing layer is over and in contact with the isolation region.

According to some embodiments, a method of manufacturing a Schottky barrier diode is provided, which includes: providing a semiconductor substrate including a first well region of a first conductivity type in the semiconductor substrate; forming a surface-doped layer having a dopant of a second conductivity type opposite to the first conductivity type in the first well region; forming a dielectric layer in contact with the surface-doped layer; performing a thermal treatment on the surface-doped layer to move the dopant of the surface-doped layer in the dielectric layer; removing the dielectric layer to expose the first well region; and forming a silicide layer in contact with the exposed first well region.

According to some embodiments, a method of manufacturing a Schottky barrier diode is provided, which includes: providing a semiconductor substrate including a first well region of a first conductivity type in the semiconductor substrate and an isolation region in the first well region to define a diode area of the first well region and a contact area of the first well region separated from each other by the isolation region; forming a surface-doped layer having a dopant of a second conductivity type opposite to the first conductivity type in the diode area of the first well region; forming a dielectric layer over the first well region and in contact with the surface-doped layer; performing a thermal treatment on the surface-doped layer to move the dopant of the surface-doped layer in the dielectric layer; patterning the dielectric layer to expose the diode area of the first well region; and forming a silicide layer in contact with the exposed diode area of the first well region.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A Schottky barrier diode, comprising:
a semiconductor substrate;
a first well region of a first conductivity type in the semiconductor substrate;
an isolation region in the first well region;
a silicide layer laterally adjacent to the isolation region and over and in contact with the first well region;
a dielectric layer over and in contact with the isolation region; and
a contact etch stop layer (CESL) over the dielectric layer and the silicide layer.

2. The Schottky barrier diode of claim **1**, wherein the dielectric layer is substantially aligned with the isolation region.

3. The Schottky barrier diode of claim **1**, further comprising a second well region of a second conductivity type opposite to the first conductivity type and surrounding the silicide layer.

4. The Schottky barrier diode of claim **3**, wherein the second well region is between the silicide layer and the isolation region.

5. The Schottky barrier diode of claim **1**, wherein the dielectric layer has a thickness in a range of 200 Å to 3000 Å.

6. The Schottky barrier diode of claim **1**, wherein the dielectric layer excludes silicon nitride.

7. The Schottky barrier diode of claim **1**, further comprising a deep well region of the first conductivity type beneath the first well region and in the semiconductor substrate.

8. A Schottky barrier diode, comprising:
a semiconductor substrate;
a first well region of a first conductivity type in the semiconductor substrate;
an isolation region in the first well region;
a silicide layer laterally adjacent to the isolation region and over and in contact with the first well region;
a dielectric layer over the isolation region and in contact with the isolation region; and
a contact etch stop layer (CESL) over the dielectric layer and the silicide layer.

9. The Schottky barrier diode of claim **8**, wherein the dielectric layer is substantially aligned with the isolation region.

10. The Schottky barrier diode of claim **8**, further comprising a second well region of a second conductivity type opposite to the first conductivity type and surrounding the silicide layer.

11. The Schottky barrier diode of claim **10**, wherein the second well region is between the silicide layer and the isolation region.

12. The Schottky barrier diode of claim **8**, wherein the dielectric layer has a thickness in a range of 200 Å to 3000 Å.

13. The Schottky barrier diode of claim **8**, further comprising a deep well region of the first conductivity type beneath the first well region and in the semiconductor substrate.

14. A Schottky barrier diode, comprising:
a semiconductor substrate;
a first well region of a first conductivity type in the semiconductor substrate and having anode and cathode areas;
an isolation region in the first well region and between the anode and cathode areas;
a silicide layer laterally adjacent to the isolation region and over and in contact with the cathode area of the first well region;
a dielectric layer over and in contact with the isolation region; and
a contact etch stop layer over the dielectric layer and the silicide layer.

15. The Schottky barrier diode of claim **14**, wherein the silicide layer is further over the anode area of the first well region.

16. The Schottky barrier diode of claim **14**, further comprising a heavily doped layer of the first conductivity type in the cathode area of the first well region.

17. The Schottky barrier diode of claim **14**, further comprising a second well region of a second conductivity type between the silicide layer and the isolation region.

18. The Schottky barrier diode of claim **8**, further comprising:
a third well region of a second conductivity type; and
a doped layer of the second conductivity type and in the third well region, wherein the silicide layer is further over and in contact with the doped layer.

19. The Schottky barrier diode of claim **8**, wherein the silicide layer has a top surface coplanar with a top surface of the isolation region.

20. The Schottky barrier diode of claim **14**, wherein the silicide layer has a top surface coplanar with a top surface of the isolation region.

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