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Chung

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(54) **ONE-TIME PROGRAMMABLE DEVICE WITH INTEGRATED HEAT SINK**

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CPC ***G11C 17/06*** (2013.01); ***G11C 7/222*** (2013.01); ***G11C 11/16*** (2013.01);
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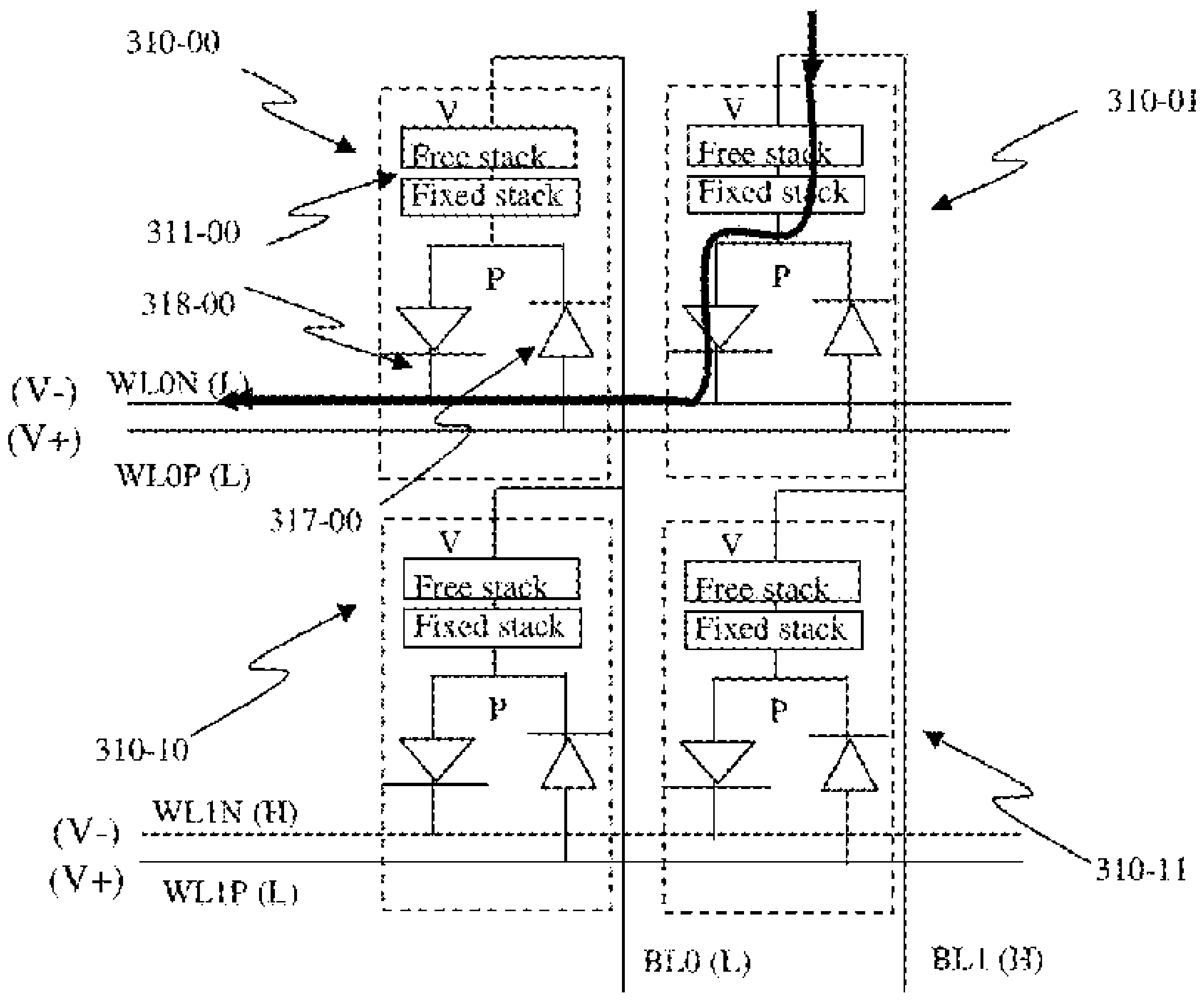
(57) **ABSTRACT**

Junction diodes fabricated in standard CMOS logic processes can be used as program selectors with at least one heat sink or heater to assist programming for One-Time Programmable (OTP) devices, such as electrical fuse, contact/via fuse, contact/via anti-fuse, or gate-oxide breakdown anti-fuse, etc. The heat sink can be at least one thin oxide area, extended OTP element area, or other conductors coupled to the OTP element to assist programming. A heater can be at least one high resistance area such as an unsilicided polysilicon, unsilicided active region, contact, via, or combined in serial, or interconnect to generate heat to assist programming. The OTP device has at least one OTP element coupled to at least one diode in a memory cell. The diode can be constructed by P+ and N+ active regions in a CMOS N well, or on an isolated active region as the P and N terminals of the diode. The isolation between P+ and the N+ active regions of the diode in a cell or between cells can be provided by dummy MOS gate, SBL, or STI/LOCOS isolations. The OTP element can be polysilicon, silicided polysilicon, silicide, polymetal, metal, metal alloy, local interconnect, metal-0, thermally isolated active region, CMOS gate, or combination thereof.

24 Claims, 46 Drawing Sheets



Related U.S. Application Data

continuation of application No. 13/842,824, filed on Mar. 15, 2013, now Pat. No. 9,070,437, which is a continuation-in-part of application No. 13/471,704, filed on May 15, 2012, now Pat. No. 8,488,359, said application No. 13/471,704 is a continuation-in-part of application No. 13/026,752, filed on Feb. 14, 2011, now Pat. No. 8,514,606, said application No. 13/471,704 is a continuation-in-part of application No. 13/026,656, filed on Feb. 14, 2011, now Pat. No. 8,644,049.

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(58) **Field of Classification Search**

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See application file for complete search history.

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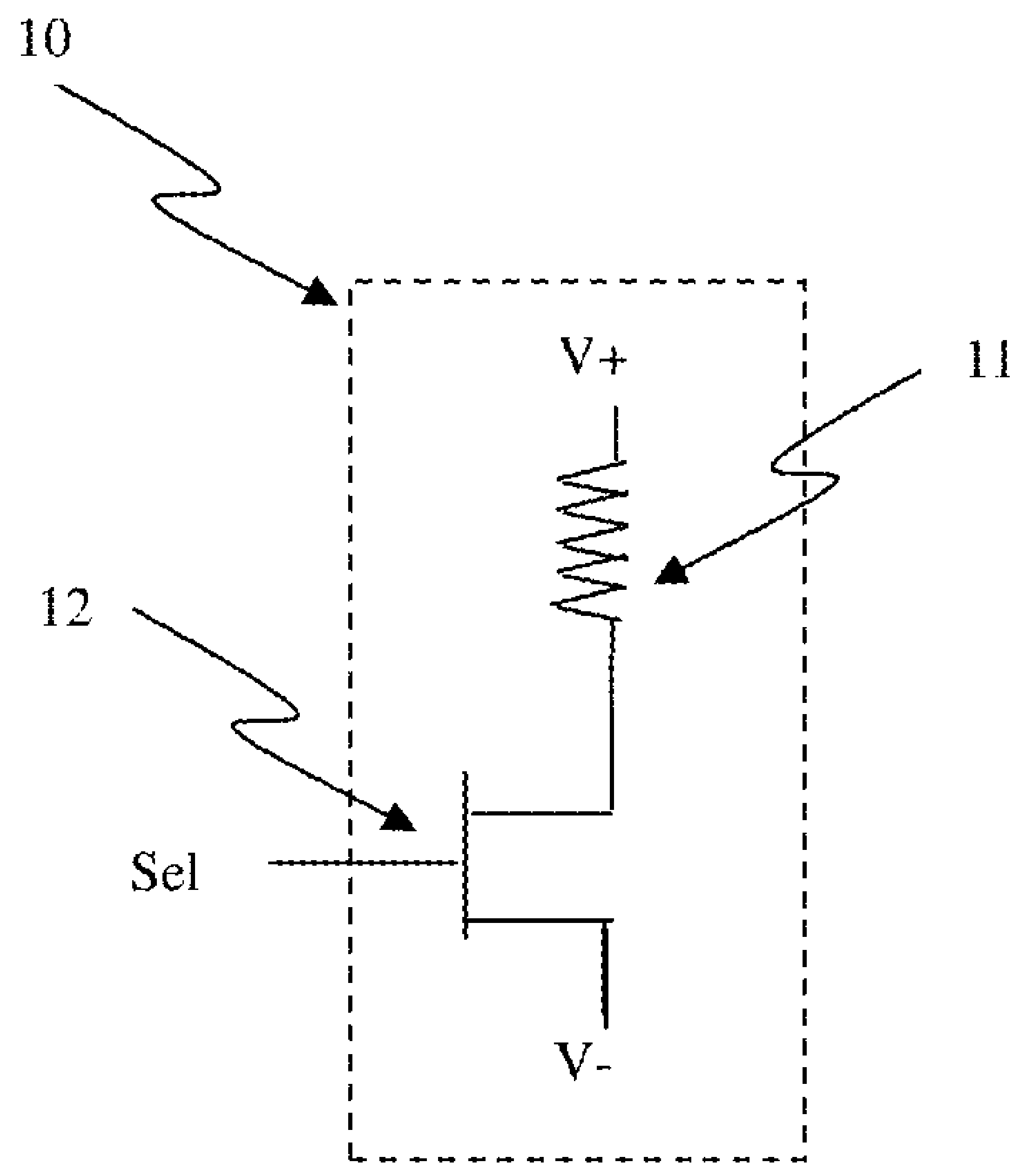

FIG. 1 (prior art)

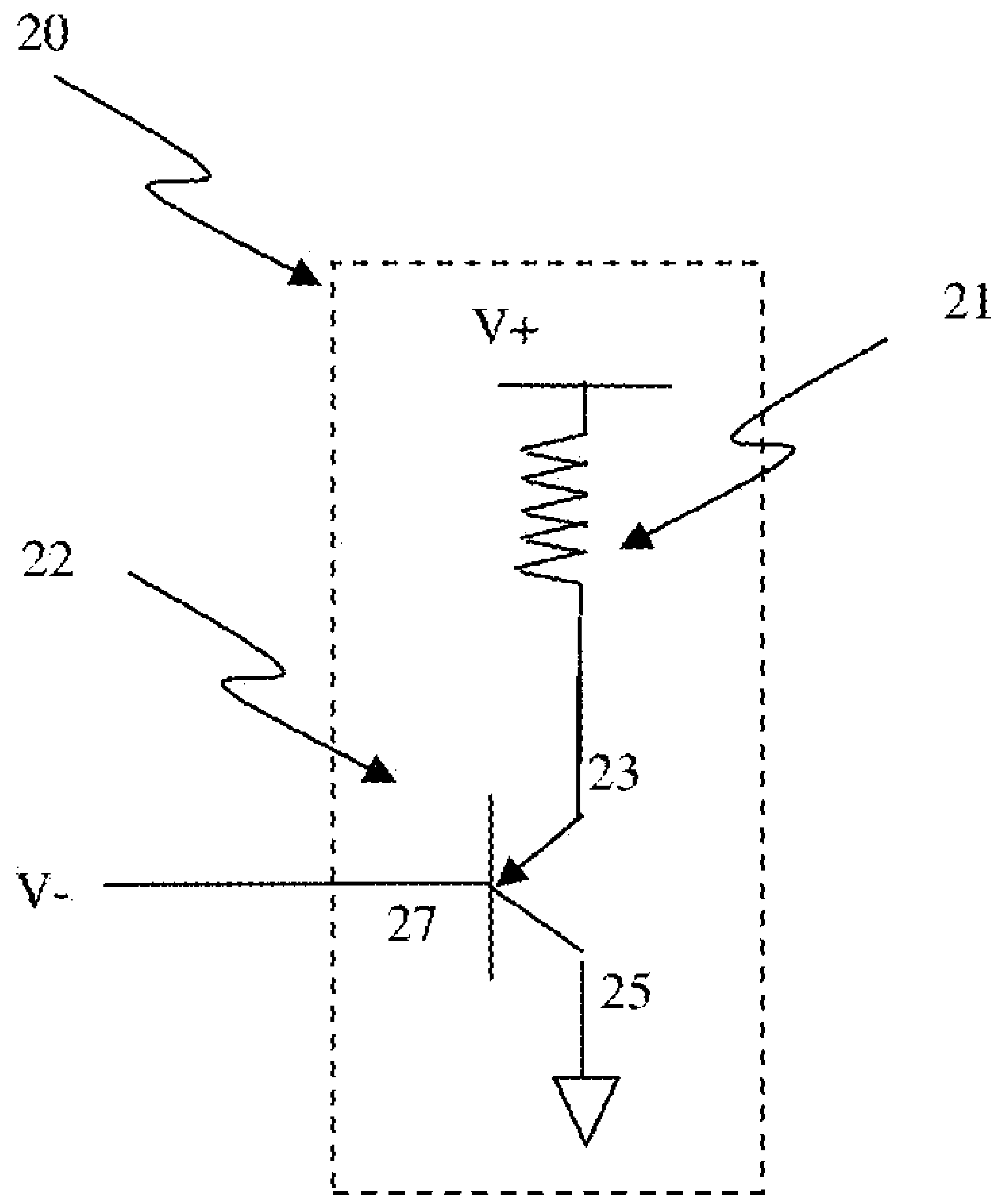
20
V+
21
22
23
V-
27
25

FIG. 2(a)

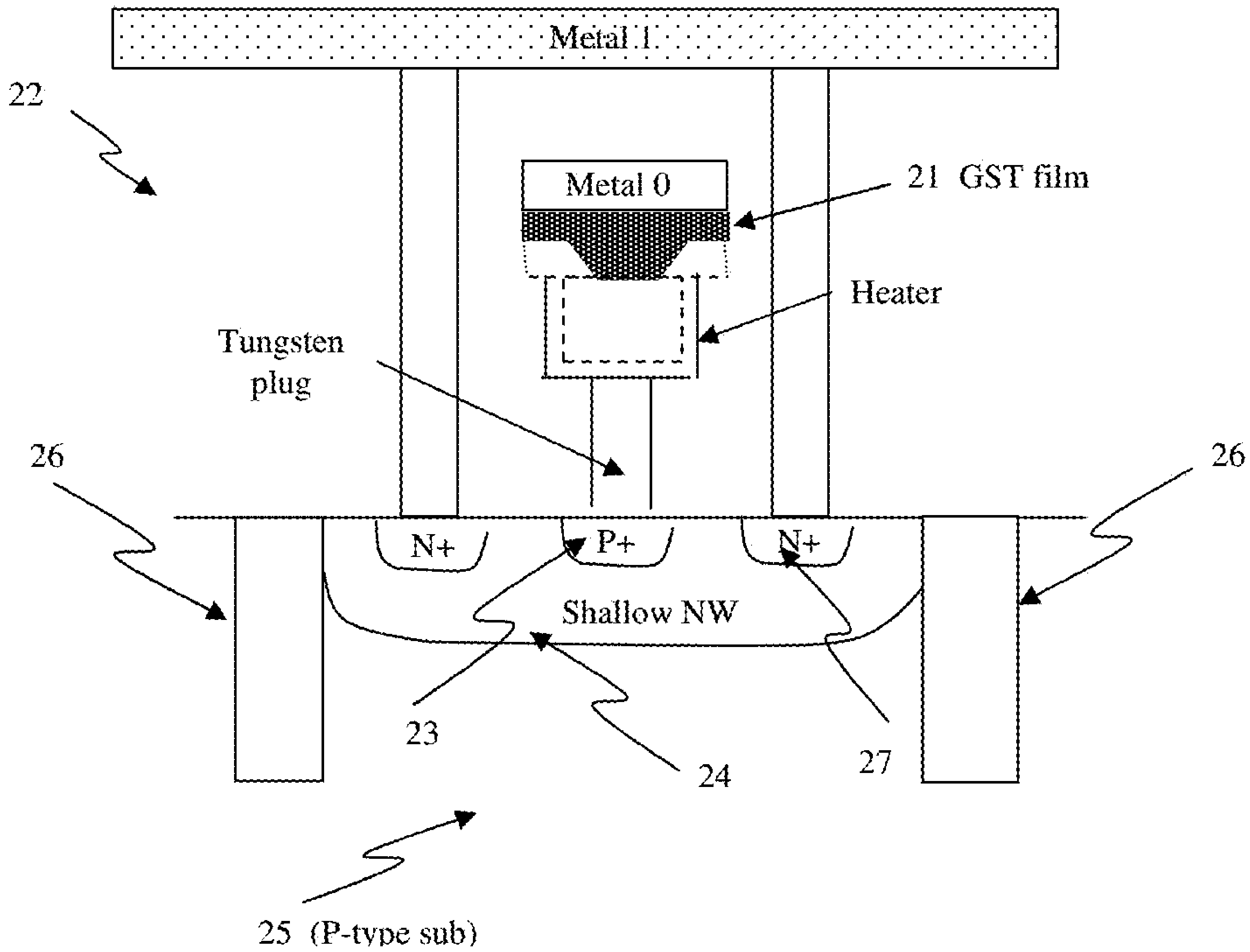
Metal 1
22
Metal 0
21 GST film
Heater
Tungsten
plug
26
26
N+
P+
N+
Shallow NW
23
24
27
25 (P-type sub)

FIG. 2(b)

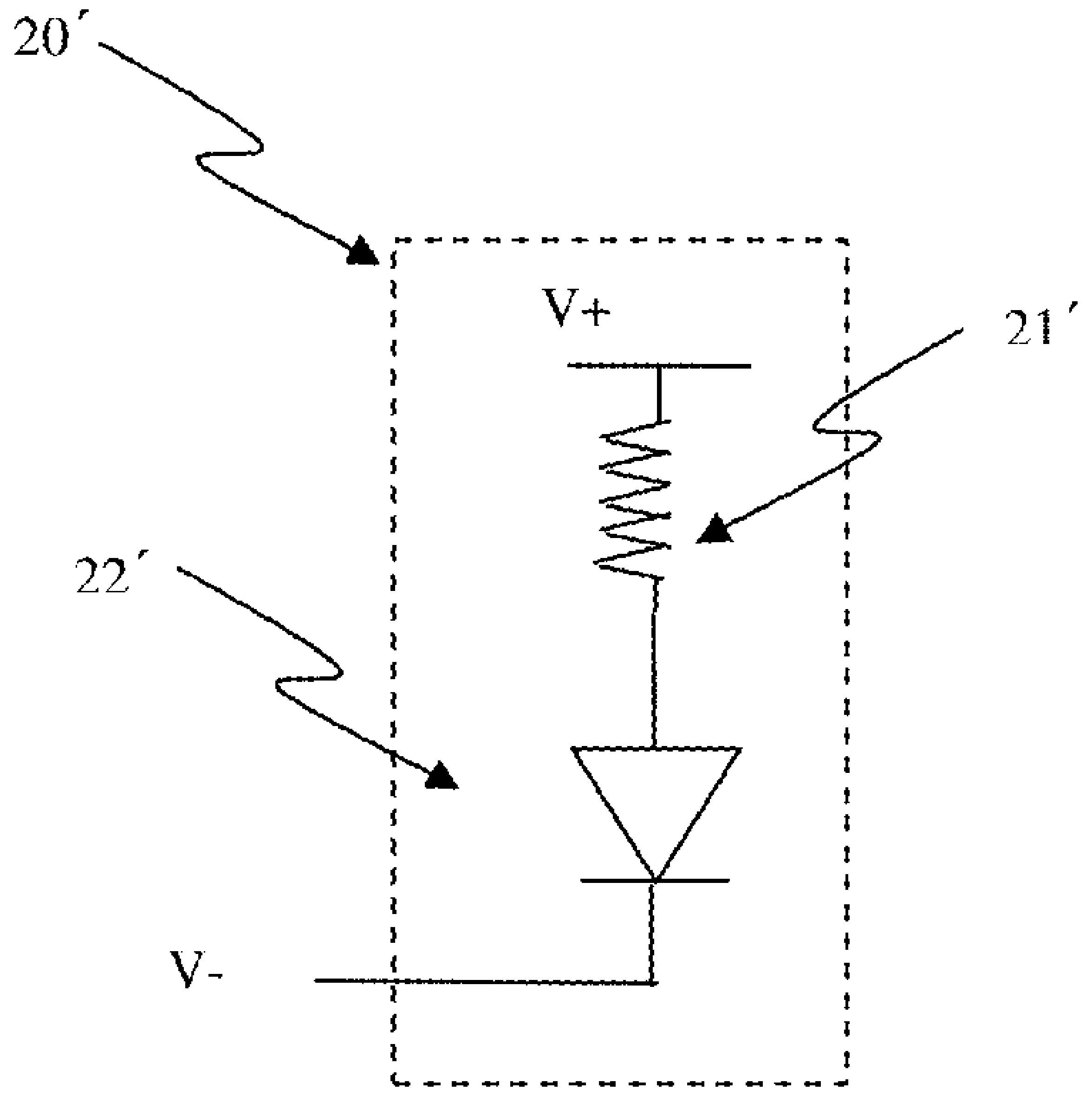

FIG. 2(c)

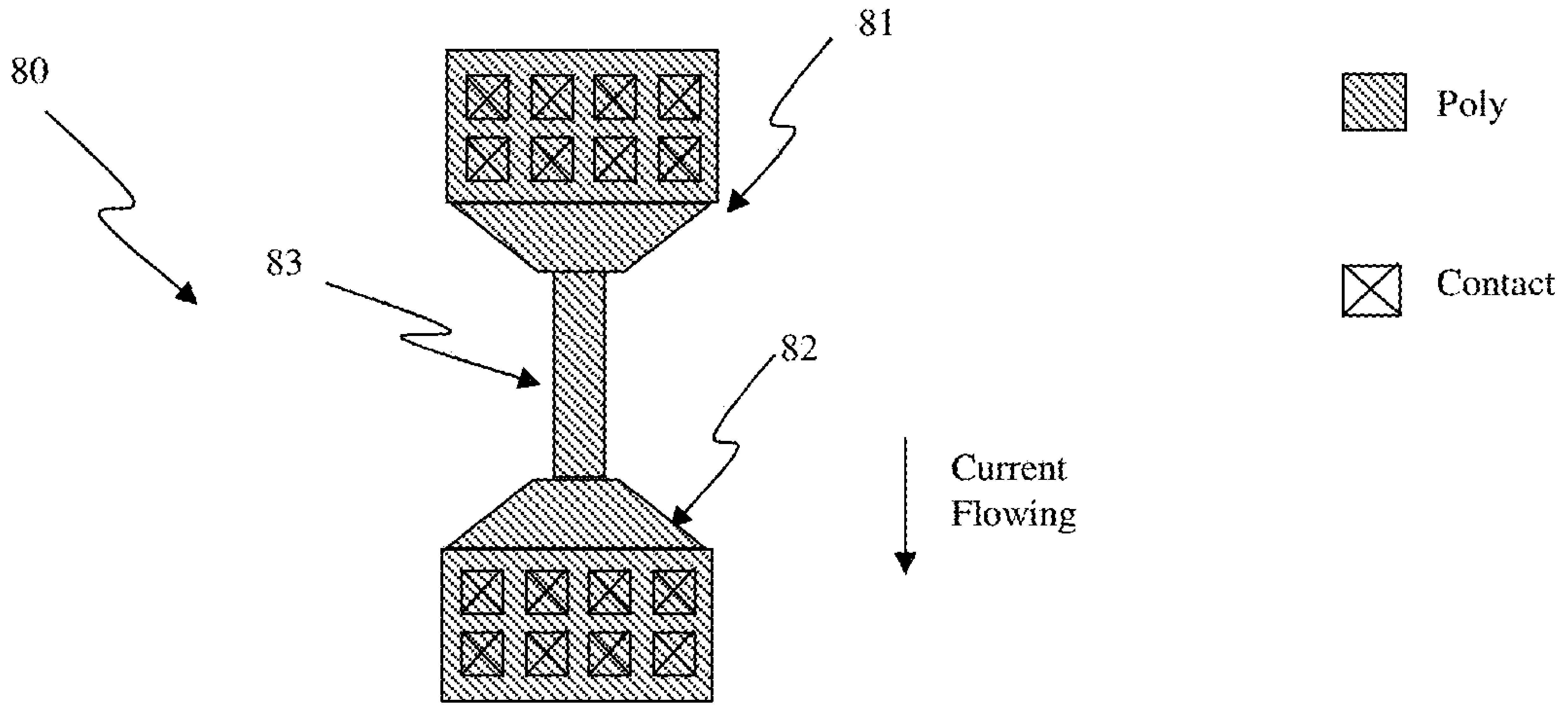
80
81
83
82
Poly
Contact
Current
Flowing

FIG. 3(a)

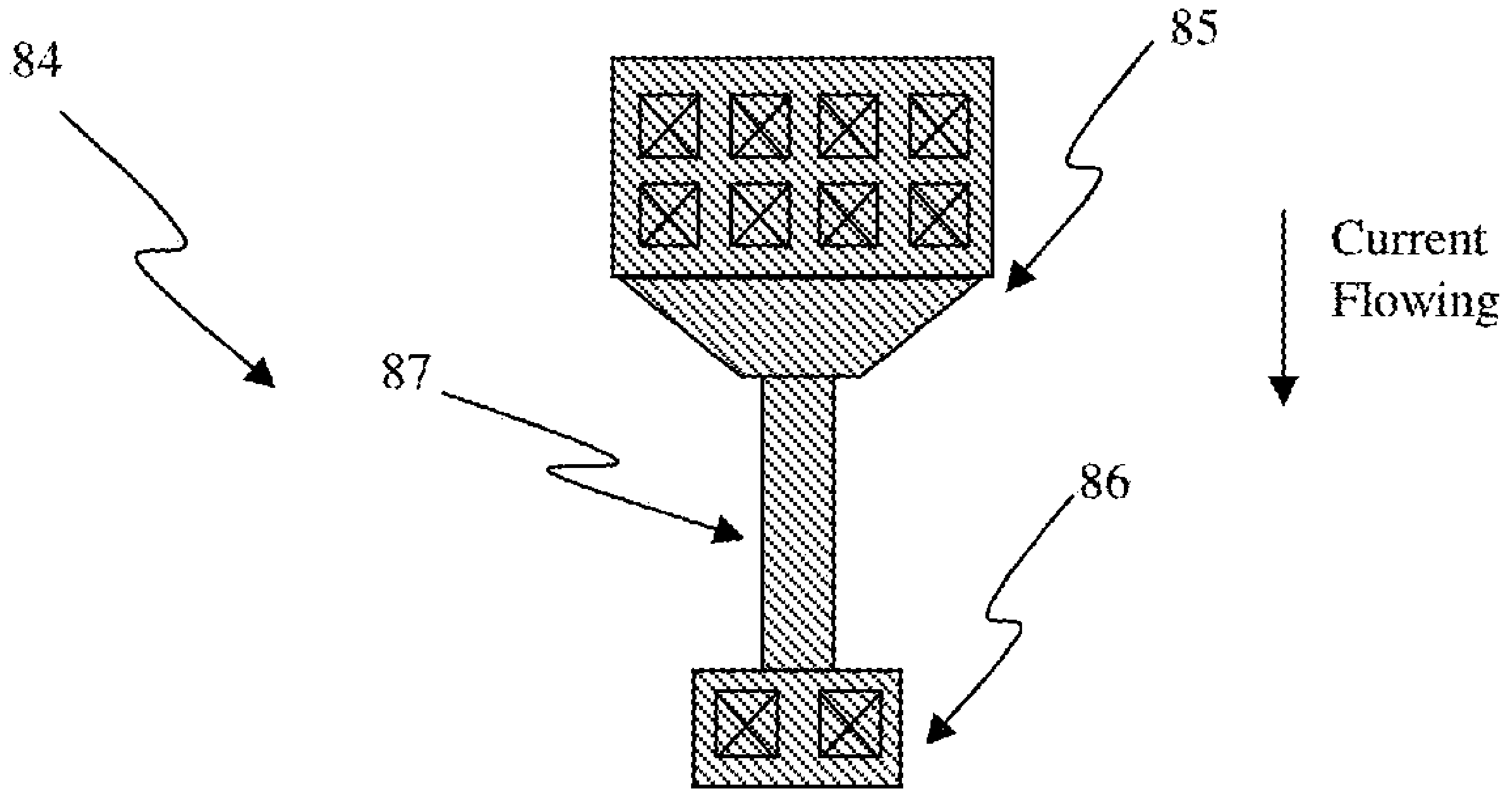
84
85
87
86
Current
Flowing

FIG. 3(b)

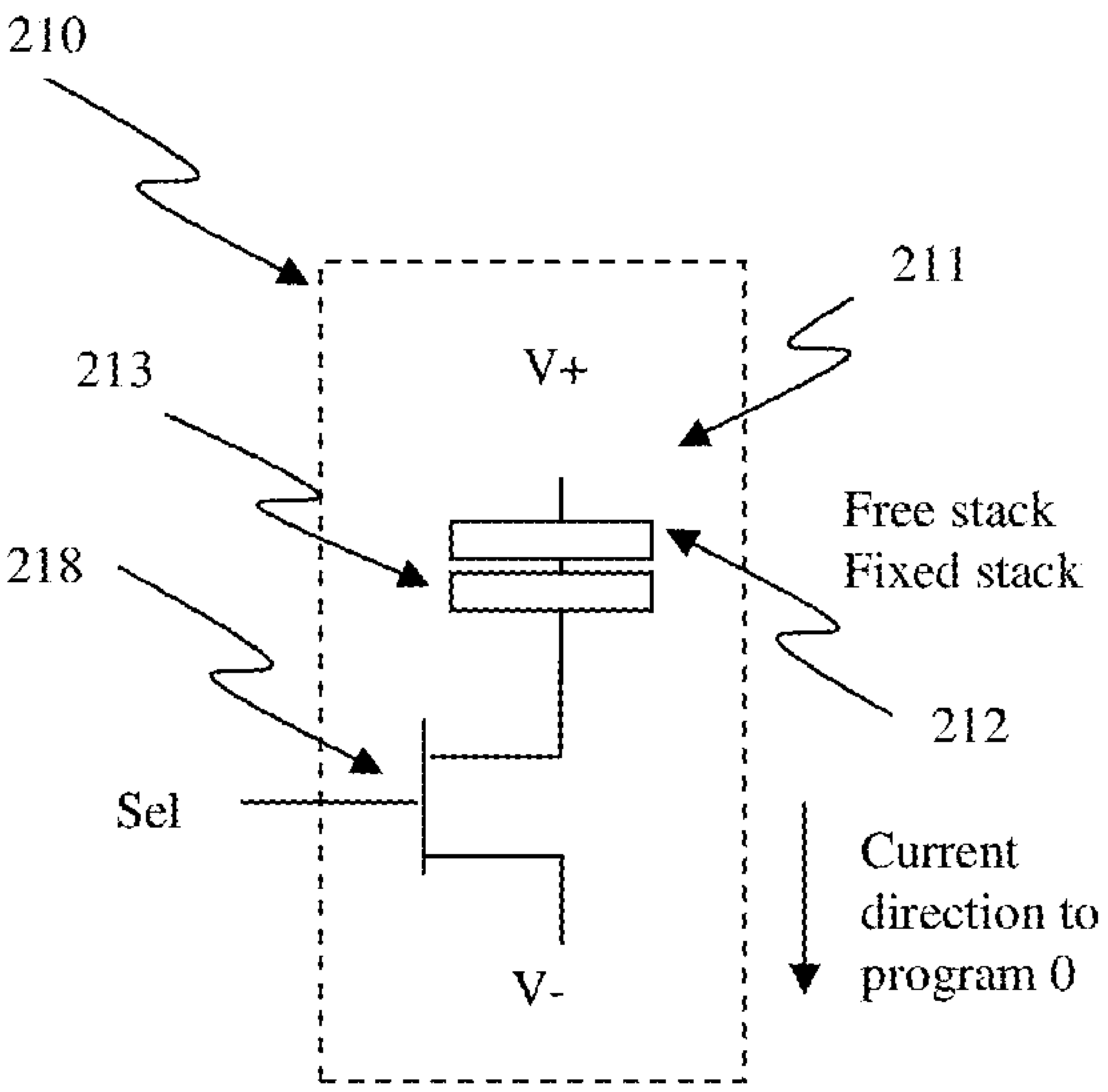
210
211
V+
213
Free stack
Fixed stack
218
212
Sel
Current
direction to
program 0
V-

FIG. 4(a)

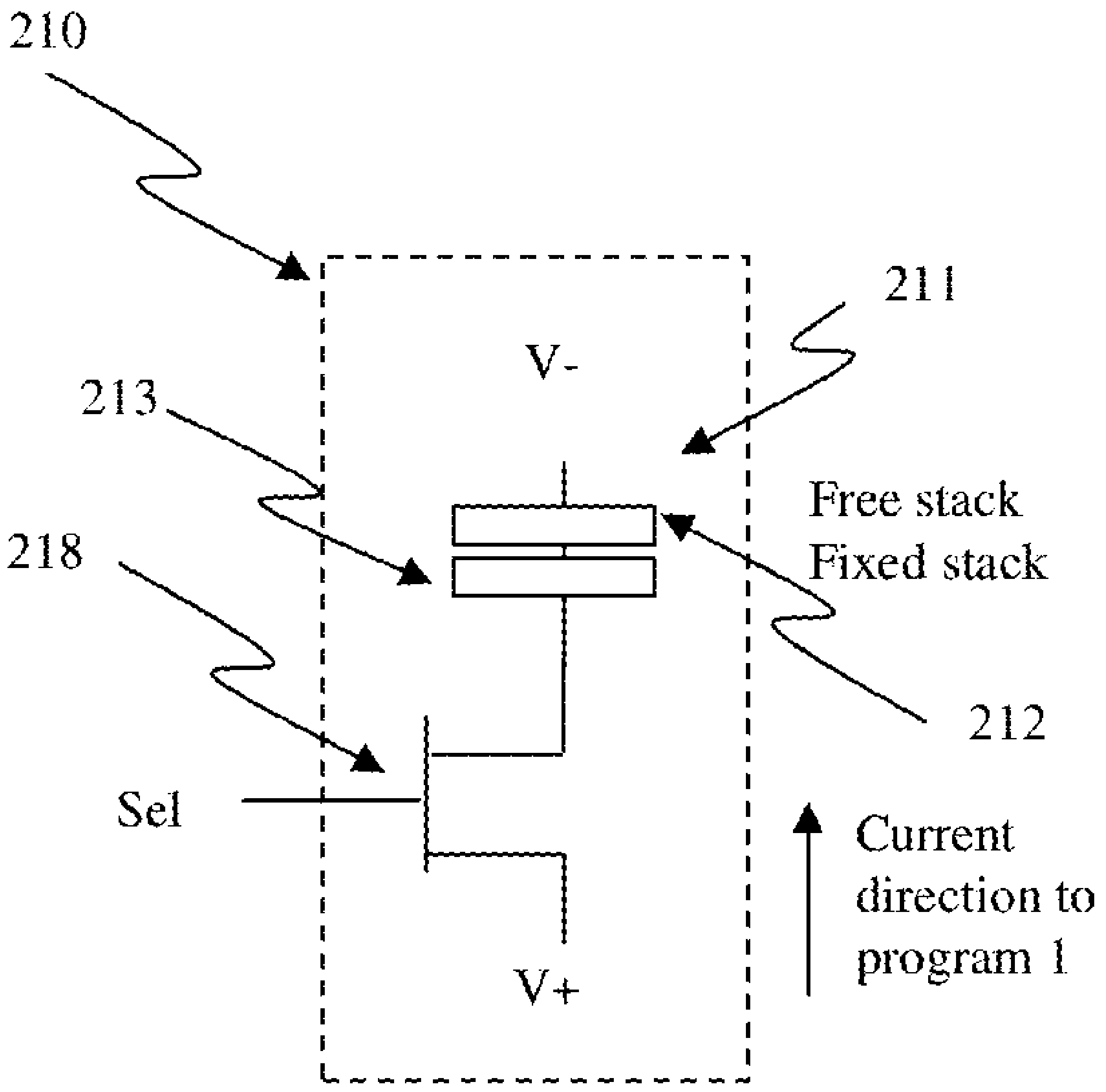
210
211
V-
213
Free stack
Fixed stack
218
212
Sel
Current
direction to
program 1
V+

FIG. 4(b)

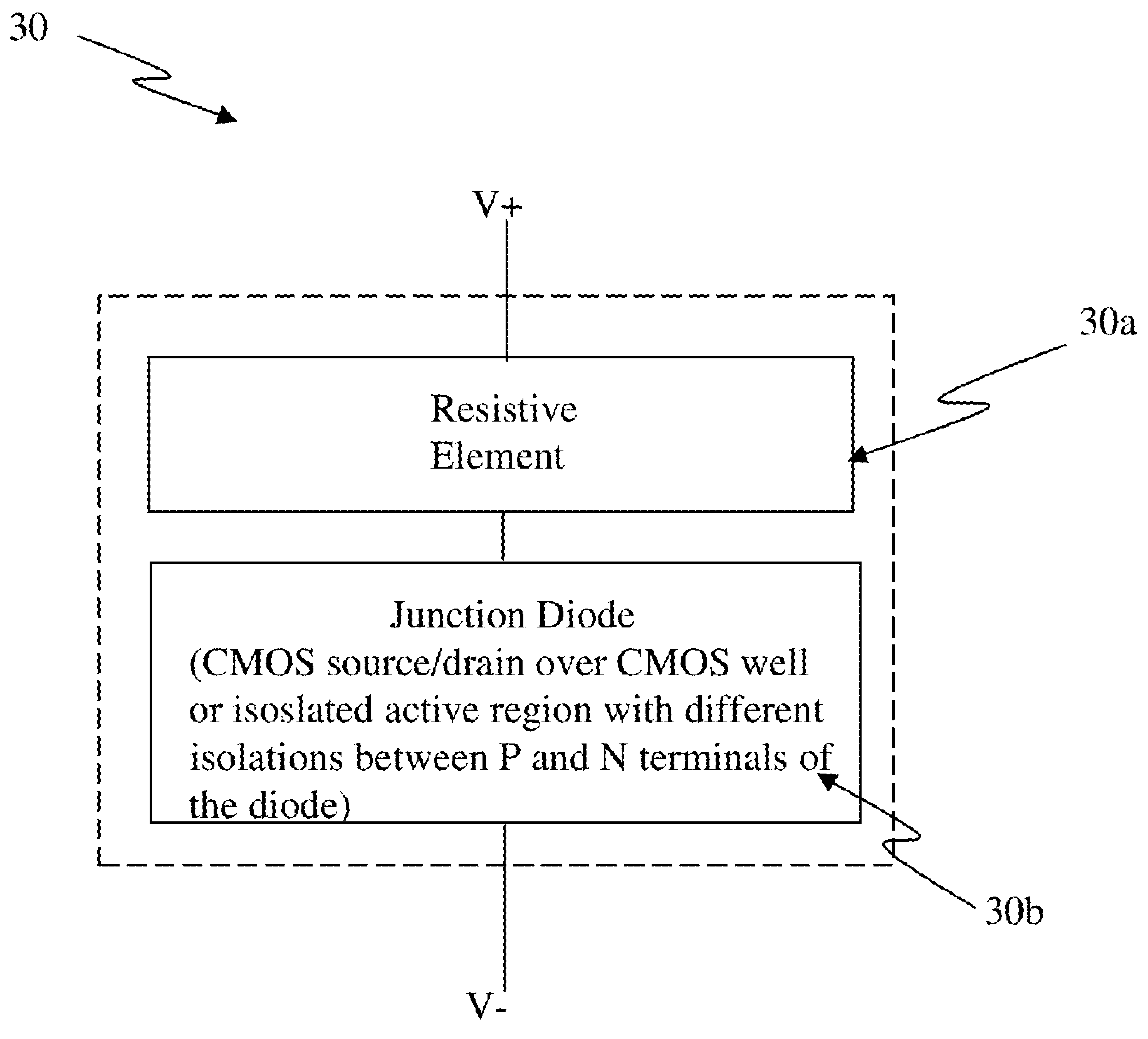
30
V+
30a
Resistive Element
Junction Diode
(CMOS source/drain over CMOS well or isoslated active region with different isolations between P and N terminals of the diode)
30b
V-

FIG. 5(a)

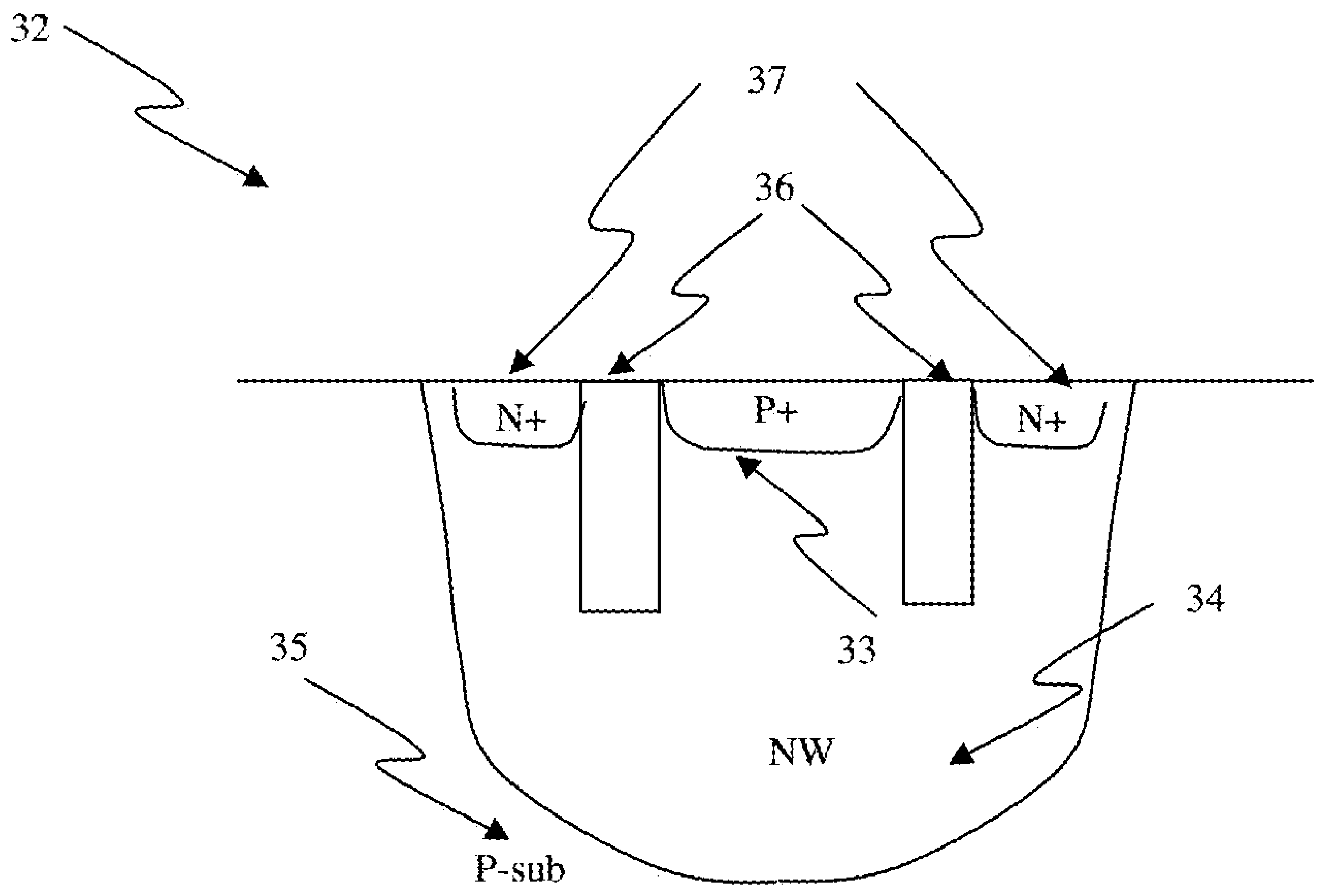
32
37
36
N+
P+
N+
33
34
35
NW
P-sub

FIG. 5(b)

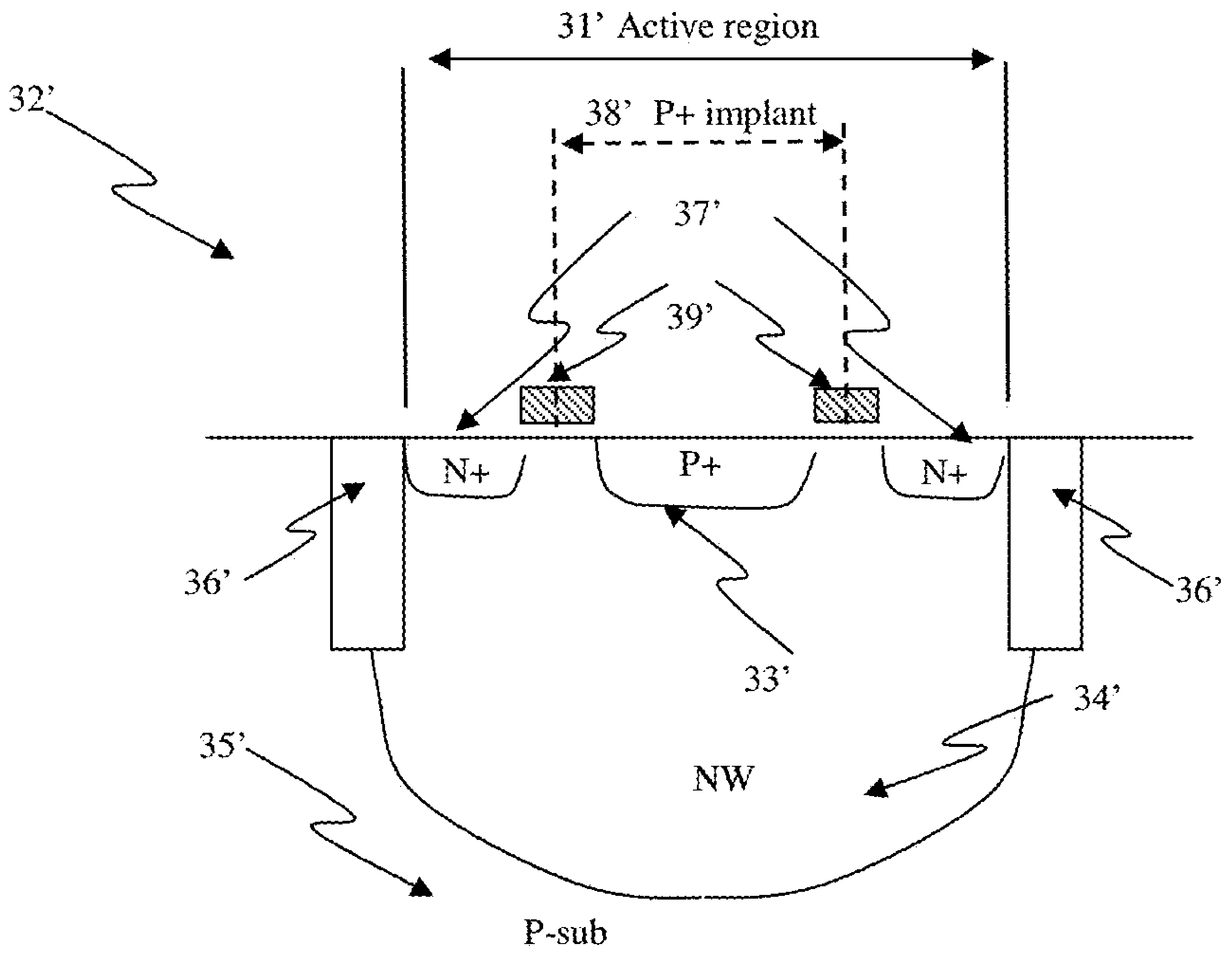
31' Active region
32'
38' P+ implant
37'
39'
N+
P+
N+
36'
36'
33'
34'
35'
NW
P-sub

FIG. 5(c)

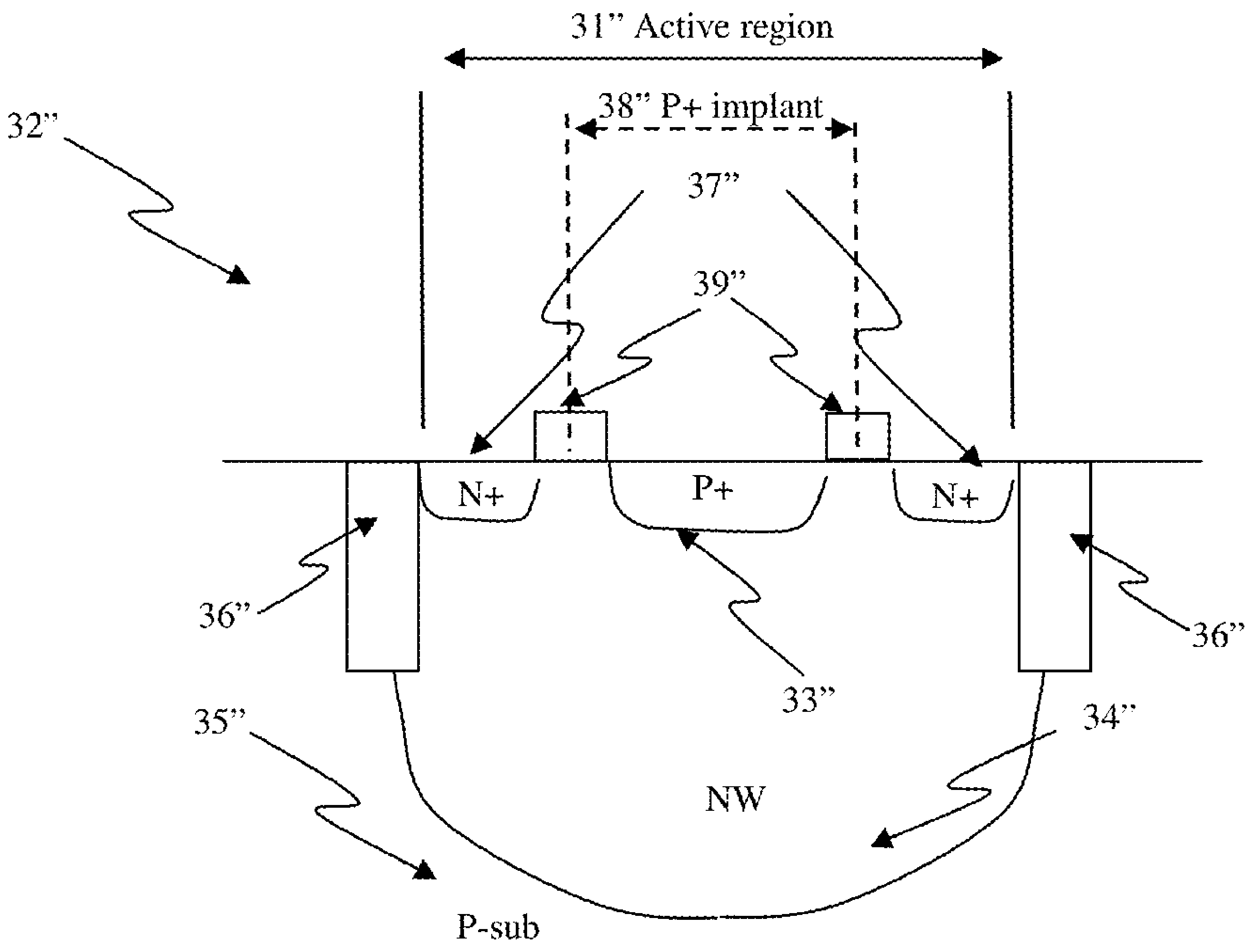

FIG. 5(d)

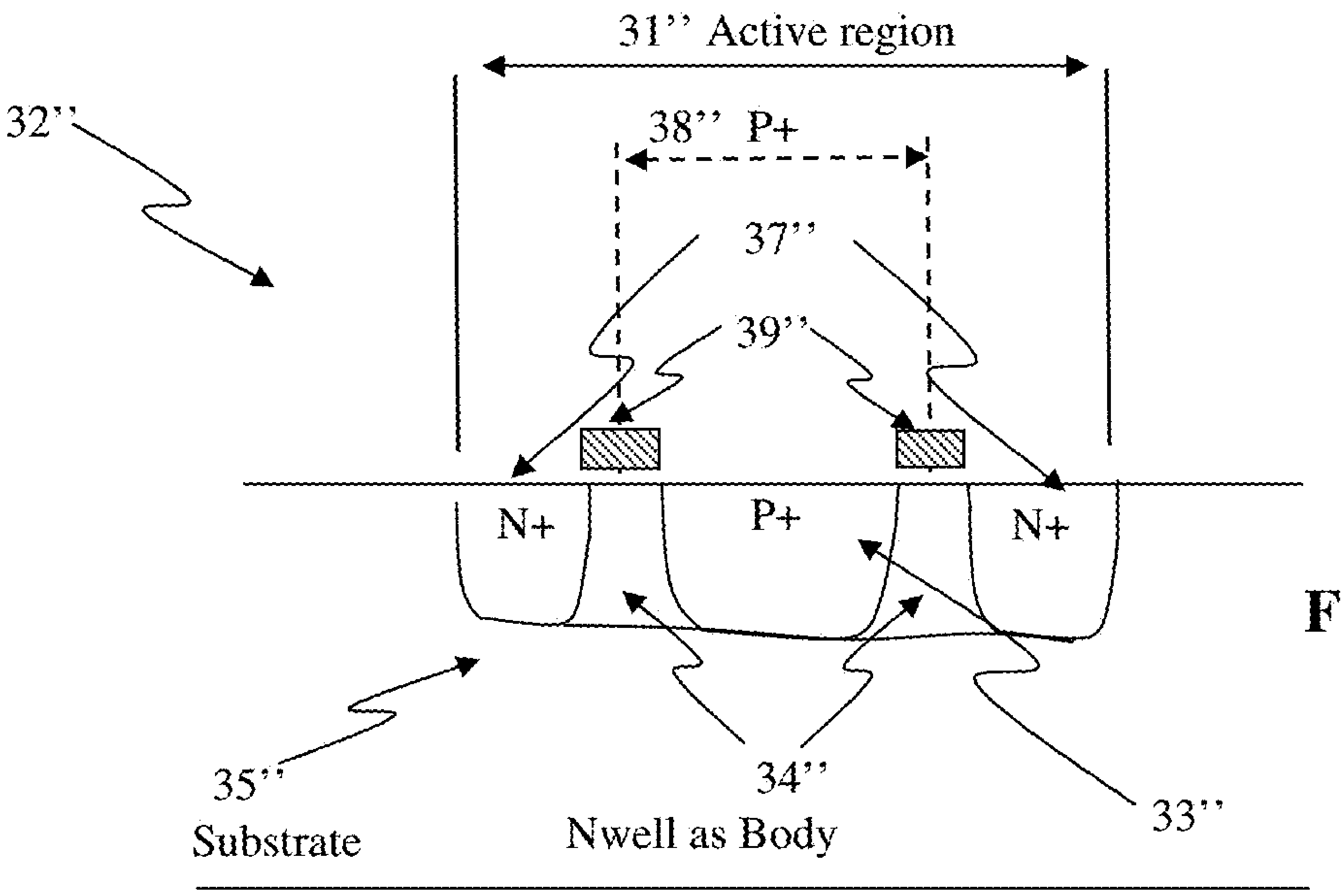

FIG. 6(a)

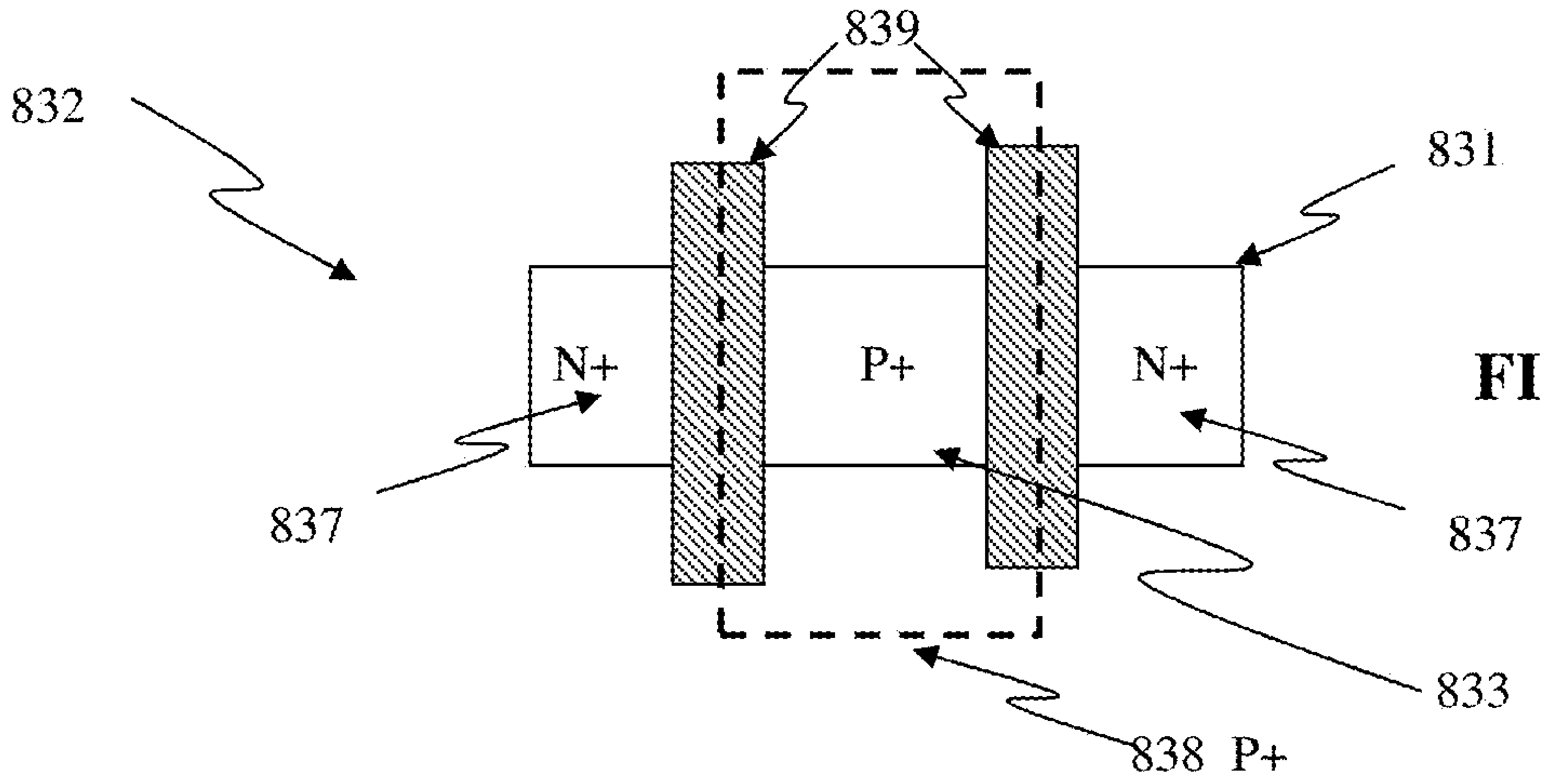

FIG. 6(a1)

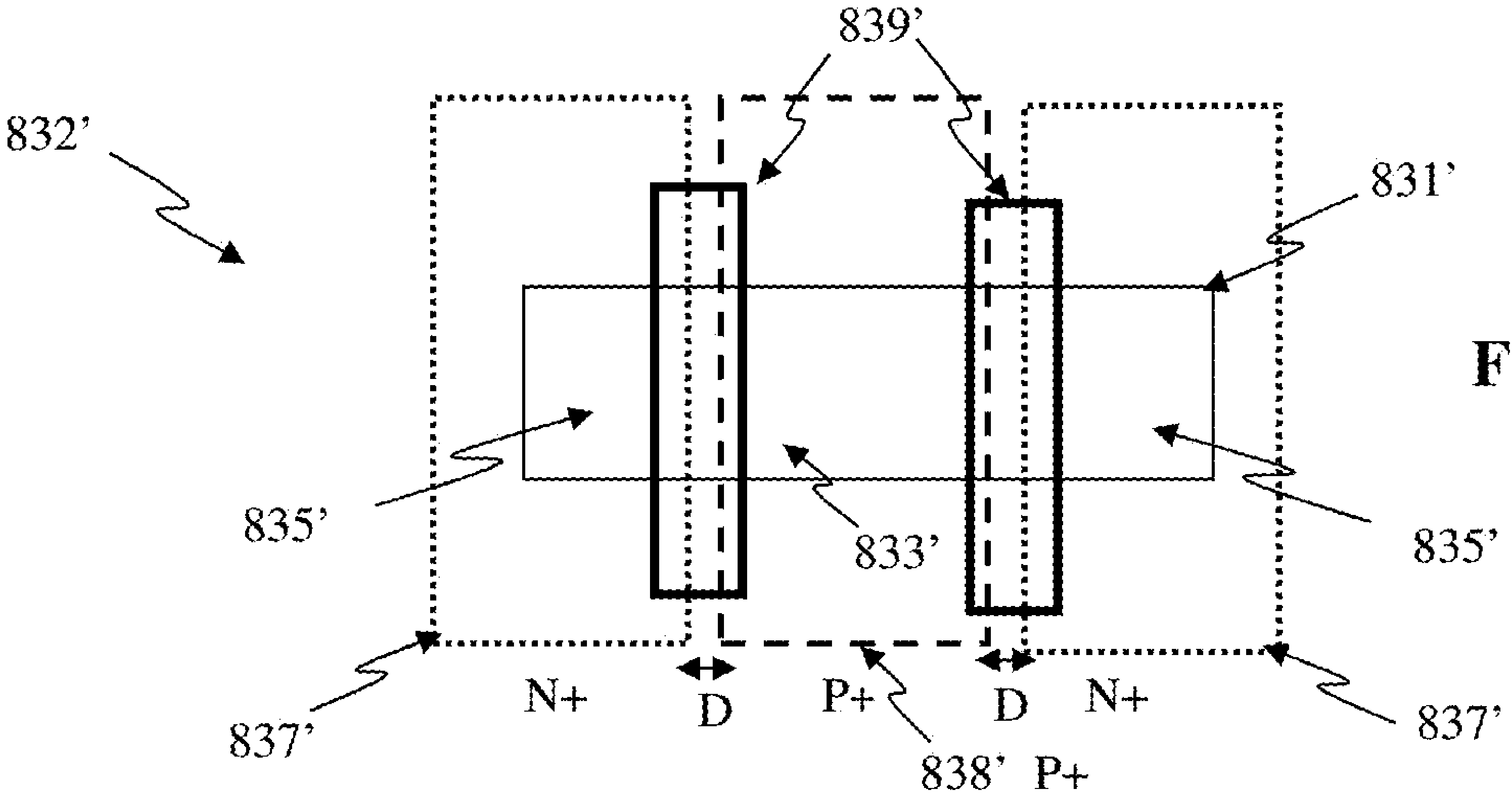

FIG. 6(a2)

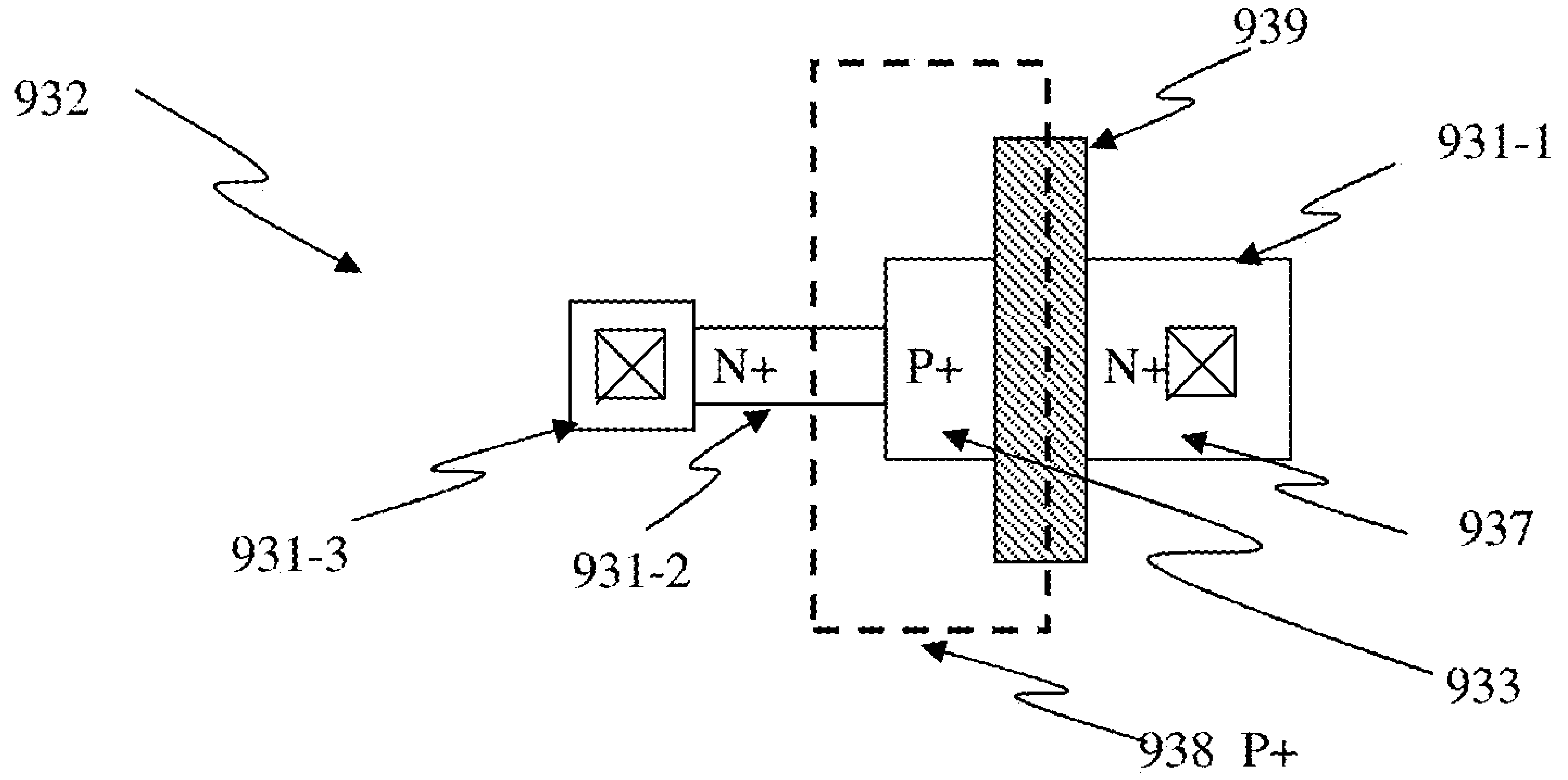

FIG. 6(a3)

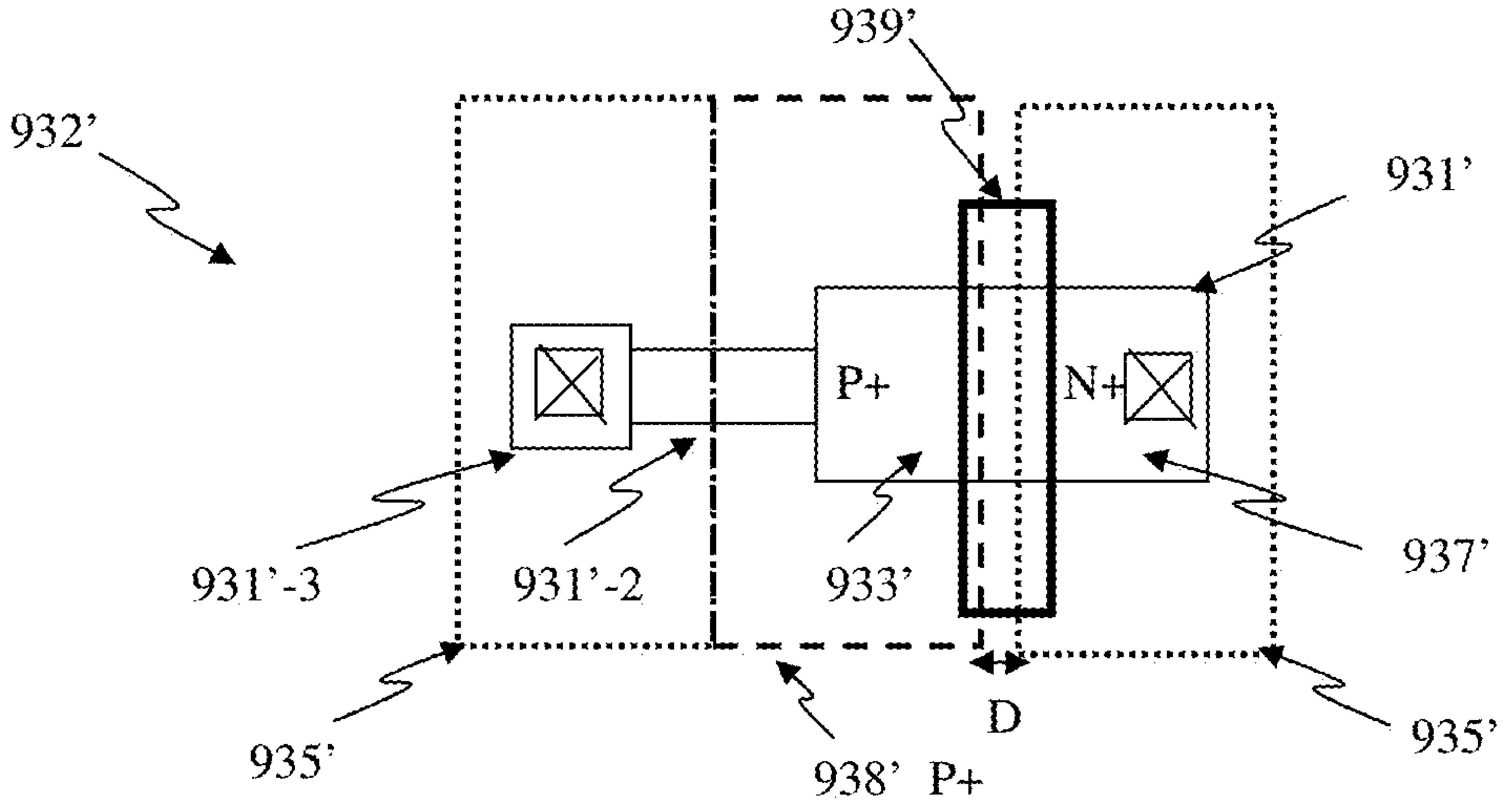

FIG. 6(a4)

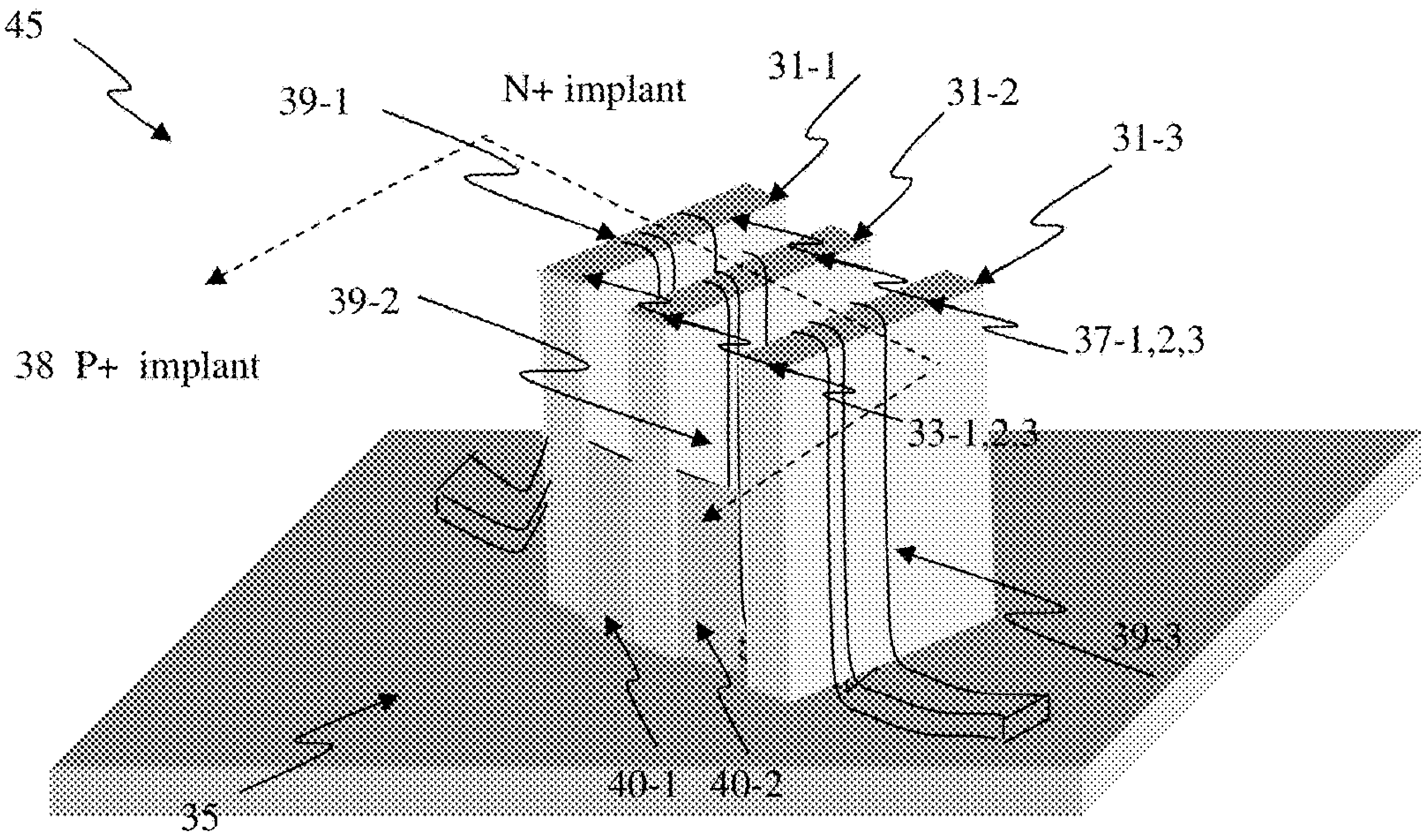

FIG. 6(b1)

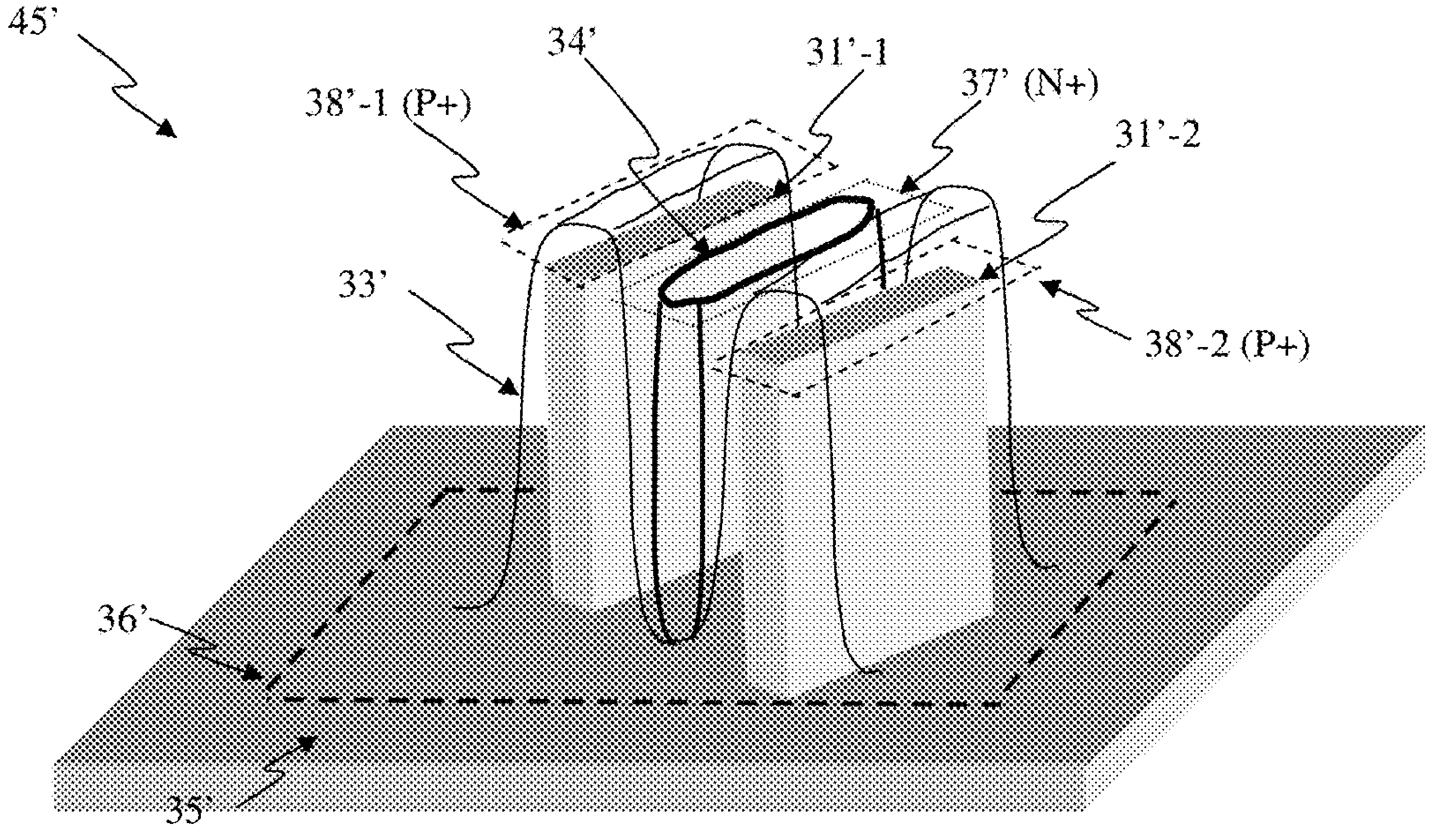

FIG. 6(b2)

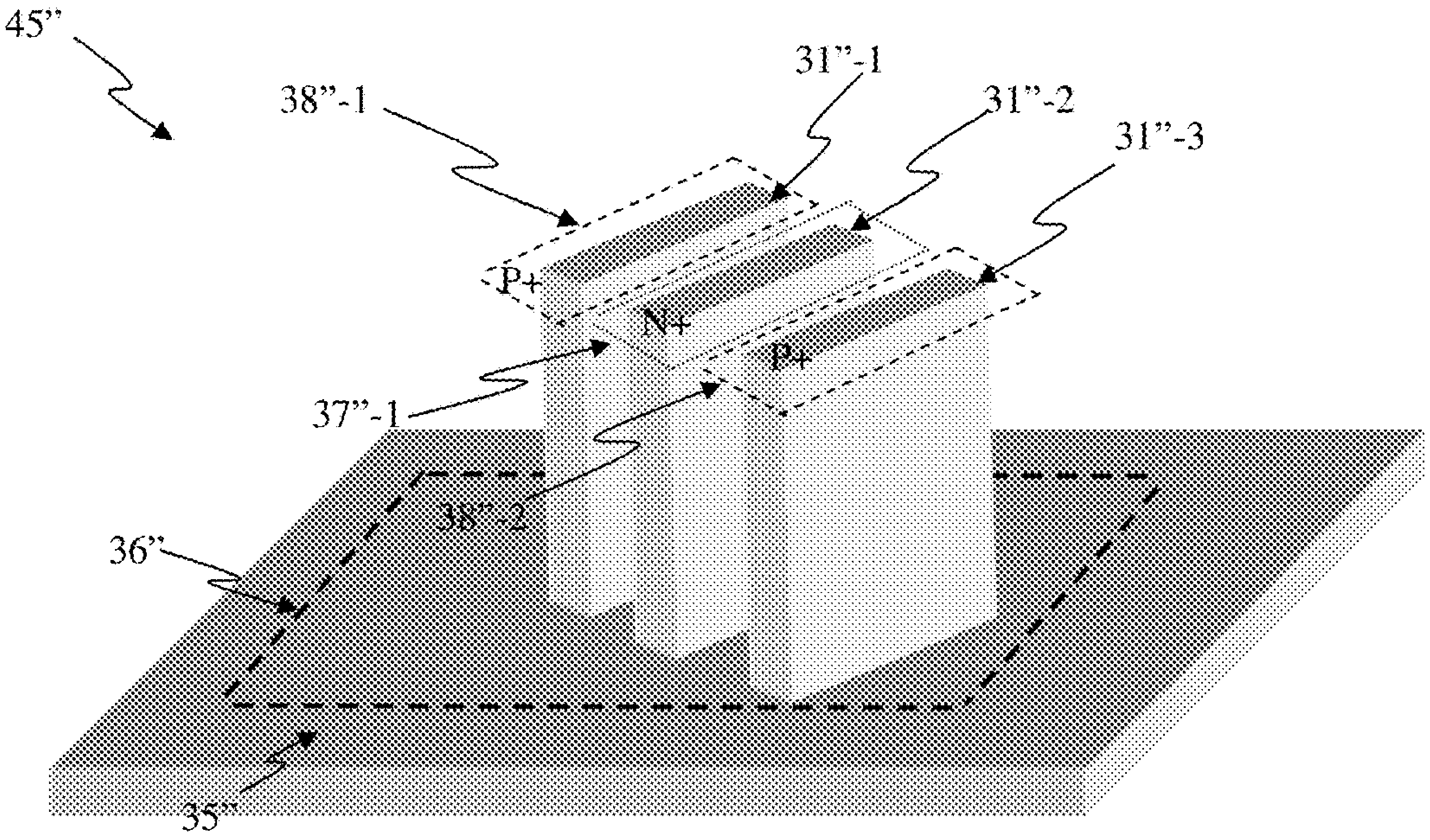

FIG. 6(b3)

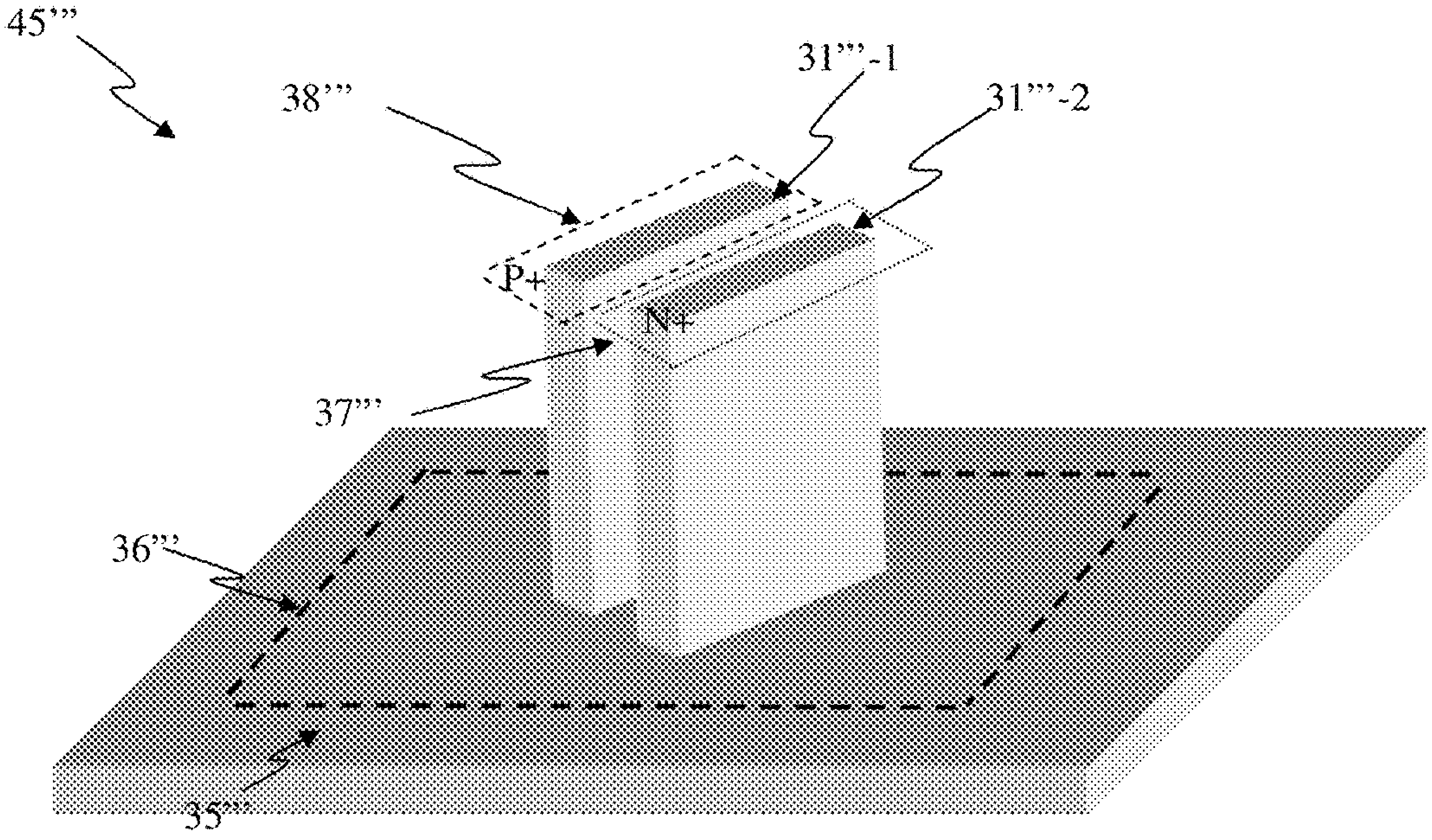

FIG. 6(b4)

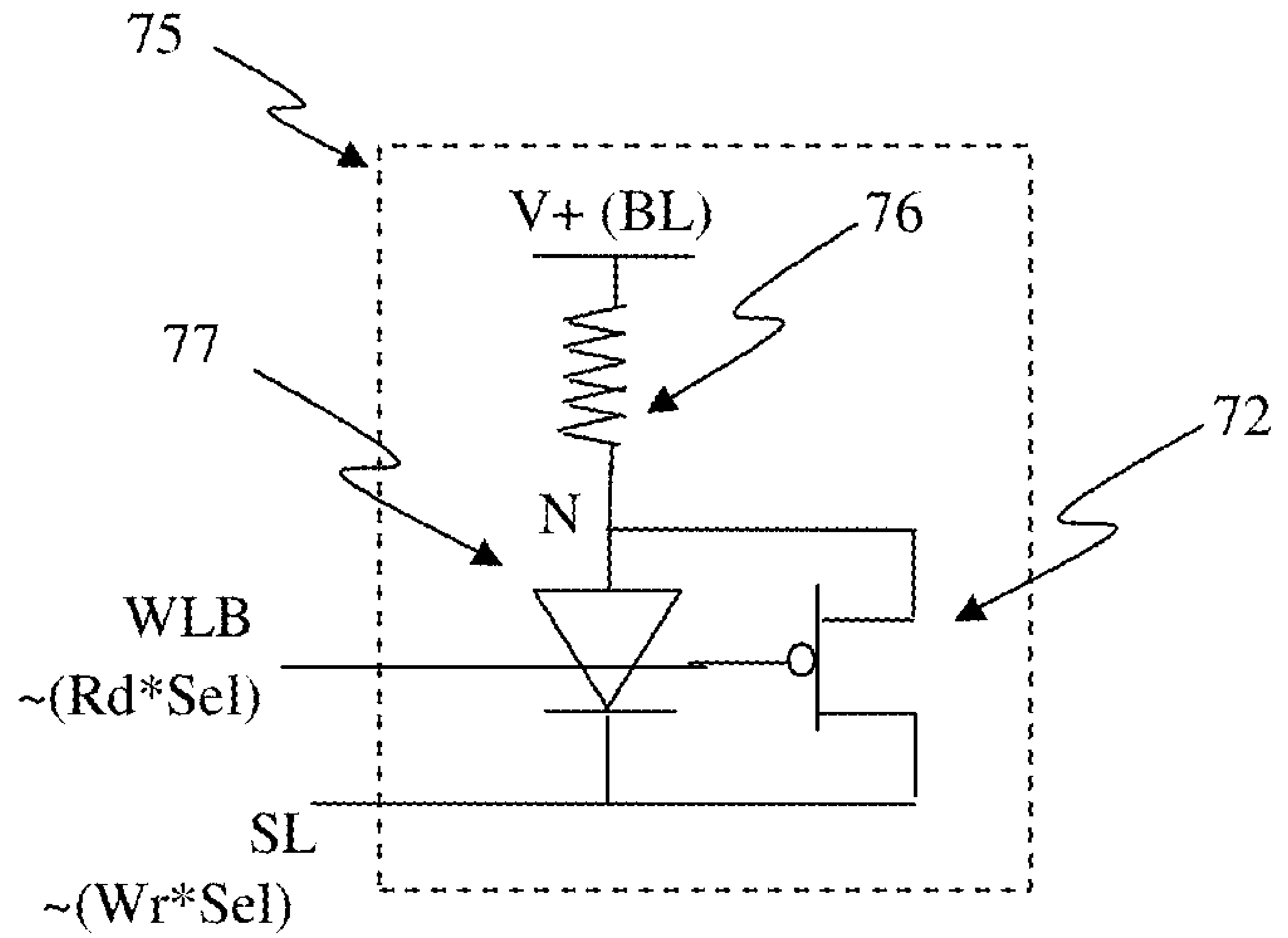

FIG. 6(c1)

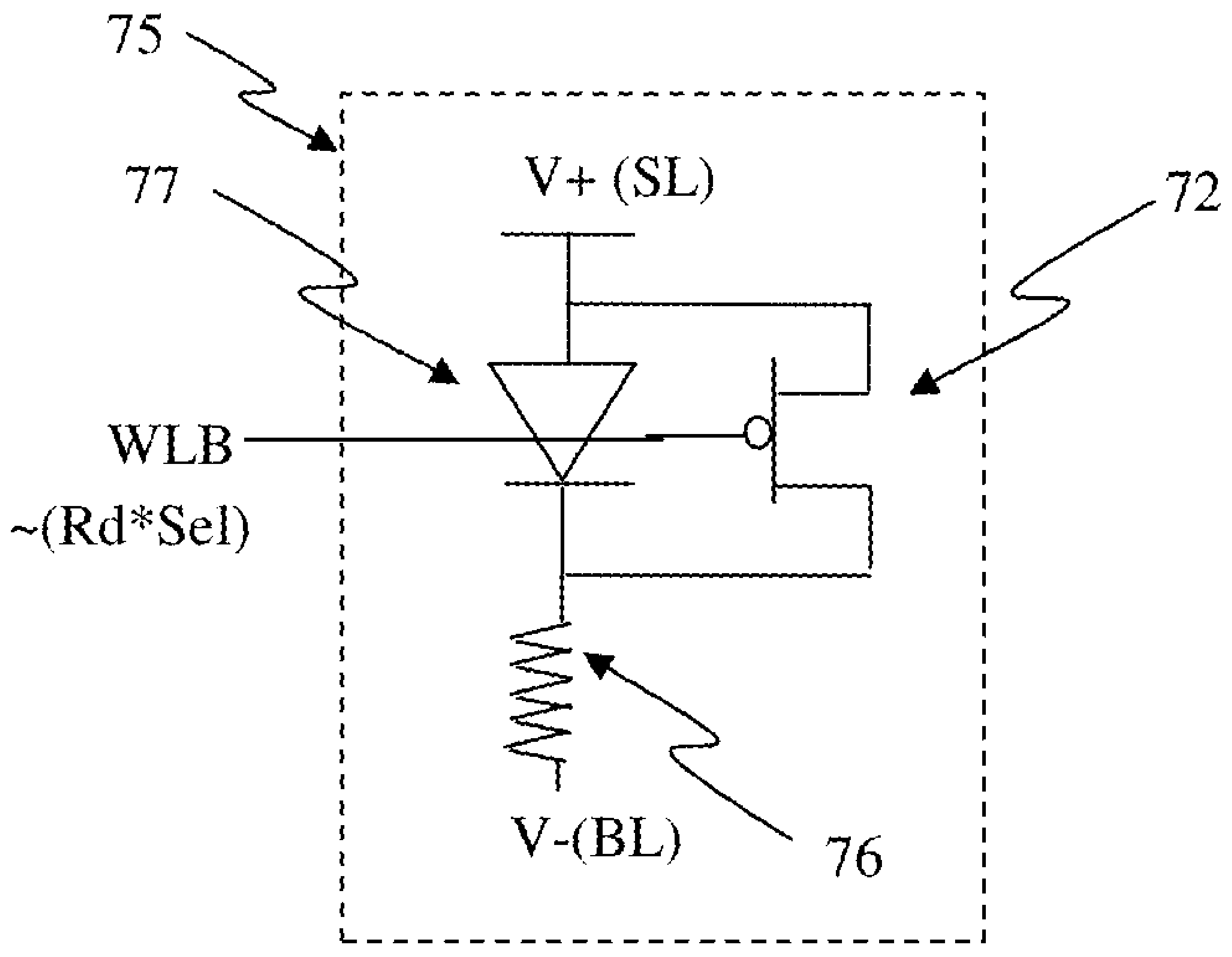

FIG. 6(c2)

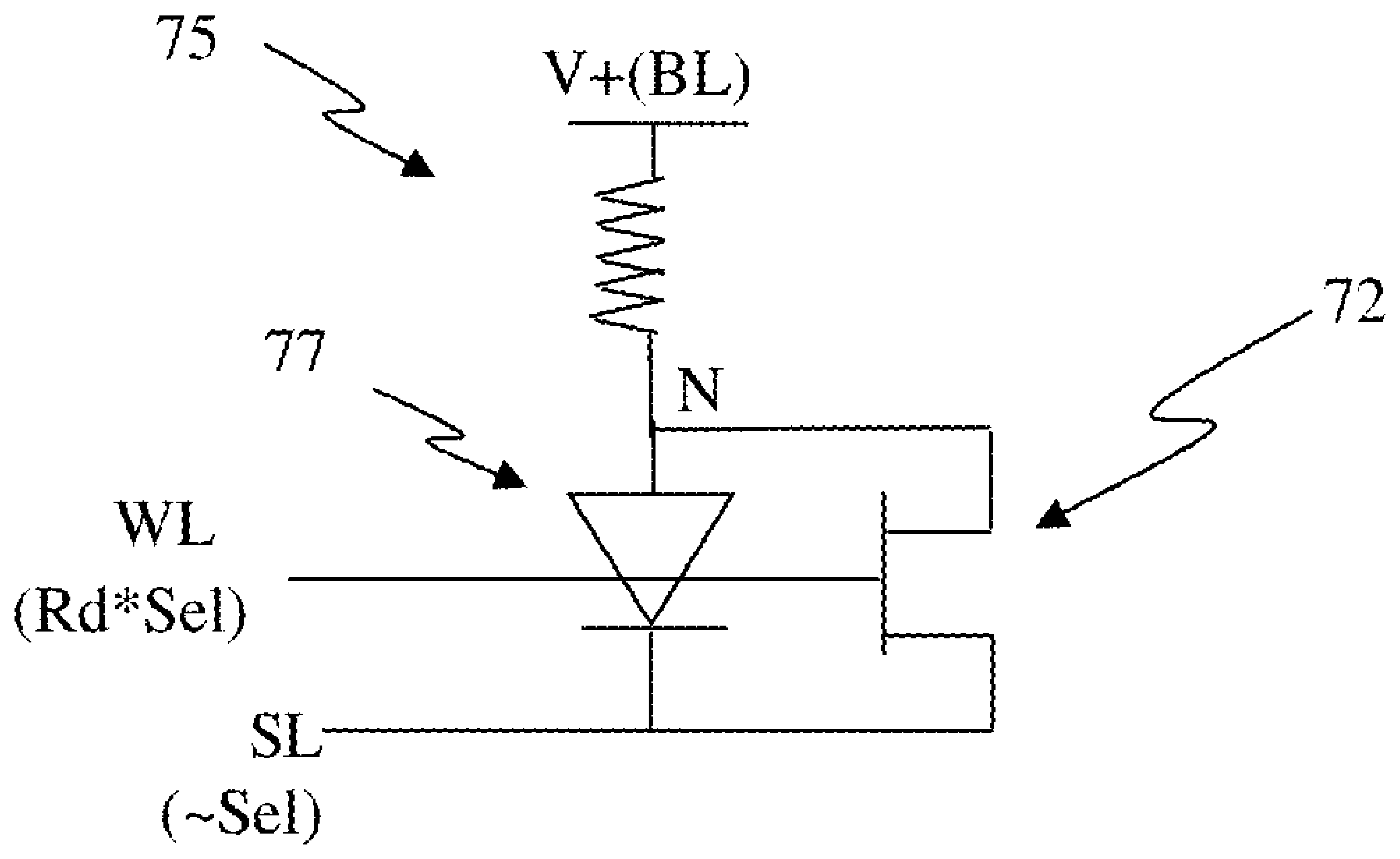

FIG. 6(c3)

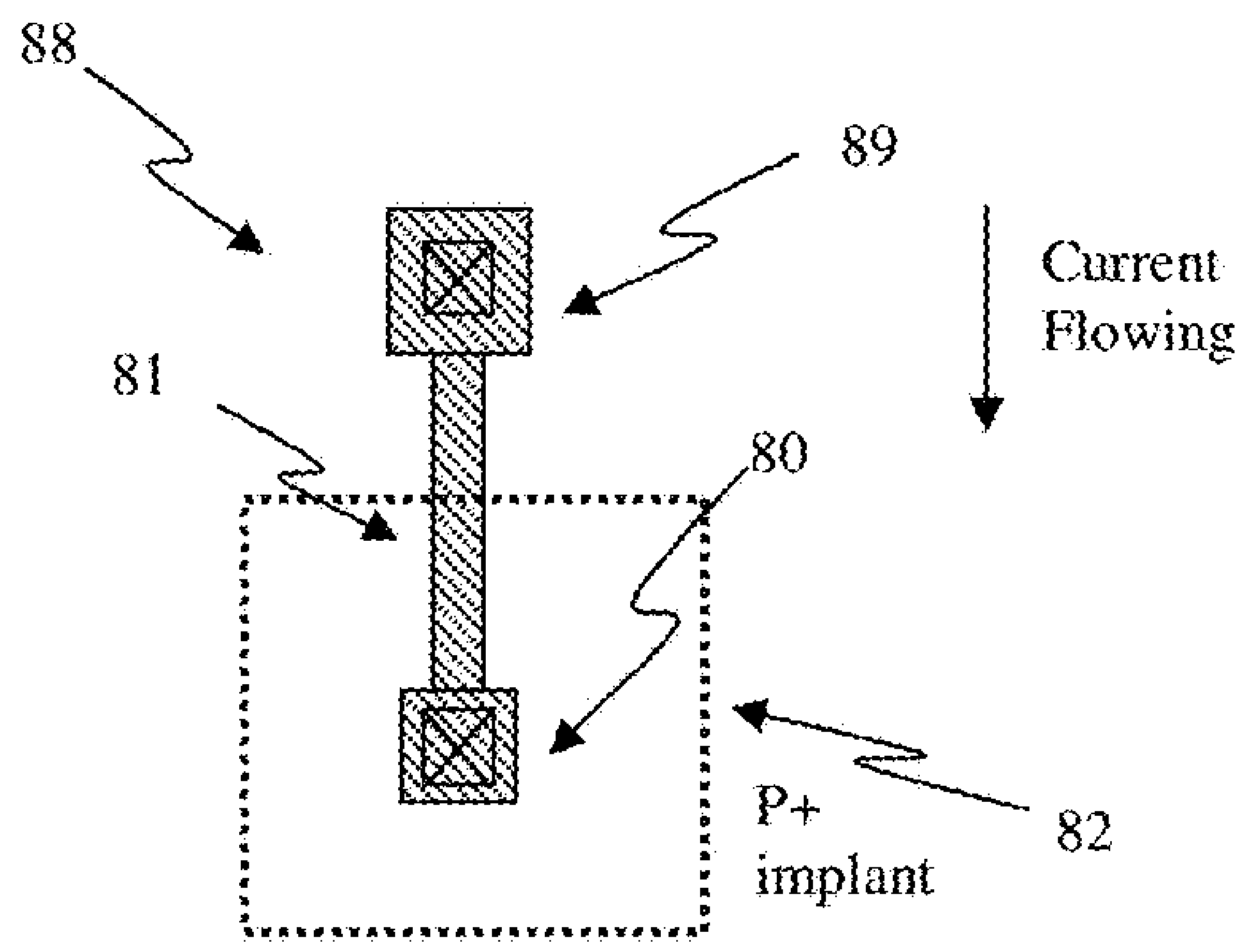

FIG. 7(a)

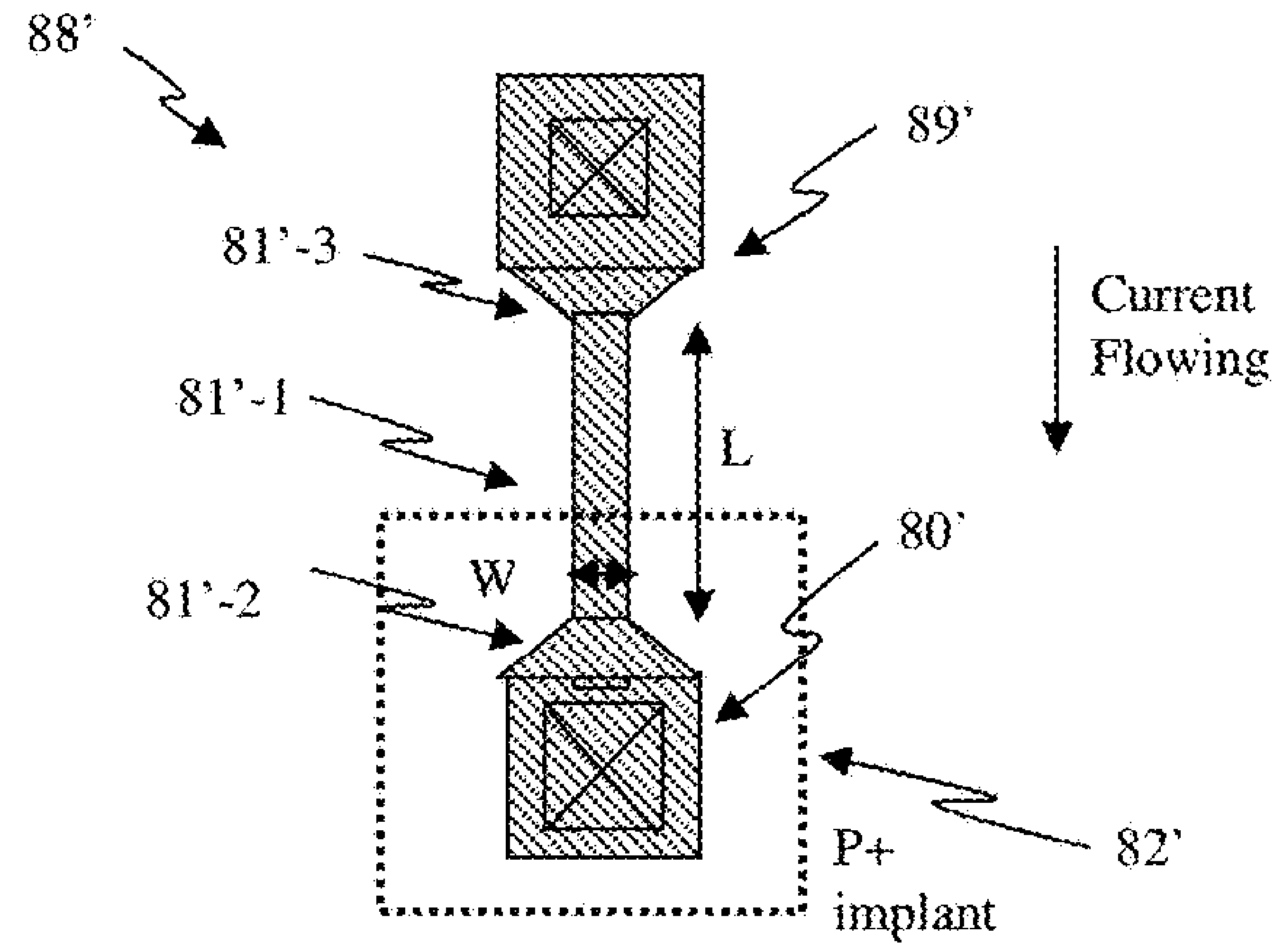

FIG. 7(a1)

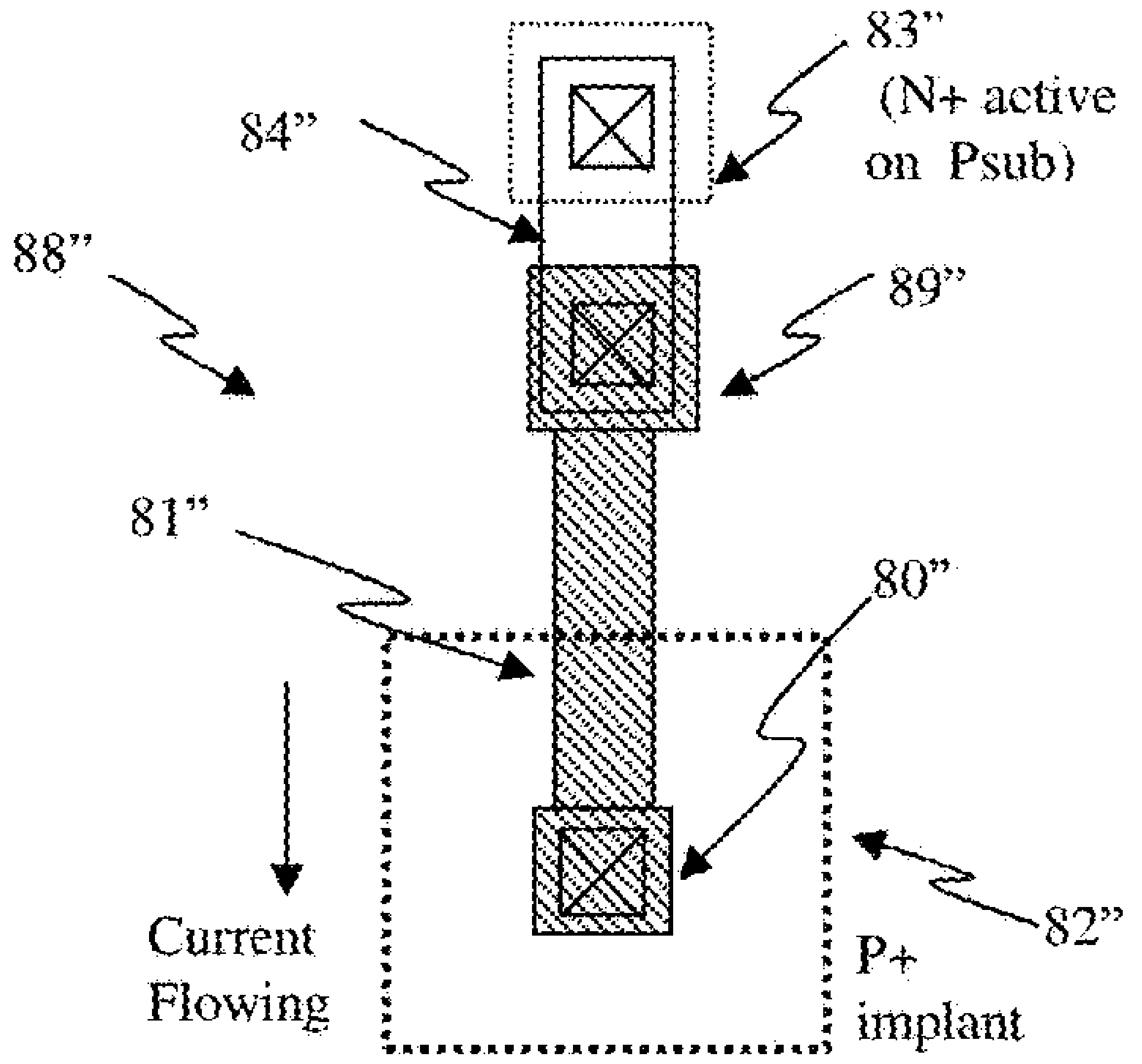

FIG. 7(a2)

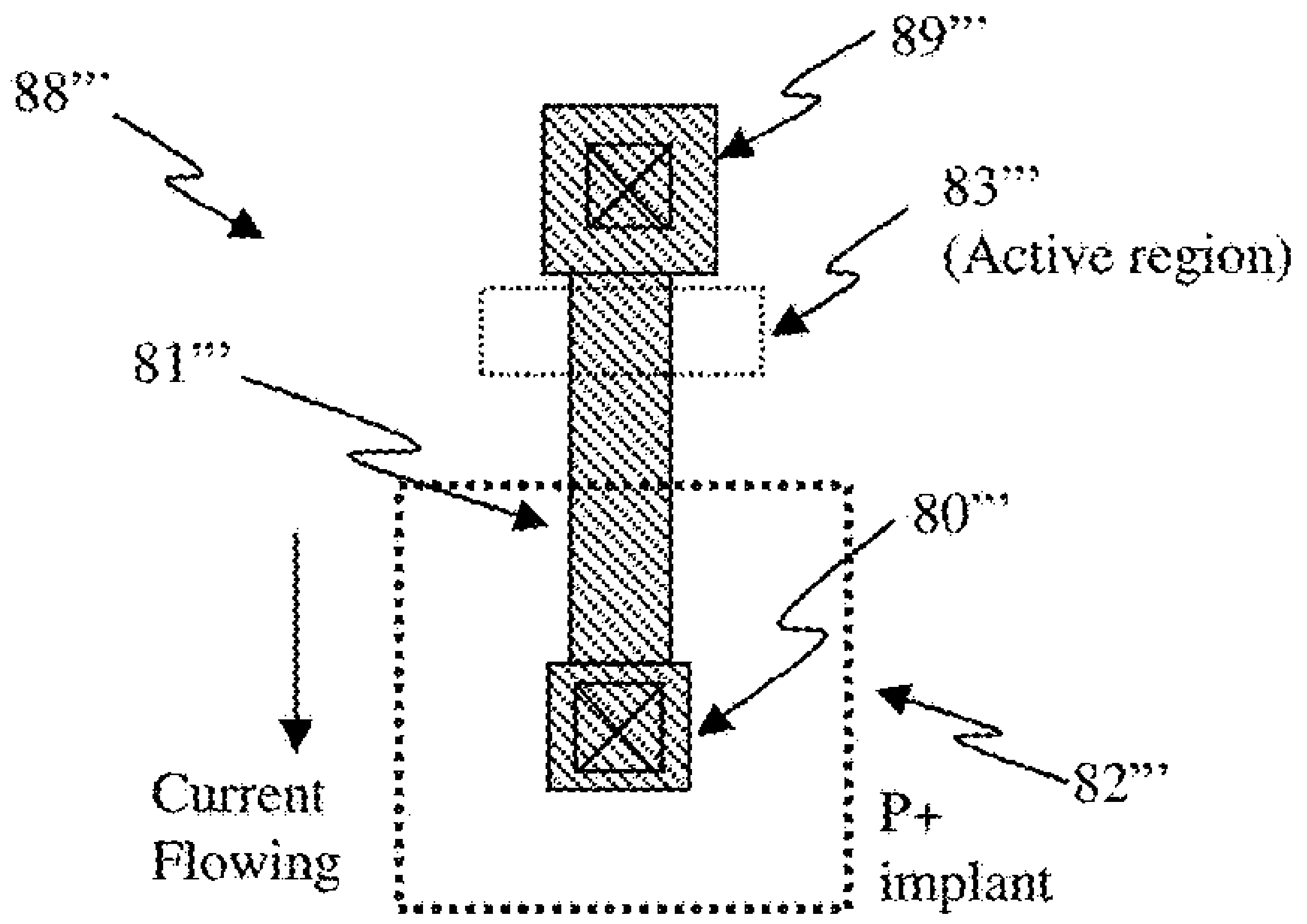

FIG. 7(a3)

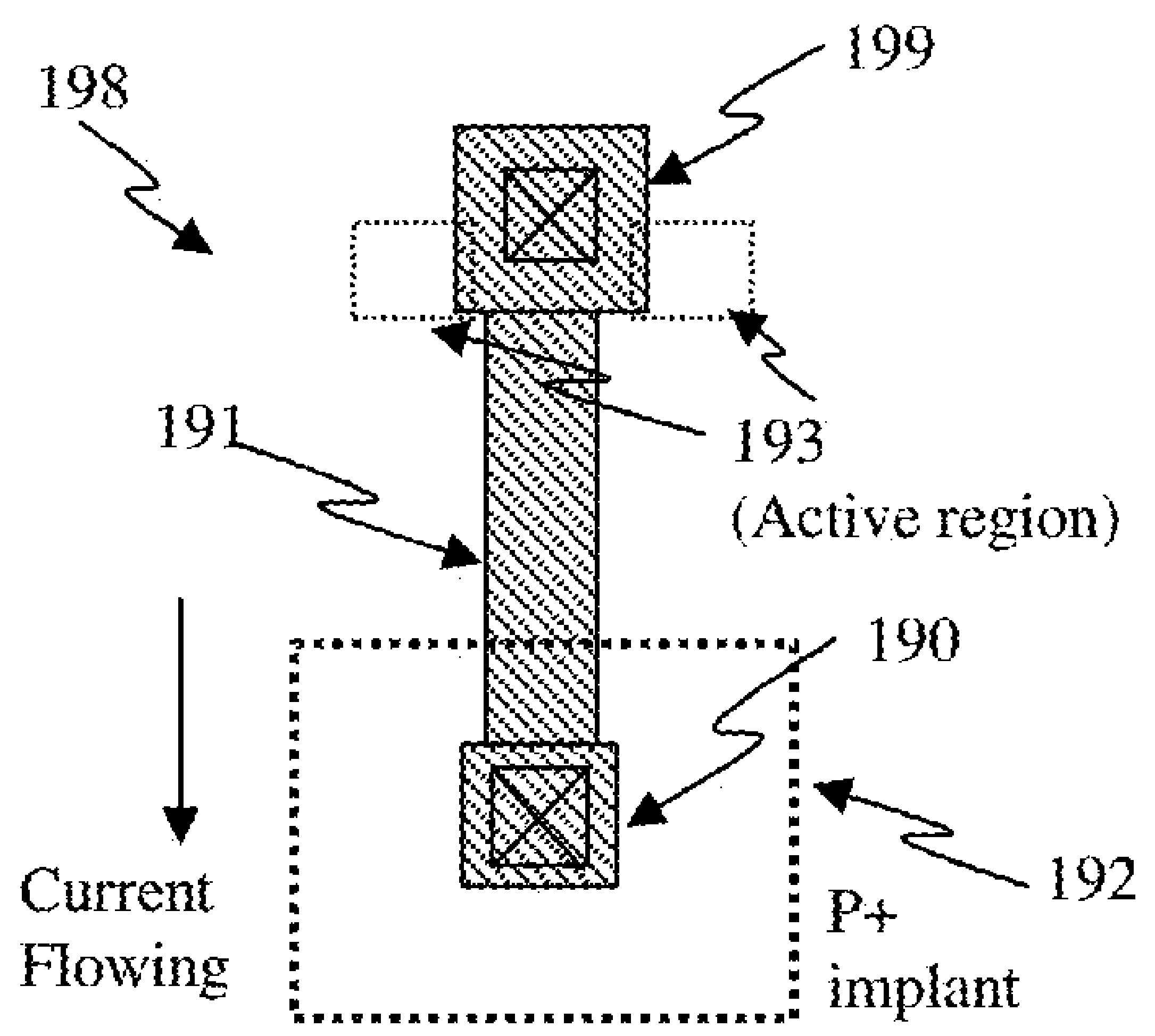

FIG. 7(a3a)

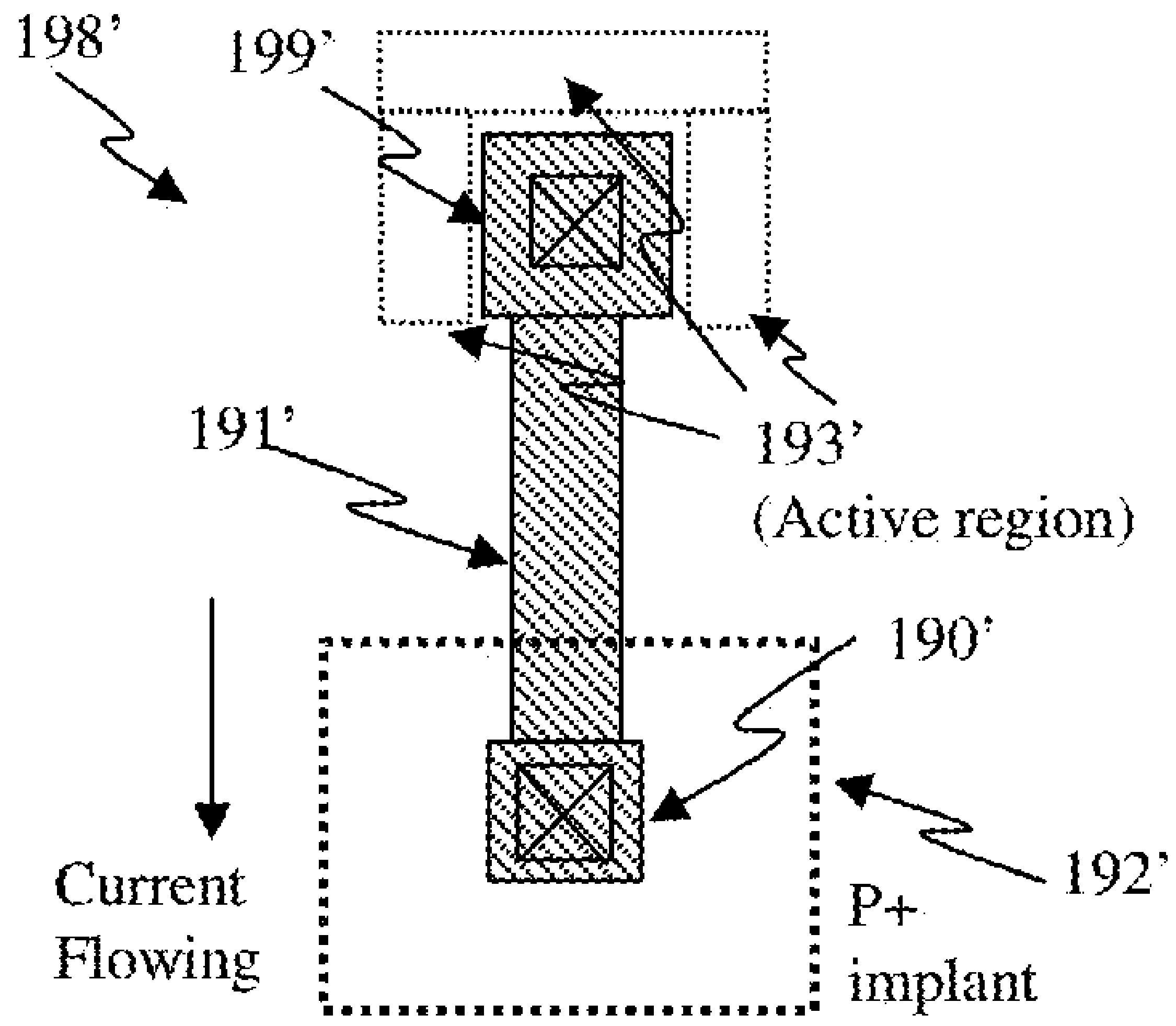

FIG. 7(a3b)

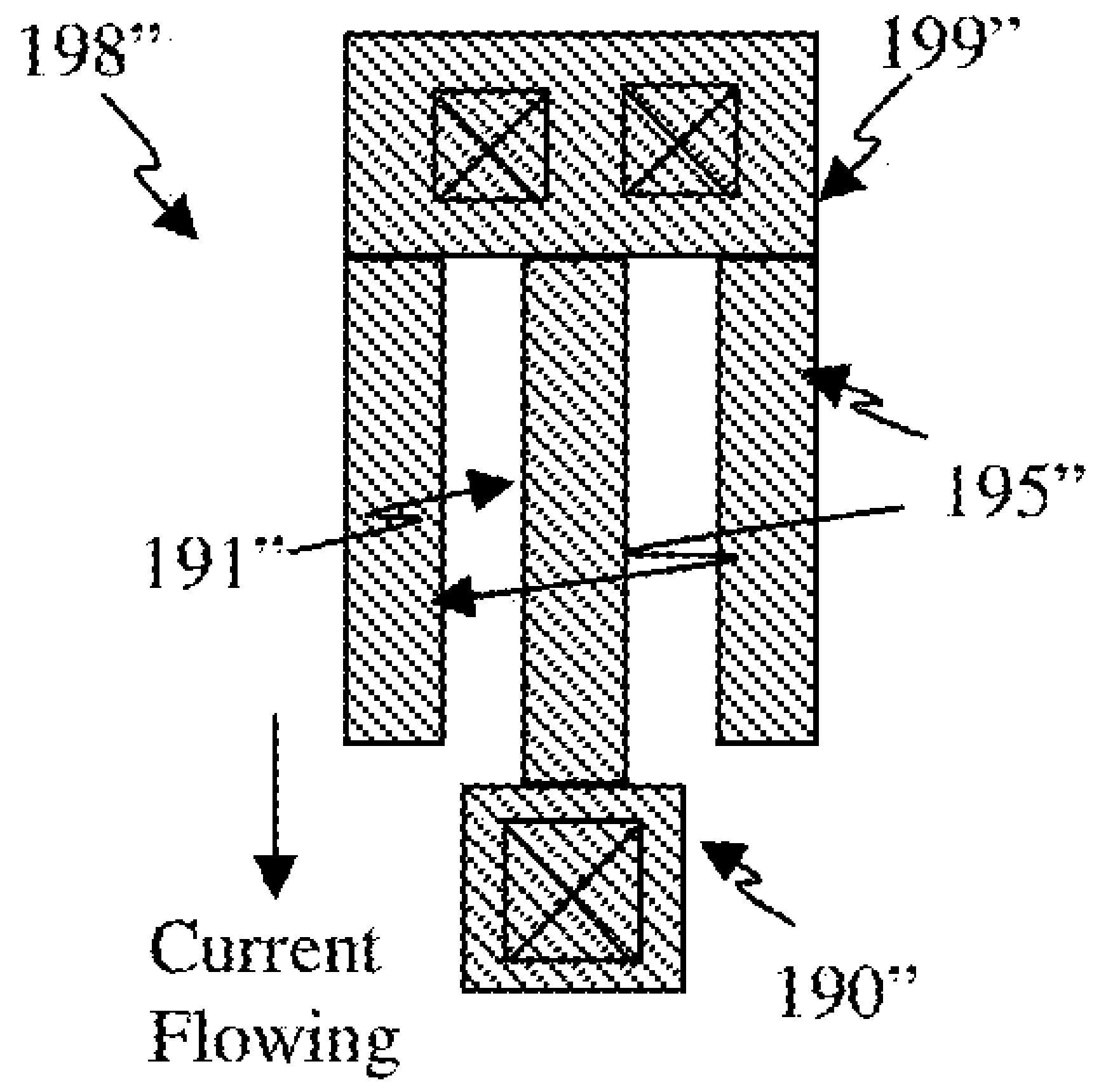

FIG. 7(a3c)

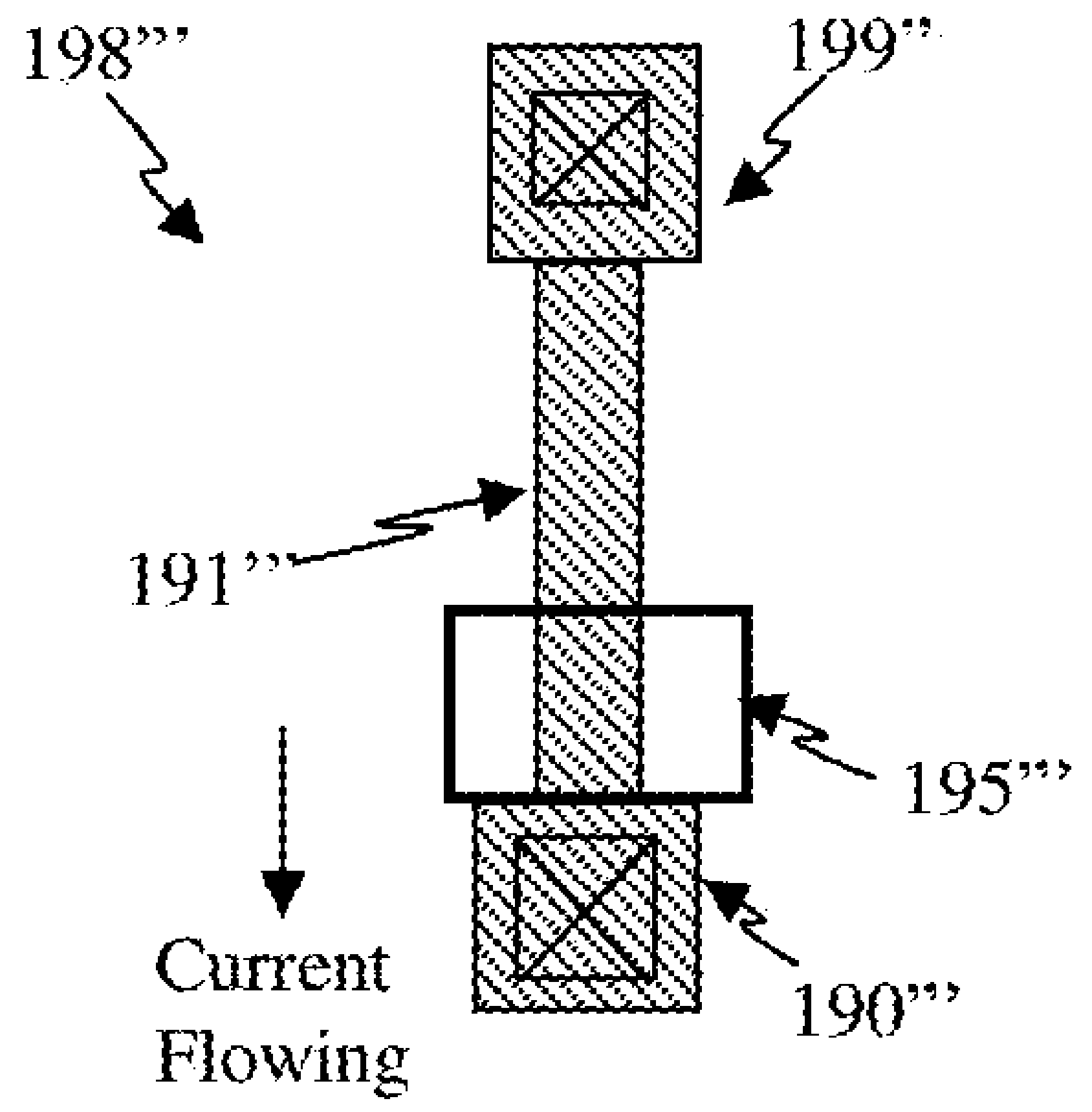

FIG. 7(a3d)

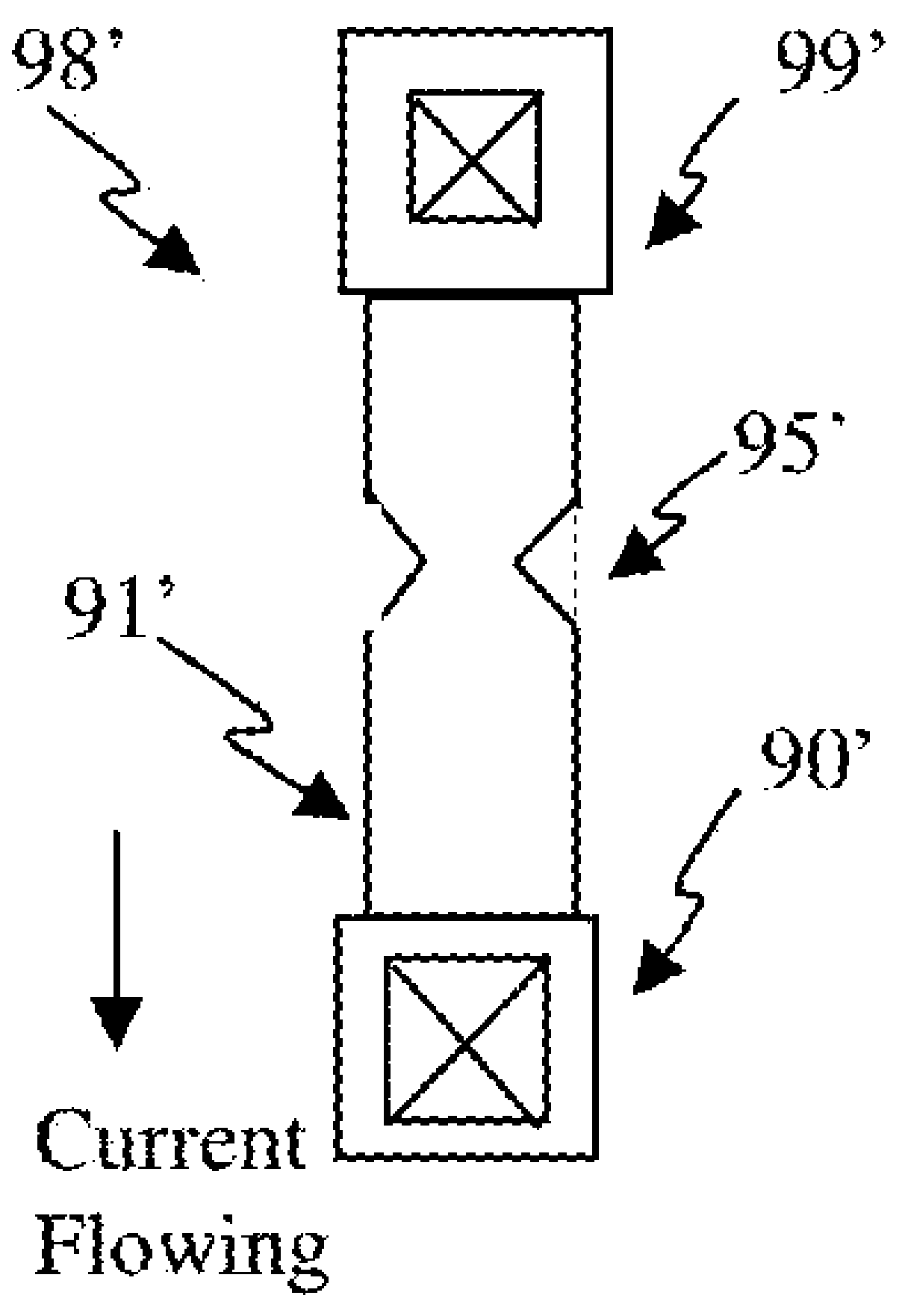

FIG. 7(a4)

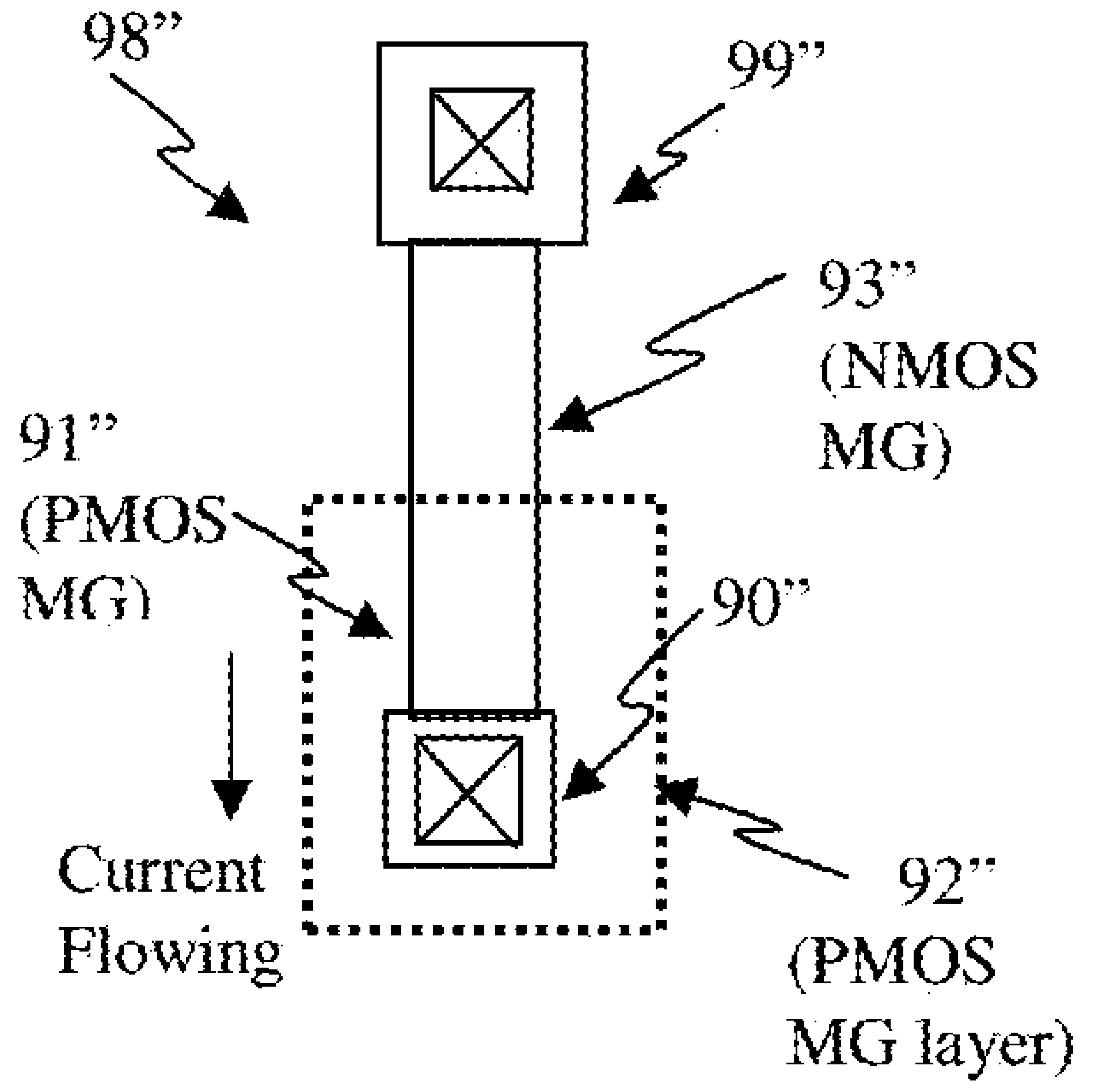

FIG. 7(a5)

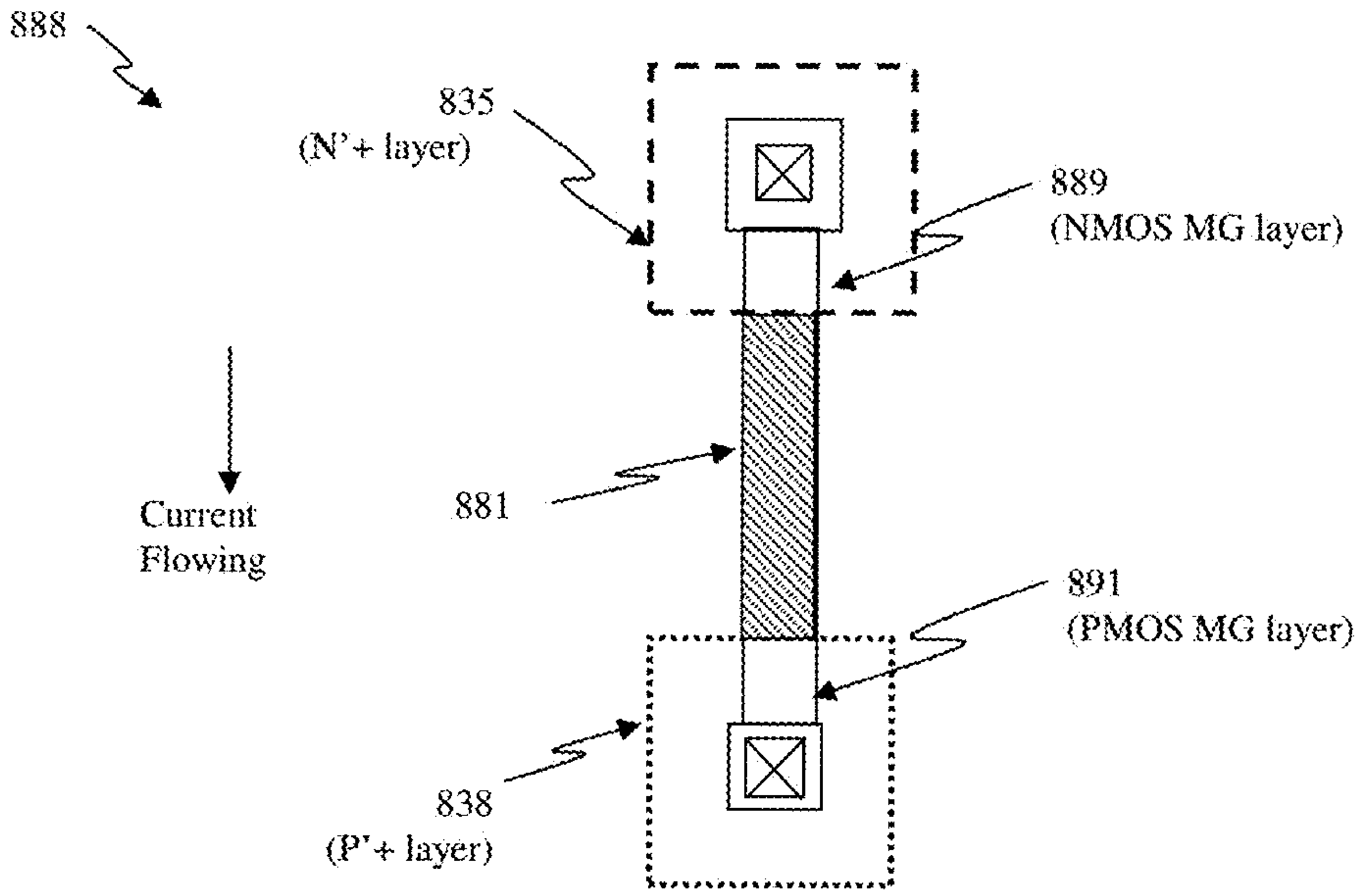

FIG. 7(a6)

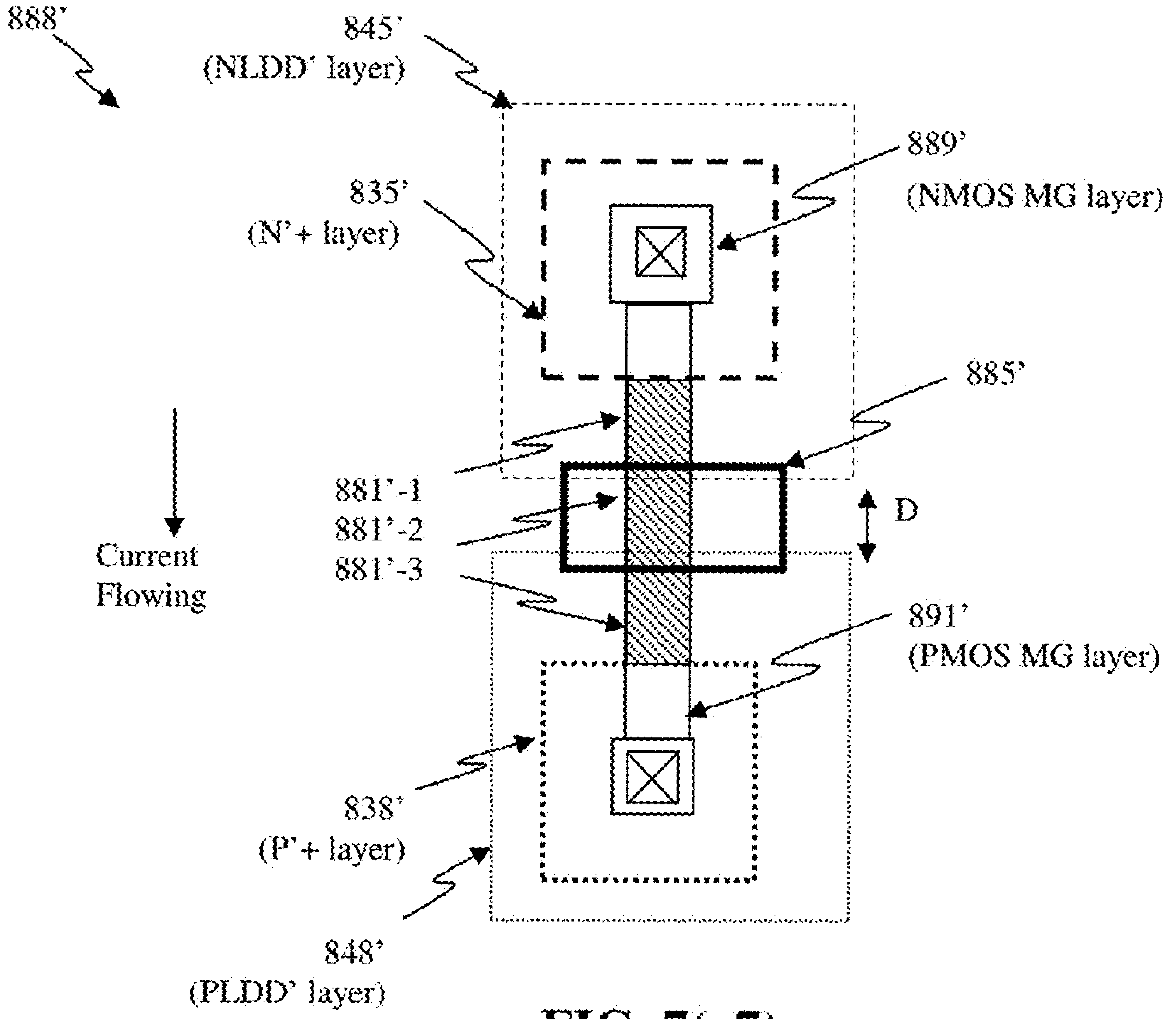

FIG. 7(a7)

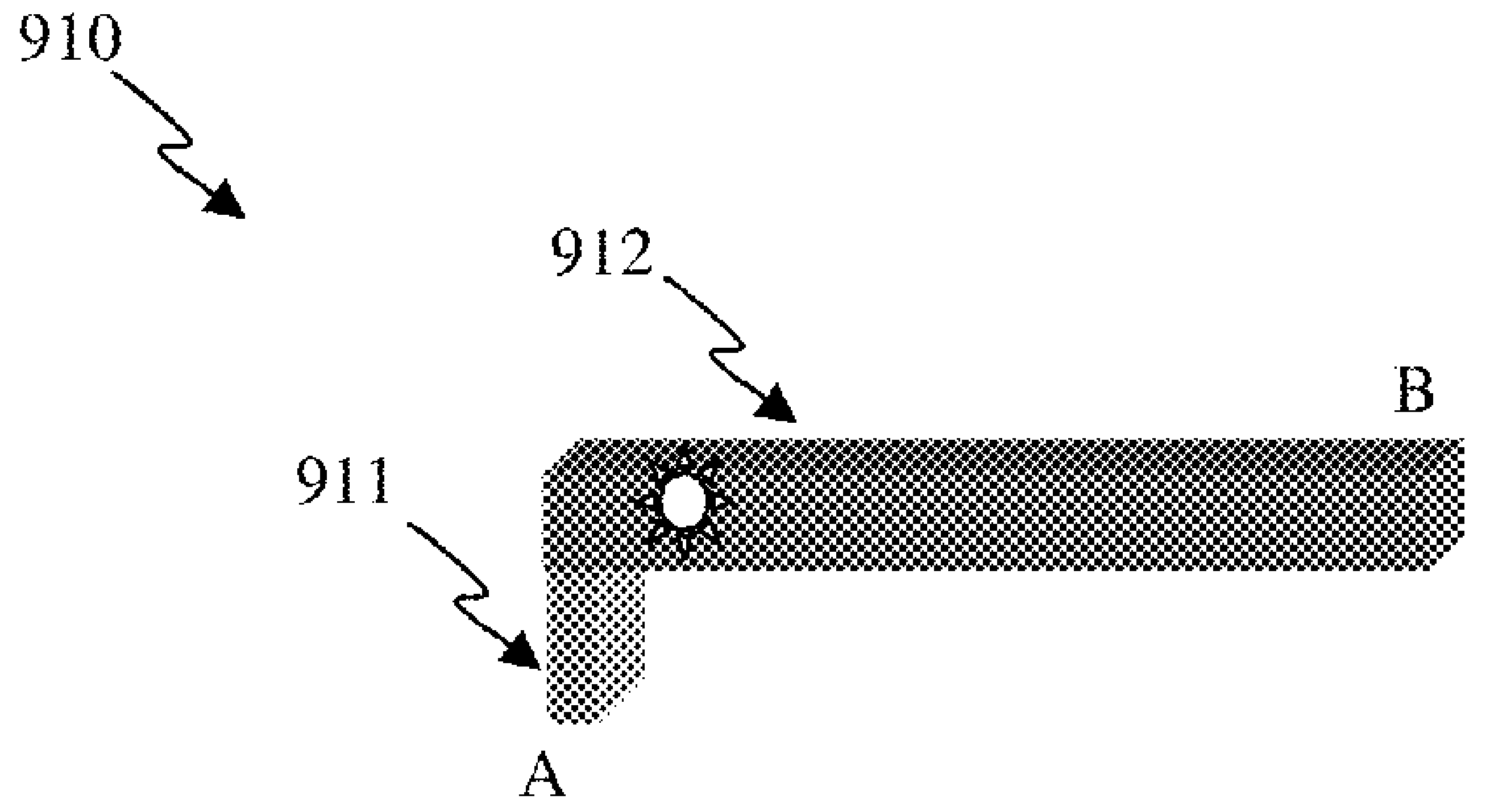

FIG. 7(a8)

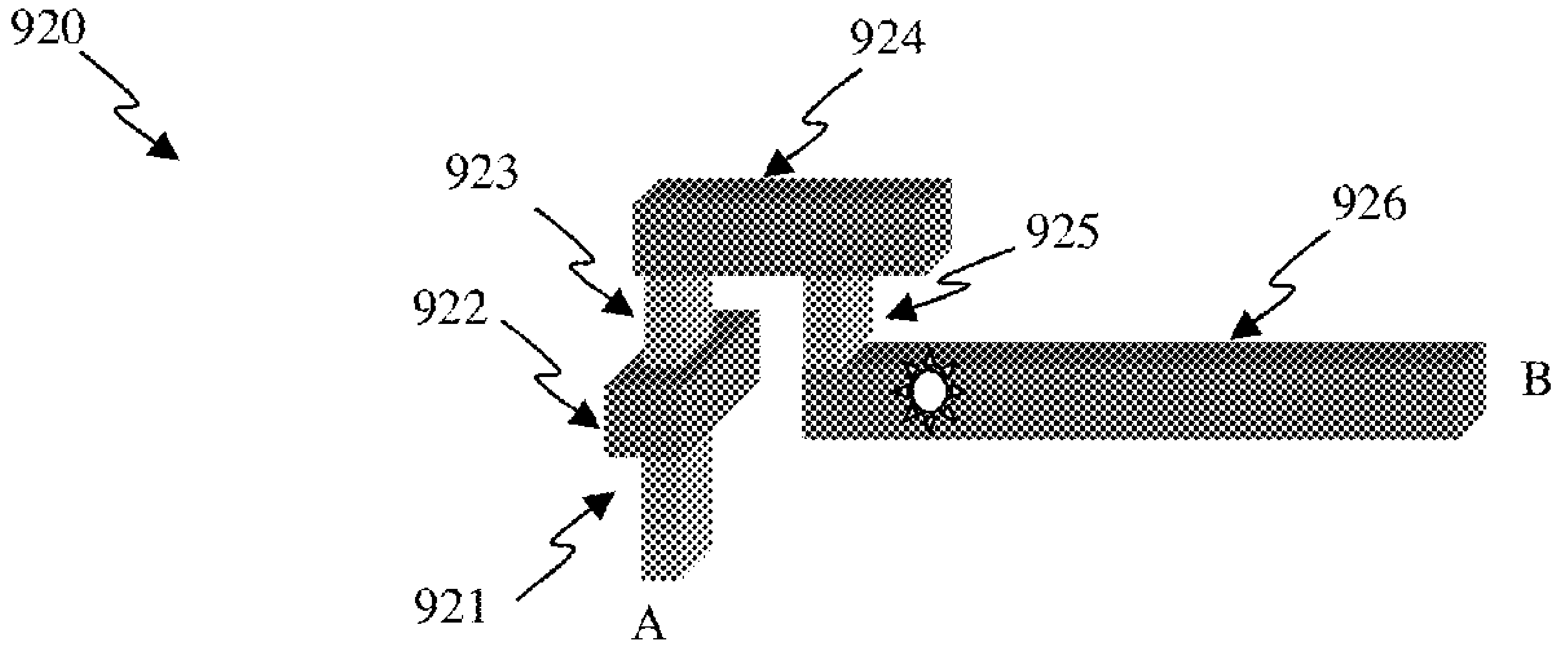

FIG. 7(a9)

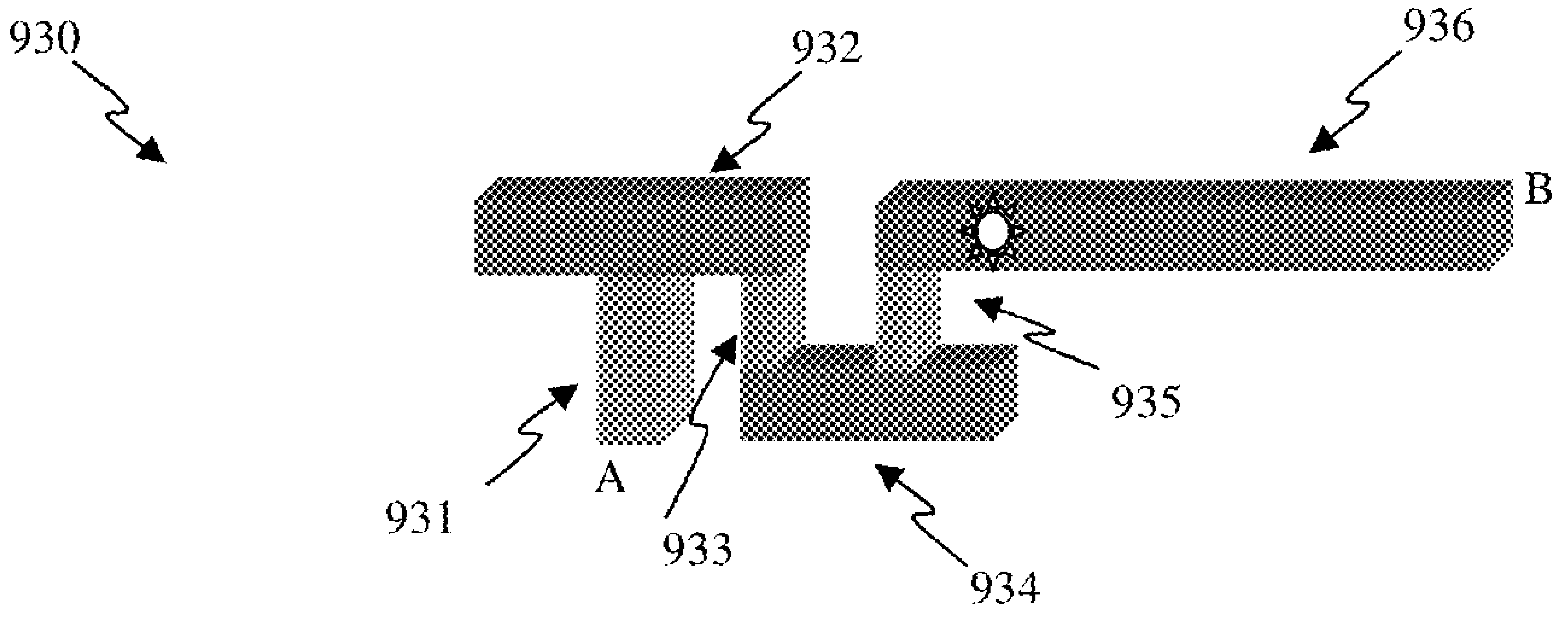

FIG. 7(a10)

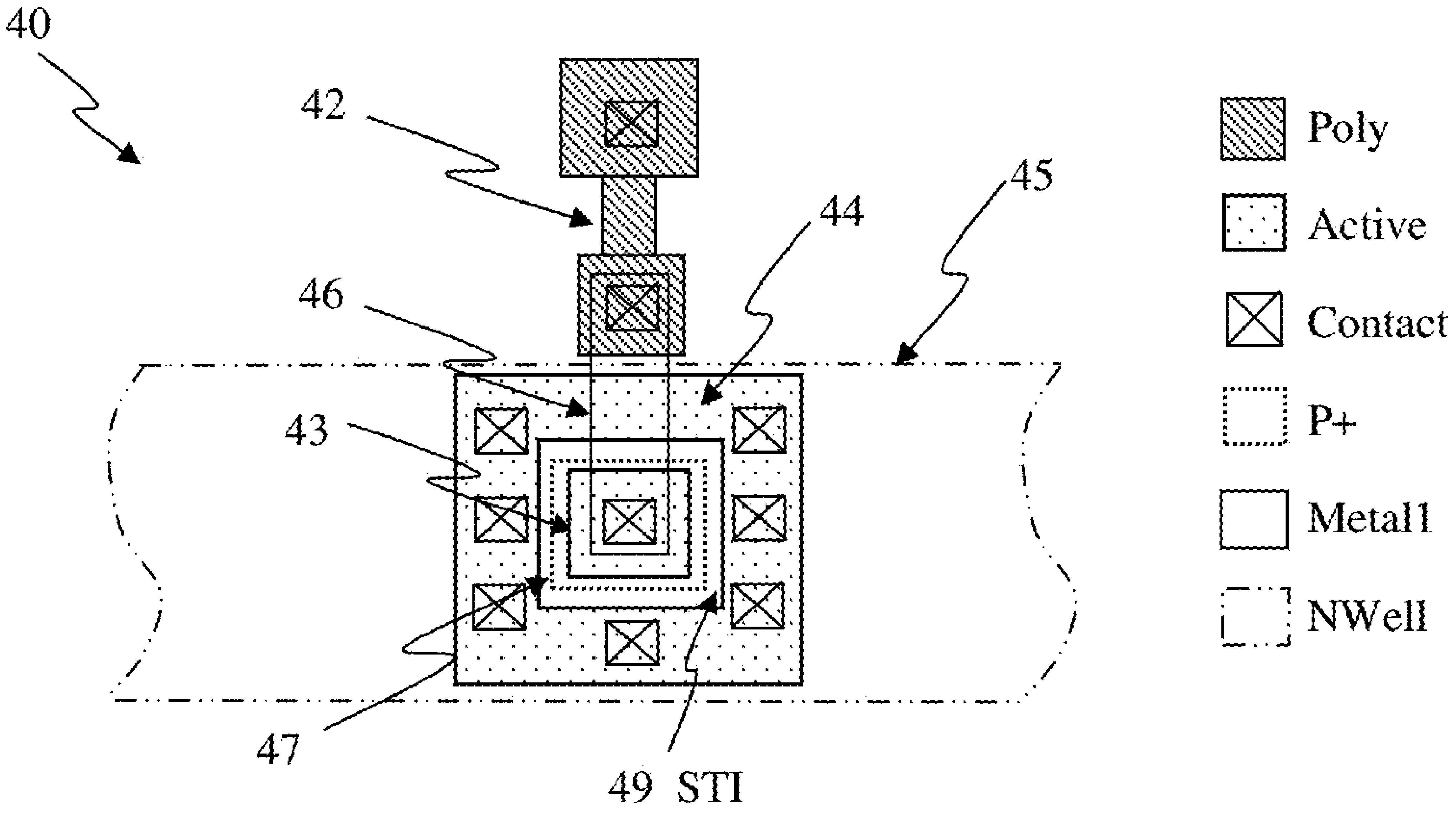

FIG. 7(b)

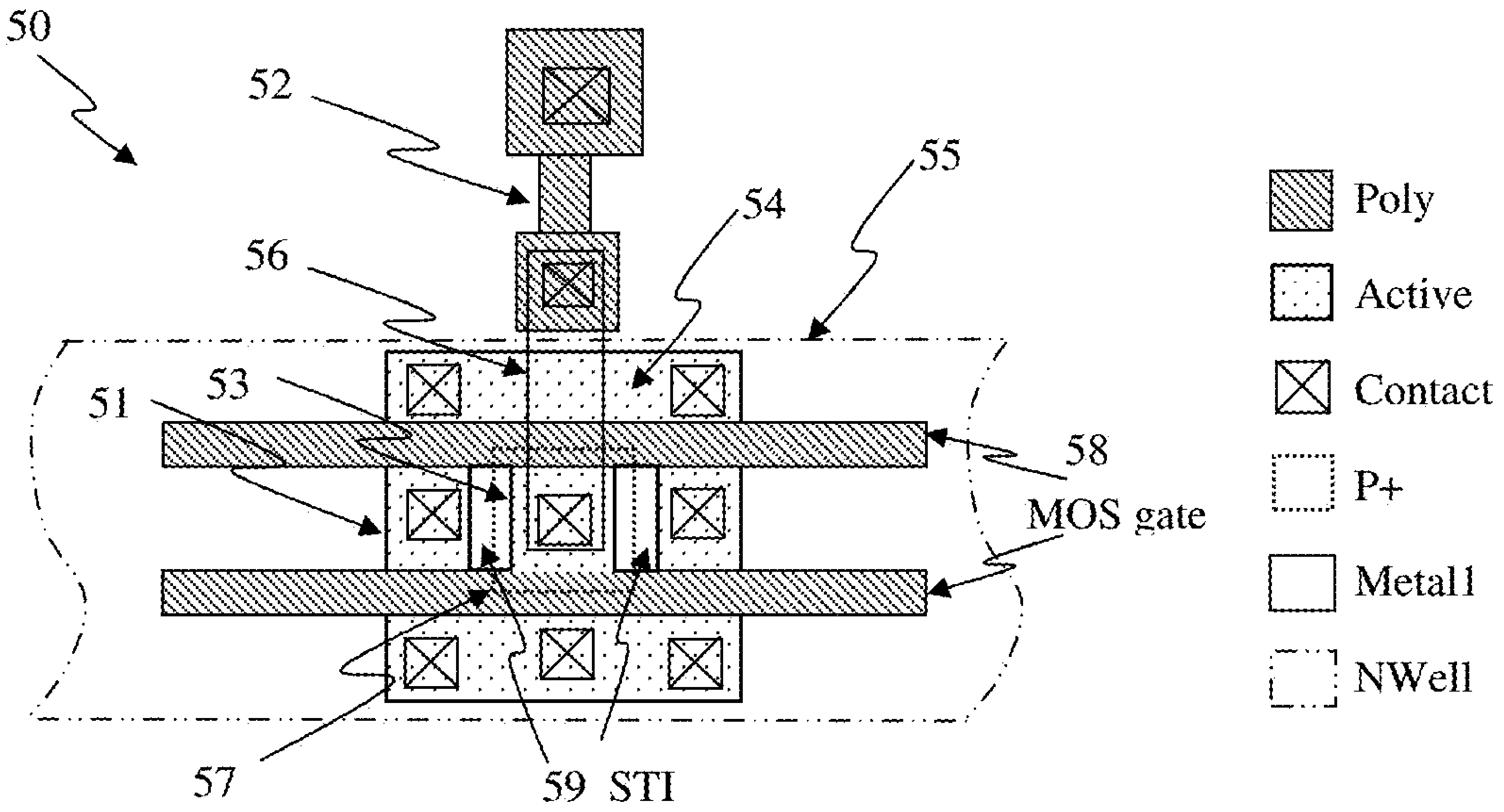
50
52
55
54
56
53
51
58
MOS gate
57
59 STI
Poly
Active
Contact
P+
Metal1
NWell

FIG. 7(c)

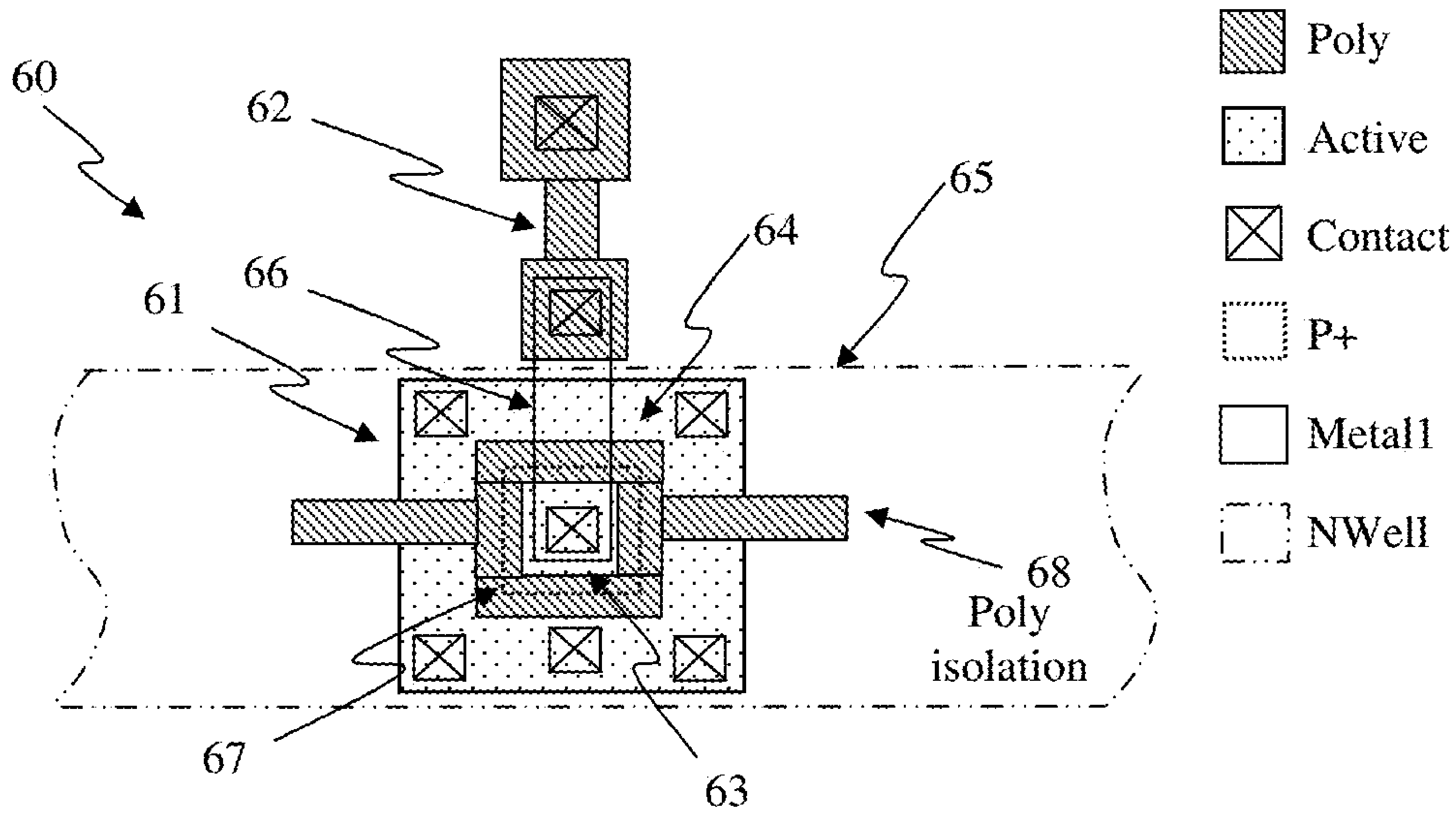
60
62
65
64
66
61
68
Poly isolation
67
63
Poly
Active
Contact
P+
Metal1
NWell

FIG. 7(d)

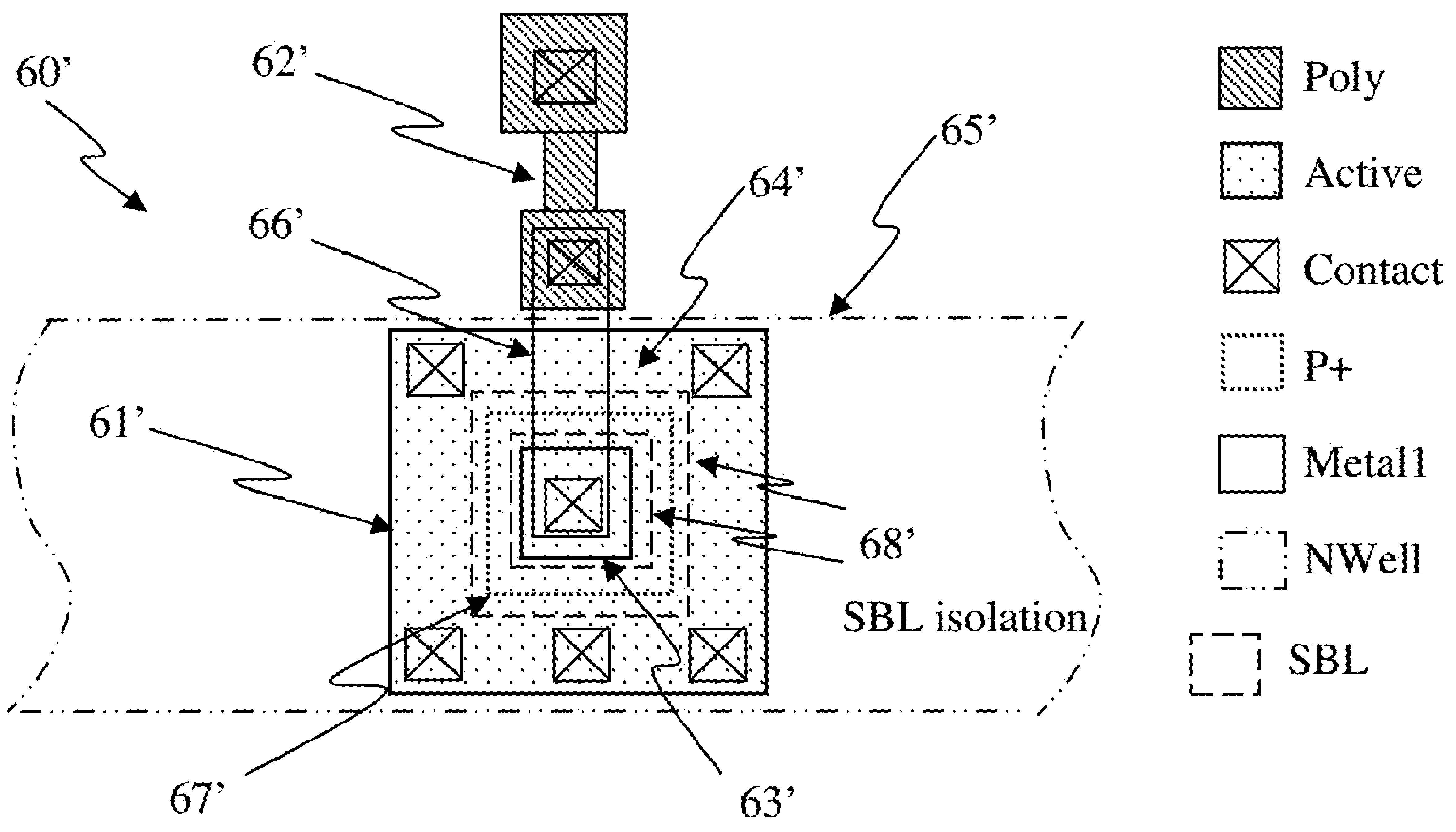
60'
62'
66'
64'
65'
61'
68'
SBL isolation
67'
63'
Poly
Active
Contact
P+
Metal1
NWell
SBL

FIG. 7(e)

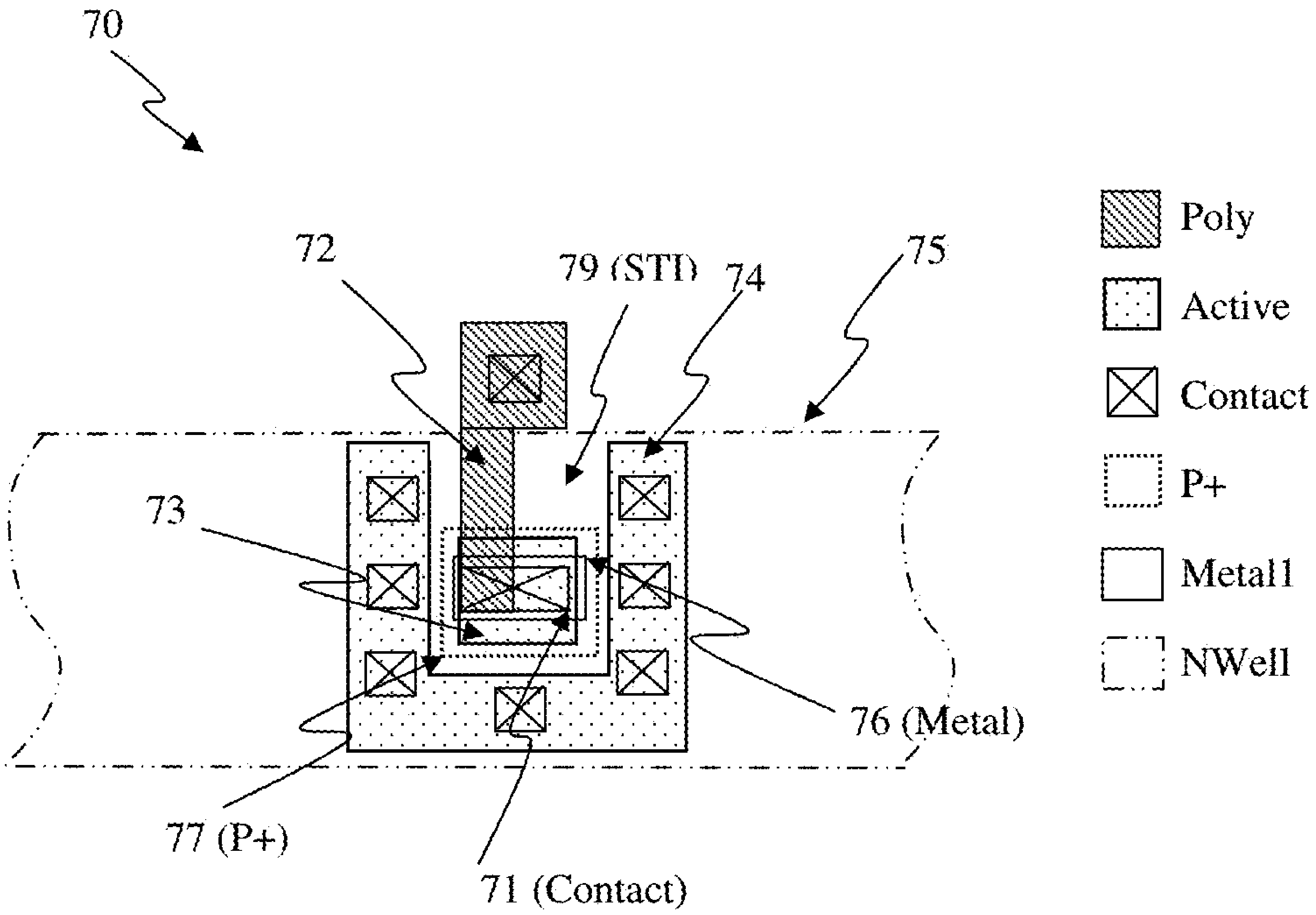
70
72
79 (STI)
74
75
73
76 (Metal)
77 (P+)
71 (Contact)
Poly
Active
Contact
P+
Metal1
NWell

FIG. 7(f)

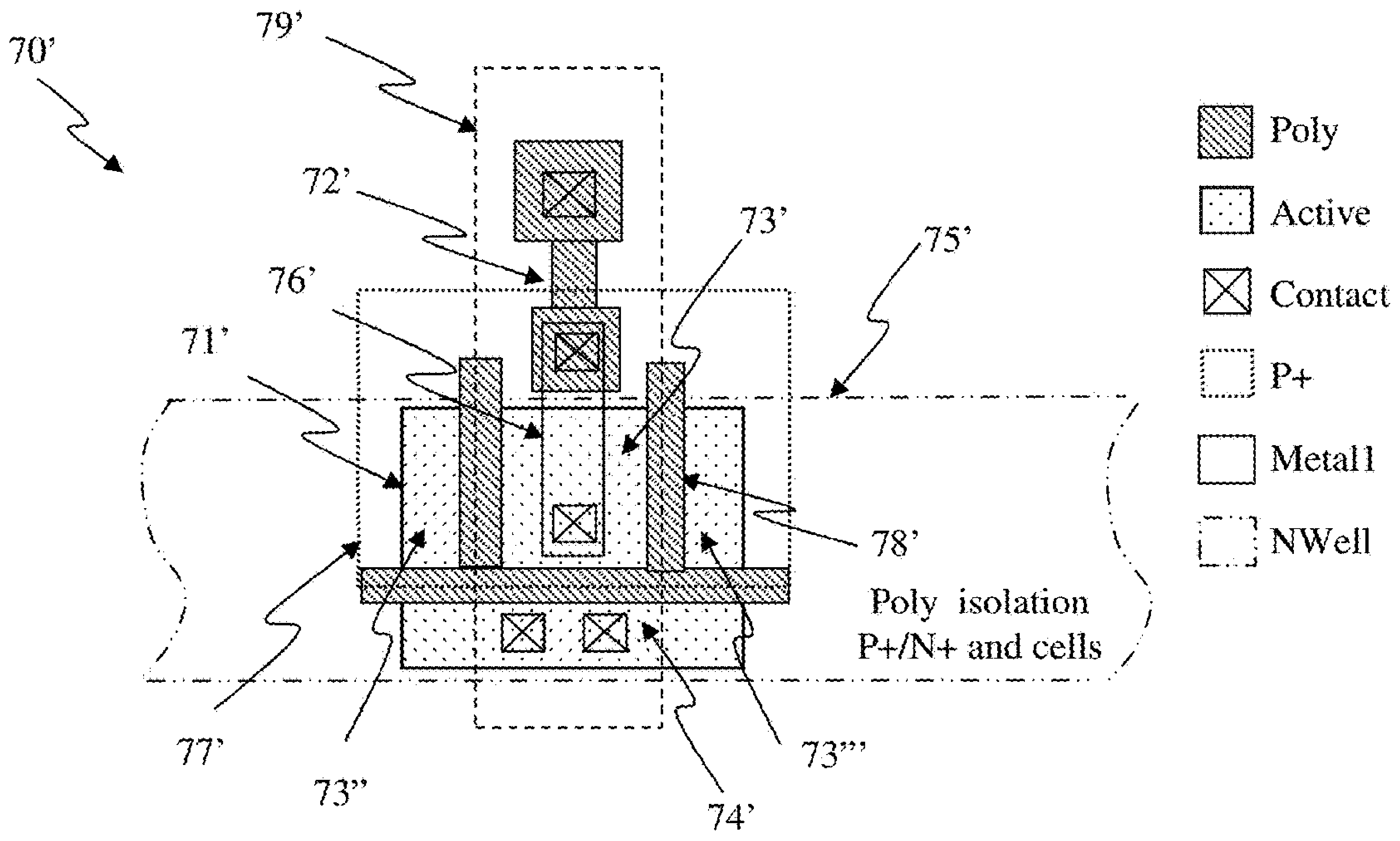
70'
79'
72'
73'
75'
76'
71'
78'
Poly isolation
P+/N+ and cells
77'
73"
74'
73'''
Poly
Active
Contact
P+
Metal1
NWell

FIG. 7(g)

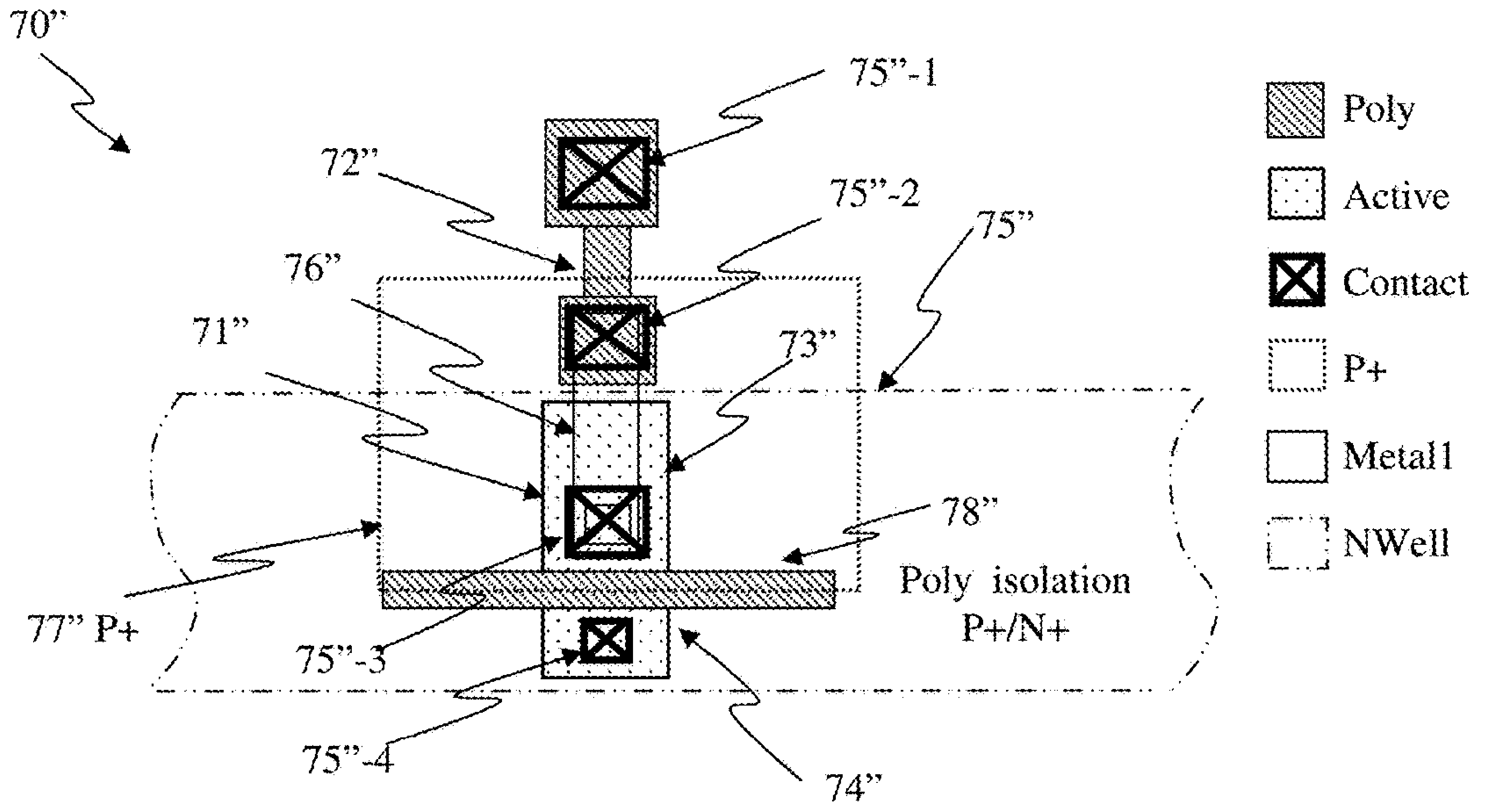
70"
75"-1
72"
75"-2
75"
76"
71"
73"
78"
Poly isolation
P+/N+
77" P+
75"-3
75"-4
74"
Poly
Active
Contact
P+
Metal1
NWell

FIG. 7(h)

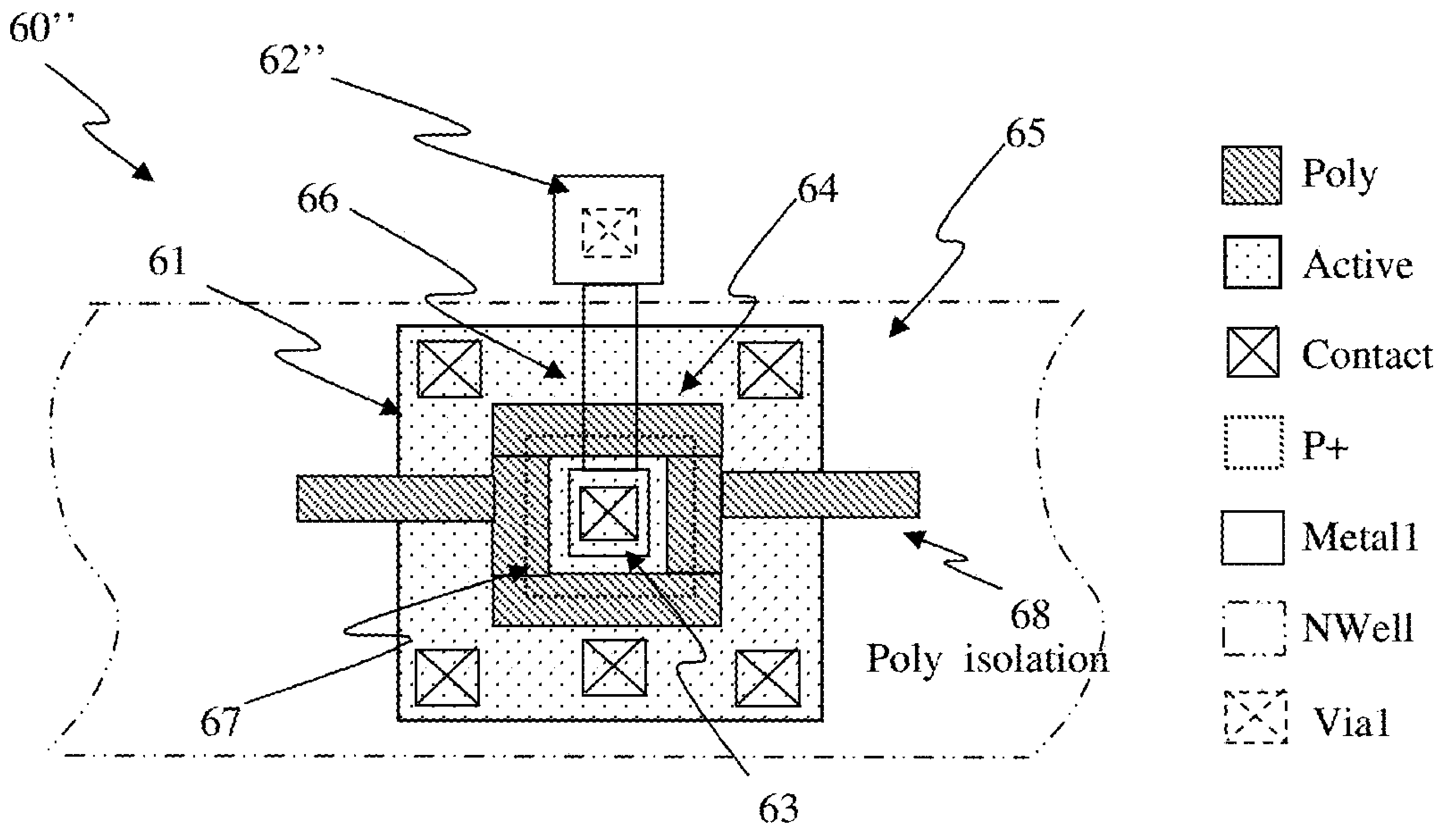
60''
62''
65
66
64
61
68
Poly isolation
67
63
Poly
Active
Contact
P+
Metal1
NWell
Via1

FIG. 8(a)

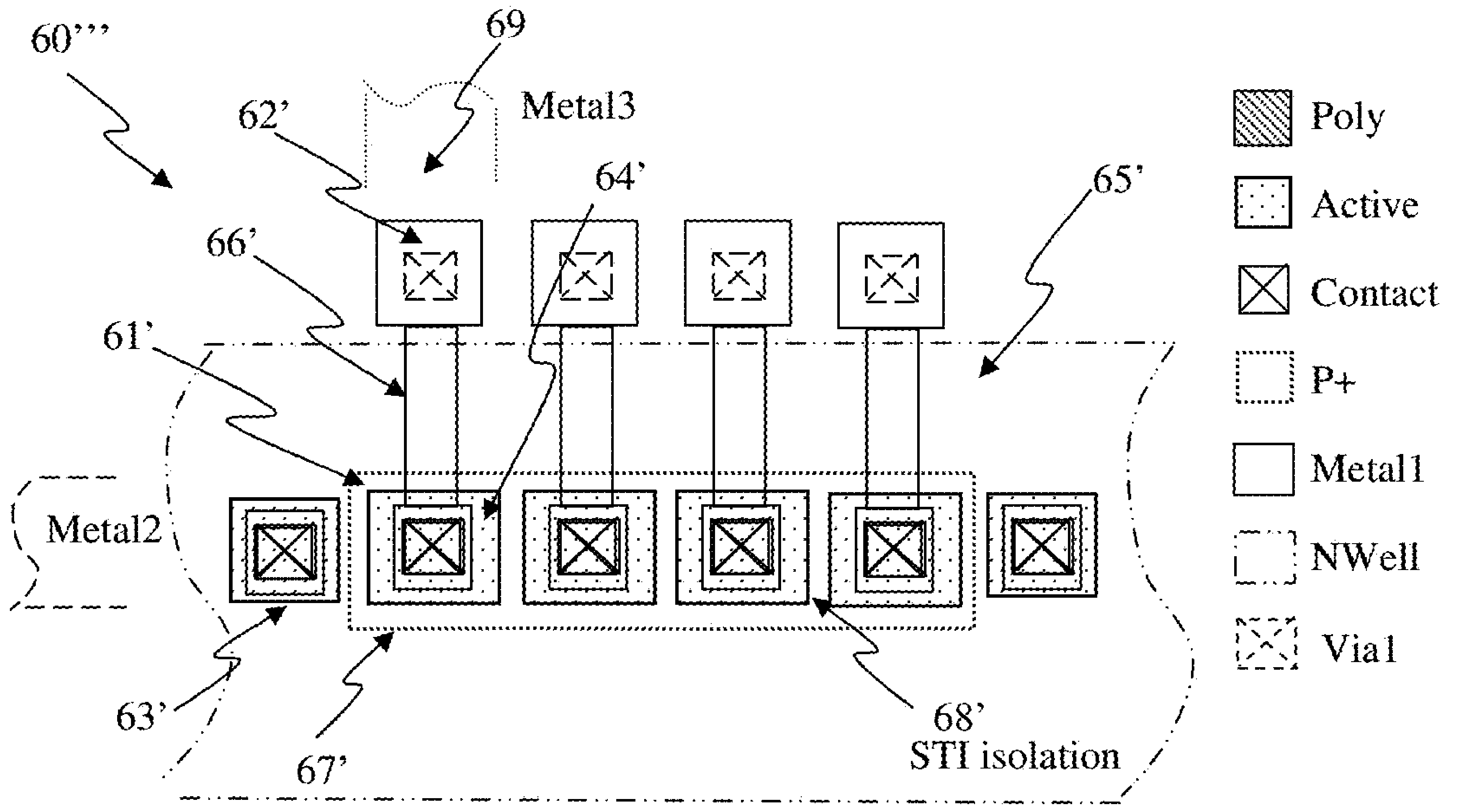
60'''
69
Metal3
62'
64'
65'
66'
61'
Metal2
63'
67'
68'
STI isolation
Poly
Active
Contact
P+
Metal1
NWell
Via1

FIG. 8(b)

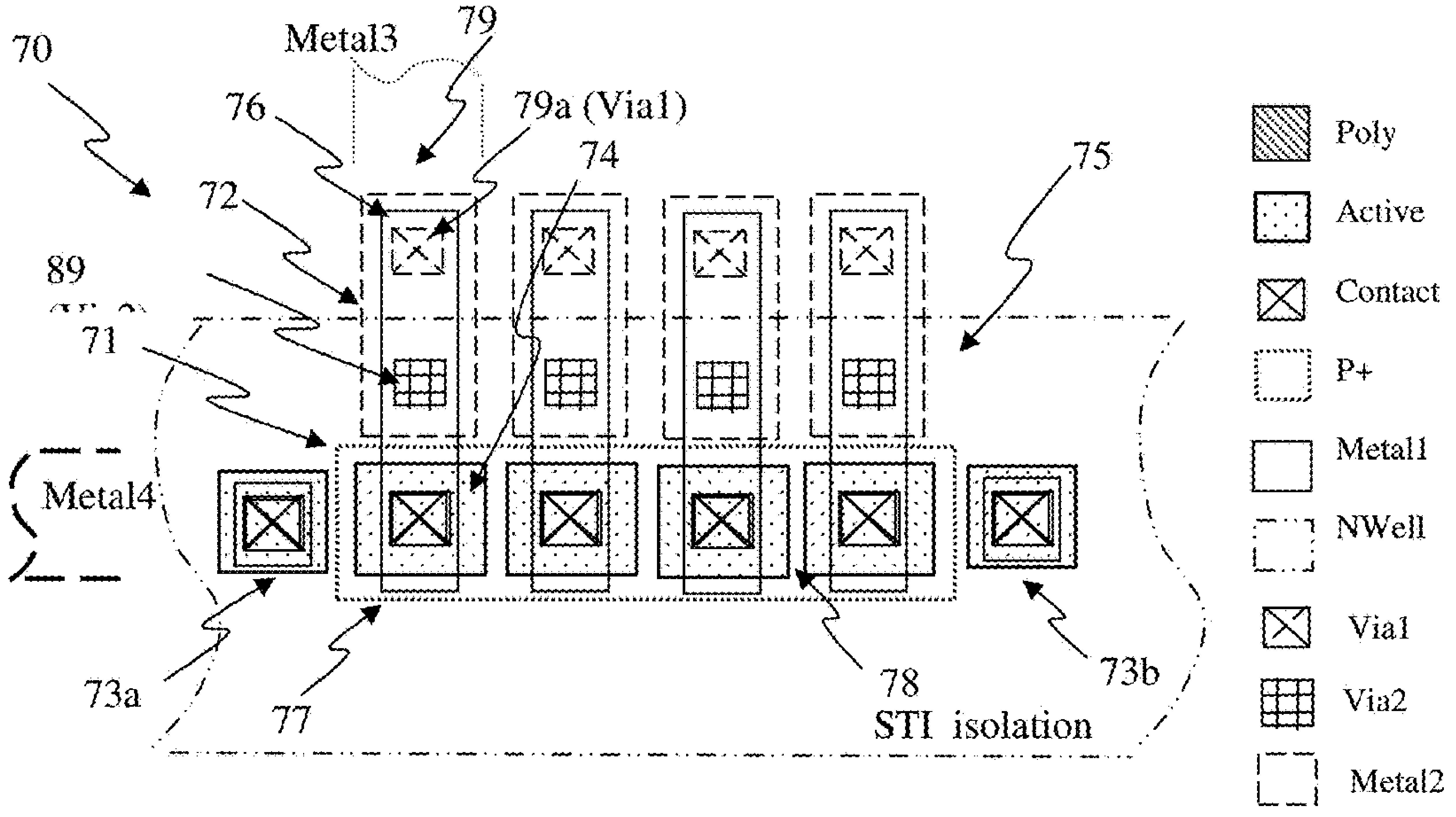
70
Metal3
79
76
79a (Via1)
74
75
72
89
71
Metal4
73a
77
78
STI isolation
73b
Poly
Active
Contact
P+
Metal1
NWell
Via1
Via2
Metal2

FIG. 8(c)

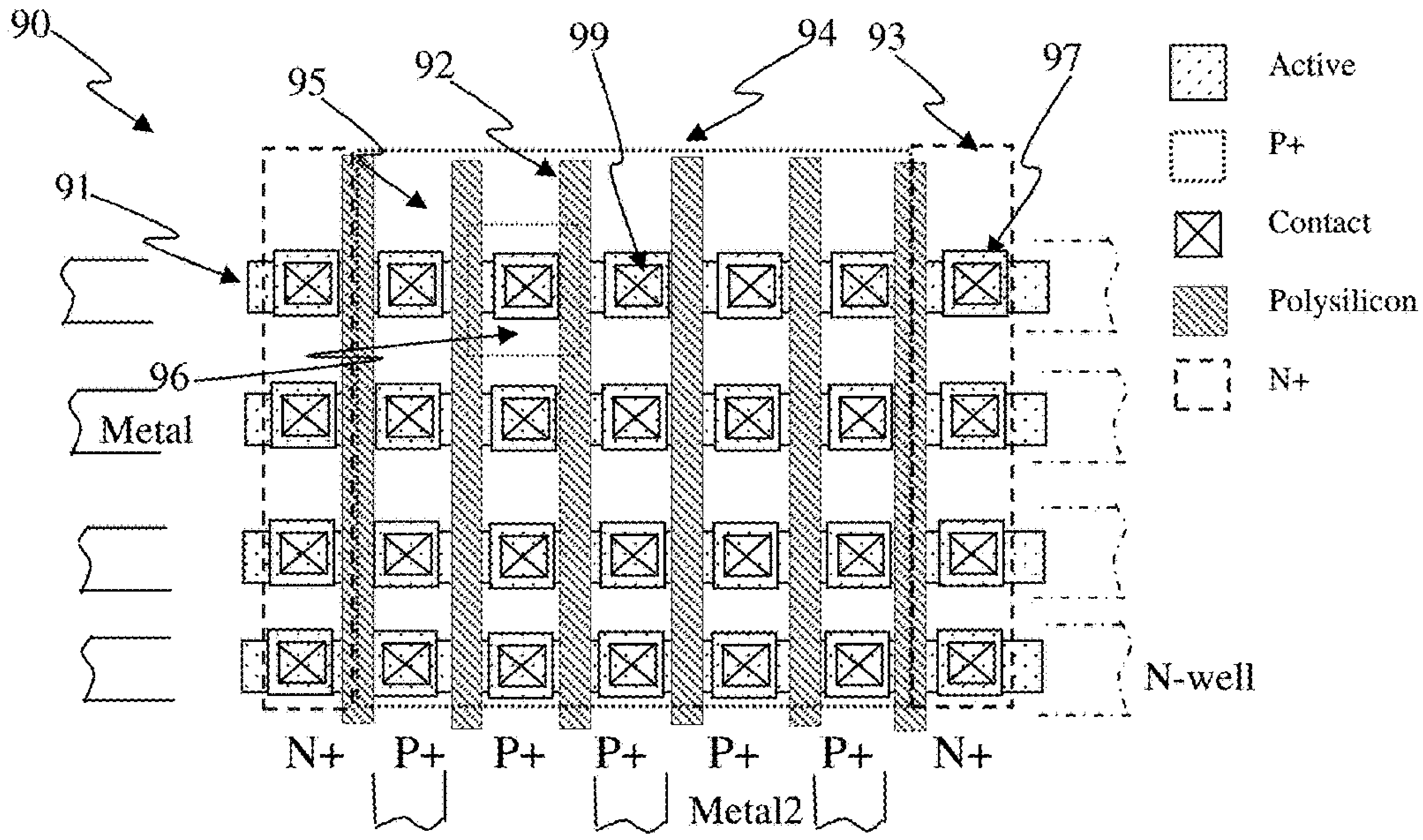
90
95
92
99
94
93
97
91
96
Metal
N-well
N+
P+
P+
P+
P+
P+
N+
Metal2
Active
P+
Contact
Polysilicon
N+

FIG. 8(d)

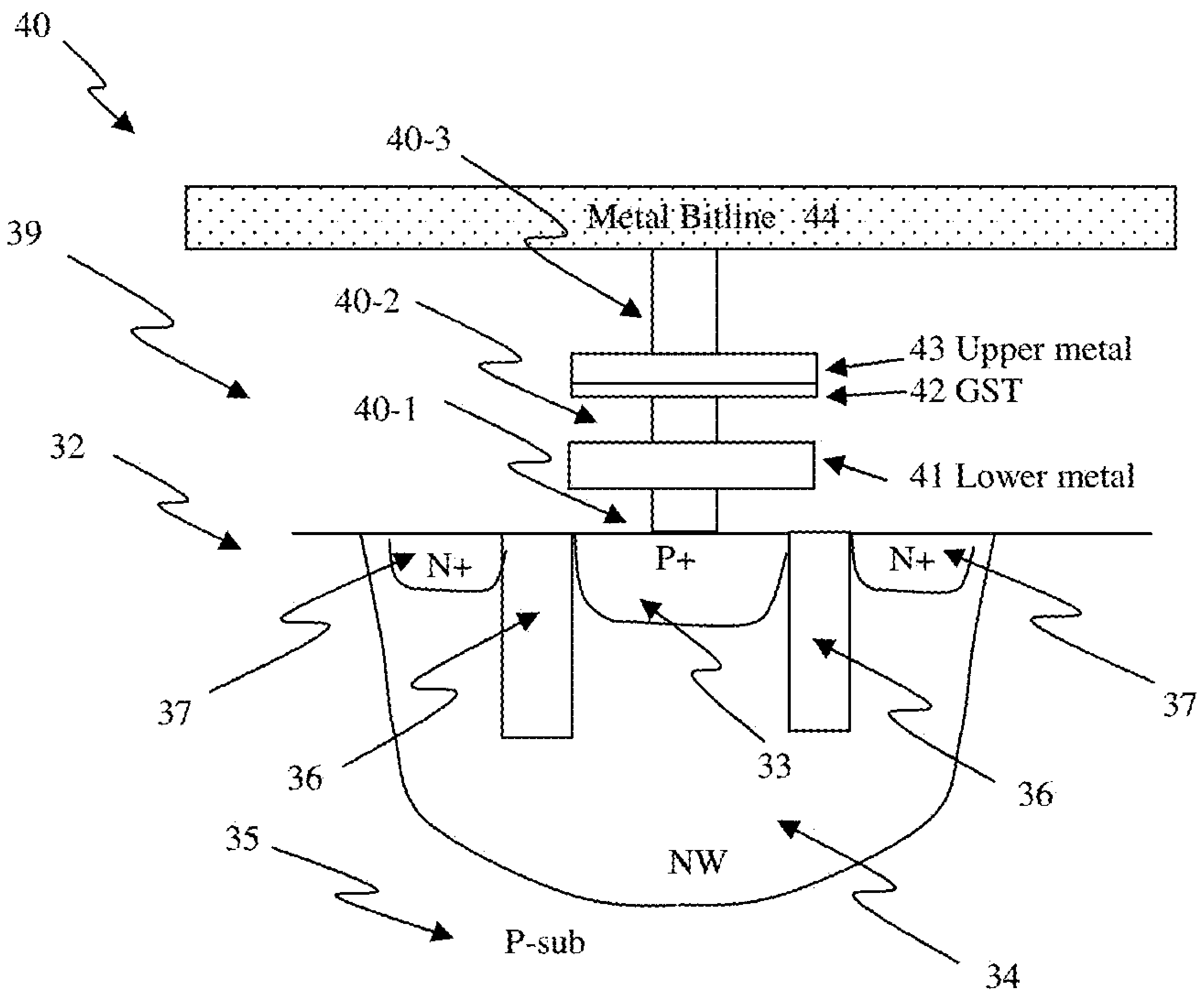
40
40-3
Metal Bitline 44
39
40-2
43 Upper metal
42 GST
40-1
41 Lower metal
32
N+
P+
N+
37
37
36
33
36
35
NW
P-sub
34

FIG. 9(a)

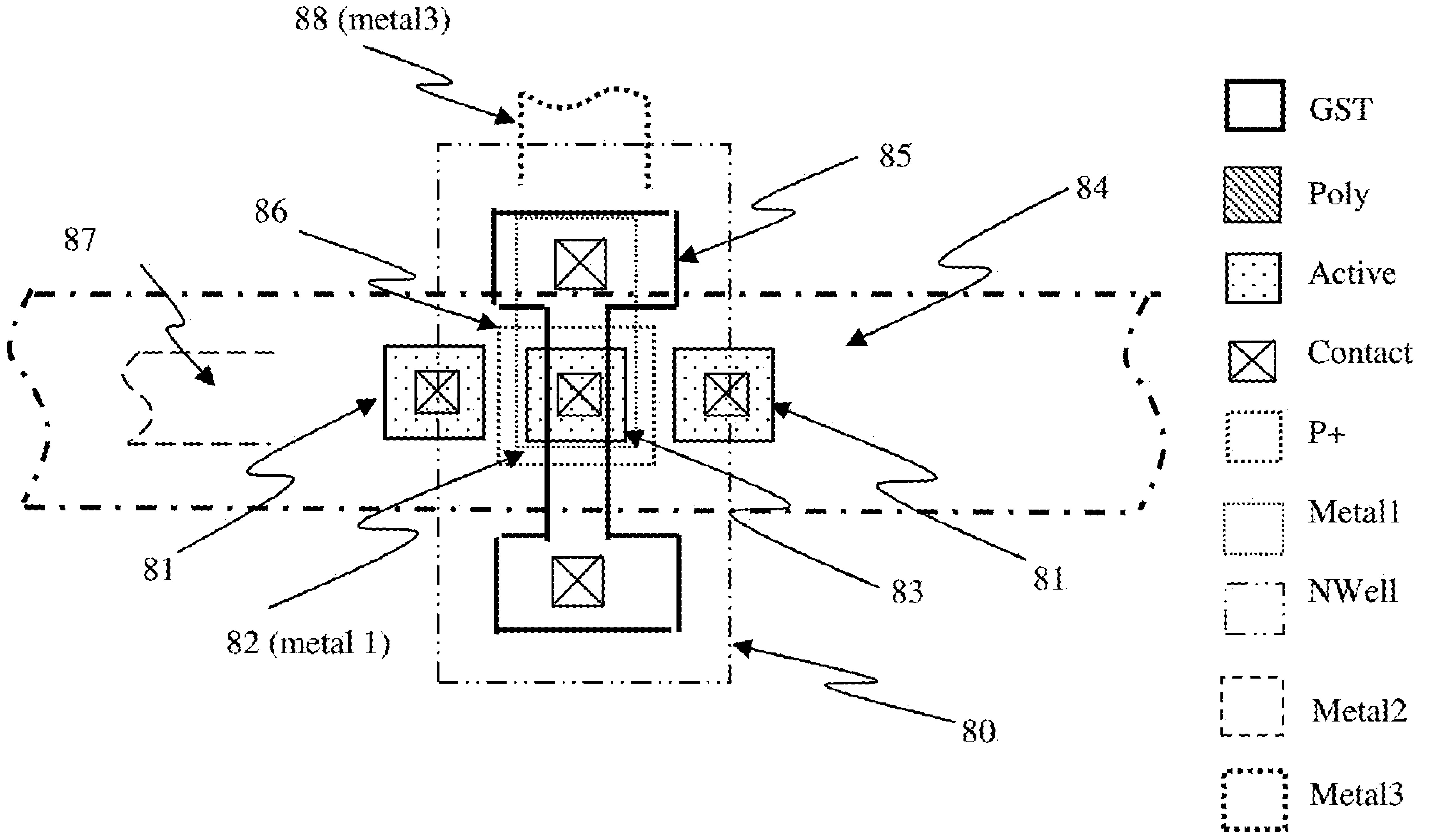
88 (metal3)
85
84
86
87
81
81
82 (metal 1)
83
80
GST
Poly
Active
Contact
P+
Metal1
NWell
Metal2
Metal3

FIG. 9(b)

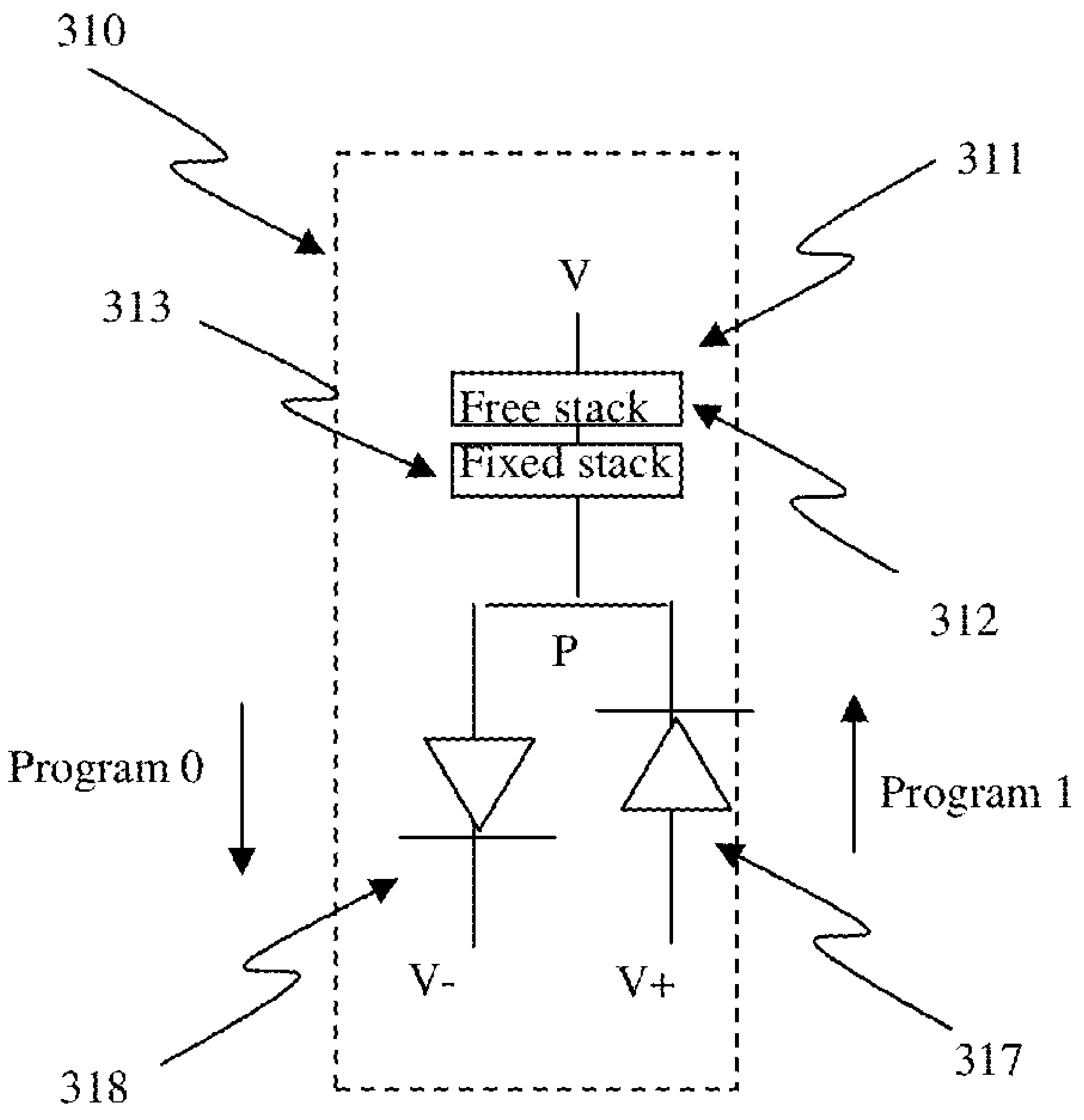
310
311
V
313
Free stack
Fixed stack
312
P
Program 0
Program 1
V-
V+
318
317

FIG. 10

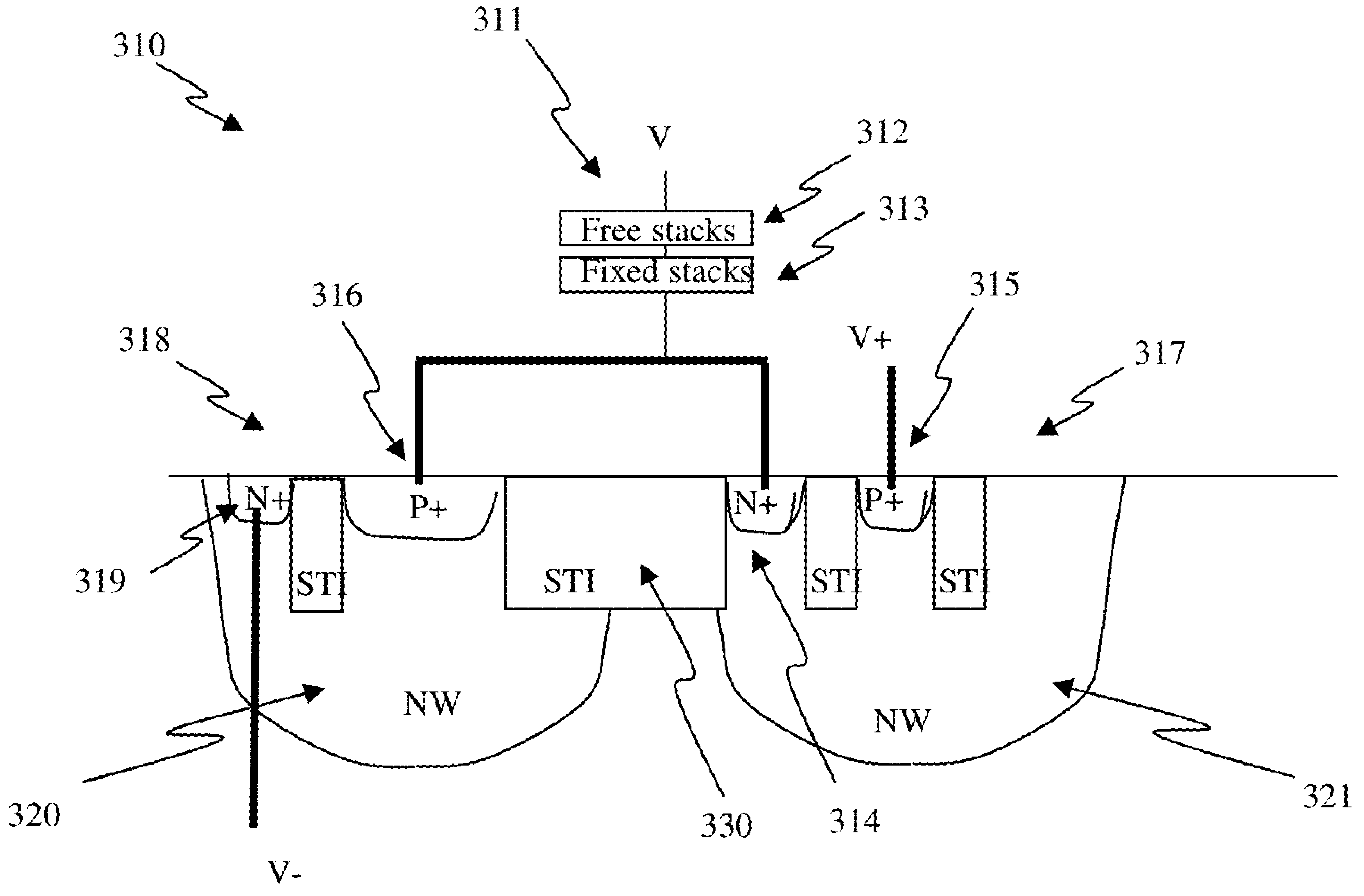

FIG. 11(a)

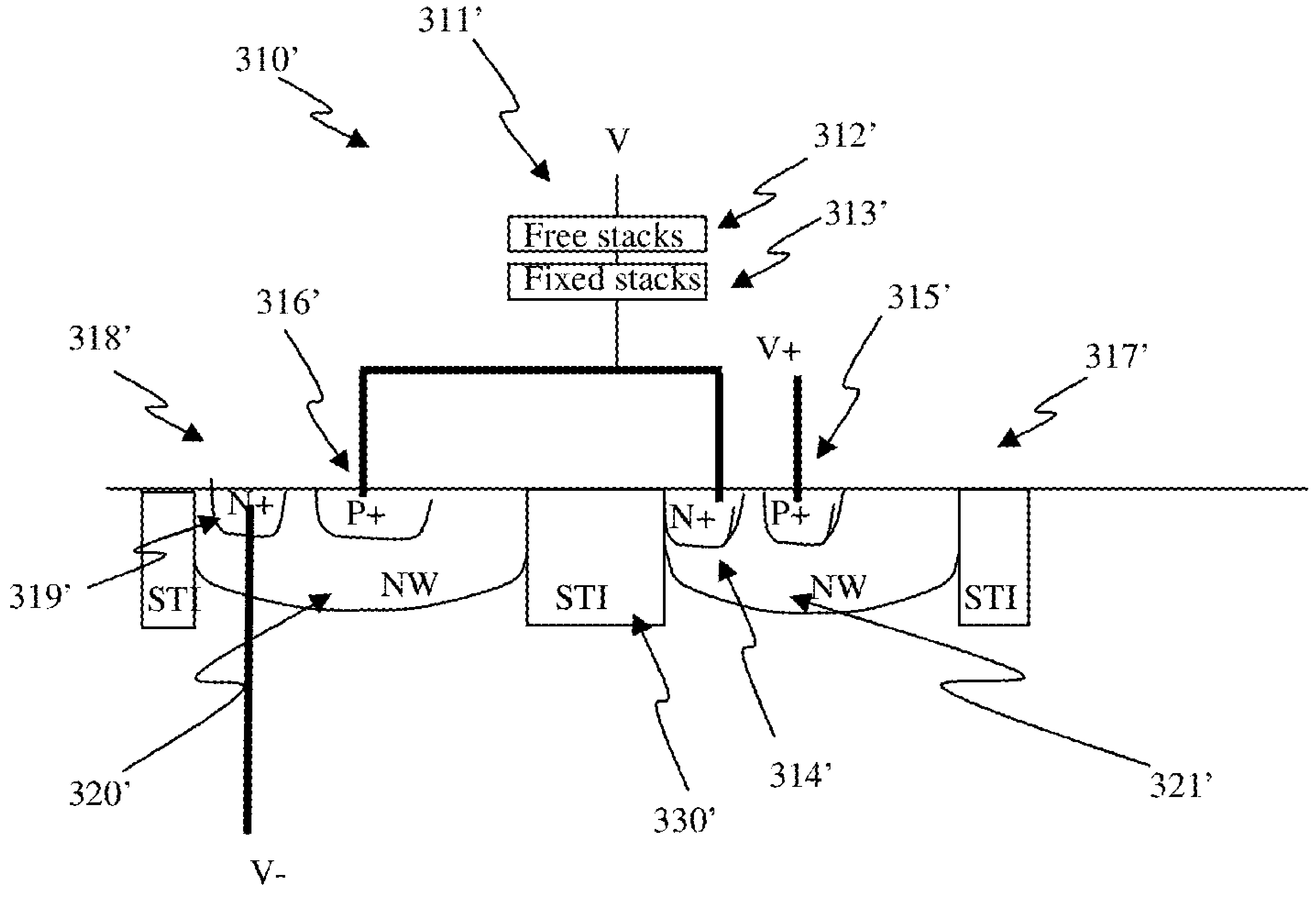

FIG. 11(b)

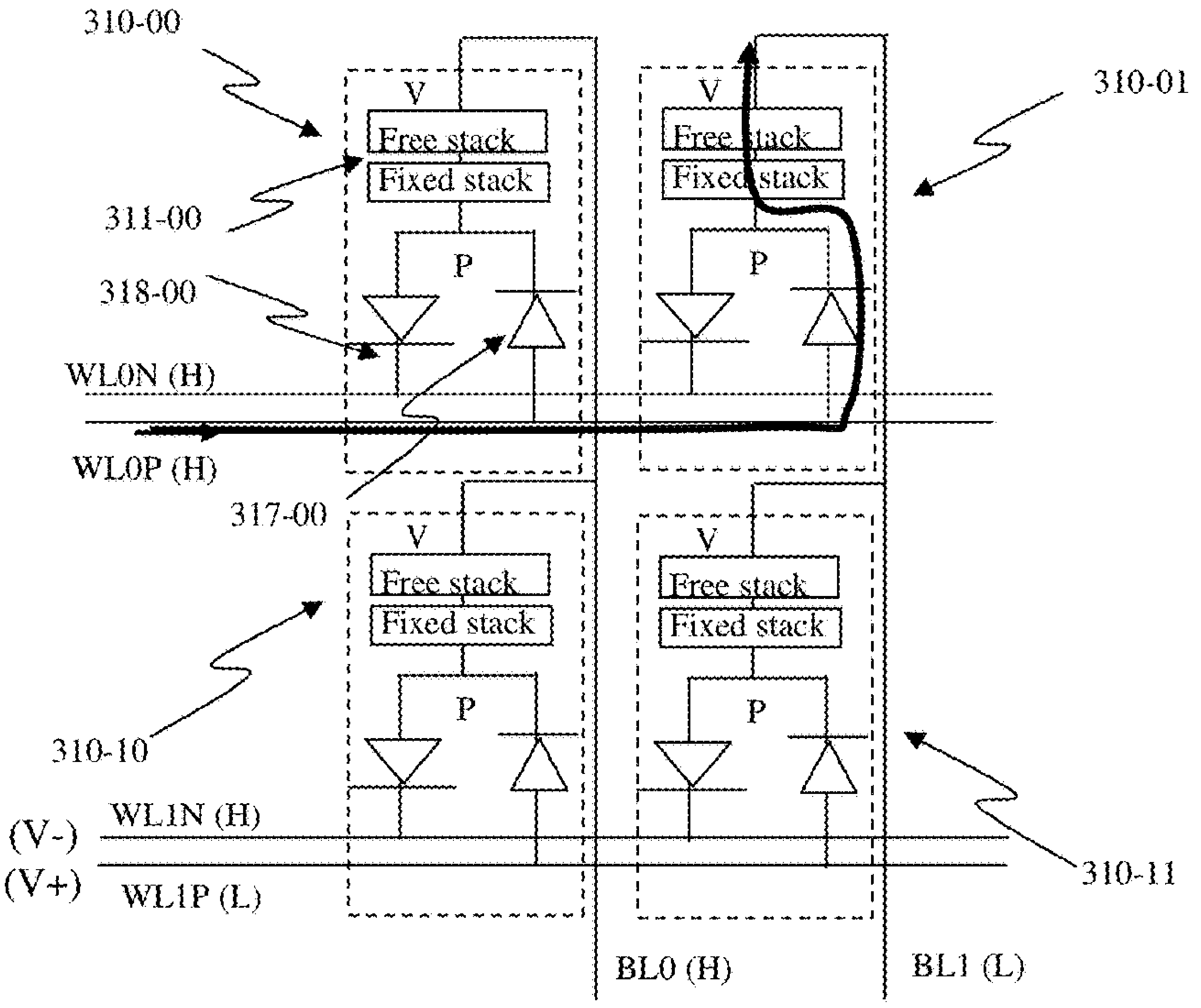

FIG. 12(a)

Condition1	BL0=H	BL1=**L**		Condition 2	BL0=Z	BL1=**L**
WL0N=H/Z	X	**1**		WL0N=H/L/Z	X	**1**
WL0P=**H**				WL0P=**H**		
WL1N=H/Z	X	X		WL1N=H/L/Z	X	X
WL1P=L/Z				WL1P=L/Z		

FIG. 12(b)

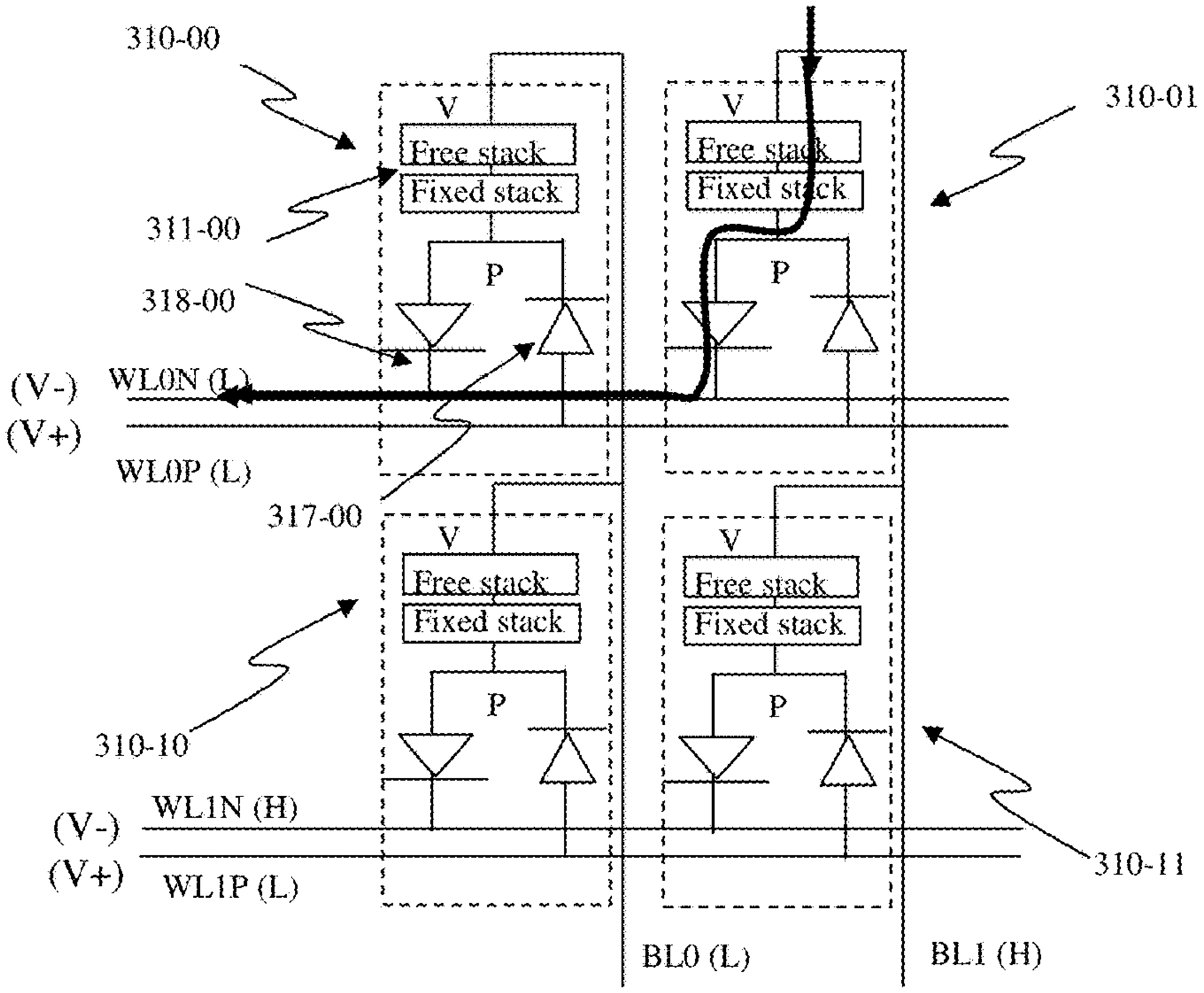

FIG. 13(a)

Condition1	BL0=L	BL1=**H**		Condition 2	BL0=Z	BL1=**H**
WL0N=**L**	X	**0**		WL0N=**L**	X	**0**
WL0P=L/Z				WL0P=H/L/Z		
WL1N=H/Z	X	X		WL1N=H/Z	X	X
WL1P=L/Z				WL1P=H/L/Z		

FIG. 13(b)

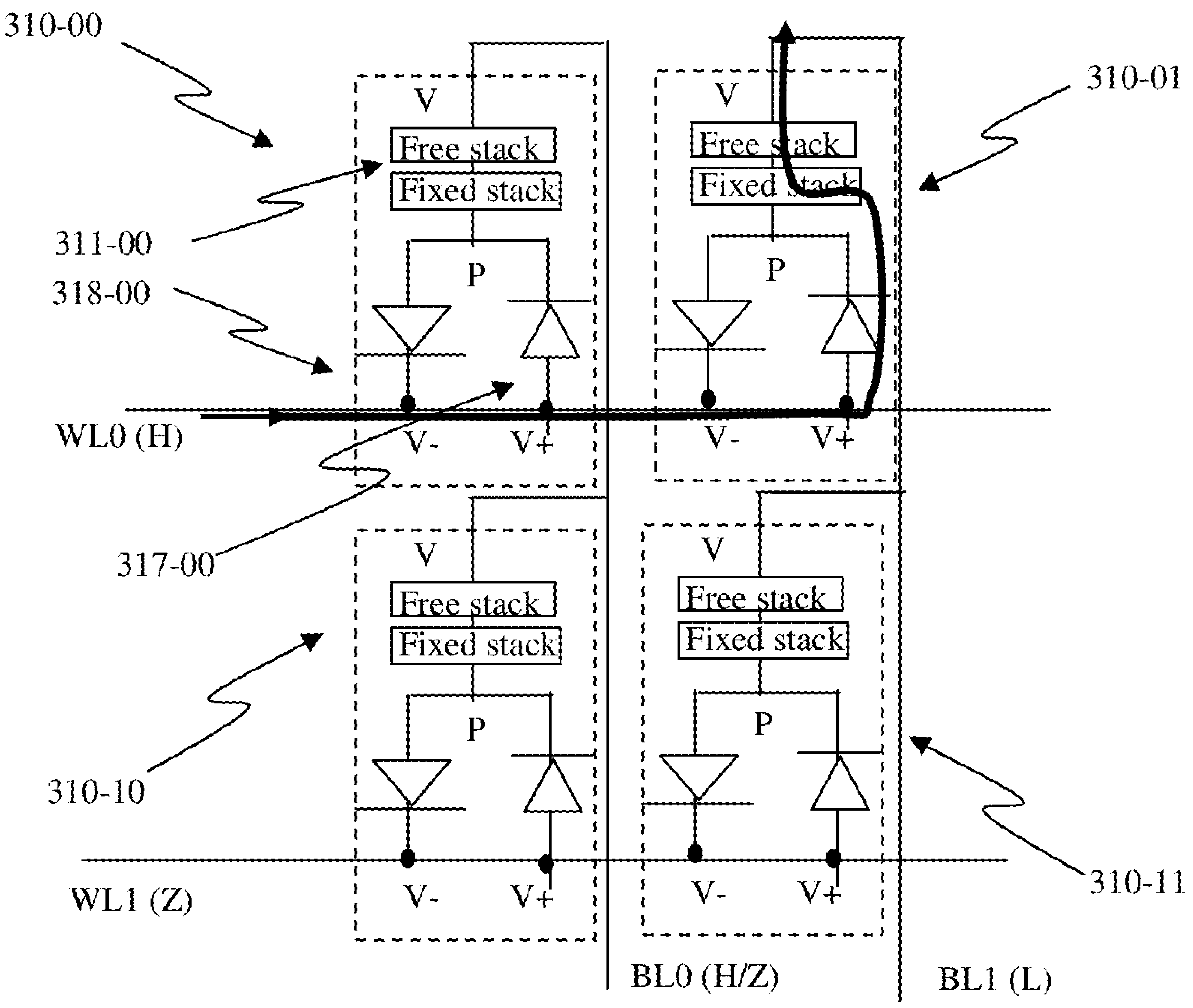

FIG. 14(a)

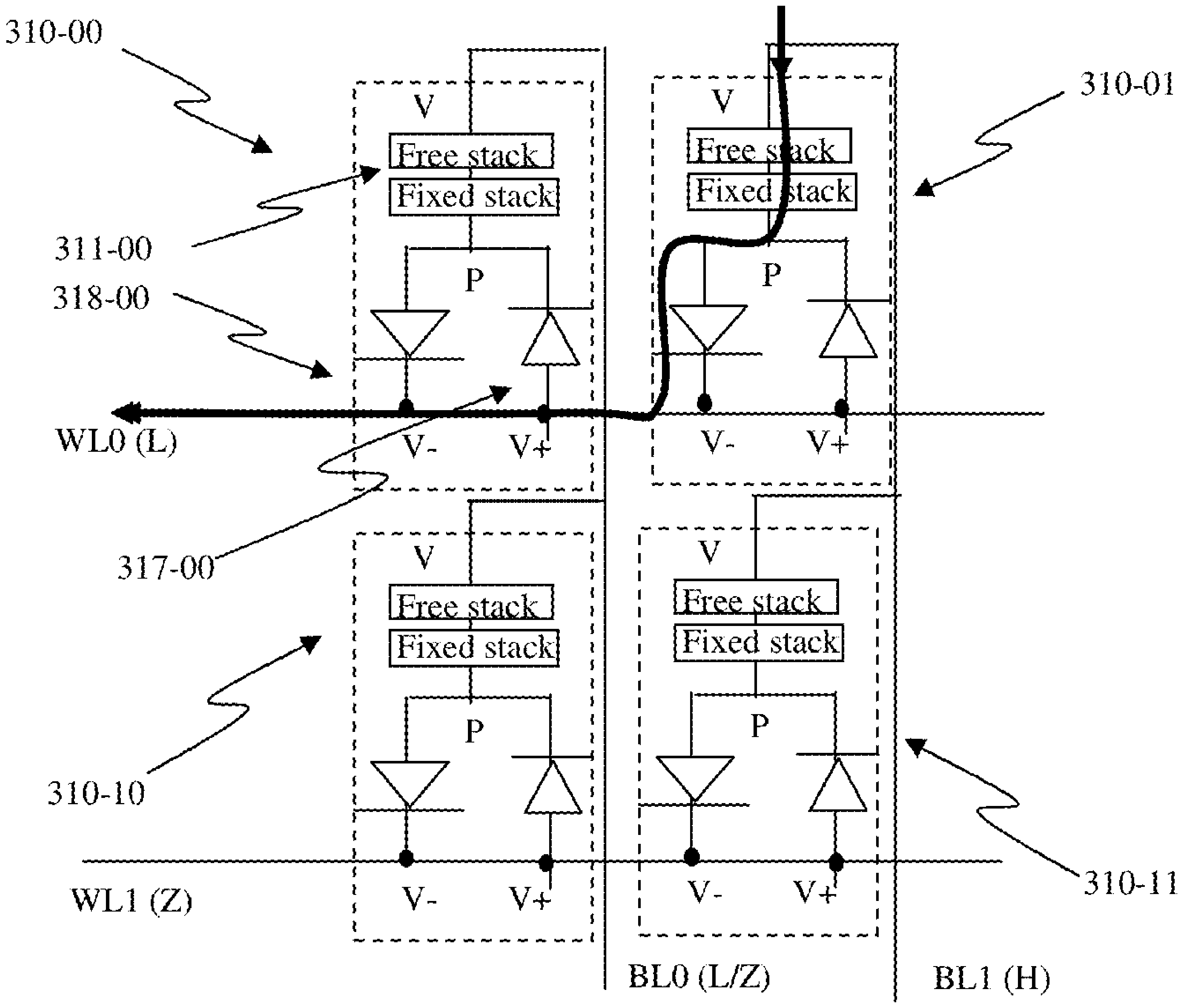

FIG. 14(b)

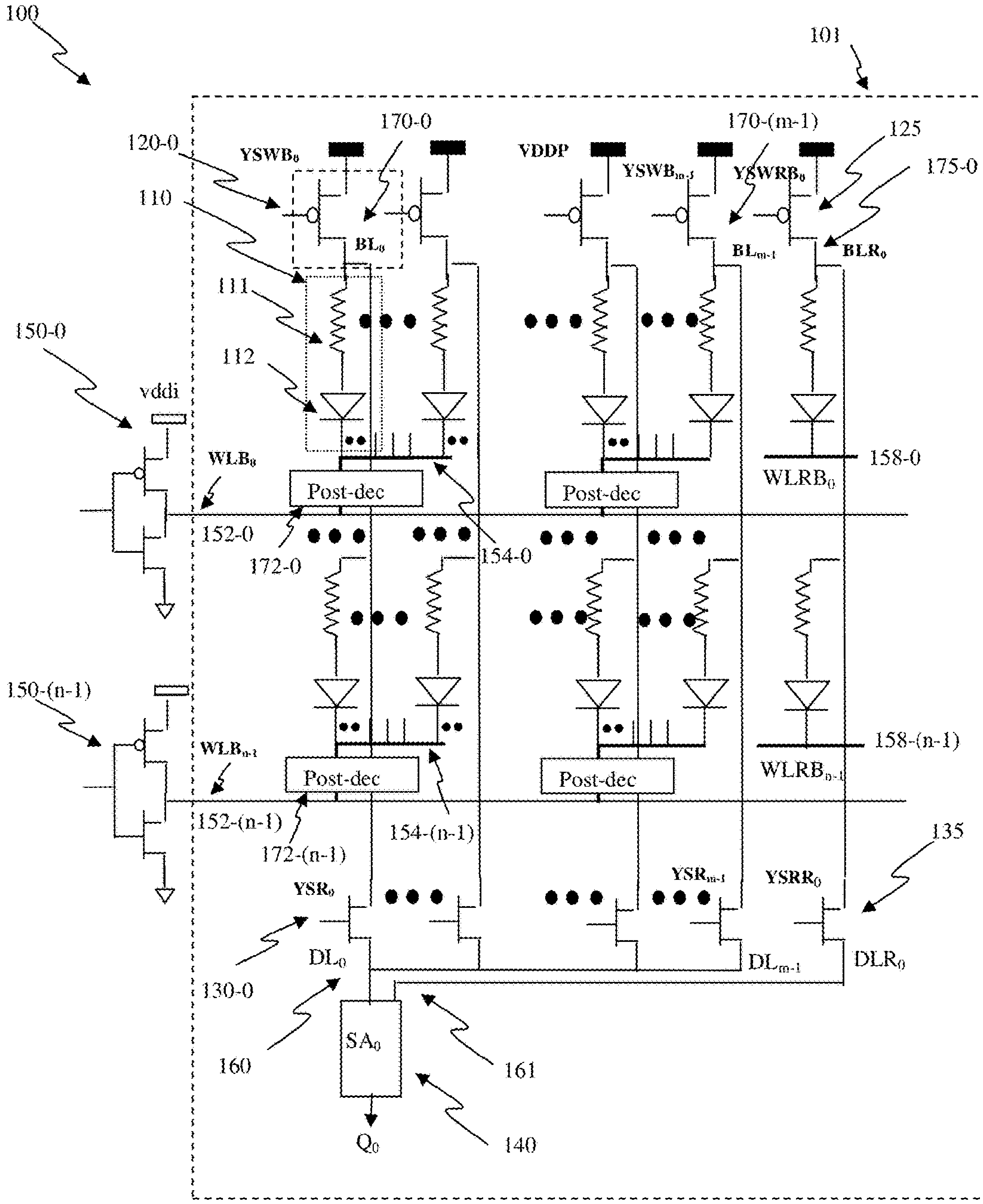
100
101
120-0
YSWB0
170-0
VDDP
YSWBm-1
170-(m-1)
YSWRB0
125
175-0
110
BL0
BLm-1
BLR0
111
112
150-0
vddi
WLB0
Post-dec
Post-dec
158-0
WLRB0
152-0
172-0
154-0
150-(n-1)
WLBn-1
Post-dec
Post-dec
158-(n-1)
WLRBn-1
152-(n-1)
172-(n-1)
154-(n-1)
135
YSR0
YSRm-1
YSRR0
130-0
DL0
DLm-1
DLR0
160
SA0
161
140
Q0

FIG. 15

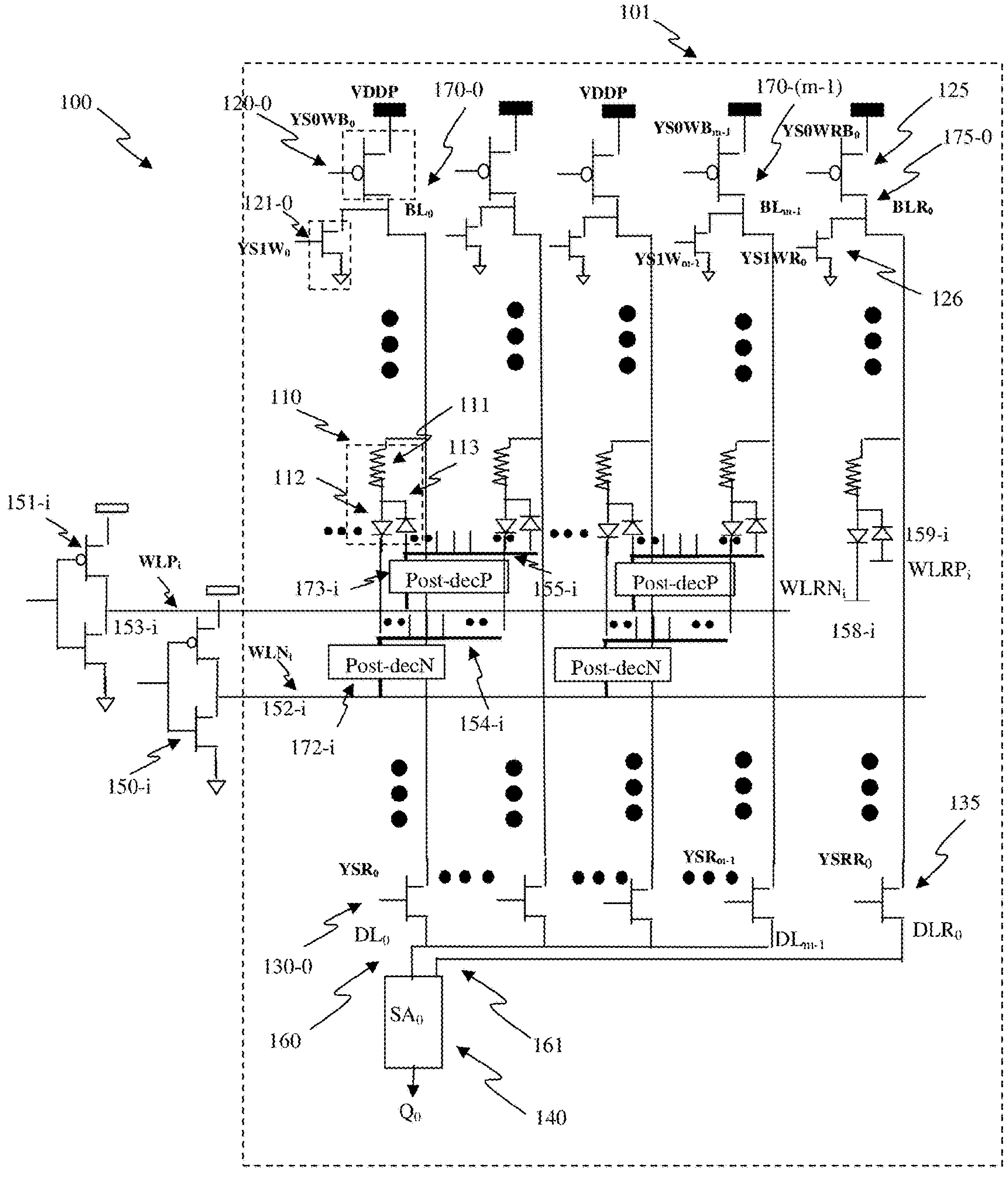
101
100
120-0
YS0WB$_0$
VDDP
170-0
VDDP
170-(m-1)
125
YS0WB$_{m-1}$
YS0WRB$_0$
175-0
121-0
BL$_0$
BL$_{m-1}$
BLR$_0$
YS1W$_0$
YS1W$_{m-1}$
YS1WR$_0$
126
110
111
113
112
151-i
159-i
WLP$_i$
173-i
Post-decP
155-i
Post-decP
WLRN$_i$
WLRP$_i$
153-i
158-i
WLN$_i$
Post-decN
Post-decN
152-i
154-i
172-i
150-i
135
YSR$_0$
YSR$_{m-1}$
YSRR$_0$
DL$_0$
DL$_{m-1}$
DLR$_0$
130-0
SA$_0$
160
161
140
Q$_0$

FIG. 16(a)

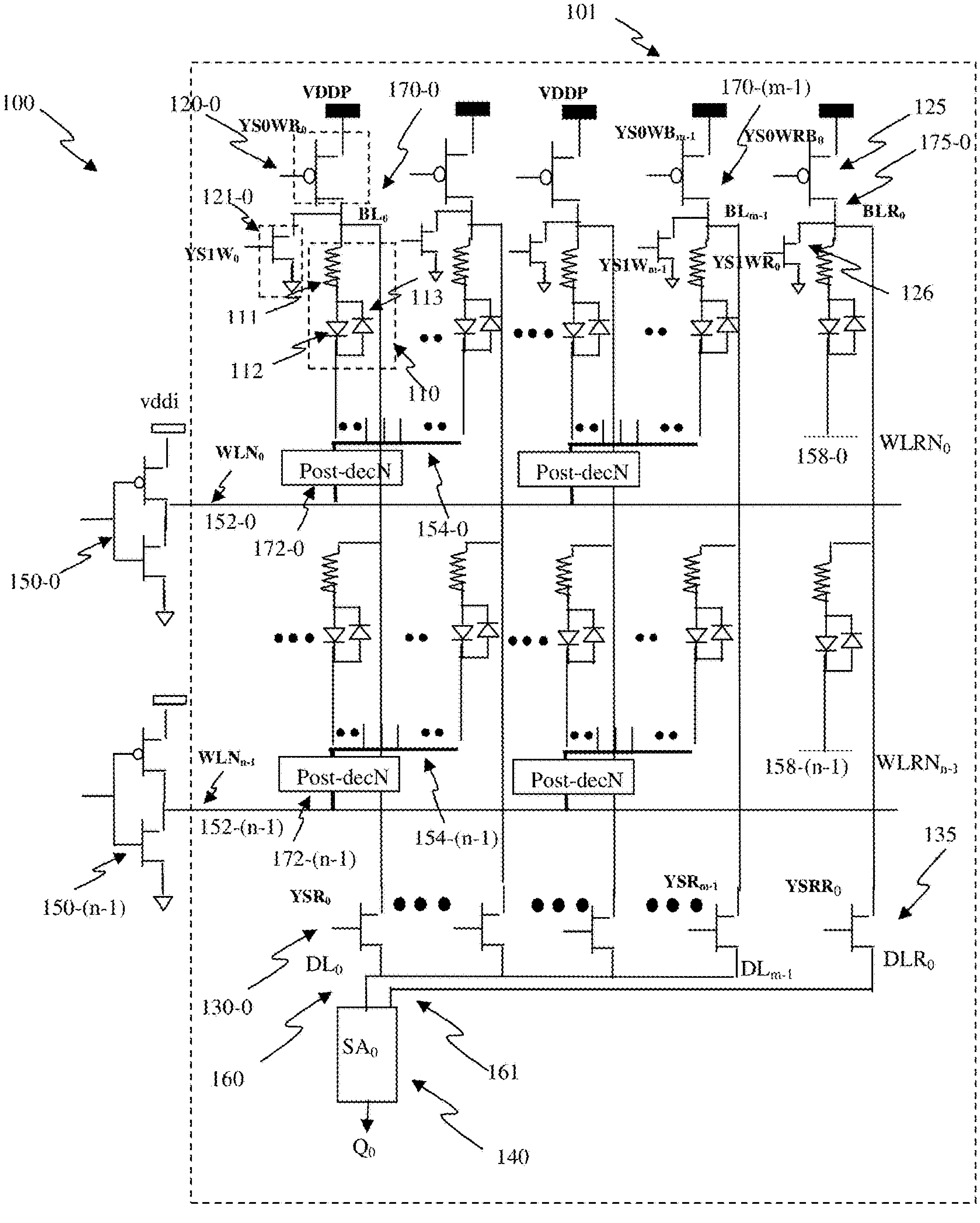
101
100
VDDP
170-0
VDDP
170-(m-1)
120-0
YS0WB0
YS0WBm-1
YS0WRB0
125
175-0
121-0
BL0
BLm-1
BLR0
YS1W0
YS1Wm-1
YS1WR0
126
111
113
112
110
vddi
WLN0
Post-decN
Post-decN
158-0
WLRN0
152-0
172-0
154-0
150-0
WLNn-1
Post-decN
Post-decN
158-(n-1)
WLRNn-1
152-(n-1)
172-(n-1)
154-(n-1)
150-(n-1)
135
YSR0
YSRm-1
YSRR0
DL0
DLm-1
DLR0
130-0
SA0
161
160
Q0
140

FIG. 16(b)

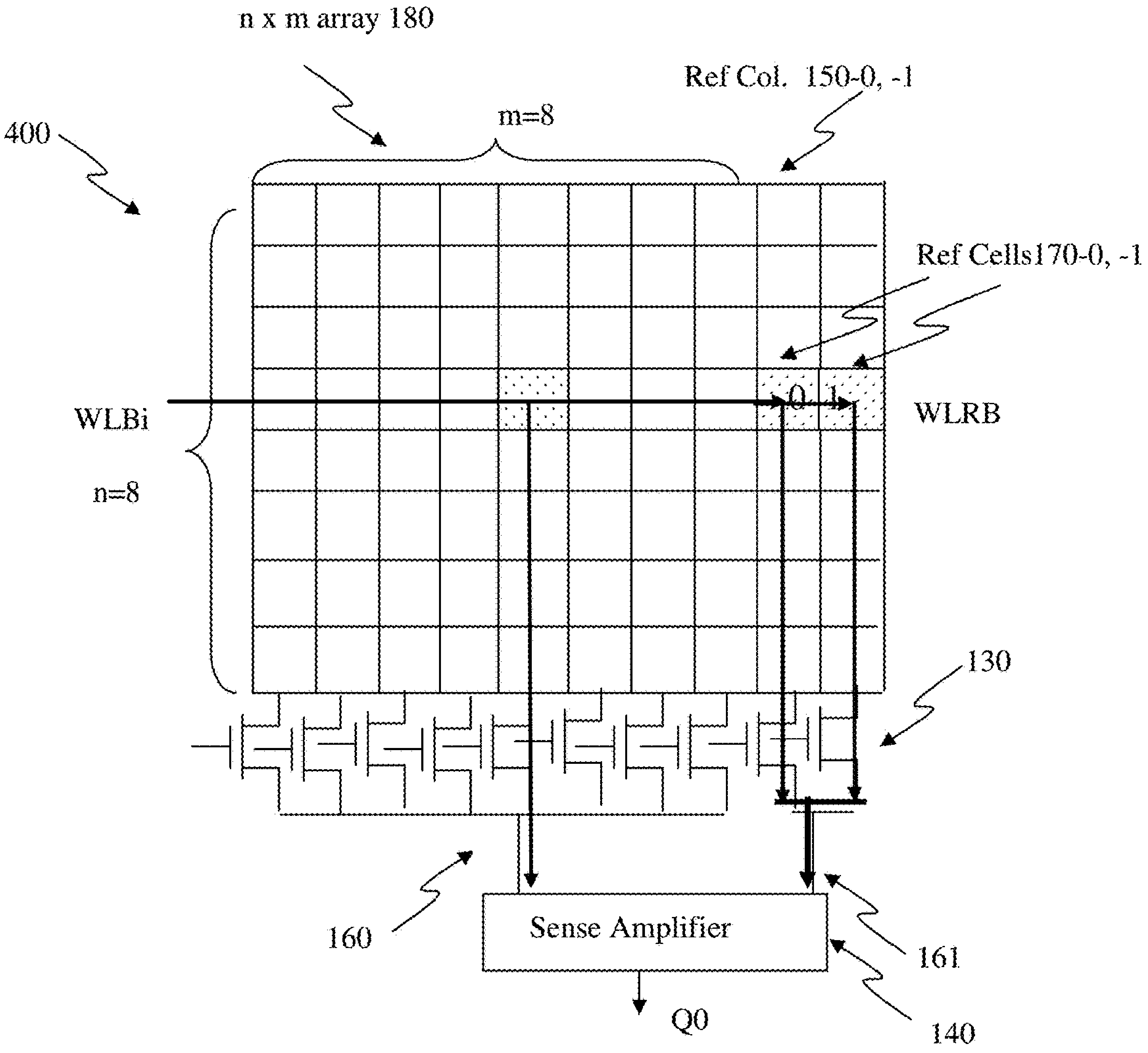
n x m array 180
Ref Col. 150-0, -1
400
m=8
Ref Cells170-0, -1
0
1
WLBi
WLRB
n=8
130
160
Sense Amplifier
161
Q0
140

FIG. 17(a)

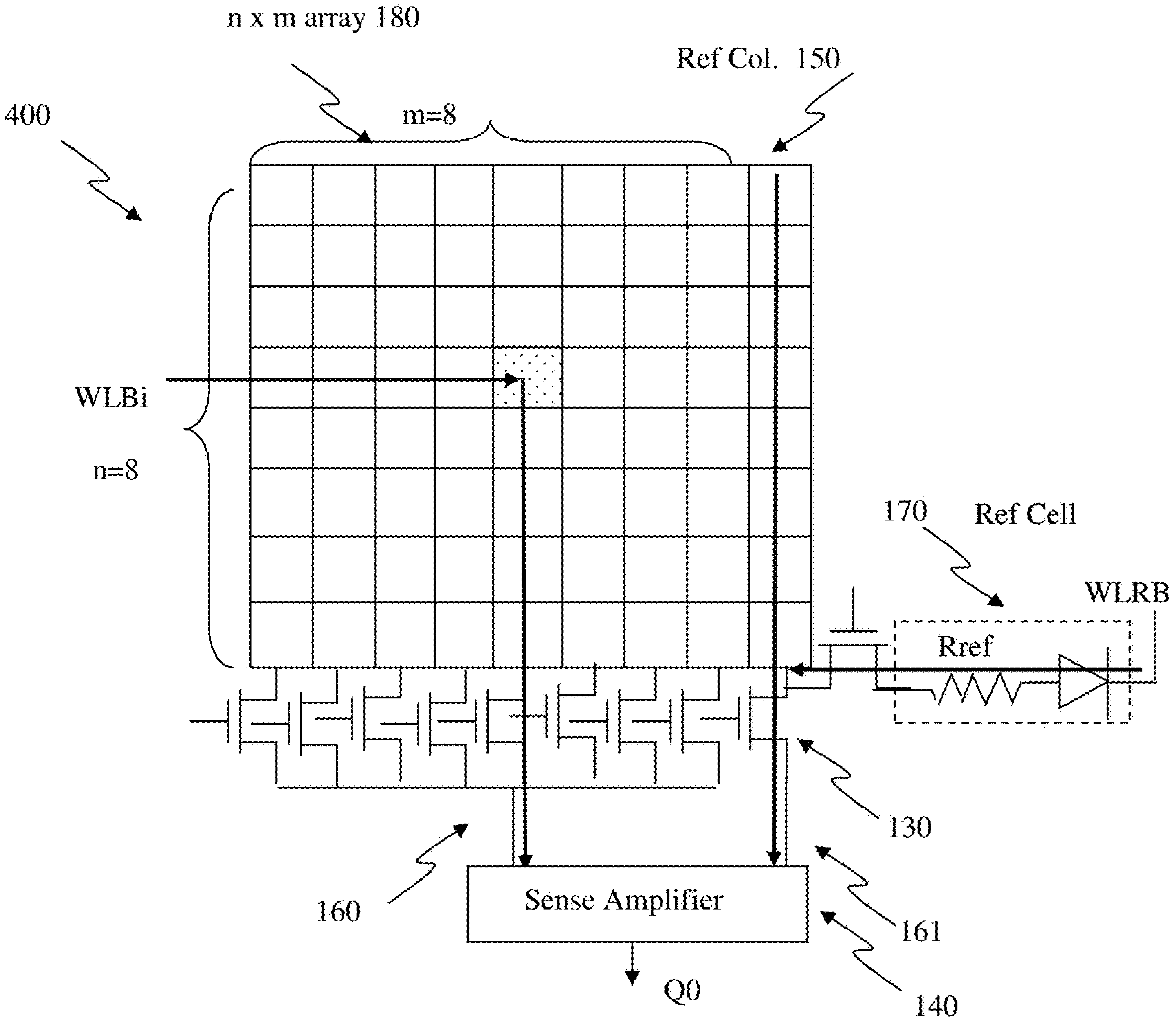
n x m array 180
Ref Col. 150
400
m=8
WLBi
n=8
170
Ref Cell
WLRB
Rref
130
160
Sense Amplifier
161
Q0
140

FIG. 17(b)

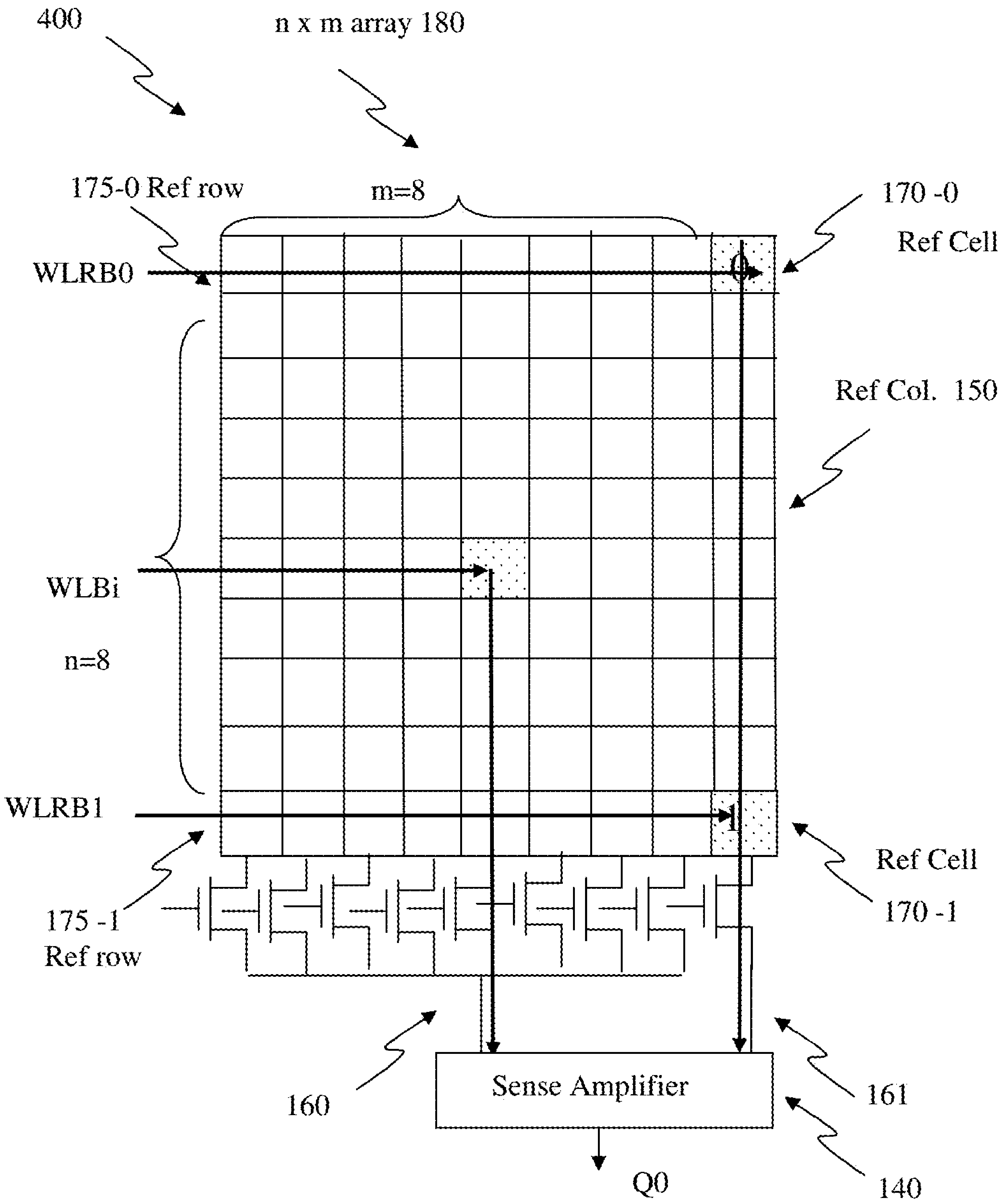
400
n x m array 180
175-0 Ref row
m=8
170 -0
Ref Cell
WLRB0
0
Ref Col. 150
WLBi
n=8
WLRB1
1
Ref Cell
170 -1
175 -1
Ref row
160
Sense Amplifier
161
140
Q0

FIG. 17(c)

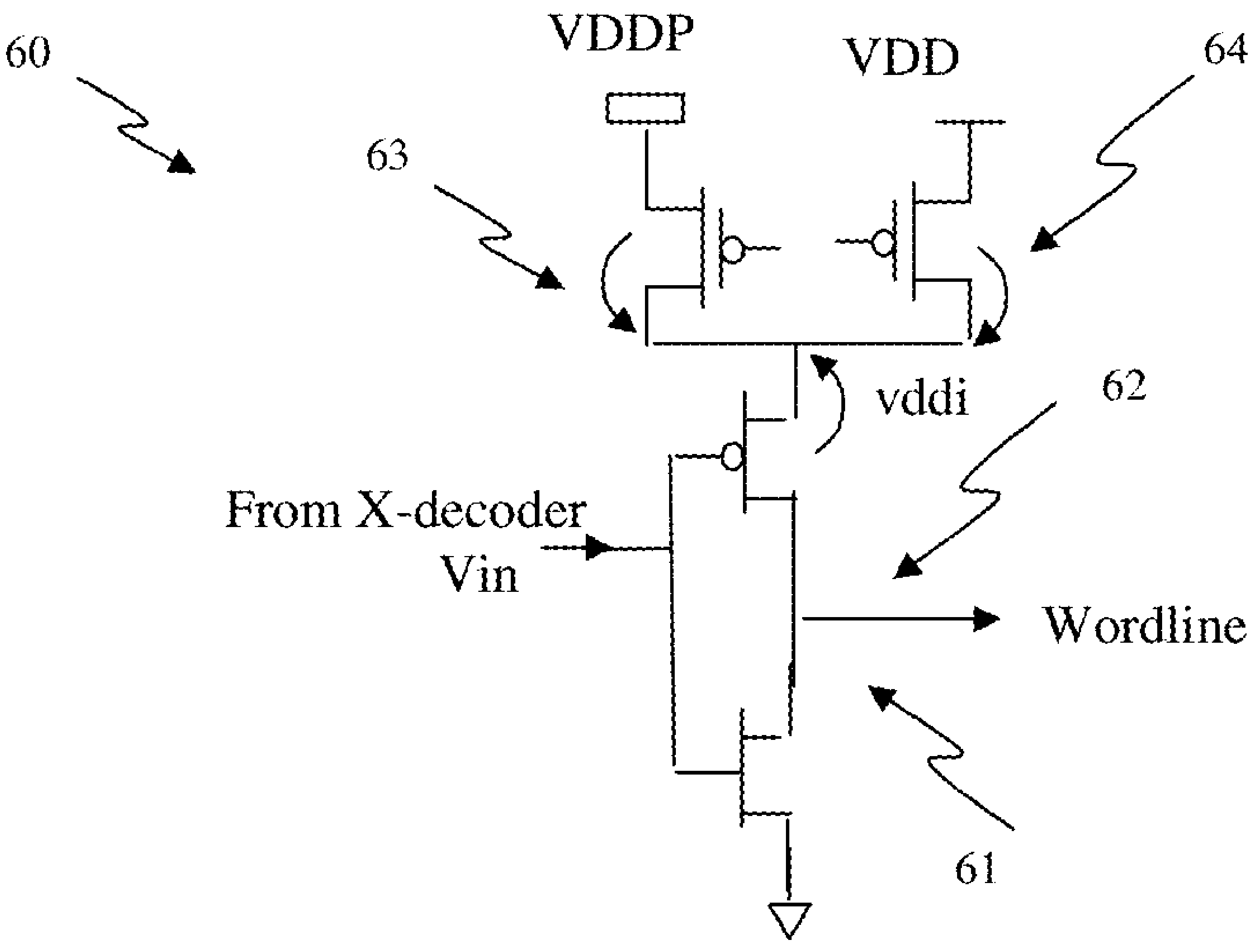

FIG. 18(a)

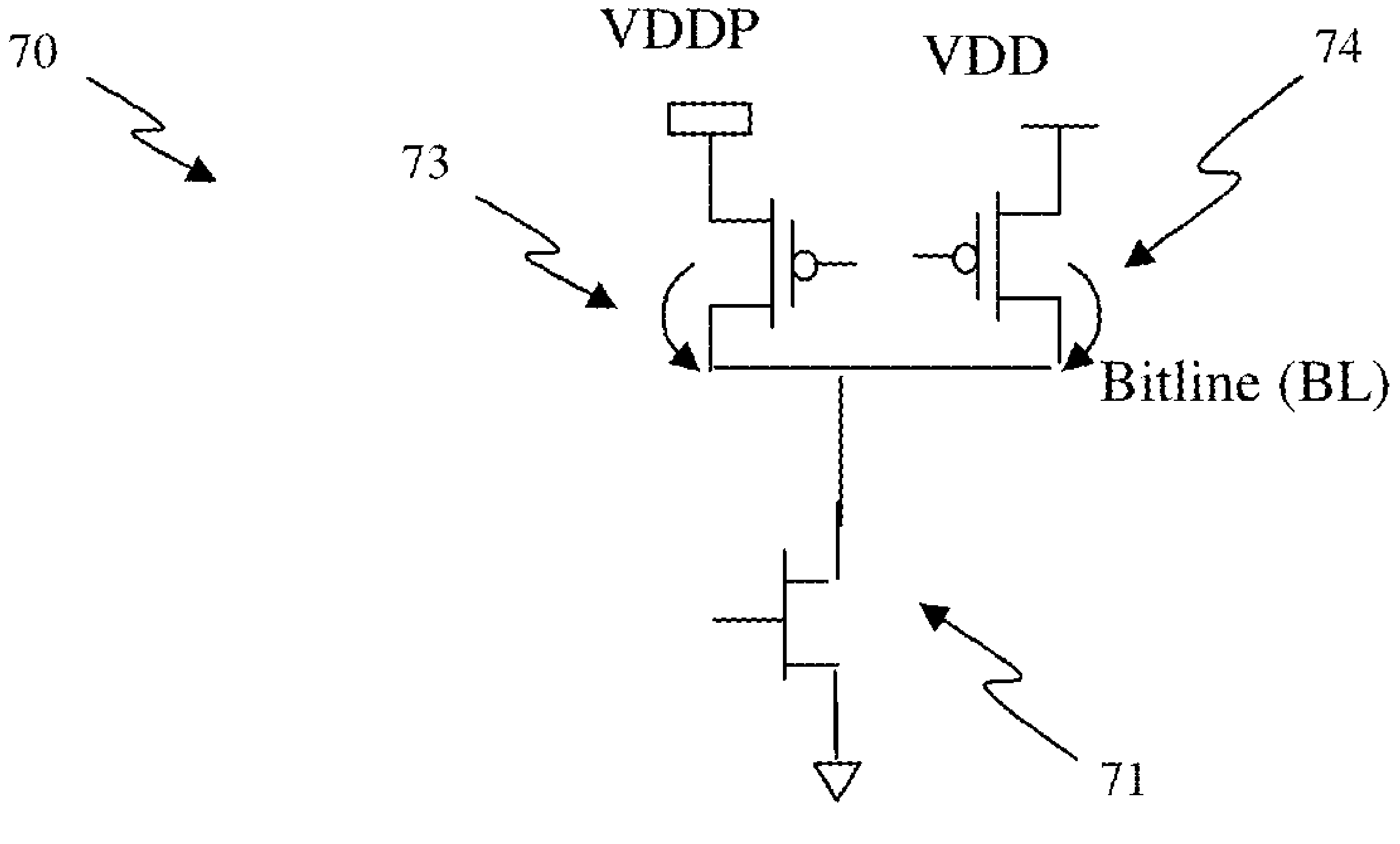

FIG. 18(b)

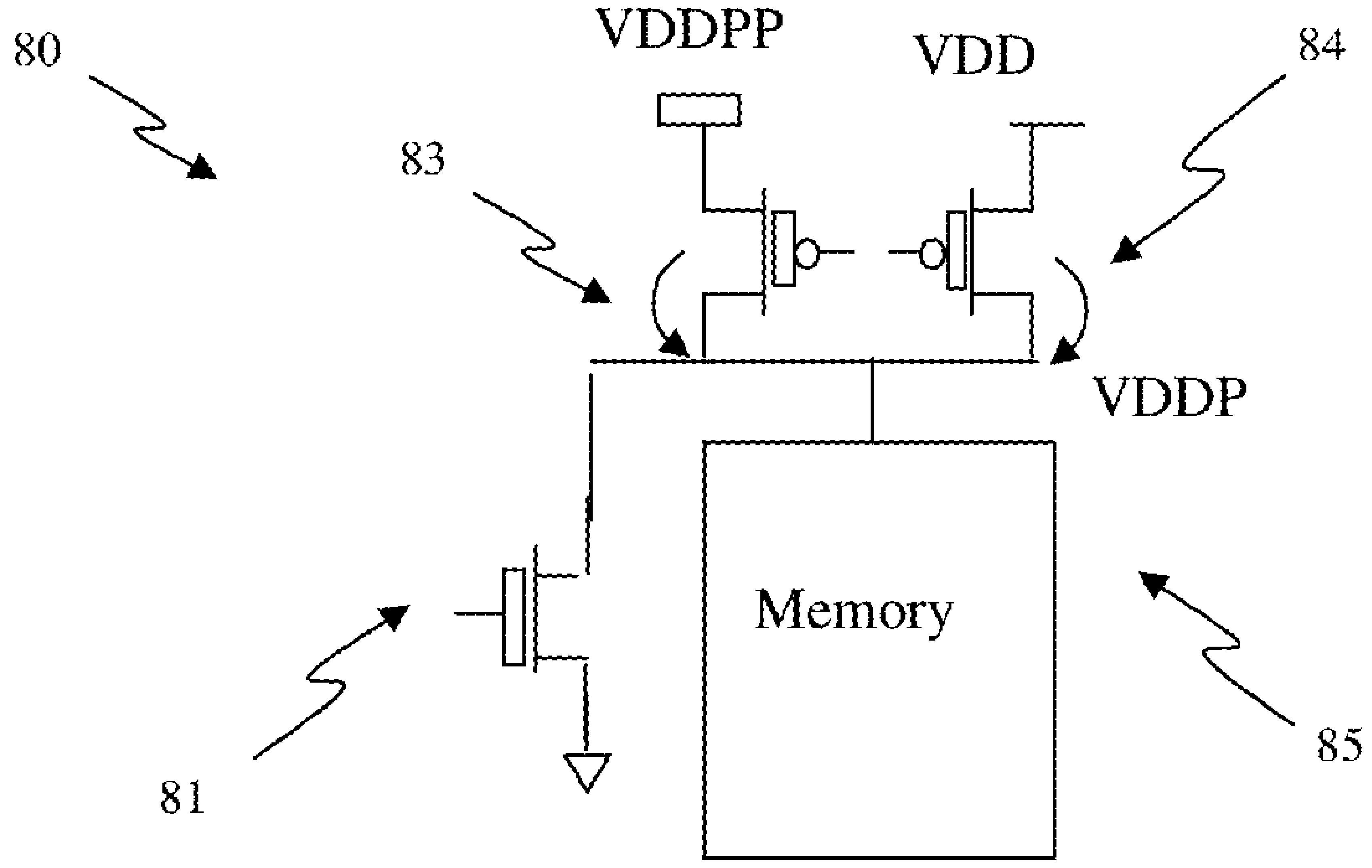

FIG. 18(c)

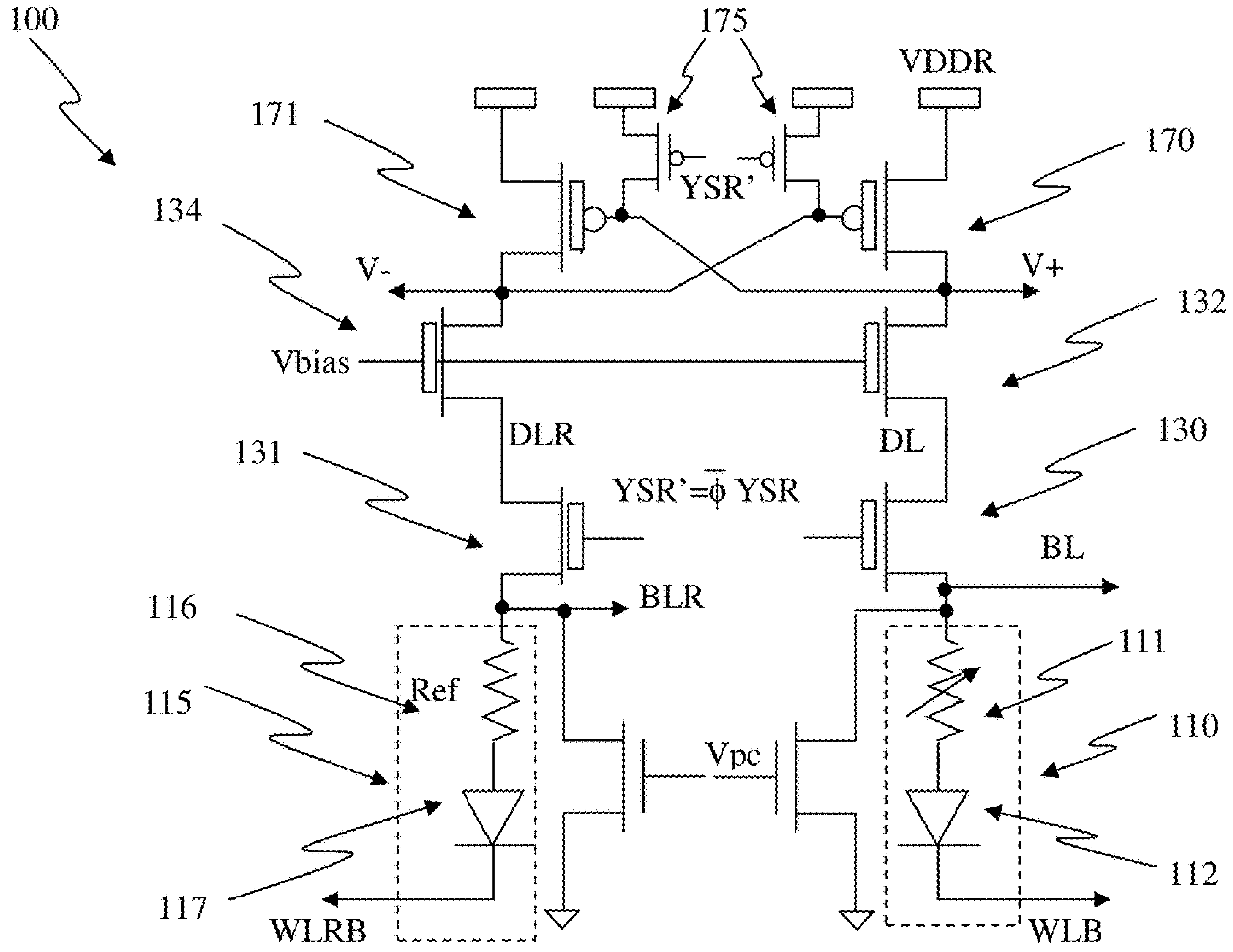
100
175
VDDR
171
170
YSR'
134
V-
V+
132
Vbias
DLR
DL
131
130
YSR'=$\bar{\phi}$ YSR
BL
116
BLR
111
Ref
115
110
Vpc
112
117
WLRB
WLB

FIG. 19(a)

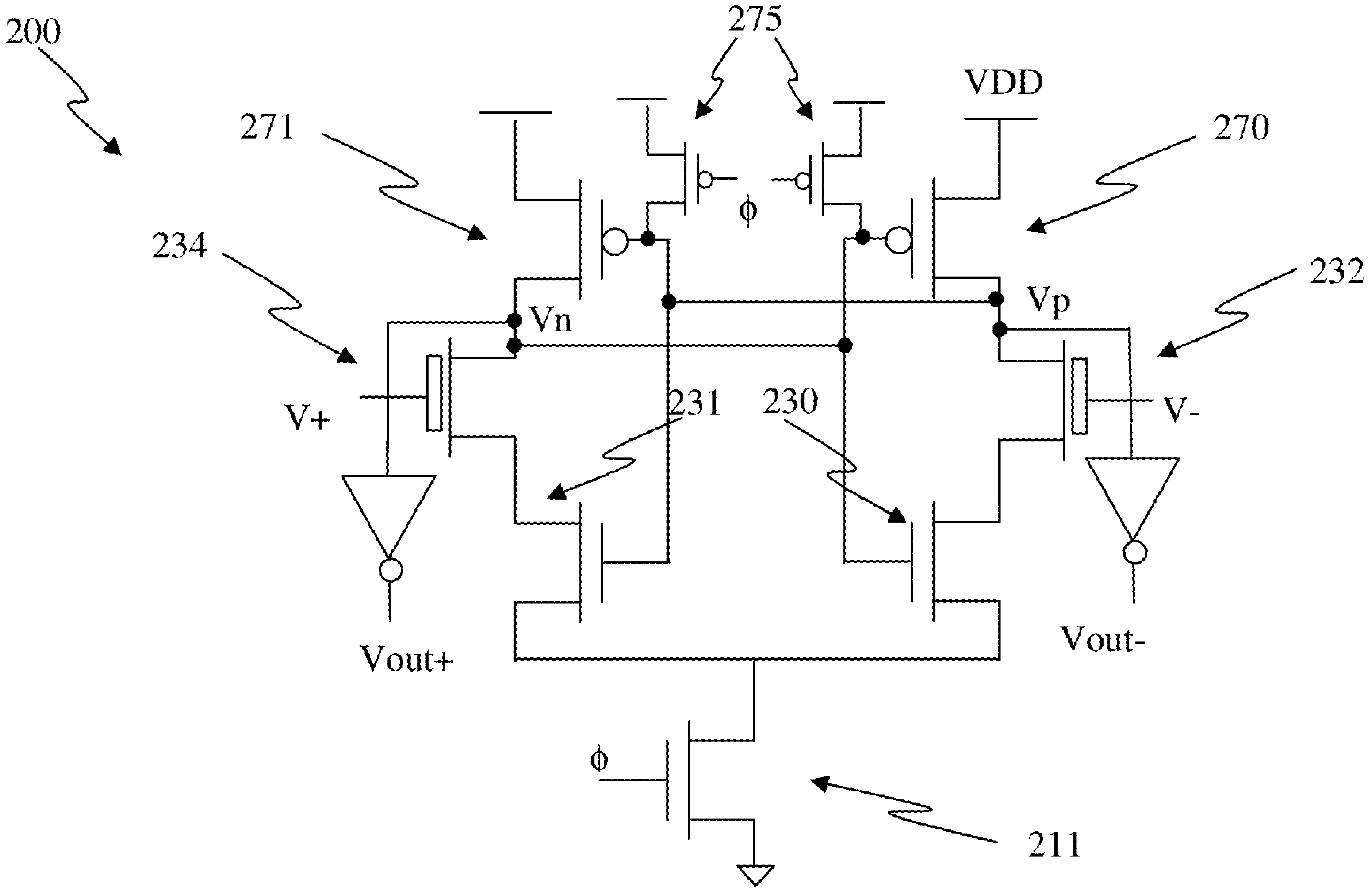

FIG. 19(b)

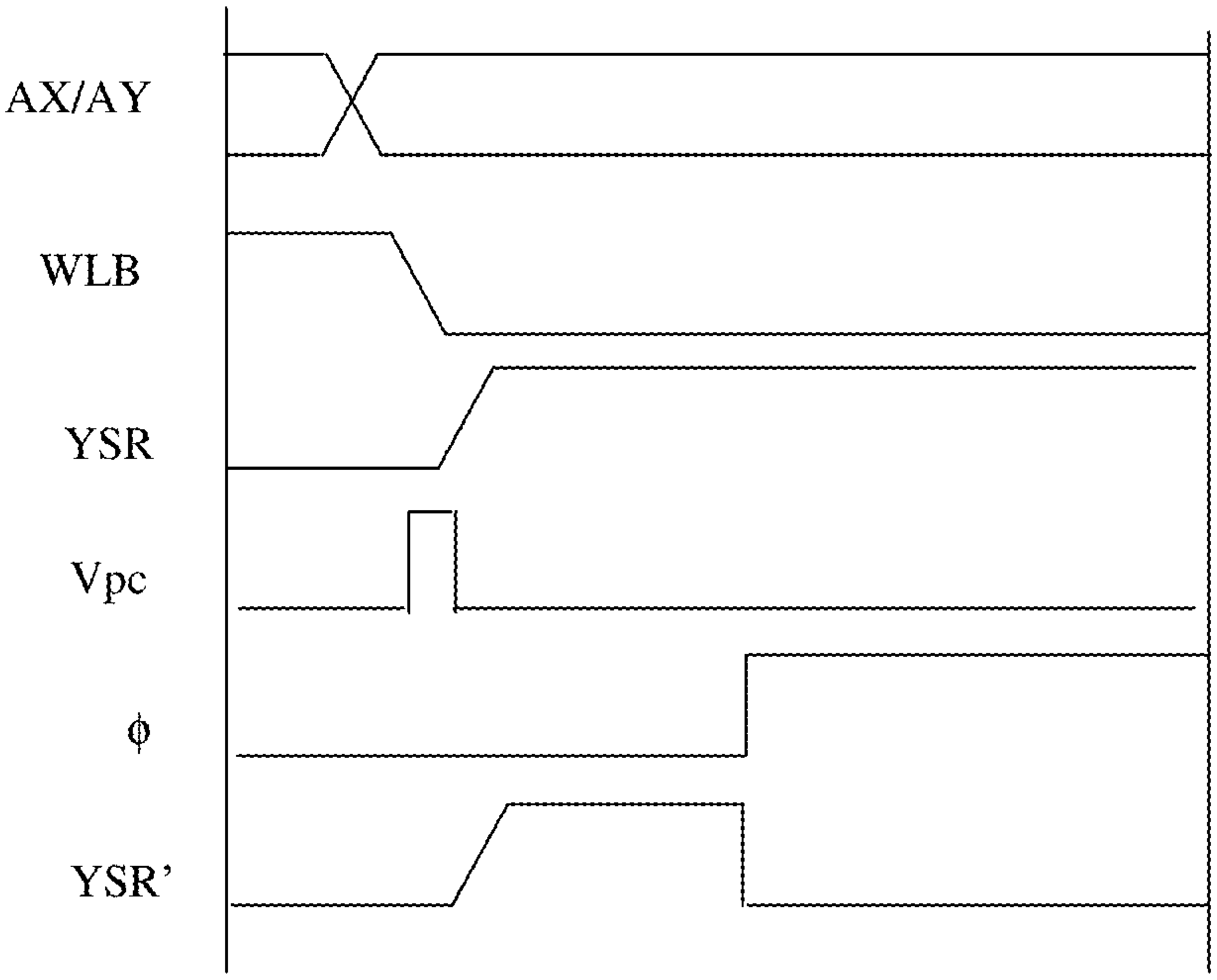

FIG. 19(c)

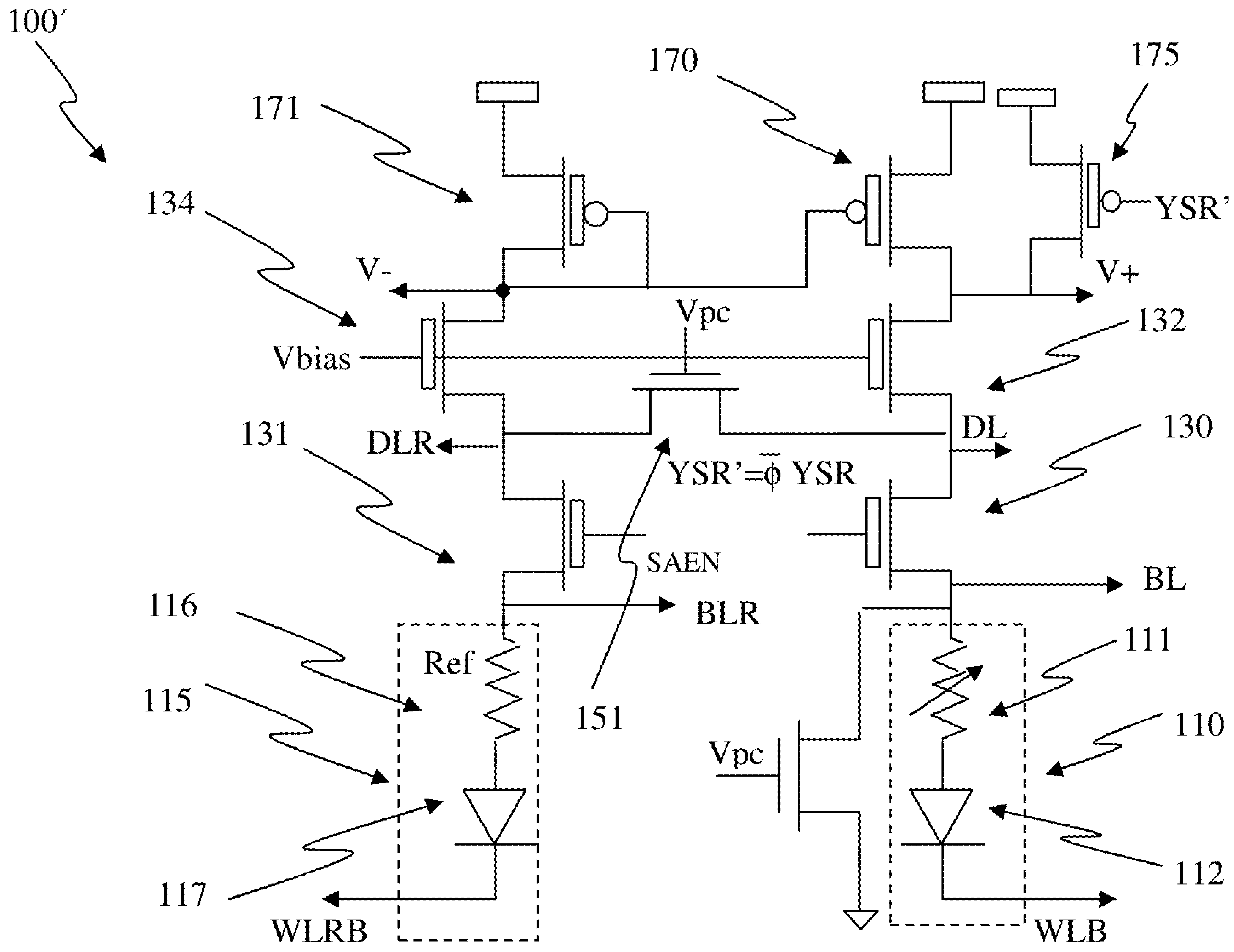
100′
171
170
175
134
YSR'
V-
V+
Vpc
132
Vbias
131
DL
130
DLR
YSR'=φ̄ YSR
SAEN
BL
116
BLR
111
Ref
115
151
110
Vpc
117
112
WLRB
WLB

FIG. 20(a)

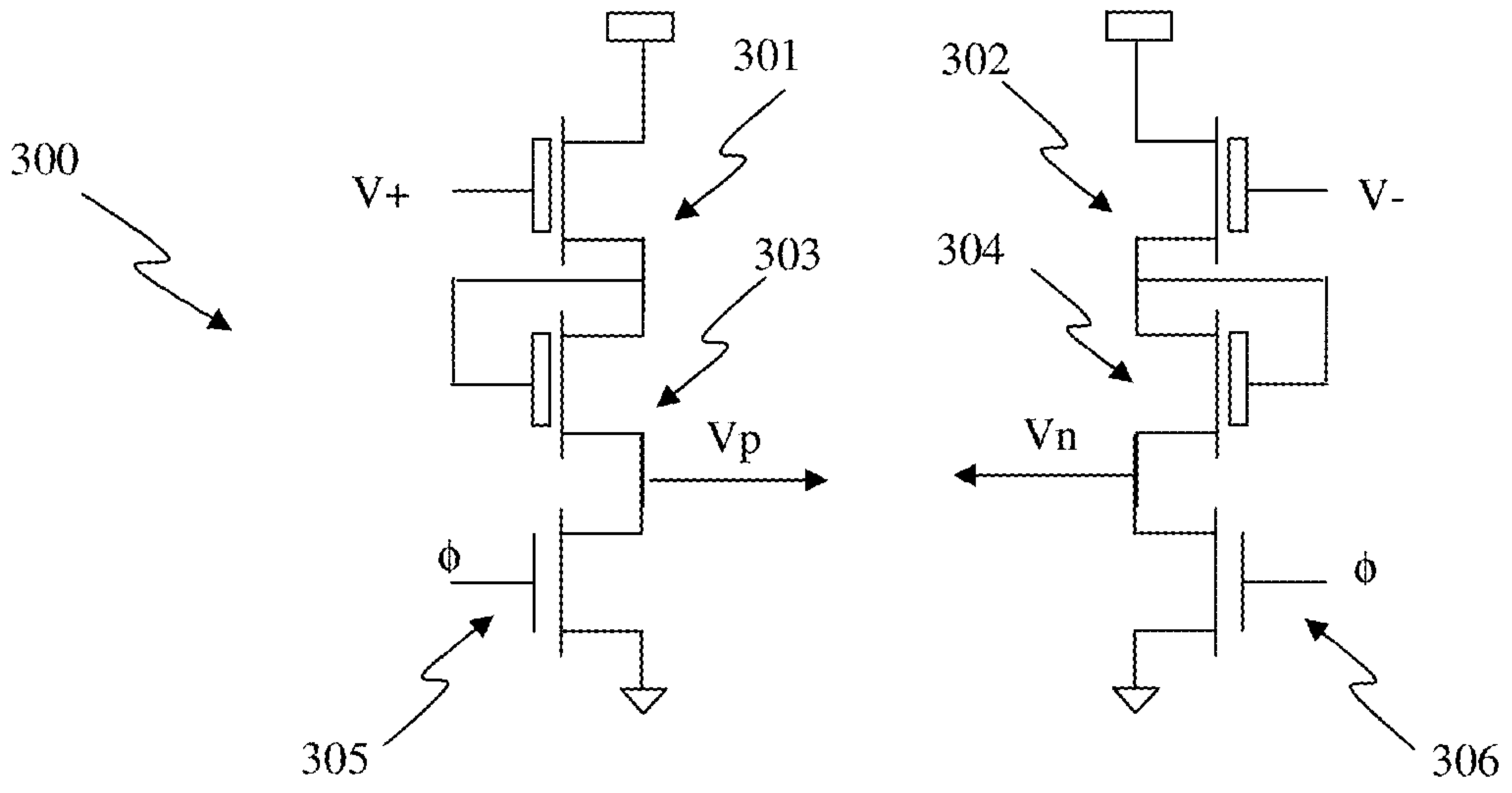

FIG. 20(b)

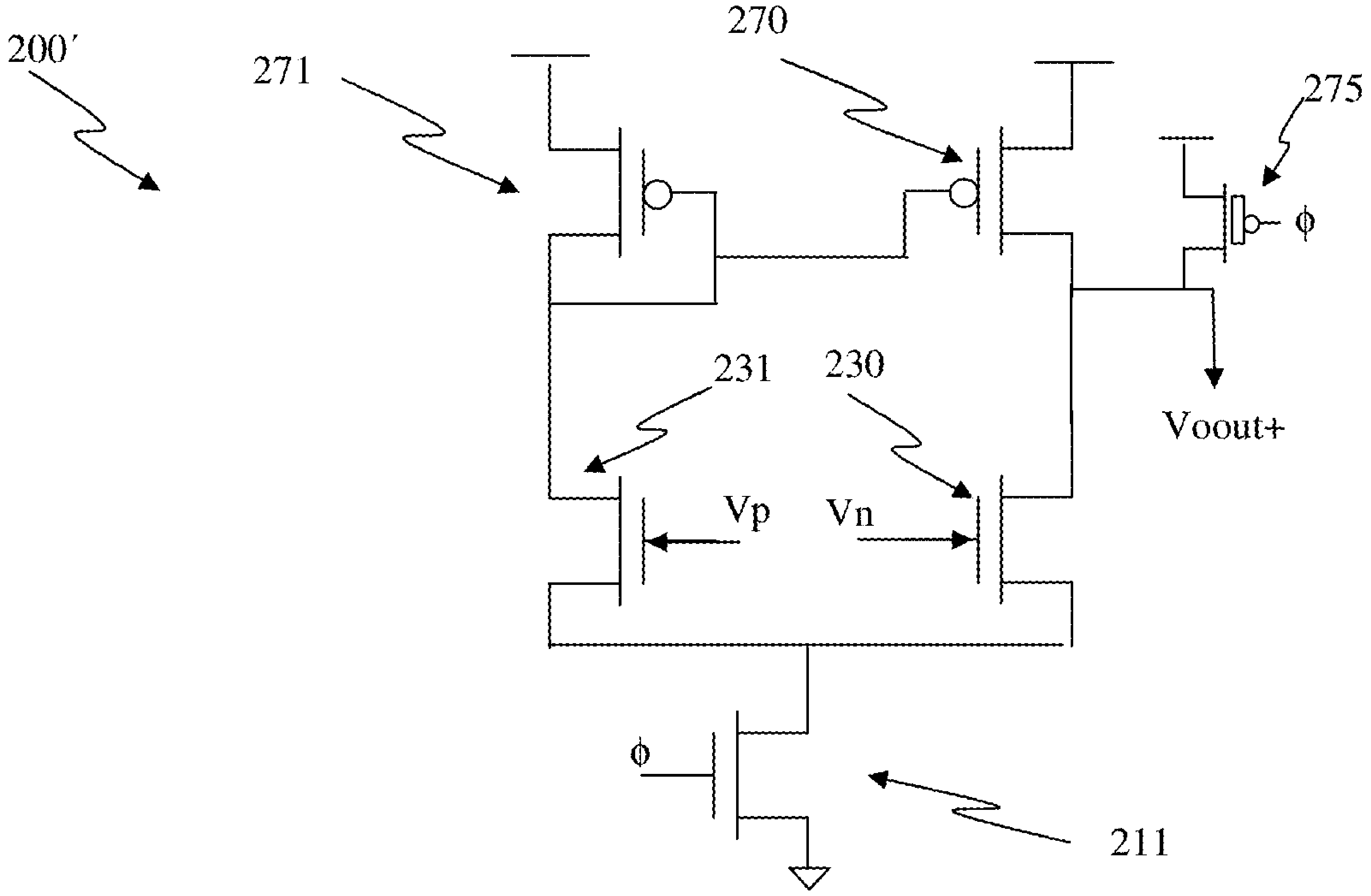

FIG. 20(c)

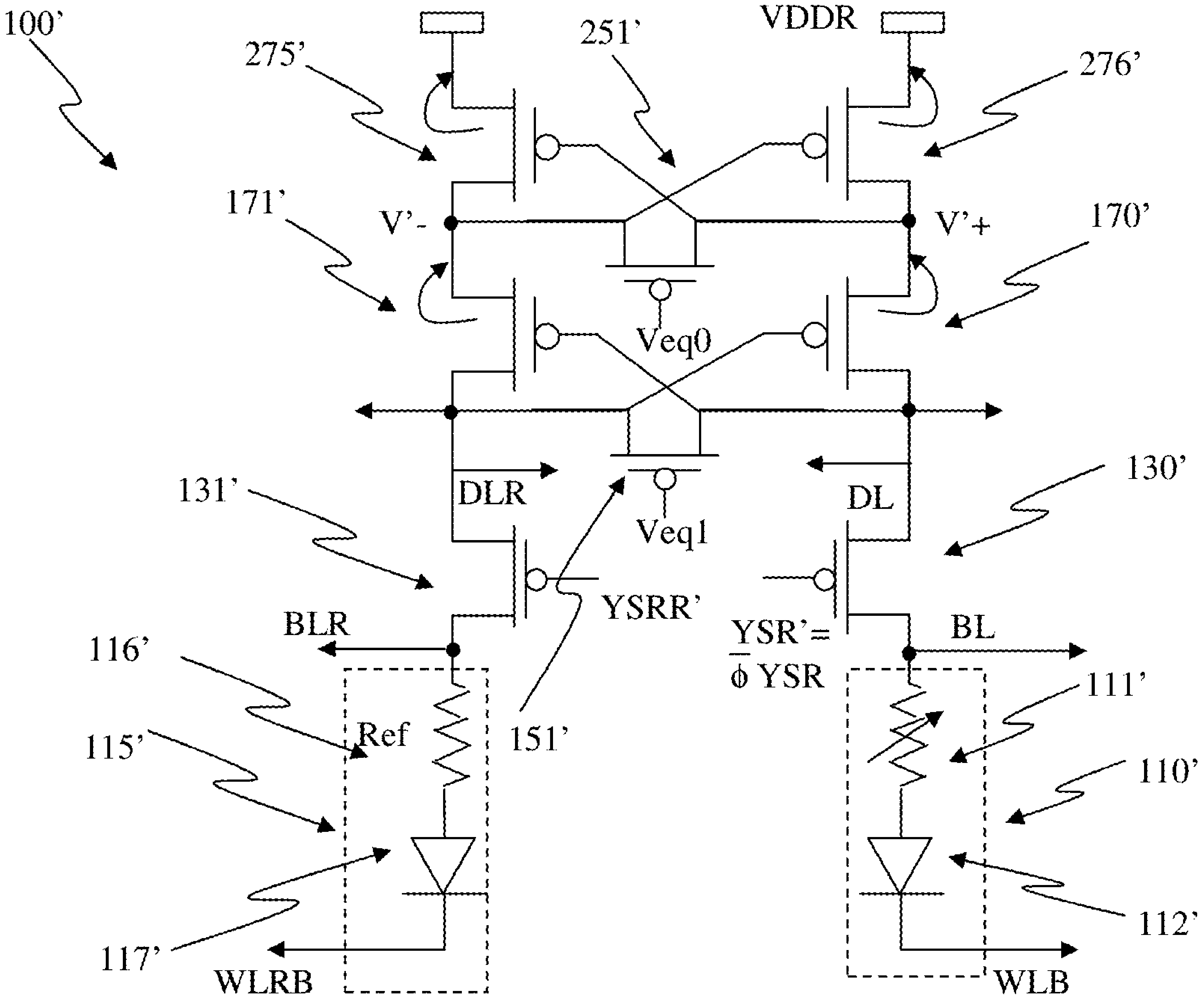
100'
275'
251'
VDDR
276'
171'
V'-
V'+
170'
Veq0
131'
DLR
Veq1
DL
130'
YSRR'
BLR
$\overline{\text{YSR'}}$=
ϕ YSR
BL
116'
111'
Ref
151'
115'
110'
117'
112'
WLRB
WLB

FIG. 20(d)

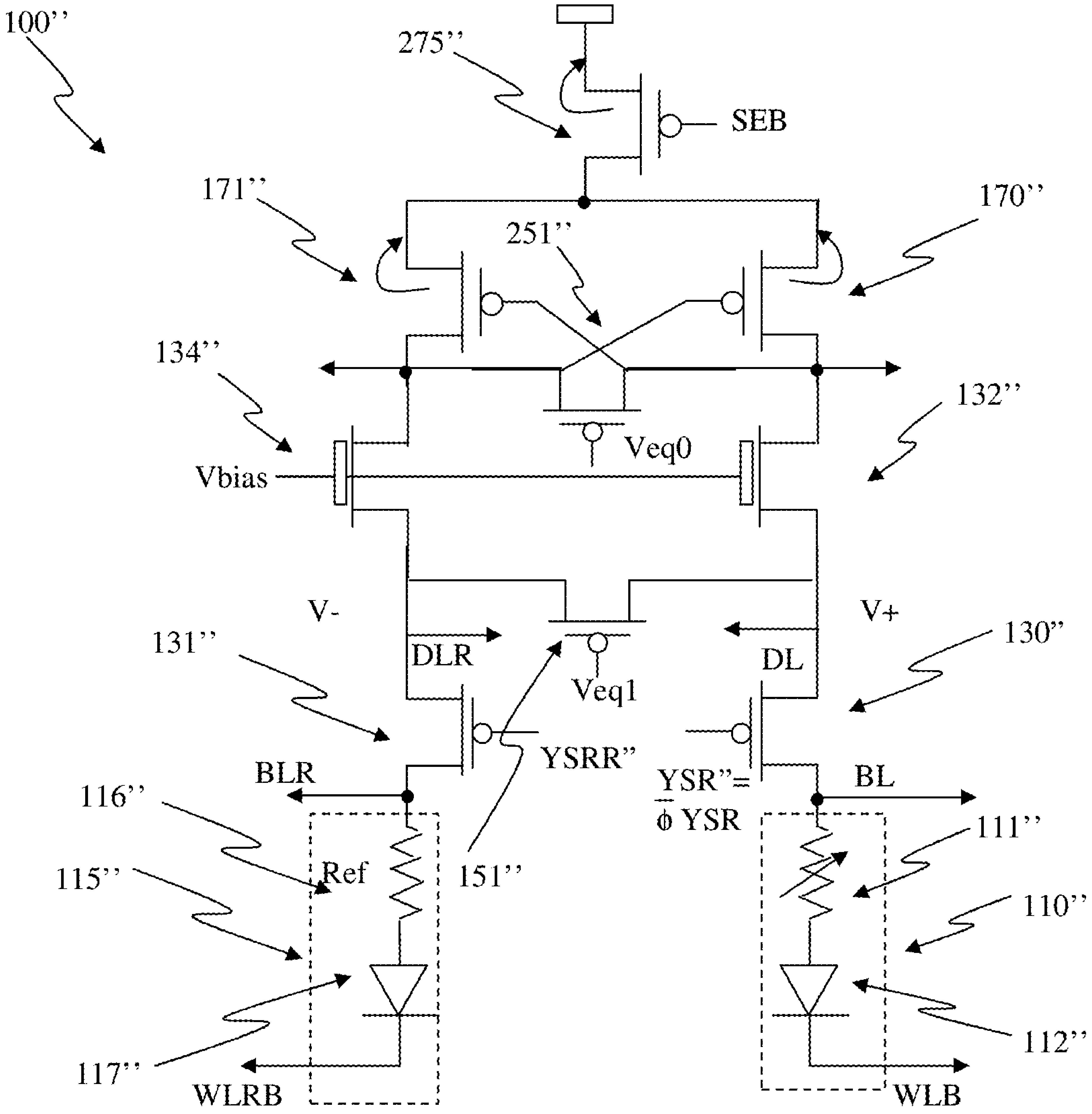
100''
275''
SEB
171''
251''
170''
134''
132''
Veq0
Vbias
V-
V+
131''
DLR
Veq1
DL
130''
YSRR''
BLR
YSR''=
$\overline{\phi}$ YSR
BL
116''
111''
Ref
151''
115''
110''
112''
117''
WLRB
WLB

FIG. 20(e)

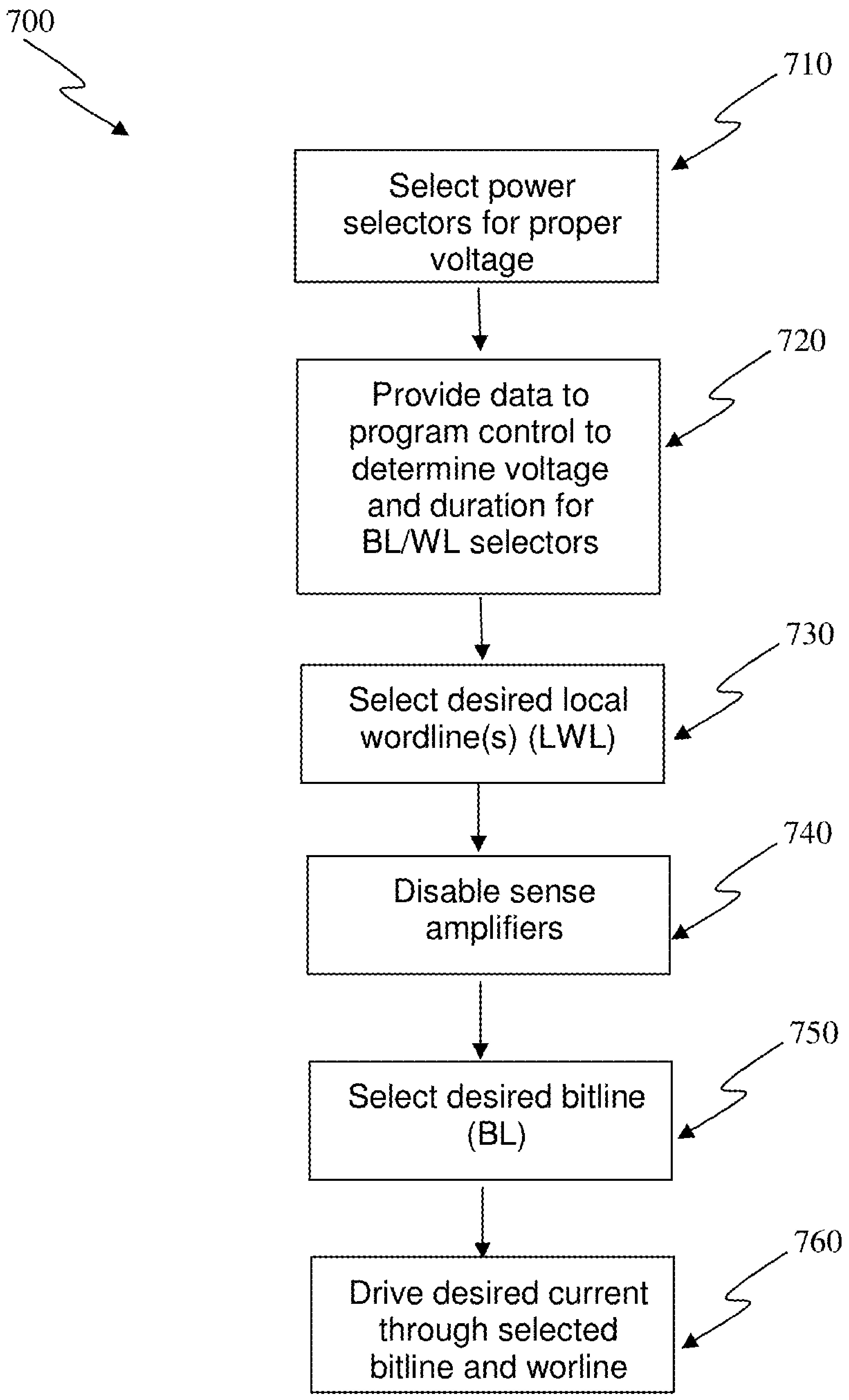
700
710
Select power selectors for proper voltage
720
Provide data to program control to determine voltage and duration for BL/WL selectors
730
Select desired local wordline(s) (LWL)
740
Disable sense amplifiers
750
Select desired bitline (BL)
760
Drive desired current through selected bitline and worline

FIG. 21(a)

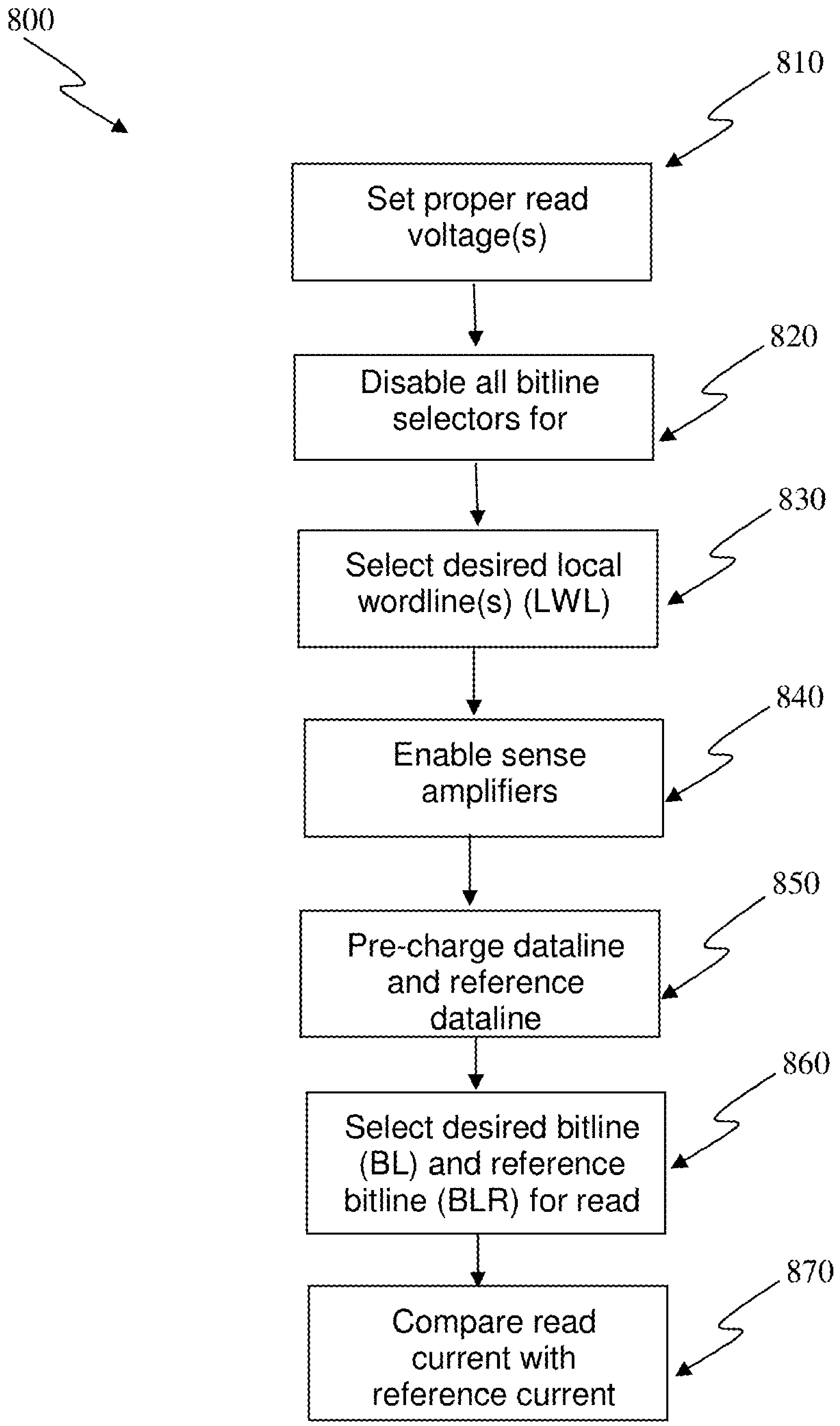
800
810
Set proper read voltage(s)
820
Disable all bitline selectors for
830
Select desired local wordline(s) (LWL)
840
Enable sense amplifiers
850
Pre-charge dataline and reference dataline
860
Select desired bitline (BL) and reference bitline (BLR) for read
870
Compare read current with reference current

FIG. 21(b)

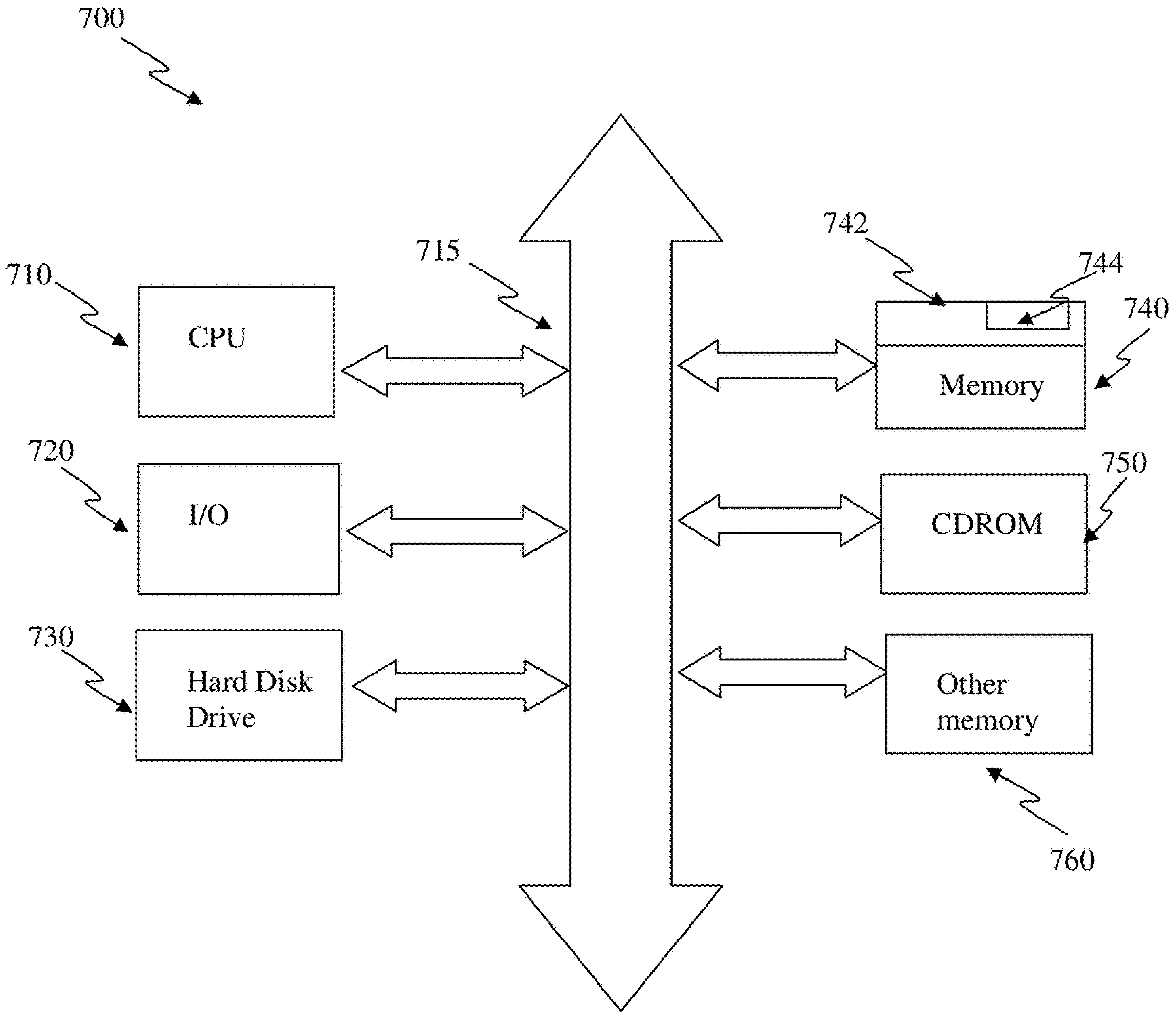
700
710
CPU
720
I/O
730
Hard Disk Drive
715
742
744
740
Memory
750
CDROM
Other memory
760

FIG. 22

ONE-TIME PROGRAMMABLE DEVICE WITH INTEGRATED HEAT SINK

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 14/749,392, filed on Jun. 24, 2015 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices with Heat Sink," now U.S. Pat. No. 9,478,306, which is hereby incorporated herein by reference, and which in turn is a continuation of U.S. patent application Ser. No. 13/842,824, filed on Mar. 15, 2013 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices with Heat Sink," now U.S. Pat. No. 9,070,437, which is hereby incorporated herein by reference.

The prior application U.S. patent application Ser. No. 13/842,824 is a continuation-in-part of U.S. patent application Ser. No. 13/471,704, filed on May 15, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," now U.S. Pat. No. 8,488,359, which is hereby incorporated herein by reference, and which claims priority benefit of U.S. Provisional Patent Application No. 61/609,353, filed on Mar. 11, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference.

The prior application U.S. patent application Ser. No. 13/842,824 also claims priority benefit of: (i) U.S. Provisional Patent Application No. 61/728,240, filed on Nov. 20, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices with Heat Sink," which is hereby incorporated herein by reference: (ii) U.S. Provisional Patent Application No. 61/668,031, filed on Jul. 5, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector and MOS as Read Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference; and (iii) U.S. Provisional Patent Application No. 61/684,800, filed on Aug. 19, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector for Metal Fuses for One-Time Programmable Devices," which is hereby incorporated herein by reference.

The prior application U.S. patent application Ser. No. 13/471,704 is a continuation-in-part of U.S. patent application Ser. No. 13/026,752, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," now U.S. Pat. No. 8,514,606, which is hereby incorporated herein by reference, and which claims priority benefit of (i) U.S. Provisional Patent Application No. 61/375,653, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Junction Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference; and (ii) U.S. Provisional Patent Application No. 61/375,660, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference.

The prior application U.S. patent application Ser. No. 13/471,704 is a continuation-in-part of U.S. patent application Ser. No. 13/026,656, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for One-Time Programmable Devices," now U.S. Pat. No. 8,644,049, which claims priority benefit of (i) U.S. Provisional Patent Application No. 61/375,653, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Junction Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference; and (ii) U.S. Provisional Patent Application No. 61/375,660, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to programmable memory devices, such as programmable resistive devices for use in memory arrays.

Description of the Related Art

A programmable resistive device is generally referred to a device's resistance states that may change after means of programming. Resistance states can also be determined by resistance values. For example, a resistive device can be a One-Time Programmable (OTP) device, such as electrical fuse, and the programming means can apply a high voltage to induce a high current to flow through the OTP element. When a high current flows through an OTP element by turning on a program selector, the OTP element can be programmed, or burned into a high or low resistance state (depending on either fuse or anti-fuse).

An electrical fuse is a common OTP which is a programmable resistive device that can be constructed from a segment of interconnect, such as polysilicon, silicided polysilicon, silicide, metal, metal alloy, or some combination thereof. The metal can be aluminum, copper, or other transition metals. One of the most commonly used electrical fuses is a CMOS gate, fabricated in silicided polysilicon, used as interconnect. The electrical fuse can also be one or more contacts or vias instead of a segment of interconnect. A high current may blow the contact(s) or via(s) into a very high resistance state. The electrical fuse can be an anti-fuse, where a high voltage makes the resistance lower, instead of higher. The anti-fuse can consist of one or more contacts or vias with an insulator in between. The anti-fuse can also be a CMOS gate coupled to a CMOS body with a thin gate oxide as insulator.

The programmable resistive device can be a reversible resistive device that can be programmed into a digital logic value "0" or "1" repetitively and reversibly. The programmable resistive device can be fabricated from phase change material, such as Germanium (Ge), Antimony (Sb), and Tellurium (Te) with composition $Ge_2Sb_2Te_5$ (GST-225) or GeSbTe-like materials including compositions of Indium (In), Tin (Sn), or Selenium (Se). Another phase change material can include a chalcogenide material such as AgInSbTe. The phase change material can be programmed into a high resistance amorphous state or a low resistance crystalline state by applying a short and high voltage pulse or a long and low voltage pulse, respectively.

Another type of reversible resistive device is a class of memory called Resistive RAM (RRAM), which is a normally insulating dielectric, but can be made conducting through filament, defects, metal migration, etc. The dielectric can be binary transition metal oxides such as NiO or TiO2, perovskite materials such as Sr(Zr)TiO3 or PCMO, organic charge transfer complexes such as CuTCNQ, or organic donor-acceptor systems such as Al AlDCN. As an example, RRAM can have cells fabricated from metal oxides between electrodes, such as Pt/NiO/Pt, TiN/TiOx/HfO2/TiN, TiN/ZnO/Pt, or W/TiN/SiO2/Si, etc. The resistance states can be changed reversibly and determined by polarity, magnitude, duration, voltage/current-limit, or the combinations thereof to generate or annihilate conductive filaments. Another programmable resistive device similar to RRAM is a Conductive Bridge RAM (CBRAM) that is based on electro-chemical deposition and removal of metal ions in a thin solid-state electrolyte film. The electrodes can be an oxidizable anode and an inert cathode and the electrolyte can be Ag- or Cu-doped chalcogenide glass such as GeSe, Cu2S, or GeS, etc. The resistance states can be changed reversibly and determined by polarity, magnitude, duration, voltage/current-limit, or combinations thereof to generate or annihilate conductive bridges. The programmable resistive device can also be an MRAM (Magnetic RAM) with cells fabricated from magnetic multi-layer stacks that construct a Magnetic Tunnel Junction (MTJ). In a Spin Transfer Torque MRAM (STT-MRAM) the direction of currents applied to an MTJ determines parallel or anti-parallel states, and hence low or high resistance states.

A conventional programmable resistive memory cell **10** is shown in FIG. **1**. The cell **10** consists of a resistive element **11** and an NMOS program selector **12**. The resistive element **11** is coupled to the drain of the NMOS **12** at one end, and to a high voltage V+ at the other end. The gate of the NMOS **12** is coupled to a select signal (Sel), and the source is coupled to a low voltage V−. When a high voltage is applied to V+ and a low voltage to V−, the resistive cell **10** can be programmed by raising the select signal (Sel) to turn on the NMOS **12**. One of the most common resistive elements is a silicided polysilicon, the same material and fabricated at the same time as a MOS gate. The size of the NMOS **12**, as program selector, needs to be large enough to deliver the required program current for a few microseconds. The program current for a silicided polysilicon is normally between a few milliamps for a fuse with width of 40 nm to about 20 mA for a fuse with width about 0.6 um. As a result, the cell size of an electrical fuse using silicided polysilicon tends to be very large. The resistive cell **10** can be organized as a two-dimensional array with all Sel's and V−'s in a row coupled as wordlines (WLs) and a ground line, respectively, and all V+'s in a column coupled as bitlines (BLs).

Another conventional programmable resistive device **20** for Phase Change Memory (PCM) is shown in FIG. **2**(*a*). The PCM cell **20** has a phase change film **21** and a bipolar transistor **22** as program selector with P+ emitter **23**, N base **27**, and P sub collector **25**. The phase change film **21** is coupled to the emitter **23** of the bipolar transistor **22** at one end, and to a high voltage V+ at the other. The N type base **27** of bipolar transistor **22** is coupled to a low voltage V−. The collector **25** is coupled to ground. By applying a proper voltage between V+ and V− for a proper duration of time, the phase change film **21** can be programmed into high or low resistance states, depending on voltage and duration. Conventionally, to program a phase-change memory to a high resistance state (or reset state) requires about 3V for 50 ns and consumes about 300 uA of current, or to program a phase-change memory to a low resistance state (or set state) requires about 2V for 300 ns and consumes about 100 uA of current.

FIG. **2**(*b*) shows a cross section of a conventional bipolar transistor **22**. The bipolar transistor **22** includes a P+ active region **23**, a shallow N well **24**, an N+ active region **27**, a P type substrate **25**, and a Shallow Trench Isolation (STI) **26** for device isolation. The P+ active region **23** and N+ active region **27** couple to the N well **24** are the P and N terminals of the emitter-base diode of the bipolar transistor **22**, while the P type substrate **25** is the collector of the bipolar transistor **22**. This cell configuration requires an N well **24** be shallower than the STI **26** to properly isolate cells from each other and needs 3-4 more masking steps over the standard CMOS logic processes which makes it more costly to fabricate.

Another programmable resistive device **20'** for Phase Change Memory (PCM) is shown in FIG. **2**(*c*). The PCM cell **20'** has a phase change film **21'** and a diode **22'**. The phase change film **21'** is coupled between an anode of the diode **22'** and a high voltage V+. A cathode of the diode **22'** is coupled to a low voltage V−. By applying a proper voltage between V+ and V− for a proper duration of time, the phase change film **21'** can be programmed into high or low resistance states, depending on voltage and duration. The programmable resistive cell **20'** can be organized as a two dimensional array with all V-'s in a row coupled as wordline bars (WLBs), and all V+'s in a column coupled as bitlines (BLs). As an example of use of a diode as program selector for each PCM cell as shown in FIG. **2**(*c*), see Kwang-Jin Lee et al., "A 90 nm 1.8V 512 Mb Diode-Switch PRAM with 266 MB/s Read Throughput," International Solid-State Circuit Conference, 2007, pp. 472-273. Though this technology can reduce the PCM cell size to only 6.8 F^2 (F stands for feature size), the diode requires very complicated process steps, such as Selective Epitaxial Growth (SEG), to fabricate, which would be very costly for embedded PCM applications.

FIGS. **3**(*a*) and **3**(*b*) show several embodiments of an electrical fuse element **80** and **84**, respectively, fabricated from an interconnect. The interconnect serves as a particular type of resistive element. The resistive element has three parts: anode, cathode, and body. The anode and cathode provide contacts for the resistive element to be connected to other parts of circuits so that a current can flow from the anode to cathode through the body. The body width determines the current density and hence the electro-migration threshold for a program current. FIG. **3**(*a*) shows a conventional electrical fuse element **80** with an anode **81**, a cathode **82**, and a body **83**. This embodiment has a large symmetrical anode and cathode. FIG. **3**(*b*) shows another conventional electrical fuse element **84** with an anode **85**, a cathode **86**, and a body **87**. This embodiment has an asymmetrical shape with a large anode and a small cathode to enhance the electro-migration effect based on polarity and reservoir effects. The polarity effect means that the electro-migration always starts from the cathode. The reservoir effect means that a smaller cathode makes electro-migration easier because the smaller area has lesser ions to replenish voids when the electro-migration occurs. The fuse elements **80**, **84** in FIGS. **3**(*a*) and **3**(*b*) are relatively large structures which makes them unsuitable for some applications.

FIGS. **4**(*a*) and **4**(*b*) show programming a conventional MRAM cell **210** into parallel (or state 0) and anti-parallel (or state 1) by current directions. The MRAM cell **210** consists of a Magnetic Tunnel Junction (MTJ) **211** and an NMOS program selector **218**. The MTJ **211** has multiple layers of ferromagnetic or anti-ferromagnetic stacks with metal oxide, such as Al_2O_3 or MgO, as an insulator in between. The MTJ **211** includes a free layer stack **212** on top and a fixed layer stack **213** underneath. By applying a proper current to the MTJ **211** with the program selector CMOS **218** turned on, the free layer stack **212** can be aligned into parallel or anti-parallel to the fixed layer stack **213** depending on the current flowing into or out of the fixed layer stack **213**, respectively. Thus, the magnetic states can be programmed and the resultant states can be determined by resistance values, lower resistance for parallel and higher resistance for anti-parallel states. The resistances in state 0 or 1 are about 5KΩ or 10KΩ, respectively, and the program currents are about +/−100-200 μA. One example of programming an MRAM cell is described in T. Kawahara, "2 Mb Spin-Transfer Torque RAM with Bit-by-Bit Bidirectional Current Write and Parallelizing-Direction Current Read," International Solid-State Circuit Conference, 2007, pp. 480-481.

SUMMARY

Embodiments of programmable resistive device cells using junction diodes as program selectors are disclosed. The programmable resistive devices can be fabricated using standard CMOS logic processes to reduce cell size and cost.

In one embodiment, a programmable resistive device and memory can use P+/N well diodes as program selectors, where the P and N terminals of the diode are P+ and N+ active regions residing in an N well. The same P+ and N+ active regions are used to create sources or drains of PMOS and NMOS devices, respectively.

Advantageously, the same N well can be used to house PMOS in standard CMOS logic processes. By using P+/N well diodes in standard CMOS processes, a small cell size can be achieved, without incurring any special processing or masks. The junction diode can be constructed in N well in bulk CMOS or can be constructed on isolated active regions in Silicon-On-Insulator (SOI) CMOS, FinFET bulk, FinFET SOI, or similar technologies. Thus, costs can be reduced substantially for variously applications, such as embedded applications.

The invention can be implemented in numerous ways, including as a method, system, device, or apparatus (including graphical user interface and computer readable medium). Several embodiments of the invention are discussed below.

As a programmable resistive memory, one embodiment can, for example, include a plurality of programmable resistive cells. At least one of the programmable resistive cells can include a resistive element coupled to a first supply voltage line, and a diode including at least a first active region and a second active region isolated from the first active region. The first active region can have a first type of dopant and the second region can have a second type of dopant. The first active region can provide a first terminal of the diode, the second active region can provide a second terminal of the diode, and both the first and second active regions can reside in a common well or on an isolated active region. The first and second regions can be isolated by Shallow Trench Isolation (STI), LOCOS (LOCal Oxidation), dummy MOS gate, or Silicide Block Layer (SBL). The first active region can also be coupled to the resistive element, and the second active region can be coupled to a second supply voltage line. The first and second active regions can be fabricated from sources or drains of CMOS devices, and in a CMOS well or on an isolated active region. The resistive element can be configured to be programmable by applying voltages to the first and second supply voltage lines to thereby change the resistance into a different logic state.

As an electronics system, one embodiment can, for example, include at least a processor, and a programmable resistive memory operatively connected to the processor. The programmable resistive memory can include at least a plurality of programmable resistive cells for providing data storage. Each of the programmable resistive cells can include at least a resistive element coupled to a first supply voltage line, and a diode including at least a first active region and a second active region isolated from the first active region. The first active region can have a first type of dopant and the second region can have a second type of dopant. The first active region can provide a first terminal of the diode, the second active region can provide a second terminal of the diode, and both the first and second active regions can reside in a common well or on an isolated active region. The first and second regions can be isolated by Shallow Trench Isolation (STI), LOCOS (LOCal Oxidation), dummy MOS gate, or Silicide Block Layer (SBL). The first active region can be coupled to the resistive element and the second active region can be coupled to a second supply voltage line. The first and second active regions can be fabricated from sources or drains of CMOS devices. The well can be fabricated from CMOS wells. The isolated active region can be fabricated from SOI or FinFET technologies. The programmable resistive element can be configured to be programmable by applying voltages to the first and the second supply voltage lines to thereby change the resistance into a different logic state.

As a method for providing a programmable resistive memory, one embodiment can, for example, include at least providing a plurality of programmable resistive cells, and programming a logic state into at least one of the programmable resistive cells by applying voltages to the first and the second voltage lines. The at least one of the programmable resistive cells can include at least (i) a resistive element coupled to a first supply voltage line, and (ii) a diode including at least a first active region and a second active region isolated from the first active region. The first active region can have a first type of dopant and the second region can have a second type of dopant. The first active region can provide a first terminal of the diode, the second active region can provide a second terminal of the diode, and both the first and second active regions can be fabricated from sources or drains of CMOS devices. Both active regions can reside in a common well fabricated from CMOS wells or on an isolated active region. The first and second regions can be isolated by Shallow Trench Isolation (STI), LOCOS (LOCal Oxidation), dummy MOS gate, or Silicide Block Layer (SBL). The first active region can be coupled to the resistive element and the second active region can be coupled to a second supply voltage line.

As a One-Time Programmable (OTP) memory, one embodiment can, for example, include at least: a plurality of OTP cells, where at least one of the cells includes at least: (i) an OTP element including at least an interconnect, the OTP element being coupled to a first supply voltage line; (ii) a diode including at least a first active region and a second active region isolated from the first active region, where the first active region having a first type of dopant and a second active region having a second type of dopant, the first active region providing a first terminal of the diode, the second active region providing a second terminal of the diode, both the first and second active regions residing in a common CMOS well or on an isolated substrate, the first active region coupled to the OTP element and the second active region coupled to a second supply voltage line, the first and second active regions being fabricated from sources or drains of CMOS devices; and (iii) at least one thermally conductive element, coupled to the OTP element, to dissipate or generate heat. The OTP element can be configured to be programmable by applying voltages to the first and the second supply voltage lines to thereby change its logic state, and the thermally conductive element can be configured to assist in programming of the OTP element.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed descriptions in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. **1** shows a conventional programmable resistive memory cell.

FIG. **2**(*a*) shows another conventional programmable resistive device for Phase Change Memory (PCM) using bipolar transistor as program selector.

FIG. **2**(*b*) shows a cross section of a conventional Phase Change Memory (PCM) using bipolar transistor as program selector.

FIG. **2**(*c*) shows another conventional Phase Change Memory (PCM) cell using diode as program selector.

FIGS. **3**(*a*) and **3**(*b*) show several embodiments of an electrical fuse element, respectively, fabricated from an interconnect.

FIGS. **4**(*a*) and **4**(*b*) show programming a conventional MRAM cell into parallel (or state 0) and anti-parallel (or state 1) by current directions.

FIG. **5**(*a*) shows a block diagram of a memory cell using a junction diode according to the invention.

FIG. **5**(*b*) shows a cross section of a junction diode as program selector with STI isolation according to one embodiment.

FIG. **5**(*c*) shows a cross section of a junction diode as program selector with CMOS gate isolation according to one embodiment.

FIG. **5**(*d*) shows a cross section of a junction diode as program selector with SBL isolation according to one embodiment.

FIG. **6**(*a*) shows a cross section of a junction diode as program selector with dummy CMOS gate isolation in SOI technologies according to one embodiment.

FIG. **6**(*a***1**) shows a top view of a junction diode as program selector with dummy CMOS gate isolation in SOI or similar technologies according to one embodiment.

FIG. **6**(*a***2**) shows a top view of a junction diode as program selector with Silicide Block Layer (SBL) isolation in SOI or similar technologies according to one embodiment

FIG. **6**(*a***3**) shows a top view of a programmable resistive cell having a resistive element and a program selector in one piece of an isolated active region with dummy gate isolation, according to one embodiment.

FIG. **6**(*a***4**) shows a top view of a programmable resistive cell having a resistive element with a program selector in one piece of an isolated active region with SBL isolation, according to another embodiment

FIG. **6**(*b***1**) shows a 3D view of at least one junction diode as program selector with dummy CMOS gate isolation in FINFET technologies according to one embodiment.

FIG. **6**(*b***2**) shows a 3D view of two junction diodes as program selectors constructed from two fins with an N well contact between fins in FINFET technologies according to another embodiment.

FIG. **6**(*b***3**) shows a 3D view of two junction diode as program selectors constructed from two P type fins and an N type fins in between in FINFET technologies according to yet another embodiment.

FIG. **6**(*b***4**) shows a 3D view of a junction diode as program selector constructed from a P type fin and an N type fin in FINFET technologies according to yet another embodiment.

FIG. **6**(*c***1**) shows a schematic of a programmable resistive cell with a PMOS for low power applications according to one embodiment.

FIG. **6**(*c***2**) shows a schematic of a programmable resistive cell with a PMOS for low power applications according to another embodiment.

FIG. **6**(*c***3**) shows a schematic of a programmable resistive cell with an NMOS for low power applications according to another embodiment.

FIG. **7**(*a*) shows an electrical fuse element according to one embodiment.

FIG. **7**(*a***1**) shows an electrical fuse element with a small body and slightly tapered structures according to another embodiment.

FIG. **7**(*a***2**) shows an electrical fuse element using a thermally conductive but electrically insulated heat sink in the anode according to another embodiment.

FIG. **7**(*a***3**) shows an electrical fuse element with a thinner oxide as heat sink underneath the body and near the anode according to another embodiment.

FIG. **7**(*a***3***a*) shows an electrical fuse element with thin oxide areas as heat sinks underneath the anode according to yet another embodiment.

FIG. **7**(*a***3***b*) shows an electrical fuse element with thin oxide areas as heat sink near to the anode according to yet another embodiment.

FIG. **7**(*a***3***c*) shows an electrical fuse element with an extended anode as heat sink according to yet another embodiment.

FIG. **7**(*a***3***d*) shows an electrical fuse element with a high resistance area as heat generator according to one embodiment.

FIG. **7**(*a***4**) shows an electrical fuse element with at least one notch according to another embodiment.

FIG. **7**(*a***5**) shows an electrical fuse element with part NMOS metal gate and part PMOS metal gate according to another embodiment.

FIG. **7**(*a***6**) shows an electrical fuse element with a segment of polysilicon between two metal gates according to another embodiment.

FIG. **7**(*a***7**) shows a diode constructed from a polysilicon between two metal gates according to another embodiment.

FIG. **7**(*a***8**) shows a 3D view of a metal fuse element constructed from a contact and a metal segment, according to one embodiment.

FIG. **7**(*a***9**) shows a 3D view of a metal fuse element constructed from a contact, two vias, and segment(s) of metal 2 and metal 1, according to another embodiment.

FIG. **7**(*a***10**) shows a 3D view of a metal fuse element constructed from 3 contacts, segment(s) of metal gate and metal-1, according to yet another embodiment.

FIG. **7**(*b*) shows a top view of an electrical fuse coupled to a junction diode with STI isolation in four sides.

FIG. **7**(*c*) shows a top view of an electrical fuse coupled to a junction diode with STI isolation in two sides and dummy CMOS isolation in another two sides.

FIG. **7**(*d*) shows a top view of an electrical fuse coupled to a junction diode with dummy CMOS isolation in four sides.

FIG. **7**(*e*) shows a top view of an electrical fuse coupled to a junction diode with Silicide Block Layer isolation in four sides.

FIG. **7**(*f*) shows a top view of an abutted contact coupled between a resistive element, P terminal of a junction diode, and metal in a single contact.

FIG. **7**(*g*) shows a top view of an electrical fuse coupled to a junction diode with dummy CMOS gate isolation between P+/N+ of a diode and adjacent cells.

FIG. **7**(*h*) shows a top view of a programmable resistive cell coupled to a junction diode with dummy CMOS gate isolation between P+/N+ and has large contacts.

FIG. **8**(*a*) shows a top view of a metal fuse coupled to a junction diode with dummy CMOS gate isolation.

FIG. **8**(*b*) shows a top view of a metal fuse coupled to a junction diode with 4 cells sharing one N well contact in each side.

FIG. **8**(*c*) shows a top view of a via1 fuse coupled to a junction diode with 4 cells sharing one N well contact in each side.

FIG. **8**(*d*) shows a top view of a two-dimensional array of via1 fuses using P+/N well diodes.

FIG. **9**(*a*) shows a cross section of a programmable resistive device cell using phase-change material as a resistive element, with buffer metals and a P+/N well junction diode, according to one embodiment.

FIG. **9**(*b*) shows a top view of a PCM cell using a P+/N well junction diode as program selector in accordance with one embodiment.

FIG. **10** shows one embodiment of an MRAM cell using diodes as program selectors in accordance with one embodiment.

FIG. **11**(*a*) shows a top view of an MRAM cell with an MTJ as a resistive element and with P+/N well diodes as program selectors in standard CMOS processes in accordance with one embodiment.

FIG. **11**(*b*) shows another top view of an MRAM cell with an MTJ as a resistive element and with P+/N well diodes as program selectors in a shallow well CMOS process in accordance with another embodiment.

FIG. **12**(*a*) shows one embodiment of a three-terminal 2×2 MRAM cell array using junction diodes as program selectors and the condition to program the upper-right cell into 1 in accordance with one embodiment.

FIG. **12**(*b*) shows alternative conditions to program the upper-right cell into 1 in a 2×2 MRAM array in accordance with one embodiment.

FIG. **13**(*a*) shows one embodiment of a three-terminal 2×2 MRAM cell array using junction diodes as program selectors and the condition to program the upper-right cell into 0 in accordance with one embodiment.

FIG. **13**(*b*) shows alternative conditions to program the upper-right cell into 0 in a 2×2 MRAM array in accordance with one embodiment.

FIGS. **14**(*a*) and **14**(*b*) show one embodiment of programming 1 and 0 into the upper-right cell, respectively, in a two-terminal 2×2 MRAM cell array in accordance with one embodiment.

FIG. **15** shows a portion of a programmable resistive memory constructed by an array of n-row by (m+1)-column single-diode-as-program-selector cells and n wordline drivers in accordance with one embodiment.

FIG. **16**(*a*) shows a portion of a programmable resistive memory constructed by an array of 3-terminal MRAM cells according to one embodiment.

FIG. **16**(*b*) shows another embodiment of constructing a portion of MRAM memory with 2-terminal MRAM cells.

FIGS. **17**(*a*), **17**(*b*), and **17**(*c*) show three other embodiments of constructing reference cells for differential sensing.

FIG. **18**(*a*) shows a schematic of a wordline driver circuit according to one embodiment.

FIG. **18**(*b*) shows a schematic of a bitline circuit according to one embodiment.

FIG. **18**(*c*) shows a portion of memory with an internal power supply VDDP coupled to an external supply VDDPP and a core logic supply VDD through power selectors.

FIG. **19**(*a*) shows one embodiment of a schematic of a pre-amplifier according to one embodiment.

FIG. **19**(*b*) shows one embodiment of a schematic of an amplifier according to one embodiment.

FIG. **19**(*c*) shows a timing diagram of the pre-amplifier and the amplifier in FIGS. **19**(*a*) and **19**(*b*), respectively.

FIG. **20**(*a*) shows another embodiment of a pre-amplifier, similar to the pre-amplifier in FIG. **18**(*a*).

FIG. **20**(*b*) shows level shifters according to one embodiment.

FIG. **20**(*c*) shows another embodiment of an amplifier with current-mirror loads.

FIG. **20**(*d*) shows another embodiment of a pre-amplifier with two levels of PMOS pullup stacked so that all core devices can be used.

FIG. **20**(*e*) shows another embodiment of a pre-amplifier with an activation device for enabling.

FIG. **21**(*a*) depicts a method of programming a programmable resistive memory in a flow chart according to one embodiment.

FIG. **21**(*b*) depicts a method of reading a programmable resistive memory in a flow chart according to one embodiment.

FIG. **22** shows a processor system according to one embodiment.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Embodiments disclosed herein use a P+/N well junction diode as program selector for a programmable resistive device. The diode can comprise P+ and N+ active regions on an N well. Since the P+ and N+ active regions and N well are readily available in standard CMOS logic processes, these devices can be formed in an efficient and cost effective manner. For standard Silicon-On-Insulator (SOI), FinFET, or similar technologies, isolated active regions can be used to construct diodes as program selectors or as programmable resistive elements. There are no additional masks or process steps to save costs. The programmable resistive device can also be included within an electronic system.

FIG. **5**(*a*) shows a block diagram of a memory cell **30** using at least a junction diode according to one embodiment. In particular, the memory cell **30** includes a resistive element **30***a* and a junction diode **30***b*. The resistive element **30***a* can be coupled between an anode of the junction diode **30***b* and a high voltage V+. A cathode of the junction diode **30***b* can be coupled to a low voltage V−. In one implementation, the memory cell **30** can be a fuse cell with the resistive element **30***a* operating as an electrical fuse. The junction diode **30***b* can serve as a program selector. The junction diode can be constructed from a P+/N well in standard CMOS processes using a P type substrate or on an isolated active region in an SOI or FinFET technologies. The P+ and N+ active regions serve as the anode and cathode of the diode are the sources or drains of CMOS devices. The N well is a CMOS well to house PMOS devices. Alternatively, the junction diode can be constructed from N+/P well in triple-well or CMOS processes using an N type substrate. The coupling of the resistive element **30***a* and the junction diode **30***b* between the supply voltages V+ and V− can be interchanged. By applying a proper voltage between V+ and V− for a proper duration of time, the resistive element **30***a* can be programmed into high or low resistance states, depending on voltage and duration, thereby programming the memory cell **30** to store a data value (e.g., bit of data). The P+ and N+ active regions of the diode can be isolated by using a dummy CMOS gate, Shallow Trench Isolation (STI) or Local Oxidation (LOCOS), or Silicide Block Layer (SBL).

Electrical fuse cell can be used as an example to illustrate the key concepts according to one embodiment. FIG. **5**(*b*) shows a cross section of a diode **32** using a P+/N well diode as program selector with Shallow Trench Isolation (STI) isolation in a programmable resistive device. P+ active region **33** and N+ active region **37**, constituting the P and N terminals of the diode **32** respectively, are sources or drains of PMOS and NMOS in standard CMOS logic processes. The N+ active region **37** is coupled to an N well **34**, which houses PMOS in standard CMOS logic processes. P substrate **35** is a P type silicon substrate. STI **36** isolates active regions for different devices. A resistive element (not shown in FIG. **5**(*b*)), such as electrical fuse, can be coupled to the P+ region **33** at one end and to a high voltage supply V+ at the other end. To program this programmable resistive device, a high voltage is applied to V+, and a low voltage or ground is applied to the N+ region **37**. As a result, a high current flows through the fuse element and the diode **32** to program the resistive device accordingly.

FIG. **5**(*c*) shows a cross section of another embodiment of a junction diode **32'** as program selector with dummy CMOS gate isolation. Shallow Trench Isolation (STI) **36'** provides isolation among active regions. An active region **31'** is defined between STI **36'**, where the N+ and P+ active regions **37'** and **33'** are further defined by a combination of a dummy CMOS gate **39'**, P+ implant layer **38'**, and N+ implant (the complement of the P+ implant **38'**), respectively, to constitute the N and P terminals of the diode **32'**. The dummy CMOS gate **39'** is a CMOS gate fabricated in standard CMOS process. The width of dummy gate **39'** is preferably close to the minimum gate width of a CMOS gate. The diode **32'** is fabricated as a PMOS-like device with **37'**, **39'**, **33'**, and **34'** as source, gate, drain, and N well, except that the source **37'** is covered by an N+ implant, rather than a P+ implant **38'**. The dummy MOS gate **39'**, preferably biased at a fixed voltage, only serves for isolation between P+ active region **33'** and N+ active region **37'** during fabrication. The N+ active **37'** is coupled to an N well **34'**, which houses PMOS in standard CMOS logic processes. P substrate **35'** is a P type silicon substrate. A resistive element (not shown in FIG. **5**(*c*)), such as electrical fuse, can be coupled to the P+ region **33'** at one end and to a high voltage supply V+ at the other end. To program this programmable resistive device, a high voltage is applied to V+, and a low voltage or ground is applied to the N+ active region **37'**. As a result, a high current flows through the fuse element and the diode **32'** to program the resistive device accordingly. This embodiment is desirable for isolation for small size and low resistance.

FIG. **5**(*d*) shows a cross section of another embodiment of a junction diode **32"** as program selector with Silicide Block Layer (SBL) isolation. FIG. **5**(*d*) is similar to **5**(*c*), except that the dummy CMOS gate **39"** in FIG. **5**(*c*) is replaced by SBL **39"** in FIG. **5**(*d*) to block a silicide grown on the top of active region **31"**. Without a dummy MOS gate or a SBL, the N+ and P+ active regions would be undesirably electrically shorted by a silicide on the surface of the active region **31"**.

FIG. **6**(*a*) shows a cross section of another embodiment of a junction diode **32"** as a program selector in Silicon-On-Insulator (SOI), FinFET, or similar technologies. In SOI technologies, the substrate **35"** is an insulator such as SiO_2 or similar material with a thin layer of silicon grown on top. All NMOS and PMOS are in active regions isolated by SiO_2 or similar material to each other and to the substrate **35"**. An active region **31"** is divided into N+ active regions **37"**, P+ active region **33"**, and bodies **34"** by a combination of a dummy CMOS gate **39"**, P+ implant **38"**, and N+ implant (the complement of P+ implant **38"**). Consequently, the N+ active regions **37"** and P+ active region **33"** constitute the N and P terminals of the junction diode **32"**. The N+ active regions **37"** and P+ active region **33"** can be the same as sources or drains of NMOS and PMOS devices, respectively, in standard CMOS processes. Similarly, the dummy CMOS gate **39"** can be the same CMOS gate fabricated in standard CMOS processes. The dummy MOS gate **39"**, which can be biased at a fixed voltage, only serves for isolation between P+ active region **33"** and N+ active region **37"** during fabrication. The width of the dummy MOS gate **39"** can vary but can, in one embodiment, be close to the minimum gate width of a CMOS gate. The N+ active regions **37"** can be coupled to a low voltage supply V−. A resistive element (not shown in FIG. **6**(*a*)), such as an electrical fuse, can be coupled to the P+ active region **33"** at one end and to a high voltage supply V+ at the other end. To program the electrical fuse cell, a high and a low voltages are applied to V+ and V−, respectively, to conduct a high current flowing through the resistive element and the junction diode **32"** to program the resistive device accordingly. Other embodiments of isolations in CMOS bulk technologies, such as dummy MOS gate, or SBL in one to four (1-4) or any sides or between cells, can be readily applied to CMOS SOI technologies accordingly.

FIG. **6**(*a***1**) shows a top view of one embodiment of a junction diode **832**, corresponding to the cross section as shown in FIG. **6**(*a*), constructed from an isolated active region as a program selector in Silicon-On-Insulator (SOI), FinFET, or similar technologies. One active region **831** is divided into N+ active regions **837**, P+ active region **833**, and bodies underneath dummy gate **839** by a combination of a dummy CMOS gate **839**, P+ implant **838**, and N+ implant (the complement of P+ implant **838**). Consequently, the N+ active regions **837** and P+ active region **833** constitute the N and P terminals of the junction diode **832**. The N+ active region **837** and P+ active region **833** can be the same as sources or drains of NMOS and PMOS devices, respectively, in standard CMOS processes. Similarly, the dummy CMOS gate **839** can be the same CMOS gate fabricated in standard CMOS processes. The dummy MOS gate **839**, which can be biased at a fixed voltage, only serves for isolation between P+ active region **833** and N+ active region **837** during fabrication. The N+ active region **837** can be coupled to a low voltage supply V−. A resistive element (not shown in FIG. **6**(*a***1**)), such as an electrical fuse, can be coupled to the P+ active region **833** at one end and to a high voltage supply V+ at the other end. To program the resistive element, high and a low voltages are applied to V+ and V−, respectively, to conduct a high current flowing through the resistive element and the junction diode **832** to program the resistive element accordingly. Other embodiments of isolations in CMOS bulk technologies, such as dummy MOS gate, or SBL in one to four (1-4) or any sides or between cells, can be readily applied to CMOS SOI technologies accordingly.

FIG. **6**(*a***2**) shows a top view of one embodiment of a diode **832'** constructed from an isolated active region as a program selector in an SOI, FinFET, or similar technologies. This embodiment is similar to that in FIG. **6**(*a***1**), except that SBL is used instead of a dummy gate for isolation. An active region **831'** is on an isolated substrate that is covered by P+ **838'** and N+ **835'** implant layers. The P+ **838'** and N+ **835'** are separated with a space D and a Silicide Block Layer (SBL) **839'** covers the space and overlap into both P+ **838'** and N+ **835'** regions. The P+ **838'** and N+ **835'** regions serve as the P and N terminals of a diode, respectively. The space regions can be doped with slightly P, N, or unintentionally doped. The space D and/or the doping level in the space regions can be used to adjust the breakdown or leakage of the diode **832'**. The diode constructed in an isolated active region can be one side, instead of two sides as is shown in FIG. **6**(*a***2**) or in another embodiment.

FIG. **6**(*a***3**) shows a top view of one embodiment of a fuse cell **932** constructed from a fuse element **931-2**, a diode **931-1** as program selector in one piece of an isolated active region, and a contact area **931-3**. These elements/regions (**931-1**, **931-2**, and **931-3**) are all isolated active regions built on the same structure to serve as a diode, fuse element, and contact area of a fuse cell **932**. The isolated active region **931-1** is divided by a CMOS dummy gate **939** into regions **933** and **937** that are further covered by P+ implant **938** and N+ implant (the complement of the P+ implant **938**) to serve as P and N terminals of the diode **931-1**. The P+ **933** is coupled to a fuse element **931-2**, which is further coupled to the contact area **931-3**. The contact area **931-3** and the contact area for cathode of the diode **931-1** can be coupled to V+ and V− supply voltage lines, respectively, through a single or plural of contacts. When high and low voltages are applied to V+ and V−, respectively, a high current can flow through the fuse element **931-2** to program the fuse into a high resistance state. In one implementation, the fuse element **931-2** can be all N or all P. In another implementation, the fuse element **931-2** can be half P and half N so that the fuse element can behave like a reverse-biased diode during read, when the silicide on top is depleted after program. If there is no silicide available, the fuse element **931-2**, which is an OTP element, can be constructed as N/P or P/N diodes for breakdown in the forward or reverse biased condition. In this embodiment, the OTP element can be coupled directly to a diode as program selector without any contacts in between. Thus, the cell area can be small and its cost can be relatively low.

FIG. **6**(*a***4**) shows a top view of one embodiment of a fuse cell **932'** constructed from a fuse element **931'-2**, a diode **931'** as program selector in one piece of an isolated active region, and a contact area **931'-3**. These elements/regions (**931'-1**, **931'-2**, and **931'-3**) are all isolated active regions built on the same structure to serve as a diode, fuse element, and contact area of a fuse cell **932'**. The isolated active region **931'-1** is divided by a Silicide Block Layer (SBL) in **939'** to regions **933'** and **937'** that are further covered by P+ implant **938'** and N+ implant **935'** to serve as P and N terminals of the diode **931'**. The P+ **933'** and N+ **937'** regions are separated with a space D, and an SBL **939'** covers the space and overlaps into both regions. The space D and/or the doping level in the space region can be used to adjust the breakdown voltage or leakage current of the diode **931'**. The P+ **933'** is coupled to a fuse element **931'-2**, which is further coupled to the contact area **931'-3**. The contact area **931'-3** and the contact area for the cathode of the diode **931'-1** can be coupled to V+ and V− supply voltage lines, respectively, through a single or plural of contacts. When high and low voltages are applied to V+ and V−, respectively, a high current can flow through the fuse element **931'-2** to program the fuse into a high resistance state. In one implementation, the fuse element **931'-2** can be all N or all P. In another implementation, the fuse element **931'-2** can be half P and half N so that the fuse element can behave like a reverse-biased diode during read, when the silicide on top is depleted after program. If there is no silicide available, the fuse element **931'-2**, which is an OTP element, can be constructed as N/P or P/N diodes for breakdown in the forward or reverse biased condition. In this embodiment, the OTP element can be coupled directly to a diode as program selector without any contacts in between. Thus, the cell area can be small and the costs can be low

FIG. **6**(*b***1**) shows a cross section of another embodiment of at least one diode **45** as program selector in FinFET technologies. FinFET refers to a fin-based, multigate transistor. FinFET technologies are similar to the conventional CMOS except that thin and tall silicon islands can be raised above the silicon substrate to serve as the bulks of CMOS devices. The bulks are divided into source, drain, and channel regions by polysilicon or non-aluminum metal gates like in the conventional CMOS. The primary difference is that the MOS devices are raised above the substrate so that channel widths are related to the height of the islands, though the direction of current flow is still in parallel to the surface. In an example of FinFET technology shown in FIG. **6**(*b***1**), the silicon substrate **35** is an epitaxial layer built on top of an insulator like SOI or a bulk silicon substrate. The silicon substrate **35** can then be etched into several tall rectangular islands **31-1**, **31-2**, and **31-3**. With proper gate oxide and field oxide grown, the islands **31-1**, **31-2**, and **31-3** can be patterned with MOS gates **39-1**, **39-2**, and **39-3**, respectively, to cover both sides of raised islands **31-1**, **31-2**, and **31-3** and to define source and drain regions. In one embodiment, the source and drain regions formed at the islands **31-1**, **31-2**, and **31-3** are then filled with silicon/SiGe called extended source/drain regions, such as **40-1** and **40-2**, so that the combined source or drain areas can be large enough to allow contacts. The extended source/drain can be fabricated from polysilicon, polycrystalline Si/SiGe, lateral epitaxial growth silicon/SiGe, or Selective Epixatial Growth (SEG) of Silicon/SiGe, etc. The extended source/drain regions **40-1** and **40-2**, or other types of isolated active regions, can be grown or deposited to the sidewall or the end of the fins. The fill **40-1** and **40-2** areas in FIG. **6**(*b***1**) are for illustrative purpose to reveal the cross section and can, for example, be filled up to the surface of the islands **31-1**, **31-2**, and **31-3**. In this embodiment, active regions **33-1,2,3** and **37-1,2,3** are covered by a P+ implant **38** and N+ implant (the complement of P+ implant **38**), respectively, rather than all covered by P+ implant **38** as PMOS in the conventional FinFET, to constitute the P and N terminals of the diode **45**. The N+ active regions **37-1,2,3** can be coupled to a low voltage supply V−. At least one resistive element (not shown in FIG. **6**(*b***1**)), such as an electrical fuse, can be coupled to the P+ active region **33-1,2,3** at one end and to a high voltage supply V+ at the other end. To program the electrical fuse, high and low voltages are applied between V+ and V−, respectively, to conduct a high current flowing through the resistive element and the diode **45** to program the resistive device accordingly. Other embodiments of isolations in CMOS bulk technologies, such as STI, dummy MOS gate or SBL, can be readily applied to FinFET technologies accordingly. The three fins **31-1**, **31-2**, and **31-3** can be constructed as 1 to 3 diodes as program selector(s). The diodes as a program selector can be constructed from any number of fins in other embodiment. There can be a plurality of dummy MOS gates across one fin to create more diodes per fin in another embodiment. If there are two dummy MOS gates across one fin and two fins are used to construct a program selector in a programmable resistive cell, the program selector can be four times the driving capabilities of a single diode.

FIG. **6**(*b***2**) shows a 3D view of two diodes **45'** as program selectors in two fin structures and one common contact, according to one embodiment. Two fins, **31'-1** and **31'-2**, are built on a substrate **35'** inside an N well **36'** with P+ implants **38'-1** and **38'-2** covering the fins **31'-1** and **31'-2**, respectively. After the fins are fabricated, a layer of dielectric **33'** covers the two fins **31'-1** and **31'-2** to provide insulation for building further upper layers of interconnects. A contact hole **34'** can be built by etching the dielectric layer **33'** into the substrate **35'**, and implanted with an N+ dopant. Then, the contact **34'** can be filled with at least one conductive material (i.e., silicon, polysilicon, SiGe, or metal) to act as an N well tap. The P+ regions **31'-1** and **31'-2** serve as the anodes of two diodes, while the contact **34'** with an N+ region on the substrate serves as a common cathode. In this embodiment, a diode can be created in only one fin pitch. The P+ regions **31'-1** and/or **31'-2** can be built with dummy gates as shown in FIG. **6**(*b***1**) to further increase the diodes' performance.

FIG. **6**(*b***3**) shows a 3D view of two diodes **45"** as program selectors in three fin structures, according to yet another embodiment. Two fins, **31"-1** and **31"-3**, are built on a substrate **35"** inside an N well **36"** with P+ implants **38"-1** and **38"-2** covering the fins **31"-1** and **31"-3**, respectively. The P+ region **31"-1** and **31"-3** serve as the anodes of two diodes, while the N+ region **31"-2** serves as the common cathode. In this embodiment, a diode can be created in only one and a half fin pitch. The N+ region **31"-2** can be placed between any number of P+ regions to serve as a common cathode in other embodiment. The P+ regions **31"-1** and/or **31"-2** can be built with dummy gates as shown in FIG. **6**(*b***1**) to further increase the diodes' performance.

FIG. **6**(*b***4**) shows a 3D view of one diode **45"** as a program selector in two fin structures, according to yet another embodiment. Two fins, **31'"-1** and **31'"-2**, are built on a substrate **35'"** inside an N well **36'"** with a P+ implant **38'"** and an N+ implant **37'"** covering the fins **31'"-1** and **31'"-2**, respectively. The P+ region **31'"-1** serves as the anodes of the diode **45'"**, while the N+ region **31'"-2** serves as the cathode. In this embodiment, a diode can be created in two fin pitches. The P+ region **31'"-1** can be built with dummy gates as shown in FIG. **6**(*b***1**) to further increase the diodes' performance.

FIG. **6**(*c***1**) shows a programmable resistive device cell **75** for low voltage and low power applications. If an I/O voltage supply of a chip is down to 1.2V, the diode's high turn-on voltage 0.7V as read/program selector can hurt the read margin. Therefore, a MOS can be used as read selector in the cell for better read operations in another embodiment. The programmable resistive cell **75** has a programmable resistive element **76**, a diode **77** as program selector, and a MOS **72** as read selector. The anode of the diode **77** (node N) is coupled to the drain of the MOS **72**. The cathode of the diode **77** is coupled to the source of the MOS **72** as Select line (SL). The programmable resistive element **76** is coupled between node N and a high voltage V+. By applying a proper voltage between V+ and SL for a proper duration of time, the programmable resistive element **76** can be programmed into high or low resistance states, depending on voltage/current and duration. The diode **77** can be a junction diode constructed from a P+ active region on N well and an N+ active region on the same N well as the P and N terminals of a diode, respectively. In another embodiment, the diode **77** can be a diode constructed from a polysilicon structure with two ends implanted by P+ and N+, respectively. The P or N terminal of either junction diode or polysilicon diode can be implanted by the same source or drain implant in CMOS devices. Either the junction diode or polysilicon diode can be built in standard CMOS processes without any additional masks or process steps.

The MOS **72** is for reading the programmable resistive element **76**. Turning on a MOS in linear mode can have a lower voltage drop than a diode's for low voltage operations. To turn on the diode **77**, the cathode of the diode can be set to low for the selected row during write, i.e., ~(Wr*Sel) in one embodiment. To turn on the MOS **72**, the gate of the MOS can be set to low for the selected row during read, i.e., ~(Rd*Sel) in one embodiment. If the program voltage is VDDP=2.5V and core voltage for read is VDD=1.0V, the selected and unselected SLs for program can be 0 and 2.5V, respectively. The SLs can be all set to 1.0V for read. The selected and unselected WLBs for read can be 0 and 1.0V, respectively. The programmable resistive memory cell **75** can be organized as a two-dimensional array with all V+'s in the same columns coupled together as bitlines (BLs) and all MOS gates and sources in the same rows coupled together as wordline bars (WLBs) and Source Lines (SLs), respectively.

FIG. **6**(*c***2**) shows a schematic of another programmable resistive cell according to another embodiment. FIG. **6**(*c***2**) is similar to FIG. **6**(*c***1**) except that the placement of the resistive element and diode/MOS are interchanged. V+'s of the cells in the same row can be coupled to a source line (SL) that can be set to VDDP for program and VDD for read. V−'s of the cells in the same column can be coupled as a bitline (BL) and further coupled to a sense amplifier for read and set to ground for program. The gates of the MOS in the same row can be coupled to a wordline bar (WLB) that can be set to low when selected during read, i.e., ~(Rd*Sel), in one embodiment. Alternatively, the source of the MOS can be coupled to a fixed voltage, such as Vdd, in another embodiment.

FIG. **6**(*c***3**) shows a schematic of another programmable resistive cell according to another embodiment. FIG. **6**(*c***3**) is similar to FIG. **6**(*c***1**) except that the PMOS is replaced by an NMOS. V+'s of the cells in the same column can be coupled as a bitline (BL) that can be coupled to VDDP for program and coupled to a sense amplifier for read. The cathodes of the diode and the sources of the MOS in the same row can be coupled as a source line (SL). The SL can be set to ground when selected for read or program. The gates of the MOS in the same row can be coupled as a wordline (WL) that can be set high when selected for read, i.e., Rd*Sel, in one embodiment. Alternatively, the source of the MOS can be coupled to a fixed voltage, such as ground, in another embodiment.

FIGS. **6**(*a*), **6**(*a***1**)-**6**(*a***4**), **6**(*b***1**)-**6**(*b***4**), and **6**(*c***1**)-**6**(*c***3**) shows various schemes of constructing diodes as program selector and/or OTP element in a fully or partially isolated active region. A diode as program selector can be constructed from an isolated active region such as in SOI or FINFET technologies. The isolated active region can be used to construct a diode with two ends implanted with P+ and N+, the same implants as the source/drain implants of CMOS devices, to serve as two terminals of a diode. A dummy CMOS gate or silicide block layer (SBL) can be used for isolation and to prevent shorting of the two terminals. In the SBL isolation, the SBL layer can overlap into the

N+ and P+ implant regions and the N+ and P+ implant regions can be separated with a space. The width and/or the doping level in the space region can be used to adjust the diode's breakdown voltage or leakage current accordingly. A fuse as OTP element can also be constructed from an isolated active region. Since the OTP element is thermally isolated, the heat generated during programming cannot be dissipated easily so that the temperature can be raised higher to accelerate programming. The OTP element can have all N+ or all P+ implant. If there is a silicide on top of the active region, the OTP element can have part N+ and part P+ implants so that the OTP element can behave like a reverse biased diode during read, such as when the silicide is depleted after OTP programming in one embodiment. If there is no silicide on top, the OTP element can have part N+ and part P+ implants as a diode to be breakdown during OTP programming in another embodiment. In either case, the OTP element or diode can be constructed on the same structure of an isolated active region to save area. In an SOI or FinFET SOI technology, an active region can be fully isolated from the substrate and from other active regions by SiO2 or similar material. Similarly, in a FINFET bulk technology, an active region can be fully isolated from the substrate and partially isolated from each other by using extended source/drain regions coupled between fin structures without any additional masks.

FIG. **7**(*a*) shows a top view of an electrical fuse element **88** according to one embodiment. The electrical fuse element **88** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **88** includes an anode **89**, a cathode **80**, and a body **81**. In this embodiment, the electrical fuse element **88** is a bar shape with a small anode **89** and cathode **80** to reduce area. In another embodiment, the width of the body **81** can be about the same as the width of cathode or anode. The width of the body **81** can be very close to the minimum feature width of the interconnect. The anode **89** and cathode **80** may protrude from the body **81** to make contacts. The contact number can be one (1) for both the anode **89** and the cathode **80** so that the area can be very small. However, the contact area for anode **89** is often made larger so that the anode **89** can resist electro-migration more than the cathode **80**. In one embodiment, the fuse body **81** can have about 0.5-8 squares, namely, the length to width ratio is about 0.5-to-8, to make efficient use of (e.g., optimize) cell area and program current. In one embodiment, the fuse body **81** can have about 2-6 squares, namely, the length to width ratio is about 2-to-6, to efficiently utilize cell area and program current. In yet another embodiment, the narrow fuse body **81** can be bent to make the length longer between the wide anode and cathode areas to efficiently utilize cell area and program current. The fuse element **88** has a P+ implant **82** covering part of the body **81** and the cathode **80**, while an N+ implant over the rest of area. This embodiment makes the fuse element **88** behave like a reverse biased diode to increase resistance after being programmed, such as when silicide on top is depleted by electro-migration, ion diffusion, silicide decomposition, and other effects. It is desirable to make the program voltage compatible with the I/O voltages, such as 3.3V, 2.5V, or 1.8V, for ease of use without the needs of building charge pumps. The program voltage pin can also be shared with at least one of the standard I/O supply voltage pins. In one embodiment, to make the cell small while reducing the contact resistance in the overall conduction path, the number of contacts in the OTP element or diode can be no more than two (<=2), in a single cell. Similarly, in another embodiment, the contact size of the OTP element or diode can be larger than at least one contact outside of the memory array. The contact enclosure can be smaller than at least one contact enclosure outside of the memory array in yet another embodiment.

FIG. **7**(*a***1**) shows a top view of an electrical fuse structure **88'** with a small body **81'-1** and at least one slightly tapered structures **81'-2** and/or **81'-3** according to another embodiment. The electrical fuse element **88'** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **88'** includes an anode **89'**, a cathode **80'**, body **81'-1**, and tapered structures **81'-2** and **81'-3**. The body **81'-1** can include a small rectangular structure coupled to at least one tapered structures **81'-2** and/or **81'-3**, which are further coupled to cathode **80'** and anode **89'**, respectively. The length (L) and width (W) ratio of the body **81'-1** is typically between 0.5 and 8. In this embodiment, the electrical fuse element **88'** is substantially a bar shape with a small anode **89'** and cathode **80'** to reduce area. The anode **89'** and cathode **80'** may protrude from the body **81-1'** to make contacts. The contact number can be one (1) for both the anode **89'** and the cathode **80'** so that the area can be very small. The contact can be larger than at least one contact outside of the memory array in another embodiment. The contact enclosure can be smaller than at least one contact enclosure outside of the memory array in yet another embodiment. P+ implant layer **82'** covers part of the body and N+ implant layer (the complement of P+) covers the other part so that the body **81'-1** and taped structure **81'-2** can behave like a reverse biased diode to enhance resistance ratio during read, such as when silicide on top is depleted after program.

FIG. **7**(*a***2**) shows a top view of an electrical fuse element **88"** according to another embodiment. The electrical fuse element **88"** is similar to the one shown in FIG. **7**(*a*) except using a thermally conductive but electrically insulated heat sink coupled to the anode. The electrical fuse element **88"** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **88"** can include an anode **89"**, a cathode **80"**, a body **81"**, and an N+ active region **83"**. The N+ active region **83"** on a P type substrate is coupled to the anode **89"** through a metal **84"**. In this embodiment, the N+ active region **83"** is electrically insulated from the conduction path (i.e., N+/P sub diode is reverse biased), but thermally conductive to the P substrate, and can serve as a heat sink. In other embodiment, the heat sink can be coupled to the anode **89"** directly without using any metal or interconnect, and can be close to or underneath the anode. The heat sink can also be coupled to the body, cathode, or anode in part or all of the fuse element in other embodiments. This embodiment of heat sink can create a steep temperature gradient to accelerate programming.

FIG. **7**(*a***3**) shows a top view of an electrical fuse element **88'"** according to another embodiment. The electrical fuse element **88'"** is similar to the one shown in FIG. **7**(*a*) except a thinner oxide region **83"** which serves as a heat sink underneath the body **81"** and near the anode **89'"**. The electrical fuse element **88'"** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **88'"** includes an anode **89'"**, a cathode **80'"**, a body **81'"**, and an active region **83'"** near the anode **89'"**. The active region **83'"** underneath the fuse element **81'"** makes the oxide thinner in the area than the other (i.e., thin gate oxide instead of thick STI oxide). The thinner oxide above the active region **83'"** can dissipate heat faster to create a temperature gradient to accelerate programming. In other embodiments, the thin oxide area **83'''** can be placed underneath the cathode, body, or anode in part or all of a fuse element as a heat sink.

FIG. **7**(*a***3***a*) shows a top view of an electrical fuse element **198** according to another embodiment. The electrical fuse element **198** is similar to the one shown in FIG. **7**(*a*) except thinner oxide regions **193** are placed in two sides of the anode **199** as another form of heat sink. The electrical fuse element **198** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **198** includes an anode **199**, a cathode **190**, a body **191**, and an active region **193** near the anode **199**. The active region **193** underneath the anode **199** makes the oxide thinner in the area than the other (i.e., thin gate oxide instead of thick STI oxide). The thinner oxide above the active region **193** can dissipate heat faster to create a temperature gradient to accelerate programming. In other embodiment, the thin oxide area can be placed underneath the cathode, body, or anode in part or in all of a fuse element as a heat sink in one side, two sides, or any sides.

FIG. **7**(*a***3***b*) shows a top view of an electrical fuse element **198'** according to another embodiment. The electrical fuse element **198'** is similar to the one shown in FIG. **7**(*a*) except thinner oxide regions **193'** are placed close to the anode **199'** as another form of heat sink. The electrical fuse element **198'** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **198'** includes an anode **199'**, a cathode **190'**, a body **191'**, and an active region **193'** near the anode **199'**. The active region **193'** close to the anode **199'** of the fuse element **198'** makes the oxide thinner in the area than the other (i.e., thin gate oxide instead of thick STI oxide) and can dissipate heat faster to create a temperature gradient to accelerate programming. In other embodiment, the thin oxide area can be placed near to the cathode, body, or anode of a fuse element in one, two, three, four, or any sides to dissipate heat faster. In other embodiment, there can be at least one substrate contact coupled to an active region, such as **193'**, to prevent latch-up. The contact pillar and/or the metal above the substrate contact can also serve as another form of heat sink.

FIG. **7**(*a***3***c*) shows a top view of an electrical fuse element **198"** according to yet another embodiment. The electrical fuse element **198"** is similar to the one shown in FIG. **7**(*a*) except an extended anode region **195"** which serves as heat sink. The electrical fuse element **198"** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **198"** includes an anode **199"**, a cathode **190"**, a body **191"**, and an extended anode region **195"**. The extended anode region **195"** can dissipate heat faster than an anode with a single contact area only and without extended region. In one embodiment, the extended anode area can be only one side, instead of two sides to fit into small cell space, and/or the length can be longer or shorter. In another embodiment, the extended area can be a portion of a cathode with one side or two sides. In yet another embodiment, a part or all of the cathode, body, or anode of a fuse element can be made larger, or coupled to a single or plural of conductors (i.e., polysilicon, metal, or active region) near by or in contact as heat sink(s) to dissipate heat faster. The extended area means there is no current flowing through but providing more surfaces or areas to increase thermal conductivity.

FIG. **7**(*a***3***d*) shows a top view of an electrical fuse element **198'''** according to yet another embodiment. The electrical fuse element **198'''** is similar to the one shown in FIG. **7**(*a*) except a heater **195'''** is created near the cathode. The electrical fuse element **198'''** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **198'''** includes an anode **199'''**, a cathode **190'''**, a body **191'''**, and high resistance area **195'''** which can serve as a heater. The high resistance area **195'''** can generate more heat to assist programming the fuse element. In one embodiment, the heater can be an unsilicided polysilicon or unsilicided active region with a higher resistance than the silicided polysilicon or silicided active region, respectively. In another embodiment, the heater can be a single or a plurality of contact and/or via in serial to contribute more resistance and generate more heat along the programming path. In yet another embodiment, the heater can be a portion of high resistance interconnect to provide more heat to assist programming. The heater **195''''** can be place to the cathode, anode, or body, in part or all of the fuse element.

A heat sink can be used to create a temperature gradient to accelerating programming. The heat sink as shown in FIGS. **7**(*a***2**), **7**(*a***3**), **7**(*a***3***a*), **7**(*a***3***b*), and **7**(*a***3***c*) are for illustrative purposes. A heat sink can be a thin oxide area placed near or underneath the anode, body, or cathode of a fuse element in one, two, three, four, or any sides to dissipate heat faster. A heat sink can be an extended area of the anode, body, or cathode of a fuse element to increase heat dissipation area without current flowing through. A heat sink can also be a single or a plurality of conductors coupled to (i.e., in contact or in proximity) the anode, body, or cathode of a fuse element to dissipate heat faster. A heat sink can also be a large area of anode or cathode with more than one contact to increase heat dissipation area. A heat sink can also be a contact pillar built above an active region near the cathode, body, or anode of the fuse element to prevent latch-up and can also dissipate heat faster. In an OTP cell that has a shared contact, i.e., using a metal to interconnect MOS gate and active region in a single contact, can be considered as another kind of heat sink for MOS gate to dissipate heat into the active region faster. With heat sink, the thermal conduction of a fuse element can be increased from 20% to 200% in some embodiments. Similarly, a heat generator can be used to create more heat to assist programming the fuse element. A heater can usually be a high resistance area placed to or near the cathode, body, or anode in part or all of the fuse element to generate more heat. A heater can be embodied as a single or a plurality of unsilicided polysilicon, unsilicided active region, a single or a plurality of contact, via, or combined in serial, or a single or a plurality of segment of high resistance interconnect in the programming path. The resistance of the heat generator can be from 8Ω to 200Ω, or more desirably from 20Ω to 100Ω, in some embodiments. The fuse element with heat sink or heater can be an interconnect made of polysilicon, silicided polysilicon, silicide, polymetal, metal, metal alloy, metal gate, local interconnect, metal-0, thermally isolated active region, or CMOS gate, etc. There are many variations and yet equivalent embodiments of heat sinks to dissipate heat and/or heaters to provide more heat to assist programming and that they are all within the scope of this invention.

FIG. **7**(*a***4**) shows a top view of an electrical fuse element **98'** according to another embodiment. The electrical fuse element **98'** is similar to the one shown in FIG. **7**(*a*) except the fuse element has at least one notch in the body to assist programming. More generally, a target portion of the body **91'** can be made formed with less area (e.g., thinner), such as a notch. The electrical fuse element **98'** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **98'** can include an anode **99'**, a cathode **90'**, and a body **91'**. The body **91'** has at least a notch **95'** so that the fuse element can be easily broken during programming. The notch can be embodied as a single or plural of narrow regions in other embodiments.

FIG. **7**(*a***5**) shows a top view of an electrical fuse element **98"** according to another embodiment. The electrical fuse element **98"** is similar to the one shown in FIG. **7**(*a*) except the fuse element is part NMOS and part PMOS metal gates. The electrical fuse element **98"** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The electrical fuse element **98"** can include an anode **99"**, a cathode **90"**, and bodies **91"** and **93"** fabricated from at least one segment of PMOS and NMOS metal gates, respectively. By using different types of metals in the same fuse element, the thermal expansion can create a large stress to rupture the fuse when the temperature is raised during programming. The PMOS and NMOS metal gates can be interchangeable between the cathode and anode in other embodiments.

FIG. **7**(*a***6**) shows a top view of an OTP element **888** according to another embodiment. The OTP element **888** is similar to the one shown in FIG. **7**(*a*) except the OTP element is built with a polysilicon between metal gates. The OTP element **888** can, for example, be used as the resistive element **31***a* illustrated in FIG. **5**(*a*). The OTP element **888** can include an NMOS metal gate as anode **889**, a PMOS metal gate as cathode **891**, and a polysilicon as body **881**. In a gate-last or Replacement Metal Gate (RMG) process, polysilicon can be provided and used as place holders for CMOS gates. After high temperature cycles of silicidation and source/drain annealing, the polysilicon gates are etched and replaced by metal gates. Different types of metals can be used for NMOS and PMOS metal gates to suite NMOS/PMOS threshold voltage requirements. Since use of polysilicon as gates or interconnects are available before being replaced by metal gates, a portion of polysilicon can be preserved by modifying the layout database with layout logic operations. For example, the N+ and P+ implant layers with N well can be used to define NMOS and PMOS in the conventional CMOS. The N+ and P+ layers can be modified with mask logic operations as N'+ layer **835** and P'+ layer **838** so that a segment of polysilicon **881** can be preserved. The polysilicon as an OTP body **881** can be implanted by NLDD, PLDD, N+ source/drain, P+ source/drain, or threshold voltage adjust implants with minimum masks increment, if any. The polysilicon **881** can be all N, all P, or part N and part P. The OTP element can be breakdown by high voltage or high current. In one embodiment, the polysilicon body can be between the same NMOS or PMOS metal gates. In another embodiment, the polysilicon body is coupled to neither NMOS nor PMOS metal gate.

FIG. **7**(*a***7**) shows a top view of a diode **888'** according to another embodiment. The diode **888'** is similar to the OTP element **888** shown in FIG. **7**(*a***6**) except the OTP body is further divided into N type and P type regions to act as a diode. The diode **888'** can, for example, be used as the resistive element **31***a* or program selector **31***b* illustrated in FIG. **5**(*a*). The diode **888'** includes an NMOS metal gate **889'** and a PMOS metal gate **891'** as interconnect, and a polysilicon **881'** as body. The polysilicon body can be created by blocking at least one portion of NMOS or PMOS metal gate, or both. The polysilicon body **881'** is further divided into three regions **881'-1**, **881'-3**, and **881'-2**, covered by modified NLDD' layer **845'**, modified PLDD' layer **848'**, and none, respectively. The layers **845'** and **848'** can be generated from NLDD and PLDD layers with mask logic operations so that the areas **881'-1** and **881'-3** can receive NLDD and PLDD implants, respectively. The NLDD' **845'** and PLDD' **848'** can be separated with a space D. The doping concentration in the space region can be slightly N or P, or unintentionally doped. The width of the space and/or the doping level in the space region can be used to adjust the diode's breakdown or leakage current. A silicide block layer (SBL) **885'** can cover the space and overlap into both regions. The SBL **885'** can be used to block silicide formation to prevent the bodies **881'-1** and **881'-3** from being shorts in one embodiment. The bodies **881'-1** and **881'-3** are coupled to NMOS metal gate **889'** and PMOS metal gate **891'**, respectively, which serve as the N and P terminals of the polysilicon diode. The diode can be used as an OTP element by junction breakdown under forward or reverse bias, or can be used as program selector. The NLDD or PLDD layer in the above discussions is for illustrative purposes. Any layers such as N+, P+, NLDD, PLDD, high-Resistance, or Vt-adjust implants can be used to construct a polysilicon diode with minimum masks increment. The diode **888'** can be placed between metal gates of same kind or different kind in different order in other embodiments.

FIG. **7**(*a***8**) shows a 3D view of a metal fuse element **910** having two ends A and B, constructed from a contact **911** and a segment of metal-1 **912** according to one embodiment. The metal fuse element **910** has one end A coupled to a contact **911**, which is coupled to a segment of metal-1 **912**. The other end of the metal-1 **912** is the end B of the metal fuse element **910**. When a high current flows through the metal fuse element **910**, the high contact resistance (i.e., 60 ohm in 28 nm CMOS, for example) can generate additional Joule heat, to supplement the metal Joule heat, to assist programming the metal-1 **912**.

FIG. **7**(*a***9**) shows a 3D view of another metal fuse element **920** having two ends A and B, constructed from a contact **921**, two vias **923** and **925**, and segment(s) of metal-1 and metal-2. The metal fuse element **920** has one end A coupled to a contact **921**, which is further coupled to a metal-2 **924** through a metal-1 **922** and a via **923**. The metal-2 **924** is coupled to another metal-1 **926** through another via **925**. The other end of the metal-1 **926** is the end B of the metal fuse element **920**. The contact **921** and vias **922** and **925** can generate additional heat to assist programming the metal-1 **926**. For example, in an advanced MOS technologies such as 28 nm, a contact resistance can be 60 ohm and a via resistance can be 10 ohm. By building up contacts and vias in series, the resistance in the programming path can be increased substantially to generate more Joule heat for programming metal-1 **926**, to supplement the metal Joule heating alone.

FIG. **7**(*a***10**) shows a 3D view of yet another metal fuse element **930** having two ends A and B, constructed from three contacts, one metal gate, and two segments of metal-1. The metal fuse element **930** has one end A coupled to a contact **931**, which is further coupled to a metal gate **934** through a metal-1 **932** and another contact **933**. The metal gate **934** is coupled to anther metal-1 **936** through another contact **935**. The other end of the metal-1 **936** is the end B of the metal fuse element **930**. There are three contacts to generate more heat, i.e., 180 ohm if each contact has 60 ohm, for programming the metal-1 **926**, to supplement the metal Joule heat alone. This embodiment is more suitable when the metal gate is harder to program than the metal-1.

The embodiments in FIGS. **7**(*a***8**), **7**(*a***9**), and **7**(*a***10**) are suitable for those interconnect fuses that have low resistivity, i.e., metal or some kinds of local interconnect that has sheet resistance of 0.1-0.5 ohm/sq, for example. By building up a plurality of contacts, vias, or combined in series, more heat can be generated to raise the temperature to assist programming. These embodiments can be applied to any kinds of metals, such as metal gate, local interconnect, metal-1, metal-2, etc. These embodiments can also be applied to any kind or any number of contacts, via1 (between metal-1 and metal-2), or via2 (between metal-2 and metal-3), etc. It is more desirable to keep metal to be programmed long (i.e., length/width>20) and the jumpers such as the other metals, metal gate, or local interconnect short (i.e., length/width<5) so that high temperature can occur in the metal to be programmed. The long metal line can be serpentine to fit into small area. Using jumpers and contacts/vias can be more than one set to further increase the resistance and raise the temperature. There can be many variations of equivalent embodiments in using contacts, vias, or combined to assist programming metal fuses. For example, the metal to be programmed can be metal gate, local interconnect, metal-1, metal-2, metal-3, or metal-4, etc. The via can be any types of via, such as via2 between metal-2 and metal-3. The number of via or contact can be any, or none. The directions of current flow can be downstream or upstream, i.e., current flows from metal-2 to metal-1 or from metal-1 to metal-2. It is more desirable for the end A coupled to a diode as program selector with no more than two contacts, and for the end B coupled to wider metals with more vias. Those skilled in the art understand that there are many equivalent embodiments of the metal fuses using heat generated from contact or via to assist programming and that are still within the scope of this invention.

The OTP elements shown in FIGS. **7**(*a*), **7**(*a***1**)-**7**(*a***10**) are only to illustrate certain embodiments. As denoted, the OTP elements can be built from any interconnects, including but not limited to polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, metal-0, metal, metal alloy, thermally isolative active region, CMOS gate, or combinations thereof. The OTP elements can be N type, P type, or part N and part P type. Each of the OTP elements can have an anode, a cathode, and at least one body. The anode or cathode contacts can be no more than 2 for polysilicon/local interconnect/metal-0, and can be no more than 4 for metal fuse, preferably. The contact size can be larger than at least one contact outside of the OTP memory array. The contact enclosure can be smaller than at least one contact enclosure outside of the OTP memory array to lower the electromigration threshold. The length to width ratio in the body can be between 0.5-8 for polysilicon/local interconnect/metal-0, or 2-6 more desirably, or in the case of metal-0/metal even larger than 10, for example. There are many variations or combinations of embodiments in part or all that can be considered equivalent embodiments.

Polysilicon used to define CMOS gates or as interconnect in a high-K/metal-gate CMOS process can also be used as OTP elements. The fuse element can be P type, N type, or part N and part P type if applicable. Particularly, the after/before resistance ratio can be enhanced for those fuse elements that have P+ and N+ implants to create a diode after being programmed, such as polysilicon, thermally isolated active region, or gate of a high-K/metal-gate CMOS. For example, if a metal-gate CMOS has a sandwich structure of polysilicon between metal alloy layers, the metal alloy layers may be blocked by masks generated from layout database to create a diode in the fuse elements. In SOI or SOI-like processes, a fuse element can also be constructed from a thermally isolated active region such that the fuse element can be implanted with N+, P+, or part N+ and part P+ in each end of the active region. If a fuse element is partly implanted with N+ and P+, the fuse element can behave like a reverse-biased diode, such as when silicide on top is depleted after being programmed. In one embodiment, if there is no silicide on top of active regions, an OTP element can also be constructed from an isolated active region with part N+ and part P+ to act as a diode for breakdown in forward or reverse biased conditions. Using isolated active region to construct an OTP element, the OTP element can be merged with part of the program-selector diode in one single active island to save area.

In some processing technologies that can offer Local Interconnect, local interconnect can be used as part or all of an OTP element. Local interconnect, can also be called as metal-0 (MO) in advanced CMOS nodes, has a capability to interconnect polysilicon or MOS gate with an active region directly. In advanced MOS technologies beyond 28 nm, the scaling along the silicon surface dimensions is much faster than scaling in the height. As a consequence, the aspect ratio of CMOS gate height to the channel length is very large such that making contacts between metal 1 and source/drain or CMOS gate very difficult in terms of device area, performance, and cost. Local interconnect can be used as an intermediate interconnect between source/drain to CMOS gate, between CMOS gate to metal1, or between source/drain to metal1 in one or two levels The local interconnects, metal-0, CMOS gate, or combination can be used as an OTP element in one embodiment. The OTP element and one terminal of the program-selector diode can be connected directly through local interconnect without needing any contacts to save area in another embodiment.

Those skilled in the art understand that the above discussions are for illustration purposes and that there are many variations and equivalents in constructing electrical fuse, anti-fuse elements, or program selectors in CMOS processes,

FIGS. **7**(*b*), **7**(*c*), **7**(*d*), **7**(*e*), **7**(*f*), **7**(*g*) and **7**(*h*) show top views of P+ on N well diodes constructed with different embodiments of isolation and fuse elements. Without isolation, P+ and N+ active regions would be shorted together by silicide grown on top. The isolation can be provided by STI, dummy CMOS gate, SBL, or some combination thereof from one to four (1-4) or any sides or between cells. The P+ and N+ active regions that act as P and N terminals of the diodes are sources or drains of CMOS devices. Both the P+ and N+ active regions reside in an N well, which is the same N well that can be used to house PMOS in standard CMOS processes. The N+ active region of the diodes in multiple cells can be shared, though for simplicity FIGS. **7**(*b*)-**7**(*h*) show only one N+ active region for one P+ active region.

FIG. **7**(*b*) shows a top view of one embodiment of an electrical fuse cell **40** including a P+/N well diode having active regions **43** and **44** with STI **49** isolation in four sides. A fuse element **42** is coupled to the active region **43** through a metal **46**. The active regions **43** and **44** are covered by a P+ implant **47** and N+ implant (the complement of P+ implant **47**), respectively, to constitute the P and N terminals of the diode **40**. The active regions **43** and **44** of the diode **40** reside in an N well **45**, the same N well can be used to house PMOS in standard CMOS processes. In this embodiment, the P+ active region **43** and N+ active region **44** are surrounded by an STI **49** in four (4) sides. Since the STI **49** is much deeper than either the N+ or P+ active region, the resistance of the diode **40** between the P+ active region **43** and N+ active region **44** is high.

FIG. **7**(*c*) shows a top view of another embodiment of an electrical fuse cell **50** including a P+/N well diode having active regions **53** and **54** with an STI **59** isolation in two sides and a dummy MOS gate **58** in another two sides. An active region **51** with two STI slots **59** in the right and left is divided into a peripheral **54** and a central **53** regions by two MOS gates **58** on top and bottom. The dummy MOS gate **58** is preferably biased to a fixed voltage. The central active region **53** is covered by a P+ implant **57**, while the peripheral active region **54** is covered by an N+ implant layer (the complement of the P+ implant), which constitute the P and N terminals of the diode **50**. The active region **51** resides in an N well **55**, the same N well can be used to house PMOS in standard CMOS processes. A fuse element **52** is coupled to the P+ active region **53**. In this embodiment, the P+ active region **53** and N+ active region **54** are surrounded by STI **59** in left and right sides and the dummy MOS gate **58** on top and bottom. The isolation provided by the dummy MOS gate **58** can have lower resistance than the STI isolation, because the space between the P+ active region **53** and N+ active region **54** may be narrower and there is no oxide to block the current path underneath the silicon surface.

FIG. **7**(*d*) shows a top view of yet another embodiment of an electrical fuse cell **60** including a P+/N well diode with dummy MOS gate **68** providing isolation in four sides. An active region **61** is divided into a center active region **63** and a peripheral active region **64** by a ring-shape MOS gate **68**. The center active region **63** is covered by a P+ implant **67** and the peripheral active region **64** is covered by an N+ implant (the complement of the P+ implant **67**), respectively, to constitute the P and N terminals of the diode **60**. The active region **61** resides in an N well, the same N well can be used to house PMOS in standard CMOS processes. A fuse element **62** is coupled to the P+ active region **63** through a metal **66**. The dummy MOS gate **68**, which can be biased at a fixed voltage, provides isolation between P+ active region **63** and N+ active region **64** regions on four sides. This embodiment offers low resistance between P and N terminals of the diode **60**.

FIG. **7**(*e*) shows a top view of yet another embodiment of an electrical fuse cell **60'** including a P+/N well diode having active regions **63'** and **64'** with Silicide Block Layer (SBL) **68'** providing isolation in four sides. An active region **61'** is divided into a center active region **63'** and a peripheral active region **64'** by an SBL ring **68'**. The center active region **63'** and the peripheral active region **64'** are covered by a P+ implant **67'** and an N+ implant (the complement of P+ implant **67'**), respectively, to constitute the P and N terminals of the diode **60'**. The boundaries between the P+ implant **67'** and N+ implants are about in the middle of the SBL ring **68'**. The active region **61'** resides in an N well **65'**. A fuse element **62'** is coupled to the P+ active region **63'** through a metal **66'**. The SBL ring **68'** blocks silicide formation on the top of the active regions between P+ active region **63'** and N+ active region **64'**. In this embodiment, the P+ active region **63'** and N+ active region **64'** are isolated in four sides by P/N junctions. This embodiment has low resistance between the P and N terminals of the diode **60'**, though the SBL may be wider than a MOS gate. In another embodiment, there is a space between the P+ implant **67'** and the N+ implant that is covered by the SBL ring **68'**.

FIG. **7**(*f*) shows a top view of another embodiment of an electrical fuse cell **70** having a P+/N well diode with an abutted contact. Active regions **73** and **74**, which are isolated by an STI **79**, are covered by a P+ implant **77** and an N+ implant (the complement of the P+ implant **77**), respectively, to constitute the P and N terminals of the diode **70**. Both of the active regions **73** and **74** reside in an N well **75**, the same N well can be used to house PMOS in standard CMOS processes. A fuse element **72** is coupled to the P+ active region **73** through a metal **76** in a single contact **71**. This contact **71** is quite different from the contacts in FIG. **7**(*b*), (*c*), (*d*), and (*e*) where a contact can be used to connect a fuse element with a metal and then another contact is used to connect the metal with a P+ active region. By connecting a fuse element directly to an active region through a metal in a single contact, the cell area can be reduced substantially. The abutted contact can be larger than a regular contact and, more particularly, can be a large rectangular contact that has about twice the area of a regular contact in a CMOS process. This embodiment for a fuse element can be constructed by a CMOS gate, including polysilicon, silicided polysilicon, or non-aluminum metal CMOS gate, that allows an abutted contact.

FIG. **7**(*g*) shows a top view of yet another embodiment of fuse cells **70'** with a central cell **79'** and a portion of left/right cells. The central cell **79'** includes an electrical fuse element **72'** and a diode as program selector. An active region **71'** is divided into upper active regions **73'**, **73"**, and **73"** and a lower active region **74'** by a U-shape dummy MOS gate **78'**. The upper active regions **73'**, **73"**, and **73"** are covered by a P+ implant **77'** while the rest of lower active region **74'** is covered by an N+ implant (the complement of the P+ implant **77'**). The active region **73'** and **74'** constitute the P and N terminals of the diode in the central cell **79'**. The active region **73"** serves as a P terminal of a diode in the left cell, while the active region **73"** serves as a P terminal of a diode in the right cell. The polysilicon **78'** isolates the P+/N+ of the diode in the central cell **79'** and also isolates the P+ terminals of the left, central, and right cells by tying the polyslicion **78'** to a high voltage (i.e., V+ in FIG. **5**(*a*)). The polysilicon **78'** can be a dummy MOS gate fabricated in standard CMOS processes. The active region **71'** resides in an N well, the same N well that can be used to house PMOS in standard CMOS processes. A fuse element **72'** is coupled to the P+ active region **73'** through a metal **76'** in the central cell **79'**. This embodiment can offer low resistance between P and N terminals of the diode in the central cell **79'** while providing isolations between the cells in the left and right.

FIG. **7**(*h*) shows a top view of yet another embodiment of a fuse cell **70"** that has a dummy MOS gate **78"** providing isolation between P+/N+ in N well as two terminals of a diode and an electrical fuse element **72"**. An active region **71"** is divided into an upper active regions **73"** and a lower active region **74"** by a dummy MOS gate **78"**. The upper active region **73"** can be covered by a P+ implant **77"** while the lower active region **74"** can be covered by an N+ implant (the complement of the P+ implant **77"**). The active regions **73"** and **74"** constitute the P and N terminals of the diode in the cell **70"**. The polysilicon **78"** provides isolation between the P+/N+ of the diode in the cell **70"** and can be tied to a fixed bias. The polysilicon **78"** is a dummy MOS gate fabricated in standard CMOS processes and can be a metal gate in advanced metal-gate CMOS processes. The width of the dummy MOS gate can be close to the minimum gate width of a CMOS technology. The active region **71"** resides in an N well **75"**, the same N well that can be used to house PMOS in standard CMOS processes. A fuse element **72"** can be coupled to the P+ active region **73"** through a metal **76"** in one end (through contacts **75"-2** and **75"-3**) and to a high voltage supply line V+ in the other end (through contact **75"-1**). The N+ region **74"** is coupled to another voltage supply line V− through another contact **75"-4**. At least one of the contacts **75"-1**, **2**, **3**, **4** can be larger than at least one contacts outside of the memory array to reduce the contact resistance in one embodiment. When high and low voltages are applied to V+ and V−, respectively, a high current can flow through the fuse element **72"** to program the fuse element **72"** into a high resistance state accordingly.

In general, a polysilicon or silicide polysilicon fuse is more commonly used as an electrical fuse because of its lower program current than metal or contact/via fuses. However, a metal fuse has some advantages such as smaller size and wide resistance ratio after being programmed. Metal as a fuse element allows making contacts directly to a P+ active region thus eliminating one additional contact as compared to using a polysilicon fuse. In advanced CMOS technologies with feature size less than 40 nm, the program voltage for metal fuses can be lower than 3.3V, which makes metal fuse a viable solution.

FIG. **8**(*a*) shows a top view of a metal1 fuse cell **60"** including a P+/N well diode **60"** with dummy CMOS gate isolation. An active region **61** is divided into a center active region **63** and a peripheral active region **64** by a ring-shape MOS gate **68**. The center active region **63** is covered by a P+ implant **67** and the peripheral active region **64** is covered by an N+ implant (the complement of the P+ implant **67**), respectively, to constitute the P and N terminals of a diode. The active region **61** resides in an N well **65**, the same N well can be used to house PMOS in standard CMOS processes. A metal1 fuse element **62"** is coupled to the P+ region **63** directly. The ring-shape MOS gate **68**, which provides dummy CMOS gate isolation, can be biased at a fixed voltage, and can provide isolation between P+ active **63** and N+ active **64** regions in four sides. In one embodiment, the length to width ratio of a metal fuse can be about or larger than 10 to 1 to lower the electromigration threshold.

The size of the metal fuse cell in FIG. **8**(*a*) can be further reduced, if the turn-on resistance of the diode is not crucial. FIG. **8**(*b*) shows a top view of a row of metal fuse cells **60"** having four metal fuse cells that share one N well contact in each side in accordance with one embodiment. Metal1 fuse **69** has an anode **62'**, a metal1 body **66'**, and a cathode coupled to an active region **64'** covered by a P+ implant **67'** that acts as the P terminal of a diode. The active region **61'** resides in an N well **65'**. Another active region **63'** covered by an N+ implant (complement of P+ implant **67'**) acts as N terminal of the diode. Four diodes are isolated by STI **68'** and share one N+ active region **63'** each side. The N+ active regions **63'** are connected by a metal2 running horizontally, and the anode of the diode is connected by a metal3 running vertically. If metal1 is intended to be programmed, other types of metals in the conduction path should be wider. Similarly, more contacts and vias should be put in the conduction path to resist undesirable programming. Using metal1 as a metal fuse in FIG. **8**(*b*) is for illustrative purposes, those skilled in the art understand that the above description can be applied to any metals, such as metal0, metal2, metal3, or metal4 in other embodiments. Similarly, those skilled in the art understand that the isolation, metal scheme, and the number of cells sharing one N+ active may vary in other embodiments.

Contact or via fuses may become more viable for advanced CMOS technologies with feature size less than 65 nm, because small contact/via size makes program current rather low. FIG. **8**(*c*) shows a top view of a row of four via1 fuse cells **70** sharing N type well contacts **73***a* and **73***b* in accordance with one embodiment. Via1 fuse cell **79** has a via1 **79***a* coupled to a metal1 **76** and a metal2 **72**. Metal2 **72** is coupled to a metal3 through via2 **89** running vertically as a bitline. Metal1 **76** is coupled to an active region **74** covered by a P+ implant **77** that acts as the P terminal of a diode **71**. Active regions **73***a* and **73***b* covered by an N+ implant (complement of P+ implant **77**) serves as the N terminal of the diode **71** in via1 fuse cell **79**. Moreover, the active regions **73***a* and **73***b* serve as the common N terminal of the diodes in the four-fuse cell **70**. They are further coupled to a metal4 running horizontally as a wordline. The active regions **74**, **73***a*, and **73***b* reside in the same N well **75**. Four diodes in via1 fuse cells **70** have STI **78** isolation between each other. If via1 is intended to be programmed, more contacts and more other kinds of vias should be put in the conduction path. And metals in the conduction path should be wider and contain large contact/via enclosures to resist undesirable programming. Via1 as a via fuse in FIG. **8**(*c*) is for illustrative purpose, those skilled in the art understand that the above description can be applied to any kinds of contacts or vias, such as via2, via3, or via4, etc. Similarly, those skilled in the art understand that the isolation, metal scheme, and the number of cells sharing one N+ active may vary in other embodiments.

FIG. **8**(*d*) shows a top view of an array of 4×5 via1 fuses **90** with dummy CMOS gate isolation in accordance with one embodiment. The one-row via fuse shown in FIG. **8**(*c*) can be extended into a two-dimensional array **90** as shown in FIG. **8**(*d*). The array **90** has four rows of active regions **91**, each residing in a separate N well, and five columns of via fuse cells **96**, isolated by dummy CMOS gates **92** between active regions. Each via fuse cell **96** has one contact **99** on an active region covered by a P+ implant **94** that acts as the P terminal of a diode, which is further coupled to a metal2 bitline running vertically. Active regions in two sides of the array **90** are covered by N+ implant **97** to serve as the N terminals of the diodes in the same row, which is further coupled to metal3 as wordlines running horizontally. To program a via fuse, select and apply voltages to the desired wordline and bitline to conduct a current from metal2 bitline, via1, metal1, contact, P+ active, N+ active, to metal3 wordline. To ensure only via1 is programmed, metals can be made wider and the numbers of other types of vias or contact can be more than one. To simplify the drawing, metal1-via1-metal2 connection can be referred to FIG. **8**(*c*) and, therefore, is not shown in each cell in FIG. **8**(*d*). Those skilled in the art understand that various types of contact or vias can be used as resistive elements and the metal schemes may change in other embodiments. Similarly, the number of cells in rows and columns, the numbers of rows or columns in an array, and the numbers of cells between N+ active may vary in other embodiments.

FIG. **9**(*a*) shows a cross section of a programmable resistive device cell **40** using phase-change material as a resistive element **42**, with buffer metals **41** and **43**, and a P+/N well diode **32**, according to one embodiment. The P+/N well diode **32** has a P+ active region **33** and N+ active region **37** on an N well **34** as P and N terminals. The isolation between the P+ active region **33** and N+ active region **37** is an STI **36**. The P+ active region **33** of the diode **32** is coupled to a lower metal **41** as a buffer layer through a contact plug **40-1**. The lower metal **41** is then coupled to a thin film of phase change material **42** (e.g., GST film such as Ge2Sb2Te5 or AgInSbTe, etc.) through a contact plug **40-2**. An upper metal **43** also couples to the thin film of the phase-change material **42**. The upper metal **43** is coupled to another metal **44** to act as a bitline (BL) through a plug **40-3**. The phase-change film **42** can have a chemical composition of Germanium (Ge), Antimony (Sb), and Tellurium (Te), such as $Ge_xSb_yTe_z$ (x, y and z are any arbitrary numbers), or as one example $Ge_2Sb_2Te_5$ (GST-225). The GST film can be doped with at least one or more of Indium (In), Tin (Sn), or Selenium (Se) to enhance performance. The phase-change cell structure can be substantially planar, which means the phase-change film **42** has an area that is larger than the film contact area coupled to the program selector, or the height from the surface of the silicon substrate to the phase-change film **42** is much smaller than the dimensions of the film parallel to silicon substrate. In this embodiment, the active area of phase-change film **42** is much larger than the contact area so that the programming characteristics can be more uniform and reproducible. The phase-change film **42** is not a vertical structure and does not sit on top of a tall contact, which can be more suitable for embedded phase-change memory applications, especially when the diode **32** (i.e., junction diode) is used as program selector to make the cell size very small. For those skilled in the art understand that the structure and fabrication processes may vary and that the structures of phase-change film (e.g., GST film) and buffer metals described above are for illustrative purpose.

FIG. **9**(*b*) shows a top view of a PCM cell using a junction diode as program selector having a cell boundary **80** in accordance with one embodiment. The PCM cell has a P+/N well diode and a phase-change material **85**, which can be a GST film. The P+/N well diode has active regions **83** and **81** covered by a P+ implant **86** and an N+ implant (complement of P+ implant **86**), respectively, to serve as the anode and cathode. Both active regions **81** and **83** reside on an N well **84**, the same N well can be used to house PMOS in standard CMOS processes. The anode is coupled to the phase-change material **85** through a metal1 **82**. The phase-change material **85** is further coupled to a metal3 bitline (BL) **88** running vertically. The cathode of the P+/N well diode (i.e., active region **81**) is connected by a metal2 wordline (WL) **87** running horizontally. By applying a proper voltage between the bitline **88** and the wordline **87** for a suitable duration, the phase-change material **85** can be programmed into a 0 or 1 state accordingly. Since programming the PCM cell is based on raising the temperature rather than electro-migration as with an electrical fuse, the phase-change film (e.g., GST film) can be symmetrical in area for both anode and cathode. Those skilled in the art understand that the phase-change film, structure, layout style, and metal schemes may vary in other embodiments.

Programming a phase-change memory (PCM), such as a phase-change film, depends on the physical properties of the phase-change film, such as glass transition and melting temperatures. To reset, the phase-change film needs to be heated up beyond the melting temperature and then quenched. To set, the phase-change film needs to be heated up between melting and glass transition temperatures and then annealed. A typical PCM film has glass transition temperature of about 200° C. and melting temperature of about 600° C. These temperatures determine the operation temperature of a PCM memory because the resistance state may change after staying in a particular temperature for a long time. However, most applications require retaining data for 10 years for the operation temperature from 0 to 85° C. or even from −40 to 125° C. To maintain cell stability over the device's lifetime and over such a wide temperature range, periodic reading and then writing back data into the same cells can be performed. The refresh period can be quite long, such as longer than a second (e.g., minutes, hours, days, weeks, or even months). The refresh mechanism can be generated inside the memory or triggered from outside the memory. The long refresh period to maintain cell stability can also be applied to other emerging memories such as RRAM, CBRAM, and MRAM, etc.

FIG. **10** shows one embodiment of an MRAM cell **310** using diodes **317** and **318** as program selectors in accordance with one embodiment. The MRAM cell **310** in FIG. **10** is a three-terminal MRAM cell. The MRAM cell **310** has an MTJ **311**, including a free layer stack **312**, a fixed layer stack **313**, and a dielectric film in between, and the two diodes **317** and **318**. The free layer stack **312** is coupled to a supply voltage V, and coupled to the fixed layer stack **313** through a metal oxide such as Al_2O_3 or MgO. The diode **317** has the N terminal coupled to the fixed layer stack **313** and the P terminal coupled to V+ for programming a 1. The diode **318** has the P terminal coupled to the fixed layer stack **313** and the N terminal coupled to V− for programming a 0. If V+ voltage is higher than V, a current flows from V+ to V to program the MTJ **311** into state 1. Similarly, if V− voltage is lower than V, a current flows from V to V− to program the MTJ **311** into state 0. During programming, the other diode is supposedly cutoff. For reading, V+ and V− can be both set to 0V and the resistance between node V and V+/V− can be sensed to determine whether the MTJ **311** is in state 0 or 1.

FIG. **11**(*a*) shows a cross section of one embodiment of an MRAM cell **310** with MTJ **311** and junction diodes **317** and **318** as program selectors in accordance with one embodiment. MTJ **311** has a free layer stack **312** on top and a fixed layer stack **313** underneath with a dielectric in between to constitute a magnetic tunneling junction. Diode **317** is used to program 1 and diode **318** is used to program 0. Diodes **317** and **318** have P+ and N+ active regions on N wells **321** and **320**, respectively, the same N wells to house PMOS in standard CMOS processes. Diode **317** has a P+ active region **315** and N+ active region **314** to constitute the P and N terminals of the program-1 diode **317**. Similarly, diode **318** has a P+ active **316** and N+ active **319** to constitute the P and N terminals of the program-0 diode **318**. FIG. **11**(*a*) shows STI **330** isolation for the P and N terminals of diodes **317** and **318**. For those skilled in the art understand that different isolation schemes, such as dummy MOS gate or SBL, can alternatively be applied.

The free stacks **312** of the MTJ **311** can be coupled to a supply voltage V, while the N terminal of the diode **318** can be coupled to a supply voltage V− and the P terminal of the diode **317** can be coupled to another supply voltage V+. Programming a 1 in FIG. **11**(*a*) can be achieved by applying a high voltage, i.e., 2V to V+ and V−, while keeping V at ground, or 0V. To program a 1, a current flows from diode **317** through the MTJ **311** while the diode **318** is cutoff. Similarly, programming a 0 can be achieved by applying a high voltage to V, i.e., 2V, and keeping V+ and V− at ground. In this case, a current flows from MTJ **311** through diode **318** while the diode **317** is cutoff.

FIG. **11**(*b*) shows a cross section of another embodiment of an M RAM cell **310'** with MTJ **311'** and junction diodes **317'** and **318'** as program selectors in accordance with one embodiment. MTJ **311'** has a free layer stack **312'** on top and a fixed layer stack **313'** underneath with a dielectric in between to constitute a magnetic tunneling junction. Diode **317'** is used to program 1 and diode **318'** is used to program 0. Diodes **317'** and **318'** have P+ and N+ active regions on N wells **321'** and **320'**, respectively, which are fabricated by shallow N wells with additional process steps. Though more process steps are needed, the cell size can be smaller. Diode **317'** has P+ active region **315'** and N+ active region **314'** to constitute the P and N terminals of the program-1 diode **317'**. Similarly, diode **318'** has P+ active **316'** and N+ active **319'** to constitute the P and N terminals of the program-0 diode **318'**. STI **330'** isolates different active regions.

The free stacks **312'** of the MTJ **311'** can be coupled to a supply voltage V, while the N terminal of the diode **318'** can be coupled to a supply voltage V− and the P terminal of the diode **317'** is coupled to another supply voltage V+. Programming a 1 in FIG. **11**(*b*) can be achieved by applying a high voltage, i.e., 2V to V+ and V−, while keeping V at ground, or 0V. To program a 1, a current will flow from diode **317'** through the MTJ **311'** while the diode **318'** is cutoff. Similarly, programming 0 can be achieved by applying a high voltage to V, i.e., 2V, and keeping V+ and V− at ground. In this case, a current will flow from MTJ **311'** through diode **318'** while the diode **317'** is cutoff.

FIG. **12**(*a*) shows one embodiment of a three-terminal 2×2 MRAM cell array using junction diodes **317** and **318** as program selectors and the condition to program 1 in a cell in accordance with one embodiment. Cells **310-00**, **310-01**, **310-10**, and **310-11** are organized as a two-dimensional array. The cell **310-00** has a MTJ **311-00**, a program-1 diode **317-00**, and a program-0 diode **318-00**. The MTJ **311-00** is coupled to a supply voltage V at one end, to the N terminal of the program-1 diode **317-00** and to the P terminal of the program-0 diode **318-00** at the other end. The P terminal of the program-1 diode **317-00** is coupled to a supply voltage V+. The N terminal of the program-0 diode **318-00** is coupled to another supply voltage V−. The other cells **310-01**, **310-10**, and **310-11** are similarly coupled. The voltage Vs of the cells **310-00** and **310-10** in the same columns are connected to BL**0**. The voltage Vs of the cells **310-01** and **310-11** in the same column are connected to BL**1**. The voltages V+ and V− of the cells **310-00** and **310-01** in the same row are connected to WL**0**P and WL**0**N, respectively. The voltages V+ and V− of the cells **310-10** and **310-11** in the same row are connected to WL**1**P and WL**1**N, respectively. To program a 1 into the cell **310-01**, WL**0**P is set high and BL**1** is set low, while setting the other BL and WLs at proper voltages as shown in FIG. **12**(*a*) to disable the other program-1 and program-0 diodes. The bold line in FIG. **12**(*a*) shows the direction of current flow.

FIG. **12**(*b*) shows alternative program-1 conditions for the cell **310-01** in a 2×2 MRAM array in accordance with one embodiment. For example, to program a 1 into cell **310-01**, set BL**1** and WL**0**P to low and high, respectively. If BL**0** is set to high in condition **1**, the WL**0**N and WL**1**N can be either high or floating, and WL**1**P can be either low or floating. The high and low voltages of an MRAM in today's technologies are about 2-3V for high voltage and 0 for low voltage, respectively. If BL**0** is floating in condition **2**, WL**0**N and WL**1**N can be high, low, or floating, and WL**1**P can be either low or floating. In a practical implementation, the floating nodes are usually coupled to very weak devices to a fixed voltage to prevent leakage. One embodiment of the program-1 condition is shown in FIG. **12**(*a*) without any nodes floating.

FIG. **13**(*a*) shows one embodiment of a three-terminal 2×2 MRAM cell array with MTJ **311** and junction diodes **317** and **318** as program selectors and the condition to program 0 in a cell in accordance with one embodiment. The cells **310-00**, **310-01**, **310-10**, and **310-11** are organized as a two-dimensional array. The cell **310-00** has a MTJ **311-00**, a program-1 diode **317-00**, and a program-0 diode **318-00**. The MTJ **311-00** is coupled to a supply voltage V at one end, to the N terminal of program-1 diode **317-00** and to the P terminal of program-0 diode **318-00** at the other end. The P terminal of the program-1 diode **317-00** is coupled to a supply voltage V+. The N terminal of the program-0 diode **318-00** is coupled to another supply voltage V−. The other cells **310-01**, **310-10**, and **310-11** are similarly coupled. The voltage Vs of the cells **310-00** and **310-10** in the same columns are connected to BL**0**. The voltage Vs of the cells **310-01** and **310-11** in the same column are connected to BL**1**. The voltages V+ and V− of the cells **310-00** and **310-01** in the same row are connected to WL**0**P and WL**0**N, respectively. The voltages V+ and V− of the cells **310-10** and **310-11** in the same row are connected to WL**1**P and WL**1**N, respectively. To program a 0 into the cell **310-01**, WL**0**N is set low and BL**1** is set high, while setting the other BL and WLs at proper voltages as shown in FIG. **13**(*a*) to disable the other program-1 and program-0 diodes. The bold line in FIG. **13**(*a*) shows the direction of current flow.

FIG. **13**(*b*) shows alternative program-0 conditions for the cell **310-01** in a 2×2 MRAM array in accordance with one embodiment. For example, to program a 0 into cell **310-01**, set BL**1** and WL**0**N to high and low, respectively. If BL**0** is set to low in condition **1**, the WL**0**P and WL**1**P can be either low or floating, and WL**1**N can be either high or floating. The high and low voltages of an MRAM in today's technologies are about 2-3V for high voltage and 0 for low voltage, respectively. If BL**0** is floating in condition **2**, WL**0**P and WL**1**P can be high, low, or floating, and WL**1**N can be either high or floating. In a practical implementation, the floating nodes are usually coupled to very weak devices to a fixed voltage to prevent leakage. One embodiment of the program-0 condition is as shown in FIG. **13**(*a*) without any nodes floating.

The cells in 2×2 MRAM arrays in FIGS. **12**(*a*), **12**(*b*), **13**(*a*) and **13**(*b*) are three-terminal cells, namely, cells with V, V+, and V− nodes. However, if the program voltage VDDP is less than twice a diode's threshold voltage Vd, i.e., VDDP<2*Vd, the V+ and V− nodes of the same cell can be connected together as a two-terminal cell. Since Vd is about 0.6-0.7V at room temperature, this two-terminal cell works if the program high voltage is less than 1.2V and low voltage is 0V. This is a common voltage configuration of MRAM arrays for advanced CMOS technologies that has supply voltage of about 1.0V. FIGS. **14**(*a*) and **14**(*b*) show schematics for programming a 1 and 0, respectively, in a two-terminal 2×2 MRAM array.

FIGS. **14**(*a*) and **14**(*b*) show one embodiment of programming 1 and 0, respectively, in a two-terminal 2×2 MRAM cell array in accordance with one embodiment. The cells **310-00**, **310-01**, **310-10**, and **310-11** are organized in a two-dimensional array. The cell **310-00** has the MTJ **311-00**, the program-1 diode **317-00**, and the program-0 diode **318-00**. The MTJ **311-00** is coupled to a supply voltage V at one end, to the N terminal of program-1 diode **317-00** and the P terminal of program-0 diode **318-00** at the other end. The P terminal of the program-1 diode **317-00** is coupled to a supply voltage V+. The N terminal of the program-0 diode **318-00** is coupled to another supply voltage V−. The voltages V+ and V− are connected together in the cell level if VDDP<2*Vd can be met. The other cells **310-01**, **310-10** and **310-11** are similarly coupled. The voltages Vs of the cells **310-00** and **310-10** in the same columns are connected to BL**0**. The voltage Vs of the cells **310-01** and **310-11** in the same column are connected to BL**1**. The voltages V+ and V− of the cells **310-00** and **310-01** in the same row are connected to WL**0**. The voltages V+ and V− of the cells **310-10** and **310-11** in the same row are connected to WL**1**.

To program a 1 into the cell **310-01**, WL**0** is set high and BL**1** is set low, while setting the other BL and WLs at proper voltages as shown in FIG. **14**(*a*) to disable other program-1 and program-0 diodes. The bold line in FIG. **14**(*a*) shows the direction of current flow. To program a 0 into the cell **310-01**, WL**0** is set low and BL**1** is set high, while setting the other BL and WLs at proper voltages as shown in FIG. **14**(*b*) to disable the other program-1 and program-0 diodes. The bold line in FIG. **14**(*b*) shows the direction of current flow.

The embodiments of constructing MRAM cells in a 2×2 array as shown in FIGS. **12**(*a*)-**14**(*b*) are for illustrative purposes. Those skilled in the art understand that the number of cells, rows, or columns in a memory can be constructed arbitrarily and rows and columns are interchangeable.

The programmable resistive devices can be used to construct a memory in accordance with one embodiment. FIG. **15** shows a portion of a programmable resistive memory **100** constructed by an array **101** of n-row by (m+1)-column single-diode-as-program-selector cells **110** and n wordline drivers **150**-*i*, where i=0, 1, . . . , n−1, in accordance with one embodiment. The memory array **101** has m normal columns and one reference column for one shared sense amplifier **140** for differential sensing. Each of the memory cells **110** has a resistive element **111** coupled to the P terminal of a diode **112** as program selector and to a bitline BLj **170**-*j* (j=0, 1, . . . m−1) or reference bitline BLR**0** **175-0** for those of the memory cells **110** in the same column. The N terminal of the diode **112** is coupled to a wordline WLBi **152**-*i* through a local wordline LWLBi **154**-*i*, where i=0, 1, . . . , n−1, for those of the memory cells **110** in the same row. Each wordline WLBi is coupled to at least one local wordline LWLBi, where i=0, 1, . . . , n−1. The LWLBi **154**-*i* is generally constructed by a high resistivity material, such as N well, polysilicon, local interconnect, metal-0, active region, or metal gate to connect cells, and then coupled to the WLBi (e.g., a low-resistivity metal WLBi) through conductive contacts or vias, buffers, or post-decoders **172**-*i*, where i=0, 1, . . . , n−1. Buffers or post-decoders **172**-*i* may be needed when using diodes as program selectors because there are currents flowing through the WLBi, especially when one WLBi drives multiple cells for program or read simultaneously in other embodiments. The wordline WLBi is driven by the wordline driver **150**-*i* with a supply voltage vddi that can be switched between different voltages for program and read. Each BLj **170**-*j* or BLR**0** **175-0** is coupled to a supply voltage VDDP through a Y-write pass gate **120**-*j* or **125** for programming, where each BLj **170**-*j* or BLR**0** **175-0** is selected by YSWBj (j=0, 1, . . . , m−1) or YSWRB**0**, respectively. The Y-write pass gate **1201** (j=0, 1, . . . , m−1) or **125** can be built by PMOS, though NMOS, diode, or bipolar devices can be employed in some embodiments. Each BLj or BLR**0** is coupled to a dataline DLj or DLR**0** through a Y-read pass gate **130**-*j* or **135** selected by YSRj (j=0, 1, . . . , m−1) or YSRR**0**, respectively. In this portion of memory array **101**, m normal datalines DLj (j=0, 1, . . . , m−1) are connected to an input **160** of a sense amplifier **140**. The reference dataline DLR**0** provides another input **161** for the sense amplifier **140** (no multiplex is generally needed in the reference branch). The output of the sense amplifiers **140** is Q0.

To program a cell, the specific WLBi and YSWBj are turned on and a high voltage is supplied to VDDP, where i=0, 1, . . . n−1 and j=0, 1, . . . , m−1. In some embodiments, the reference cells can be programmed to 0 or 1 by turning on WLRBi, and YSWRB**0**, where i=0, 1, . . . , n−1. To read a cell, a data column **160** can be selected by turning on the specific WLBi and YSRj, where i=0, 1, . . . , n−1, and j=0, 1, . . . , m−1, and a reference cell coupled to the reference dataline DLR**0** **161** can be selected for the sense amplifier **140** to sense and compare the resistance difference between normal/reference BLs and ground, while disabling all YSWBj and YSWRB**0** where j=0, 1, . . . , m−1.

The programmable resistive devices can be used to construct a memory in accordance with one embodiment. FIG. **16**(*a*) shows a portion of a programmable resistive memory **100** constructed by an array **101** of 3-terminal MRAM cells **110** in n rows and m+1 columns and n pairs of wordline drivers **150**-*i* and **151**-*i*, where i=0, 1, . . . , n−1, according to one embodiment. The memory array **101** has m normal columns and one reference column for one shared sense amplifier **140** for differential sensing. Each of the memory cells **110** has a resistive element **111** coupled to the P terminal of a program-0 diode **112** and N terminal of a program-1 diode **113**. The program-0 diode **112** and the program-1 diode **113** serve as program selectors. Each resistive element **111** is also coupled to a bitline BLj **1701** (j=0, 1, . . . m−1) or reference bitline BLR**0** **175-0** for those of the memory cells **110** in the same column. The N terminal of the diode **112** is coupled to a wordline WLNi **152**-*i* through a local wordline LWLNi **154**-*i*, where i=0, 1, . . . , n−1, for those of the memory cells **110** in the same row. The P terminal of the diode **113** is coupled to a wordline WLPi **153**-*i* through a local wordline LWLPi **155**-*i*, where i=0, 1, . . . , n−1, for those cells in the same row. Each wordline WLNi or WLPi is coupled to at least one local wordline LWLNi or LWLPi, respectively, where i=0, 1, . . . , n−1. The LWLNi **154**-*i* and LWLPi **155**-*i* are generally constructed by a high resistivity material, such as N well, polysilicon, local interconnect, metal-0, active region, or metal gate to connect cells, and then coupled to the WLNi or WLPi (e.g., low-resistivity metal WLNi or WLPi) through conductive contacts or vias, buffers, or post-decoders **172**-*i* or **173**-*i* respectively, where i=0, 1, . . . , n−1. Buffers or post-decoders **172**-*i* or **173**-*i* may be needed when using diodes as program selectors because there are currents flowing through WLNi or WLPi, especially when one WLNi or WLPi drivers multiple cells for program or read simultaneously in some embodiments. The wordlines WLNi and WLPi are driven by wordline drivers **150**-*i* and **151**-*i*, respectively, with a supply voltage vddi that can be switched between different voltages for program and read. Each BLj **170**-*j* or BLR**0** **175-0** is coupled to a supply voltage VDDP through a Y-write-0 pass gate **120**-*j* or **125** to program 0, where each BLj **1701** or BLR**0** **175-0** is selected by YS**0**WBj (j=0, 1, . . . , m−1) or YS**0**WRB**0**, respectively. Y-write-0 pass gate **120**-*j* or **125** can be built by PMOS, though NMOS, diode, or bipolar devices can be employed in other embodiments. Similarly, each BLj **170**-*j* or BLR**0** **175-0** is coupled to a supply voltage 0V through a Y-write-1 pass gate **121**-*j* or **126** to program 1, where each BLj **170**-*j* or BLR**0** **175-0** is selected by YS**1**Wj (j=0, 1, . . . , m−1) or YS**1**WR**0**, respectively. Y-write-1 pass gate **1211** or **126** is can be built by NMOS, though PMOS, diode, or bipolar devices can be employed in other embodiments. Each BLj or BLR**0** is coupled to a dataline DLj or DLR**0** through a Y-read pass gate **130**-*j* or **135** selected by YSRj (j=0, 1, . . . , m−1) or YSRR**0**, respectively. In this portion of memory array **101**, m normal datalines DLj (j=0, 1, . . . , m−1) are connected to an input **160** of a sense amplifier **140**. Reference dataline DLR**0** provides another input **161** for the sense amplifier **140**, except that no multiplex is generally needed in a reference branch. The output of the sense amplifier **140** is Q0.

To program a 0 into a cell, the specific WLNi, WLPi and BLj are selected as shown in FIG. **13**(*a*) or **13**(*b*) by wordline drivers **150**-*i*, **151**-*i*, and Y-pass gate **1201** by YS**0**WBj, respectively, where i=0, 1, . . . n−1 and j=0, 1, . . . , m−1, while the other wordlines and bitlines are also properly set. A high voltage is applied to VDDP. In some embodiments, the reference cells can be programmed into 0 by setting proper voltages to WLRNi **158**-*i*, WLRPi **159**-*i* and YS**0**WRB**0**, where i=0, 1, . . . , n−1. To program a 1 to a cell, the specific WLNi, WLPi and BLj are selected as shown in FIG. **12**(*a*) or **12**(*b*) by wordline driver **150**-*i*, **151**-*i*, and Y-pass gate **121**-*j* by YS**1**Wj, respectively, where i=0, 1, . . . n−1 and j=0, 1, . . . , m−1, while the other wordlines and bitlines are also properly set. In some embodiments, the reference cells can be programmed to 1 by setting proper voltages to WLRNi **158**-*i*, WLRPi **159**-*i* and YS**1**WR**0**, where i=0, 1, . . . , n−1. To read a cell, a data column **160** can be selected by turning on the specific WLNi, WLPi and YSRj, where i=0, 1, . . . , n−1, and j=0, 1, . . . , m−1, and a reference cell coupled to the reference dataline DLR **161** for the sense amplifier **140** to sense and compare the resistance difference between normal/reference BLs and ground, while disabling all YS**0**WBj, YS**0**WRB**0**, YS**1**Wj and YS**1**WR**0**, where j=0, 1, . . . , m−1.

Another embodiment of constructing an MRAM memory with 2-terminal MRAM cells is shown in FIG. **16**(*b*), provided the voltage difference VDDP, between high and low states, is less than twice of the diode's threshold voltage Vd, i.e., VDDP<2*Vd. As shown in FIG. **16**(*b*), two wordlines per row WLNi **152**-*i* and WLPi **153**-*i* in FIG. **16**(*a*) can be merged into one wordline driver WLNi **152**-*i*, where i=0, 1, . . . , n−1. Also, the local wordlines LWLNi **154**-*i* and LWLP **155**-*i* per row in FIG. **16**(*a*) can be merged into one local wordline LWLNi **154**-*i*, where i=0, 1, . . . , n−1, as shown in FIG. **16**(*b*). Still further, two wordline drivers **150**-*i* and **151**-*i* in FIG. **16**(*a*) can be merged into one, i.e., wordline driver **150**-*i*. The BLs and WLNs of the unselected cells are applied with proper program 1 and 0 conditions as shown in FIGS. **14**(*a*) and **14**(*b*), respectively. Since half of wordlines, local wordlines, and wordline drivers can be eliminated in this embodiment, cell and macro areas can be reduced substantially.

Differential sensing is a common for programmable resistive memory, though single-end sensing can be used in other embodiments. FIGS. **17**(*a*), **17**(*b*), and **17**(*c*) show three other embodiments of constructing reference cells for differential sensing. In FIG. **17**(*a*), a portion of memory **400** has a normal array **180** of n× m cells, two reference columns **150-0** and **150-1** of n×1 cells each storing all data 0 and 1 respectively, m+1 Y-read pass gates **130**, and a sense amplifier **140**. As an example, n=8 and m=8 are used to illustrate the concept. There are n wordlines WLBi and n reference wordlines WLRBi for each column, where i=0, 1, . . . , n−1. When a wordline WLBi is turned on to access a row, a corresponding reference wordline WLRBi (i=0, 1, . . . , n−1) is also turned on to activate two reference cells **170-0** and **170-1** in the same row to provide mid-level resistance after proper scaling in the sense amplifier. The selected dataline **160** along with the reference dataline **161** are input to a sense amplifier **140** to generate an output Q0. In this embodiment, each WLRBi and WLBi (i=0, 1, . . . , n−1) are hardwired together and every cells in the reference columns need to be pre-programmed before read.

FIG. **17**(*b*) shows another embodiment of using a reference cell external to a reference column. In FIG. **17**(*b*), a portion of memory **400** has a normal array **180** of n×m cells, a reference column **150** of n×1 cells, m+1 Y-read pass gates **130**, and a sense amplifier **140**. When a wordline WLBi (i=0, 1, . . . , n−1) is turned on, none of the cells in the reference column **150** are turned on. An external reference cell **170** with a pre-determined resistance is turned on instead by an external reference wordline WLRB. The selected dataline **160** and the reference dataline **161** are input to a sense amplifier **140** to generate an output Q0. In this embodiment, all internal reference wordlines WLRBi (i=0, 1, . . . , n−1) in each row are disabled. The reference column **150** provides a loading to match with that of the normal columns. The reference cells or the reference column **150** can be omitted in other embodiments.

FIG. **17**(*c*) shows another embodiment of constructing reference cells for differential sensing. In FIG. **17**(*c*), a portion of memory **400** has a normal array **180** of n×m cells, one reference column **150** of n×1, two reference rows **175-0** and **175-1** of 1×m cells, m+1 Y-read pass gates **130**, and a sense amplifier **140**. As an example, n=8 and m=8 are used to illustrate the approach. There are n wordlines WLBi and 2 reference wordlines WLRB**0** **175-0** and WLRB**1** **175-1** on top and bottom of the array, where i=0, 1, . . . , n−1. When a wordline WLBi (i=0, 1, . . . , n−1) is turned on to access a row, the reference wordline WLRB**0** and WLRB**1** are also turned on to activate two reference cells **170-0** and **170-1** in the upper and lower right corners of the array **180**, which store data 0 and 1 respectively. The selected dataline **160** along with the reference dataline **161** are input to a sense amplifier **140** to generate an output Q0. In this embodiment, all cells in the reference column **150** are disabled except that the cells **170-0** and **170-1** on top and bottom of the reference column **150**. Only two reference cells are used for the entire n×m array that needs to be pre-programmed before read.

For those programmable resistive devices that have a very small resistance ratio between states 1 and 0, such as 2:1 ratio in MRAM, FIGS. **17**(*a*) and **17**(*c*) are desirable embodiments, depending on how many cells are suitable for one pair of reference cells. Otherwise, FIG. **17**(*b*) is a desirable embodiment for electrical fuse or PCM that has resistance ratio of more than about 10.

FIGS. **15**, **16**(*a*), **16**(*b*), **17**(*a*), **17**(*b*), and **17**(*c*) show only a few embodiments of a portion of programmable resistive memory in a simplified manner. The memory array **101** in FIGS. **15**, **16**(*a*), and **16**(*b*) can be replicated s times to read or program s-cells at the same time. In the case of differential sensing, the number of reference columns to normal columns may vary and the physical location can also vary relative to the normal data columns. Rows and columns are interchangeable. The numbers of rows, columns, or cells likewise may vary. For those skilled in the art understand that the above descriptions are for illustrative purpose. Various embodiments of array structures, configurations, and circuits are possible and are still within the scope of this invention.

The portions of programmable resistive memories shown in FIGS. **15**, **16**(*a*), **16**(*b*), **17**(*a*), **17**(*b*) and **17**(*c*) can include different types of resistive elements. The resistive element can be an electrical fuse including a fuse fabricated from an interconnect, contact/via fuse, contact/via anti-fuse, or gate oxide breakdown anti-fuse. The interconnect fuse can be formed from silicide, polysilicon, silicided polysilicon, metal, metal alloy, local interconnect, metal-0, thermally isolated active region, or some combination thereof, or can be constructed from a CMOS gate. The resistive element can also be fabricated from phase-change material in PCRAM, resistive film in RRAM/CBRAM, or MTJ in MRAM, etc. For the electrical fuse fabricated from an interconnect, contact, or via fuse, programming requirement is to provide a sufficiently high current, about 4-20 mA range, for a few microseconds to blow the fuse by electro-migration, heat, ion diffusion, or some combination thereof. For anti-fuse, programming requirement is to provide a sufficiently high voltage to breakdown the dielectrics between two ends of a contact, via or CMOS gate/body. The required voltage is about 6-7V for a few millisecond to consume about 100 uA of current in today's technologies. Programming Phase-Change Memory (PCM) requires different voltages and durations for 0 and 1. Programming to a 1 (or to reset) requires a high and short voltage pulse applied to the phase-change film. Alternatively, programming to a 0 (or to set) requires a low and long voltage pulse applied to the phase change film. The reset needs about 3V for 50 ns and consumes about 300 uA, while set needs about 2V for 300 ns and consumes about 100 uA. For MRAM, the high and low program voltages are about 2-3V and 0V, respectively, and the current is about +/−100-200 uA.

Most programmable resistive devices have a higher voltage VDDP (~2-3V) for programming than the core logic supply voltage VDD (~1.0V) for reading. FIG. **18**(*a*) shows a schematic of a wordline driver circuit **60** according to one embodiment. The wordline driver includes devices **62** and **61**, as shown as the wordline driver **150** in FIGS. **15**, **16**(*a*) and **16**(*b*). The supply voltage vddi is further coupled to either VDDP or VDD through power selectors **63** and **64** (e.g., PMOS power selectors) respectively. The input of the wordline driver Vin is from an output of an X-decoder. In some embodiments, the power selectors **63** and **64** are implemented as thick oxide I/O devices to sustain high voltage. The bodies of power selector **63** and **64** can be tied to vddi to prevent latchup.

Similarly, bitlines tend to have a higher voltage VDDP (~2-3V) for programming than the core logic supply voltage VDD (~1.0V) for reading. FIG. **18**(*b*) shows a schematic of a bitline circuit **70** according to one embodiment. The bitline circuit **70** includes a bitline (BL) coupled to VDDP and VDD through power selectors **73** and **74** (e.g., PMOS power selectors), respectively. If the bitline needs to sink a current such as in an MRAM, an NMOS pulldown device **71** can be provided. In some embodiments, the power selectors **73** and **74** as well as the pulldown device **71** can be implemented as thick-oxide I/O devices to sustain high voltage. The bodies of power selector **73** and **74** can be tied to vddi to prevent latchup.

Using junction diodes as program selectors may have high leakage current if a memory size is very large. Power selectors for a memory can help reducing leakage current by switching to a lower supply voltage or even turning off when a portion of memory is not in use. FIG. **18**(*c*) shows a portion of memory **85** with an internal power supply VDDP coupled to an external supply VDDPP and a core logic supply VDD through power selectors **83** and **84**. VDDP can even be coupled to ground by an NMOS pulldown device **81** to disable this portion of memory **85**, if this portion of memory is temporarily not in use.

FIG. **19**(*a*) shows one embodiment of a schematic of a pre-amplifier **100** according to one embodiment. The pre-amplifier **100** needs special considerations because the supply voltage VDD for core logic devices is about 1.0V that does not have enough head room to turn on a diode to make sense amplifiers functional, considering a diode's threshold is about 0.7V. One embodiment is to use another supply VDDR, higher than VDD, to power at least the first stage of sense amplifiers. The programmable resistive cell **110** shown in FIG. **19**(*a*) has a resistive element **111** and a diode **112** as program selector, and can be selected for read by asserting YSR' to turn on a gate of a MOS **130** and wordline bar WLB. The MOS **130** is a Y-select pass gate to select a signal from one of the at least one bitline(s) (BL) coupled to cells to a dataline (DL) for sensing. The pre-amplifier **100** also has a reference cell **115** including a reference resistive element **116** and a reference diode **117**. The reference cell **115** can be selected for differential sensing by asserting YSRR' to turn on a gate of a MOS **131** and reference wordline WLRB. The MOS **131** is a reference pass gate to pass a signal from a reference bitline (BLR) to a reference dataline (DLR) for sensing. YSRR' is similar to YSR' to turn on a reference cell rather than a selected cell, except that the reference branch typically has only one reference bitline (BLR). The resistance Ref of the reference resistive element **116** can be set at a resistance approximately half-way between the minimum of state 1 and maximum of state 0 resistance. MOS **151** is for pre-charging DL and DLR to the same voltage before sensing by a pre-charge signal Vpc. Alternatively, the DL or DLR can be pre-charged to each other or to a diode voltage above ground in other embodiments. The reference resistor element **116** can be a plurality of resistors for selection to suit different cell resistance ranges in another embodiment.

The drains of MOS **130** and **131** are coupled to sources of NMOS **132** and **134**, respectively. The gates of **132** and **134** are biased at a fixed voltage Vbias. The channel width to length ratios of NMOS **132** and **134** can be relatively large to clamp the voltage swings of dataline DL and reference dataline DLR, respectively. The drain of NMOS **132** and **134** are coupled to drains of PMOS **170** and **171**, respectively. The drain of PMOS **170** is coupled to the gate of PMOS **171** and the drain of PMOS **171** is coupled to the gate of PMOS **170**. The outputs V+ and V− of the pre-amplifier **100** are the drains of PMOS **170** and PMOS **171** respectively. The sources of PMOS **170** and PMOS **171** are coupled to a read supply voltage VDDR. The outputs V+ and V− are pulled up by a pair of PMOS **175** to VDDR when the pre-amplifier **100** is disabled. VDDR is about 2-3V (which is higher than about 1.0V VDD of core logic devices) to turn on the diode selectors **112** and **117** in the programmable resistive cell **110** and the reference cell **115**, respectively. The CMOS **130**, **131**, **132**, **134**, **170**, **171**, and **175** can be embodied as thick-oxide I/O devices to sustain high voltage VDDR. The NMOS **132** and **134** can be native NMOS (i.e., the threshold voltage is ~0V) to allow operating at a lower VDDR. In another embodiment, the read selectors **130** and **131** can be PMOS devices. In another embodiment, the sources of PMOS **170** and **171** can be coupled to the drain of a PMOS pullup (an activation device not shown in FIG. **19**(*a*)), whose source is then coupled to VDDR. This sense amplifier can be activated by setting the gate of the PMOS pullup low after turning on the reference and Y-select pass gates.

FIG. **19**(*b*) shows one embodiment of a schematic of an amplifier **200** according to one embodiment. In another embodiment, the outputs V+ and V− of the pre-amplifier **100** in FIG. **19**(*a*) can be coupled to gates of NMOS **234** and **232**, respectively, of the amplifier **200**. The NMOS **234** and **232** can be relatively thick oxide I/O devices to sustain the high input voltage V+ and V− from a pre-amplifier. The sources of NMOS **234** and **232** are coupled to drains of NMOS **231** and **230**, respectively. The sources of NMOS **231** and **230** are coupled to a drain of an NMOS **211**. The gate of NMOS **211** is coupled to a clock ϕ to turn on the amplifier **200**, while the source of NMOS **211** is coupled to ground. The drains of NMOS **234** and **232** are coupled to drains of PMOS **271** and **270**, respectively. The sources of PMOS **271** and **270** are coupled to a core logic supply VDD. The gates of PMOS **271** and NMOS **231** are connected and coupled to the drain of PMOS **270**, as a node Vp. Similarly, the gates of PMOS **270** and NMOS **230** are connected and coupled to the drain of PMOS **271**, as a node Vn. The nodes Vp and Vn are pulled up by a pair of PMOS **275** to VDD when the amplifier **200** is disabled when ϕ goes low. The output nodes Vout+ and Vout− are coupled to nodes Vn and Vp through a pair of inverters as buffers.

FIG. **19**(*c*) shows a timing diagram of the pre-amplifier **100** and the amplifier **200** in FIGS. **19**(*a*) and **19**(*b*), respectively. The X- and Y-addresses AX/AY are selected to read a cell. After some propagation delays, a cell is selected for read by turning WLB low and YSR high to thereby select a row and a column, respectively. Before activating the pre-amplifier **100**, a pulse Vpc can be generated to precharge DL and DLR to ground, to a diode voltage above ground, or to each other. The pre-amplifier **100** would be very slow if the DL and DLR voltages are high enough to turn off the cascode devices (e.g., NMOS **132** and **134**). After the pre-amplifier outputs V+ and V− are stabilized, the clock ϕ is set high to turn on the amplifier **200** and to amplify the final output Vout+ and Vout− into full logic levels. The precharge scheme can be omitted in other embodiments.

FIG. **20**(*a*) shows another embodiment of a pre-amplifier **100'**, similar to the pre-amplifier **100** in FIG. **19**(*a*), with PMOS pull-ups **171** and **170** configured as current mirror loads. The reference branch can be turned on by a level signal, Sense Amplifier Enable (SAEN), to enable the pre-amplifier, or by a cycle-by-cycle signal YSRR' as in FIG. **19**(*a*). MOS **151** is for pre-charging DL and DLR to the same voltage before sensing by a pre-charge signal Vpc. Alternatively, the DL or DLR can be pre-charged to ground or to a diode voltage above ground in other embodiments. In this embodiment, the number of the reference branches can be shared between different pre-amplifiers at the expense of increasing power consumption. The reference resistor **116** can be a plurality of resistors for selection to suit different cell resistance ranges in another embodiment.

FIG. **20**(*b*) shows level shifters **300** according to one embodiment. The V+ and V− from the pre-amplifier **100**, **100'** outputs in FIG. **19**(*a*) or FIG. **20**(*a*) are coupled to gates of NMOS **301** and **302**, respectively. The drains of NMOS **301** and **302** are coupled to a supply voltage VDDR. The sources of NMOS **301** and **302** are coupled to drains of NMOS **303** and **304**, respectively, which have gates and drains connected as diodes to shift the voltage level down by one Vtn, the threshold voltage of an NMOS. The sources of NMOS **303** and **304** are coupled to the drains of pulldown devices NMOS **305** and **306**, respectively. The gates of NMOS **305** and **306** can be turned on by a clock ϕ. The NMOS **301**, **302**, **303** and **304** can be thick-oxide I/O devices to sustain high voltage VDDR. The NMOS **303** and **304** can be cascaded more than once to shift V+ and V− further to proper voltage levels Vp and Vn. In another embodiment, the level shifting devices **303** and **304** can be built using PMOS devices.

FIG. **20**(*c*) shows another embodiment of an amplifier **200'** with current-mirror loads having PMOS **270** and **271** as loads. The inputs Vp and Vn of the amplifier **200'** are from the outputs Vp and Vn of the level shifter **300** in FIG. **20**(*b*) that can be coupled to gates of NMOS **231** and **230**, respectively. The drains of NMOS **231** and **230** are coupled to drains of PMOS **271** and **270** which provide current-mirror loads. The drain and gate of PMOS **271** are connected and coupled to the gate of PMOS **270**. The sources of NMOS **231** and **230** are coupled to the drain of an NMOS **211**, which has the gate coupled to a clock signal ϕ and the source to ground. The clock signal ϕ enables the amplifier **200'**. The drain of PMOS **270** provides an output Vout+. The PMOS pullup **275** keeps the output Vout+ at logic high level when the amplifier **200'** is disabled.

FIG. **20**(*d*) shows one embodiment of a pre-amplifier **100'** based on all core devices according to one embodiment. The programmable resistive cell **110'** has a resistive element **111'** and a diode **112'** as program selector that can be selected for read by asserting YSR' to turn on a gate of a MOS **130'** and wordline bar WLB. The MOS **130'** is a Y-select pass gate to select a signal from one of the at least one bitline(s) (BL) coupled to cells to a dataline (DL) for sensing. The pre-amplifier **100'** also has a reference cell **115'** including a reference resistive element **116'** and a reference diode **117'**. The reference resistor **116'** can be a plurality of resistors for selection to suit different cell resistance ranges in another embodiment. The reference cell **115'** can be selected for differential sensing by asserting YSRR' to turn on a gate of a MOS **131'** and reference wordline WLRB. The MOS **131'** is a reference pass gate to pass a signal from a reference bitline (BLR) to a reference dataline (DLR) for sensing. YSRR' is similar to YSR' to turn on a reference cell rather than a selected cell, except that the reference branch typically has only one reference bitline (BLR). The drains of MOS **130'** and **131'** are coupled to drains of PMOS **170'** and **171'**, respectively. The gate of **170'** is coupled to the drain of **171'** and the gate of **171'** is coupled to the drain of **170'**. The sources of MOS **170'** and **171'** are coupled to the drains of MOS **276'** and **275'**, respectively. The gate of **275'** is coupled to the drain of **276'** and the gate of **276'** is coupled to the drain of **275'**. The drains of **170'** and **171'** are coupled by a MOS equalizer **151'** with a gate controlled by an equalizer signal Veq**1**. The drains of **276'** and **275'** are coupled by a MOS equalizer **251'** with a gate controlled by an equalizer signal Veq**0**. The equalizer signals Veq**0** and Veq**1** can be dc or ac signals to reduce the voltage swing in the drains of **170'**, **171'** and **275'**, **276'**, respectively. By reducing the voltage swings of the PMOS devices in the pullup and by stacking more than one level of cross-coupled PMOS, the voltage swings of the **170'**, **171'**, **275'**, and **276'** can be reduced to VDD range so that core logic devices can be used. For example, the supply voltage of the sense amplifier VDDR is about 2.5V, while the VDD for core logic devices is about 1.0V. The DL and DLR are about 1V, based on diode voltage of about 0.7V with a few hundred millivolts drop for resistors and pass gates. If the cross-coupled PMOS are in two-level stacks, each PMOS only endures voltage stress of (2.5−1.0)/2=0.75V. Alternatively, merging MOS **275'** and **276'** into a single MOS or using a junction diode in the pullup is another embodiment. Inserting low-Vt NMOS as cascode devices between **170'** and **130'**; **171'** and **131'** is another embodiment. The output nodes from the drains of **170'** and **171'** are about 1.0-1.2V so that the sense amplifier as shown in FIG. **19**(*b*) can be used with all core logic devices.

FIG. **20**(*e*) shows another embodiment of a pre-amplifier **100"** with an activation device **275"** according to one embodiment. The programmable resistive cell **110"** has a resistive element **111"** and a diode **112"** as program selector that can be selected for read by asserting YSR" to turn on a gate of a MOS **130"** and wordline bar WLB. The MOS **130"** is a Y-select pass gate to select a signal from one of the at least one bitline(s) (BL) coupled to cells to a dataline (DL) for sensing. The pre-amplifier **100"** also has a reference cell **115"** including a reference resistive element **116"** and a reference diode **117"**. The reference resistor **116** can be a plurality of resistors to suit different cell resistance ranges in another embodiment. The reference cell **115"** can be selected for differential sensing by asserting YSRR" to turn on a gate of a MOS **131"** and reference wordline WLRB. The MOS **131"** is a reference pass gate to pass a signal from a reference bitline (BLR) to a reference dataline (DLR) for sensing. YSRR" is similar to YSR" to turn on a reference cell rather than a selected cell, except that the reference branch typically has only one reference bitline (BLR). The drains of MOS **130"** and **131"** are coupled to the sources of MOS **132"** and **134"**, respectively. The drains of MOS **132"** and **134"** are coupled to the drains of PMOS **170"** and **171"**, respectively. The gate of **170"** is coupled to the drain of **171"** and the gate of **171"** is coupled to the drain of **170"**. The sources of MOS **170"** and **171"** are coupled to the drain of MOS **275"** whose source is coupled to a supply voltage and gate coupled to a Sensing Enable Bar (SEB). The drains of **170"** and **171"** are coupled by a MOS equalizer **251"** with a gate controlled by an equalizer signal Veq**0**. The sources of **132"** and **134"** are coupled by a MOS equalizer **151"** with a gate controlled by an equalizer signal Veq**1**. The equalizer signals Veq**0** and Veq**1** can be dc or ac signals to reduce the voltage swings in the sources of **170"**, **171"** and **132"**, **134"**, respectively.

FIGS. **19**(*a*), **20**(*a*), **20**(*d*) and **20**(*e*) only show four of many pre-amplifier embodiments. Similarly, FIGS. **19**(*b*), **20**(*c*) and **20**(*b*) only show several of many amplifier and level shifter embodiments. Various combinations of pre-amplifiers, level shifters, and amplifiers in NMOS or PMOS, in core logic or I/O devices, with devices stacked or with an activation device, operated under high voltage VDDR or core supply VDD can be constructed differently, separately, or mixed. The equalizer devices can be embodied as PMOS or NMOS, and can be activated by a dc or ac signal. In some embodiments, the precharge or equalizer technique can be omitted.

FIGS. **21**(*a*) and **21**(*b*) show a flow chart depicting embodiments of a program method **700** and a read method **800**, respectively, for a programmable resistive memory in accordance with certain embodiments. The methods **700** and **800** are described in the context of a programmable resistive memory, such as the programmable resistive memory **100** in FIGS. **15**, **16**(*a*) and **16**(*b*). In addition, although described as a flow of steps, one of ordinary skilled in the art will recognize that at least some of the steps may be performed in a different order, including simultaneously, or skipped.

FIG. **21**(*a*) depicts a method **700** of programming a programmable resistive memory in a flow chart according to one embodiment. In the first step **710**, proper power selectors can be selected so that high voltages can be applied to the power supplies of wordline drivers and bitlines. In the second step **720**, the data to be programmed in a control logic (not shown in FIGS. **15**, **16**(*a*), and **16**(*b*)) can be analyzed, depending on what types of programmable resistive devices. For electrical fuse, this is a One-Time-Programmable (OTP) device such that programming always means blowing fuses into a non-virgin state and is irreversible. Program voltage and duration tend to be determined by external control signals, rather than generated internally from the memory. For PCM, programming into a 1 (to reset) and programming into a 0 (to set) require different voltages and durations such that a control logic determines the input data and select proper power selectors and assert control signals with proper timings. For MRAM, the directions of current flowing through MTJs are more important than time duration. A control logic determines proper power selectors for wordlines and bitlines and assert control signals to ensure a current flowing in the desired direction for desired time. In the third step **730**, a cell in a row can be selected and the corresponding local wordline can be turned on. In the fourth step **740**, sense amplifiers can be disabled to save power and prevent interference with the program operations. In the fifth step **750**, a cell in a column can be selected and the corresponding Y-write pass gate can be turned on to couple the selected bitline to a supply voltage. In the last step **760**, a desired current can be driven for a desired time in an established conduction path to complete the program operations. For most programmable resistive memories, this conduction path is from a high voltage supply through a bitline select, resistive element, diode as program selector, and an NMOS pulldown of a local wordline driver to ground. Particularly, for programming a 1 to an MRAM, the conduction path is from a high voltage supply through a PMOS pullup of a local wordline driver, diode as program selector, resistive element, and bitline select to ground.

FIG. **21**(*b*) depicts a method **800** of reading a programmable resistive memory in a flow chart according to one embodiment. In the first step **810**, proper power selectors can be selected to provide supply voltages for local wordline drivers, sense amplifiers, and other circuits. In the second step **820**, all Y-write pass gates, i.e., bitline program selectors, can be disabled. In the third step **830**, desired local wordline(s) can be selected so that the diode(s) as program selector(s) have a conduction path to ground. In the fourth step **840**, sense amplifiers can be enabled and prepared for sensing incoming signals. In the fifth step **850**, the dataline and the reference dataline can be pre-charged to the V− voltage of the programmable resistive device cell. In the sixth step **860**, the desired Y-read pass gate can be selected so that the desired bitline is coupled to an input of the sense amplifier. A conduction path is thus established from the bitline to the resistive element in the desired cell, diode(s) as program selector(s), and the pulldown of the local wordline driver(s) to ground. The same applies for the reference branch. In the last step **870**, the sense amplifiers can compare the read current with the reference current to determine a logic output of 0 or 1 to complete the read operations.

FIG. **22** shows a processor system **700** according to one embodiment. The processor system **700** can include a programmable resistive device **744**, such as in a cell array **742**, in memory **740**, according to one embodiment. The processor system **700** can, for example, pertain to a computer system. The computer system can include a Central Process Unit (CPU) **710**, which communicate through a common bus **715** to various memory and peripheral devices such as I/O **720**, hard disk drive **730**, CDROM **750**, memory **740**, and other memory **760**. Other memory **760** is a conventional memory such as SRAM, DRAM, or flash, typically interfaces to CPU **710** through a memory controller. CPU **710** generally is a microprocessor, a digital signal processor, or other programmable digital logic devices. Memory **740** is preferably constructed as an integrated circuit, which includes the memory array **742** having at least one programmable resistive device **744**. The memory **740** typically interfaces to CPU **710** through a memory controller. If desired, the memory **740** may be combined with the processor, for example CPU **710**, in a single integrated circuit.

The invention can be implemented in a part or all of an integrated circuit in a Printed Circuit Board (PCB), or in a system. The programmable resistive device can be fuse, anti-fuse, or emerging nonvolatile memory. The fuse can be silicided or non-silicided polysilicon fuse, thermally isolated active-region fuse, local interconnect fuse, metal-**0** fuse, metal fuse, contact fuse, via fuse, or fuse constructed from CMOS gates. The anti-fuse can be a gate-oxide breakdown anti-fuse, contact or via anti-fuse with dielectrics in-between. The emerging nonvolatile memory can be Magnetic RAM (MRAM), Phase Change Memory (PCM), Conductive Bridge RAM (CBRAM), or Resistive RAM (RRAM). Though the program mechanisms are different, their logic states can be distinguished by different resistance values.

The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modifications and substitutions of specific process conditions and structures can be made without departing from the spirit and scope of the present invention.

The many features and advantages of the present invention are apparent from the written description and, thus, it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation as illustrated and described. Hence, all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

What is claimed is:

1. An One-Time Programmable (OTP) memory, comprising:

a plurality of OTP cells, at least one of the cells comprising:

an OTP element coupled to a first supply voltage line;

a selector including at least one active region divided by a MOS gate into at least one first active region and a second active region, where the first active region having a first type of dopant and a second active region having the first or a second type of dopant, the first active region providing a first terminal for the selector, the second active region providing a second terminal for the selector, the MOS gate providing a third terminal for the selector, both the first and second active regions residing in a common CMOS well or on an isolated substrate, the first active region coupled to the OTP element and the second active region coupled to a second supply voltage line, the MOS gate coupled to a third supply voltage line, the first and second active regions being fabricated from sources or drains of CMOS devices; and

at least one thermally conductive element, the at least one thermally conductive element coupled to the OTP element to dissipate or generate heat,

wherein the OTP element is configured to be programmable by applying voltages to the first, second, and the third supply voltage lines to thereby change its logic state, and wherein the thermally conductive element is configured to assist in programming of the OTP element.

2. An OTP memory as recited in claim **1**, wherein the OTP element includes at least one of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, thermally isolated active region, metal-0, metal, metal alloy, metal gate, or combination thereof.

3. An OTP memory as recited in claim **1**, wherein the OTP element has an anode, a cathode, and a long-and-narrow body.

4. An OTP memory as recited in claim **3**, wherein the anode has an area that is larger than an area of the cathode.

5. An OTP memory as recited in claim **3**, wherein the at least one thermally conductive element has an extended area coupled to and extending beyond the anode that is longer than required by design rules and/or has reduced current or substantially no current flowing through.

6. An OTP memory as recited in claim **5**, wherein the at least one thermally conductive element has a bar shape and is coupled to and extends beyond the anode.

7. An OTP memory as recited in claim **3**, wherein the at least one thermally conductive element has an extended area coupled to and extending beyond the anode that is bent 90 degrees at least once and runs along the body of the OTP element in one side.

8. An OTP memory as recited in claim **3**, wherein the anode has more contacts coupled thereto than are coupled to the cathode.

9. An OTP memory as recited in claim **3**, wherein the cathode or anode has at least one contact that is larger than at least one contact outside of the OTP cells.

10. An OTP memory as recited in claim **3**, wherein the cathode or anode has at least one contact that is wider than the width of the underline OTP element.

11. An OTP memory as recited in claim **1**, wherein the OTP element or the selector is built on at least one fin structure in a FinFET technology.

12. An electronic system, comprising:

a processor; and

an One-Time Programmable (OTP) memory operatively connected to the processor, the OTP memory including a plurality of OTP cells, at least one of the cells comprising:

an OTP element coupled to a first supply voltage line;

a selector including at least one active region divided by at least one MOS gate into at least one first active region and a second active region, where the first active region having a first type of dopant and the second region having the first or a second type of dopant, the first active region providing a first terminal of the selector, the second active region providing a second terminal of the selector, the MOS gate providing a third terminal of the selector, both the first and second active regions residing in a common CMOS well or on an isolated substrate, the first active region coupled to the OTP element, the second active region coupled to a second supply voltage line, and the MOS gate coupled to a third supply voltage, the first and second active regions being fabricated from sources or drains of CMOS devices,

at least one heat sink or heat source, coupled to the OTP element, to dissipate or generate heat, and

wherein the OTP element is configured to be programmable by applying voltages to the first, the second, and the third supply voltage lines to thereby change the resistance into a different logic state, and wherein the heat sink or heat source is configured to assist in programming of the OTP element.

13. An electronic system as recited in claim **12**, wherein the OTP element has at least one of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, thermally isolated active region, metal-0, metal, metal alloy, metal gate, or combination thereof.

14. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled between the first end and the second end.

15. An electronic system as recited in claim **12**, wherein the OTP element includes an anode, a cathode and a body coupled between the first end and the second end, and wherein the area of the anode is larger than the area of the cathode.

16. An electronic system as recited in claim **14**, wherein the heat sink or heat source comprises an extended area beyond the anode that is longer than required by design rules and/or has reduced current or substantially no current flowing through.

17. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled between the first end and the second end, and has a bar shape, and wherein the heat sink or heat source comprises an extended area that extents outward from the first end of the OTP element.

18. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled between the first end and the second end, and the first end has an extended area bent 90 degrees more than once and runs at least in part along the body of the OTP element on one side thereof.

19. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled therebetween, and wherein the first end has more contacts coupled thereon than does the second end.

20. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled therebetween, and wherein the first end or the second end has at least one contact coupled thereon that is larger than at least one contact outside of the OTP cells.

21. An electronic system as recited in claim **12**, wherein the OTP element has a first end, a second end, and a body coupled therebetween, and wherein the first end or the second end has at least one contact coupled thereon that is wider than a width of any of the first end, the second end and the body of the underline OTP element.

22. An electronic system as recited in claim **12**, wherein the OTP element or the selector is built on at least one fin structure in a FinFET technology.

23. A One-Time Programmable (OTP) memory, comprising:

a plurality of OTP cells, at least one of the cells comprising:

an OTP element having an anode, a body, and a cathode, the anode being provided by an anode structure, the body being provided by a body structure, and the cathode being provided by a cathode structure, the anode structure having at least one thermally conductive element thermally coupled thereto to manage thermal conditions at the OTP element,

wherein the OTP element is configured to be programmable by applying voltages to change its logic state, and

wherein substantially no current flows through the least one thermally conductive element during programming.

24. A One-Time Programmable (OTP) memory, comprising:

a plurality of OTP cells, at least one of the cells comprising:

an OTP element having an anode, a body, and a cathode, the anode being provided by an anode structure, the body being provided by a body structure, and the cathode being provided by a cathode structure, the anode structure being significantly larger or longer than the cathode structure; and

at least one contact coupled to the cathode structure;

a plurality of contacts coupled to the anode structure;

the number of contacts coupled to the anode structure is greater than the number of contacts coupled to the cathode structure so that the anode structure has greater thermal conductivity than the cathode structure,

wherein the OTP element is configured to be programmable by applying voltages to change its logic state.

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