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(54) **REGULATOR AND SEMICONDUCTOR INTEGRATED CIRCUIT**

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G05F 3/26 (2006.01)

(52) **U.S. Cl.**
CPC ***G05F 3/267*** (2013.01)

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USPC 323/271, 282–285, 299, 311–317
See application file for complete search history.

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(57) **ABSTRACT**

According to one embodiment, a regulator is provided which comprises a reference voltage generating circuit that generates a reference voltage, a first voltage dividing circuit that divides a regulator output in voltage, an error amplifier that compares a first divided voltage obtained by dividing the regulator output and the reference voltage, and an output transistor that generates the regulator output based on the output of the error amplifier. The reference voltage generating circuit comprises a diode-connected first transistor. The reference voltage is generated based on a diode voltage generated by the first transistor.

18 Claims, 5 Drawing Sheets

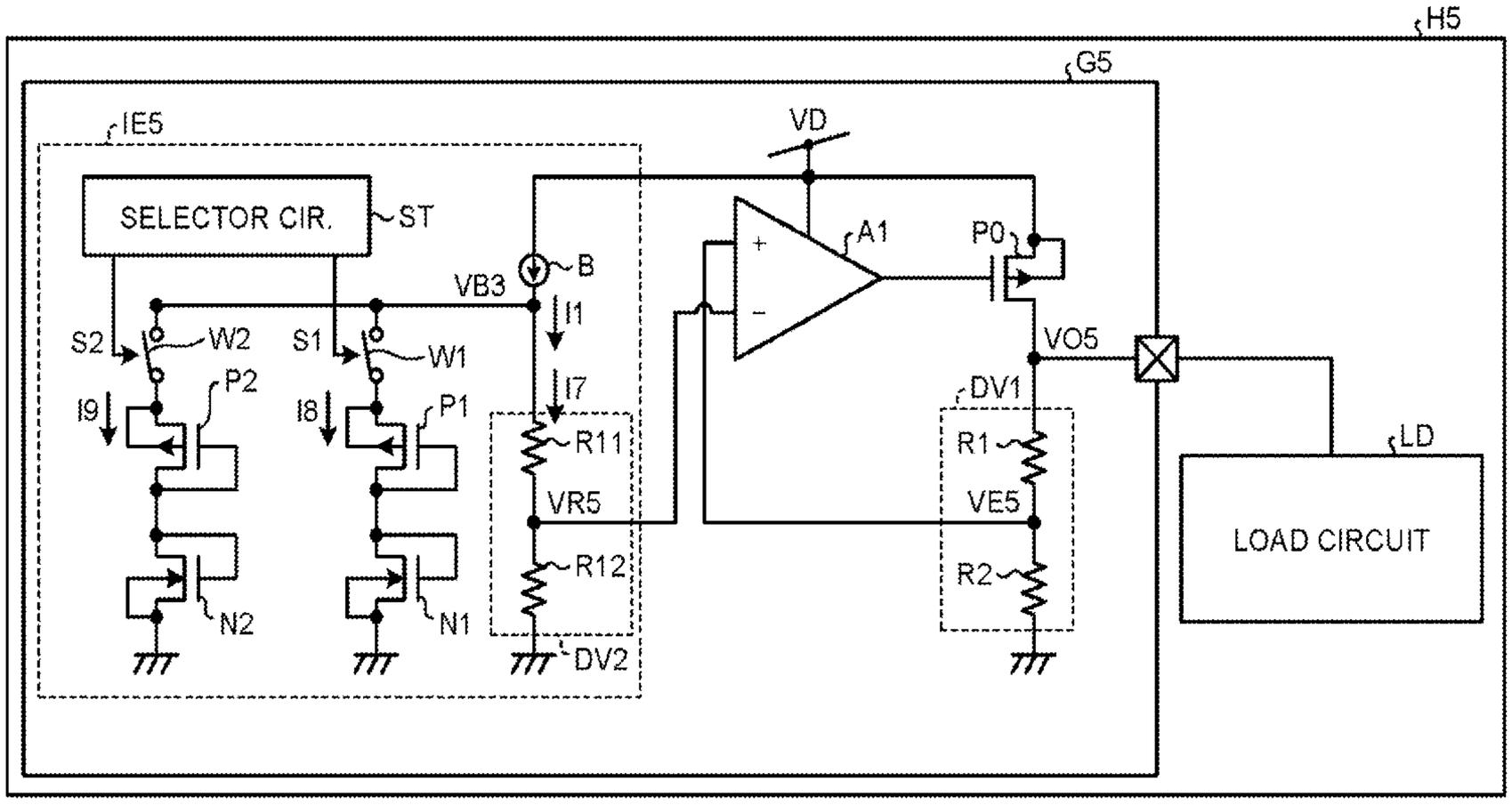


FIG.1

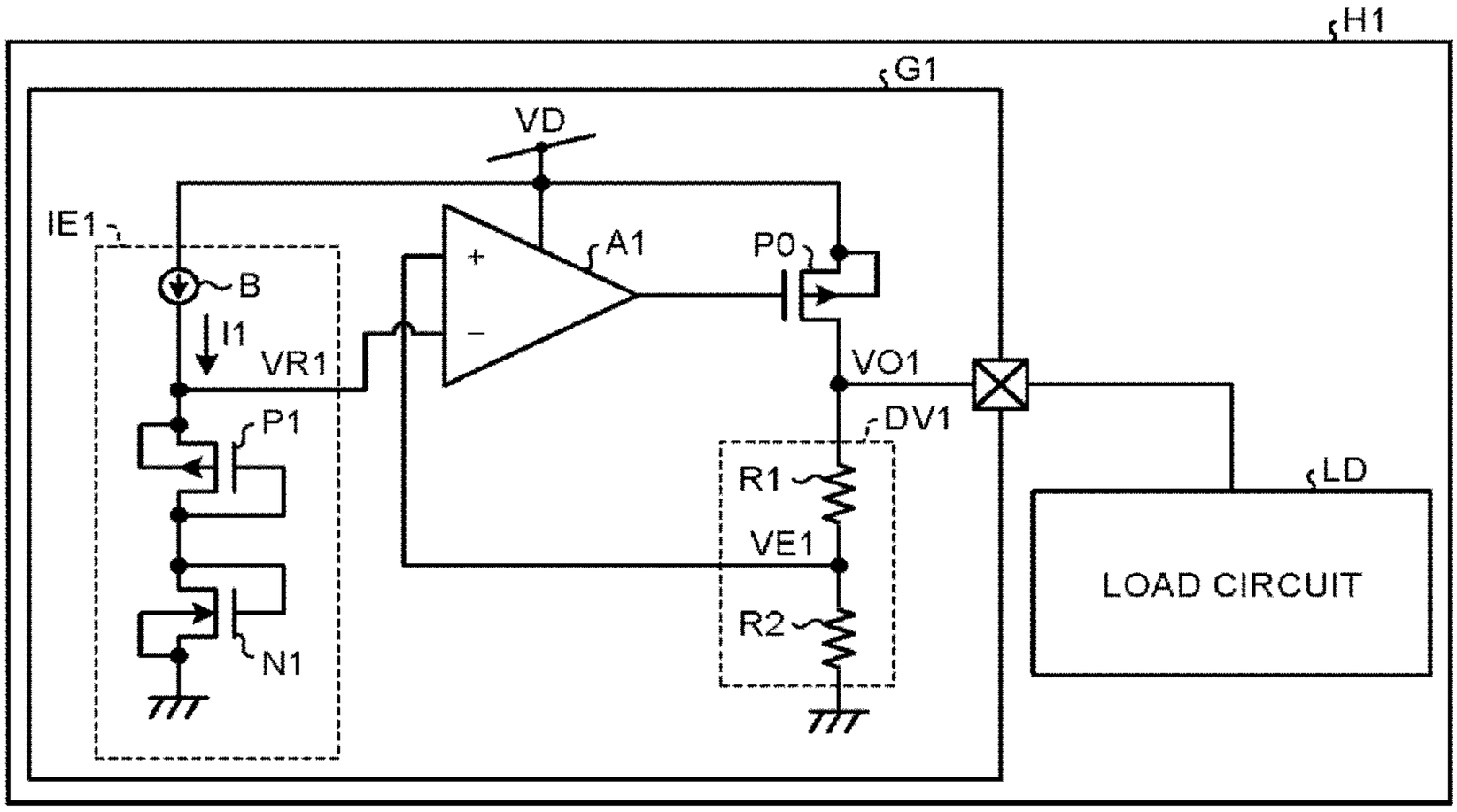

H1
G1
VD
IE1
A1
P0
B
I1
VR1
VO1
P1
DV1
R1
VE1
R2
N1
LD
LOAD CIRCUIT

FIG.2

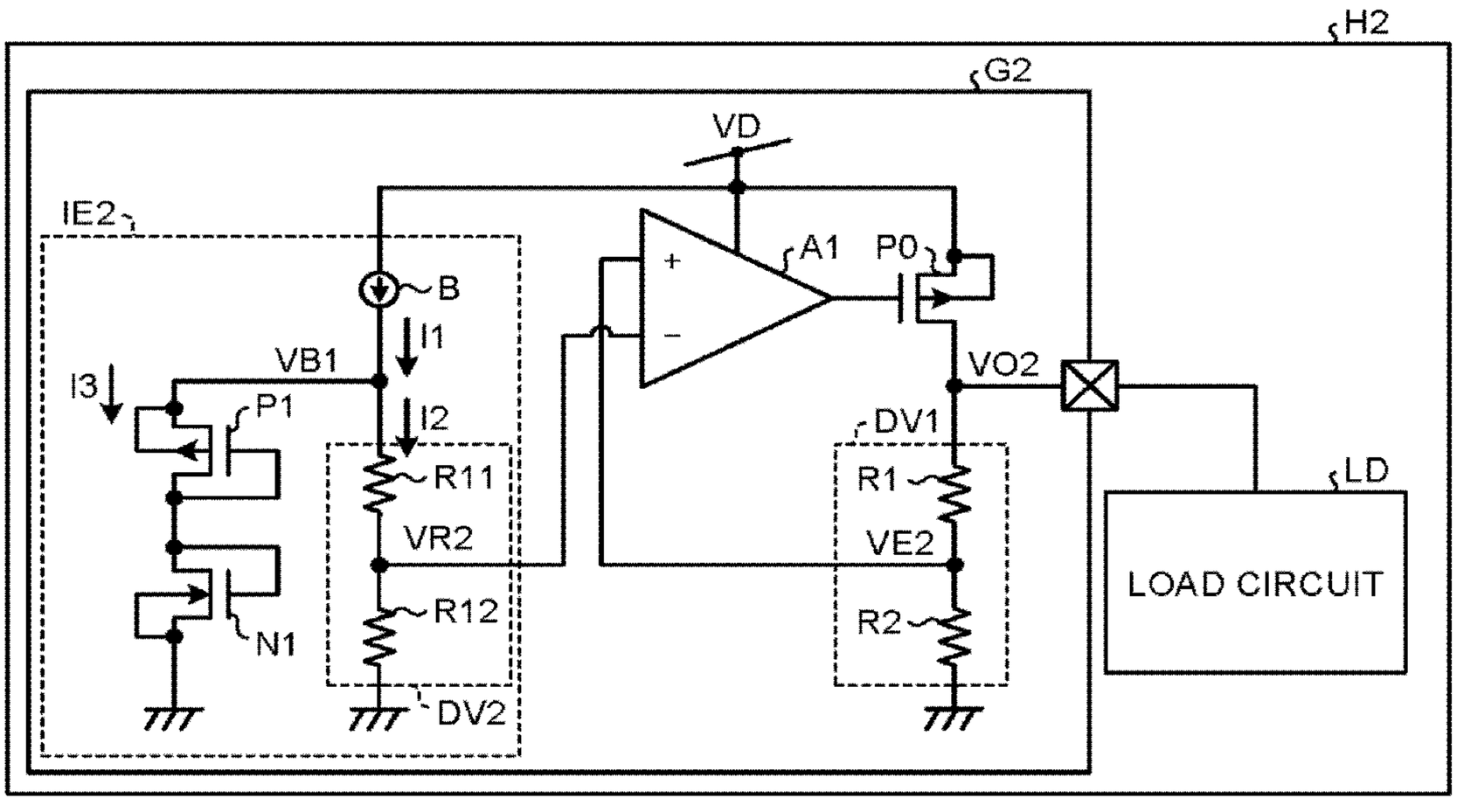

H2
G2
VD
IE2
A1
P0
B
I1
VB1
I3
P1
I2
VO2
DV1
R11
R1
VR2
VE2
LD
R12
R2
N1
DV2
LOAD CIRCUIT

FIG.3

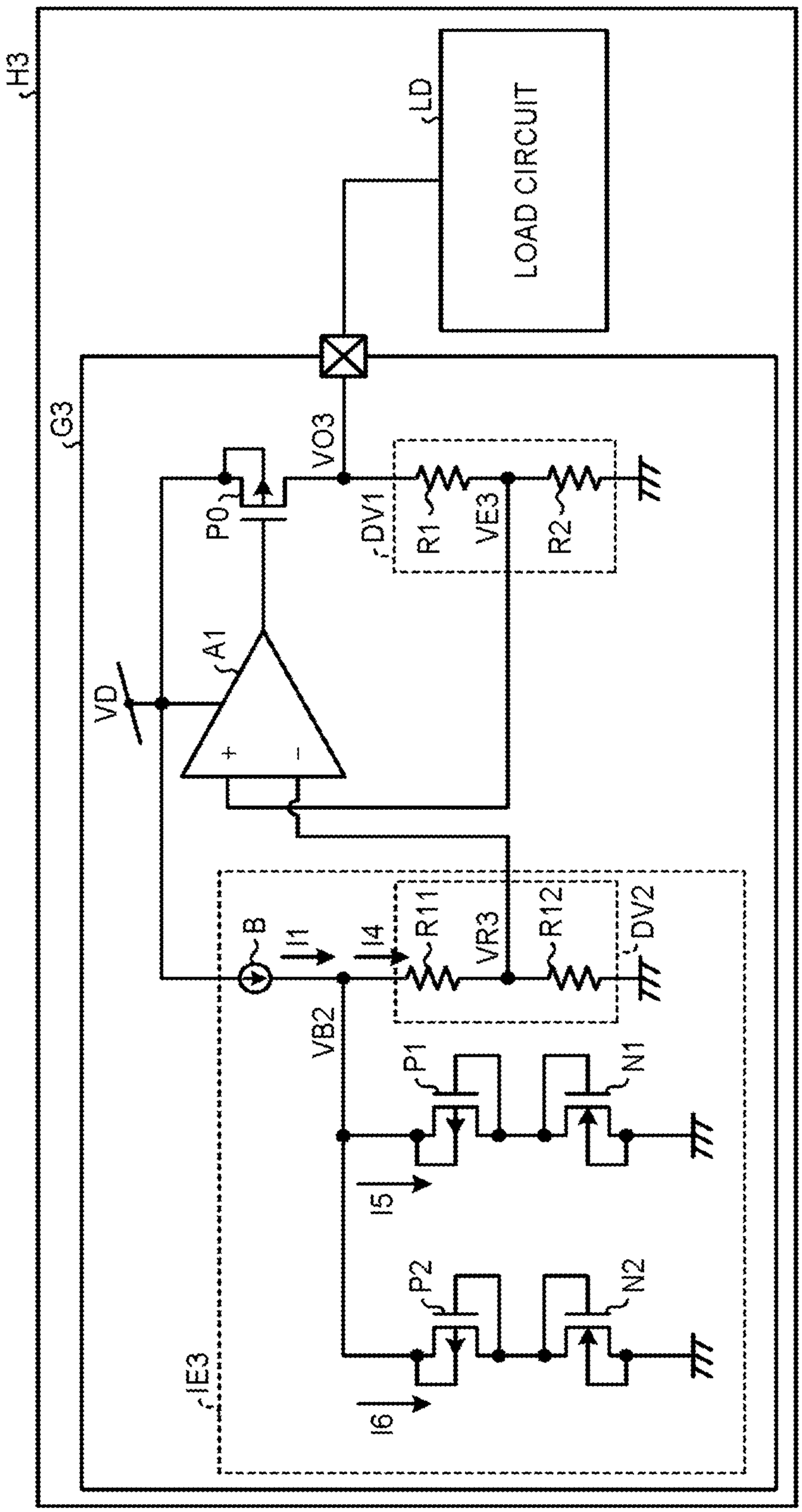

H3
LD
LOAD CIRCUIT
G3
VO3
P0
DV1
R1
VE3
R2
A1
VD
+
−
B
I11
I4
R11
VR3
R12
DV2
VB2
P1
N1
I5
P2
N2
I6
IE3

FIG.4

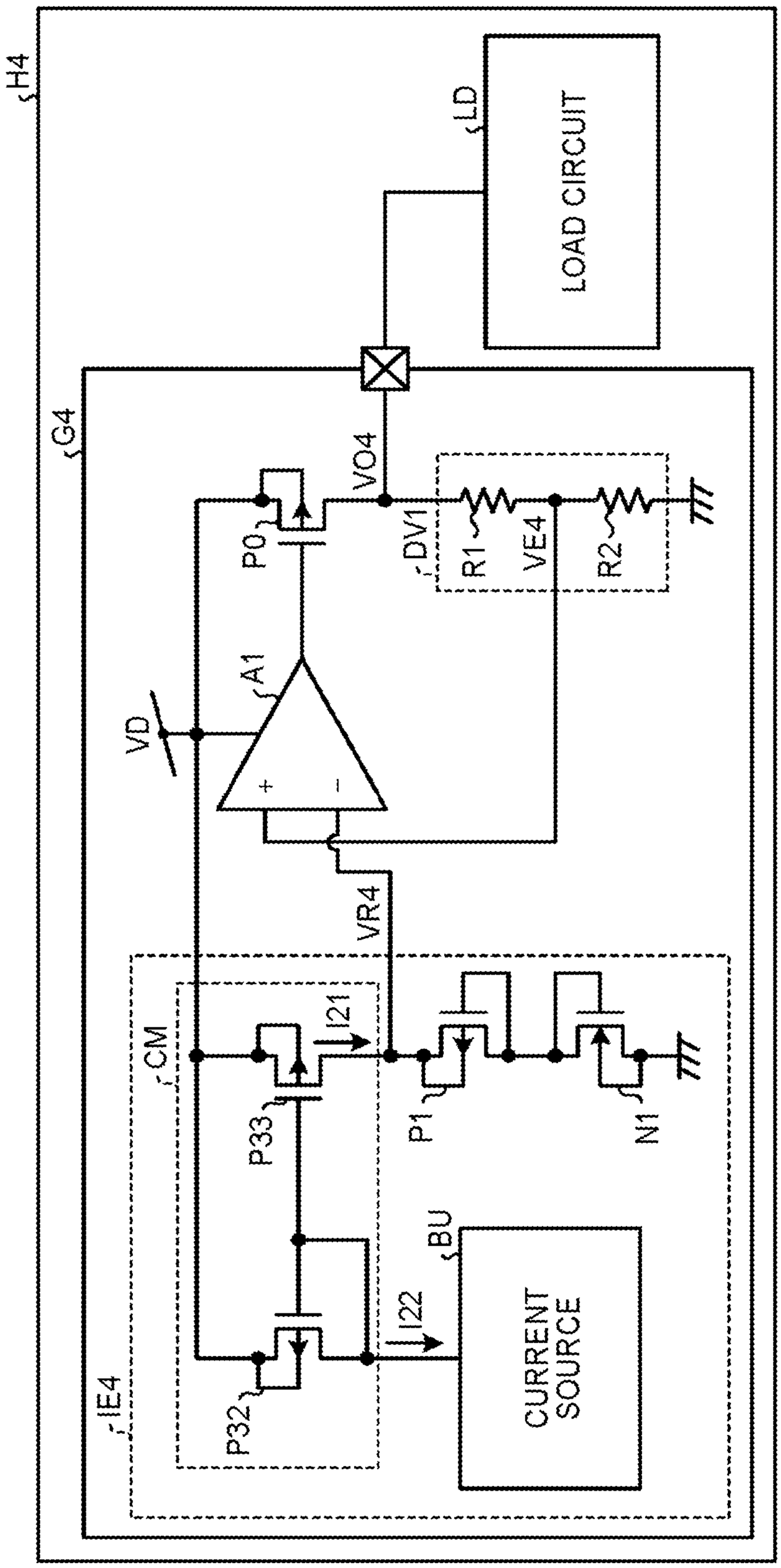

H4
LD
LOAD CIRCUIT
G4
VO4
P0
DV1
R1
VE4
R2
A1
VD
VR4
CM
I21
P33
P1
N1
BU
I22
CURRENT SOURCE
IE4
P32

FIG.5

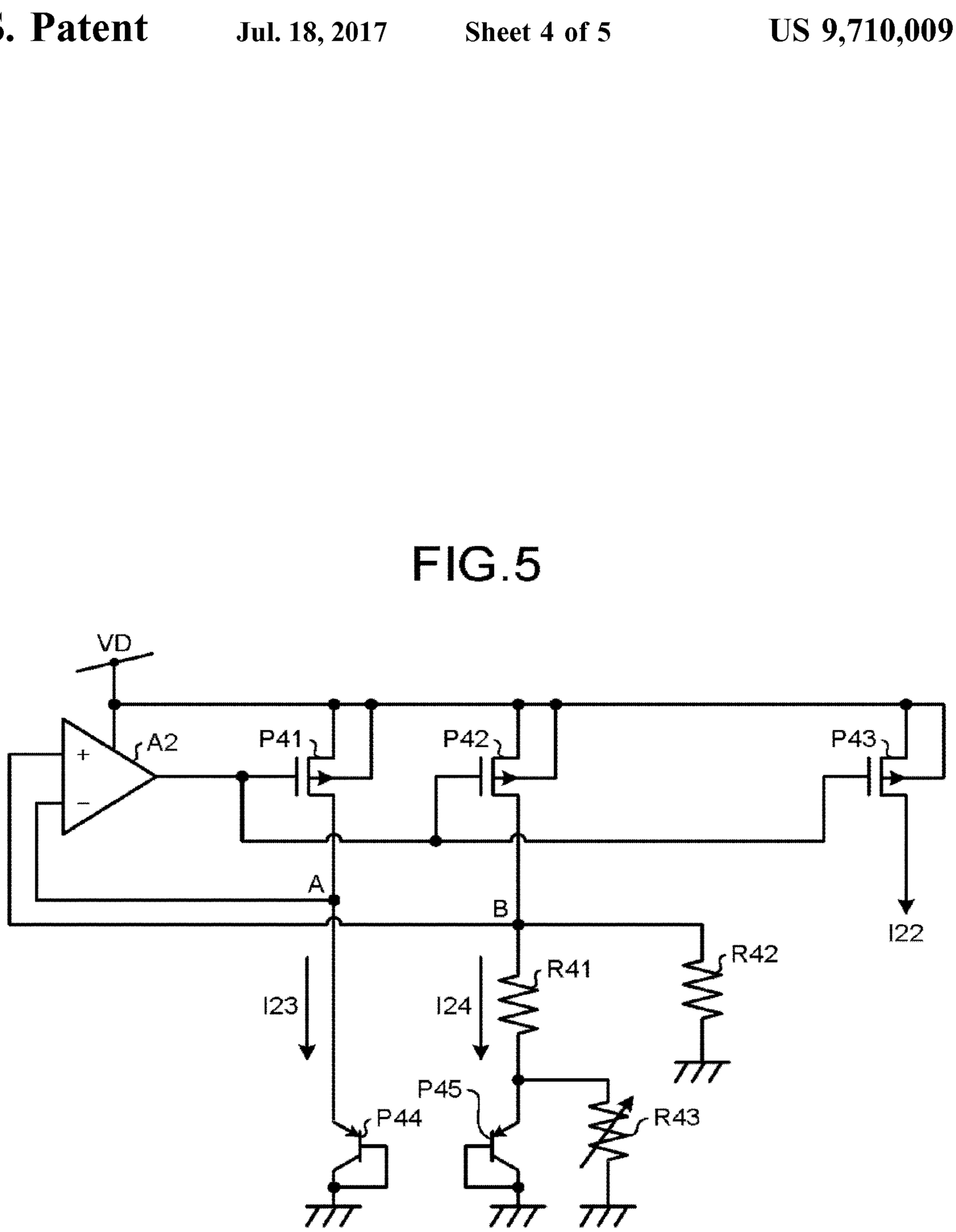
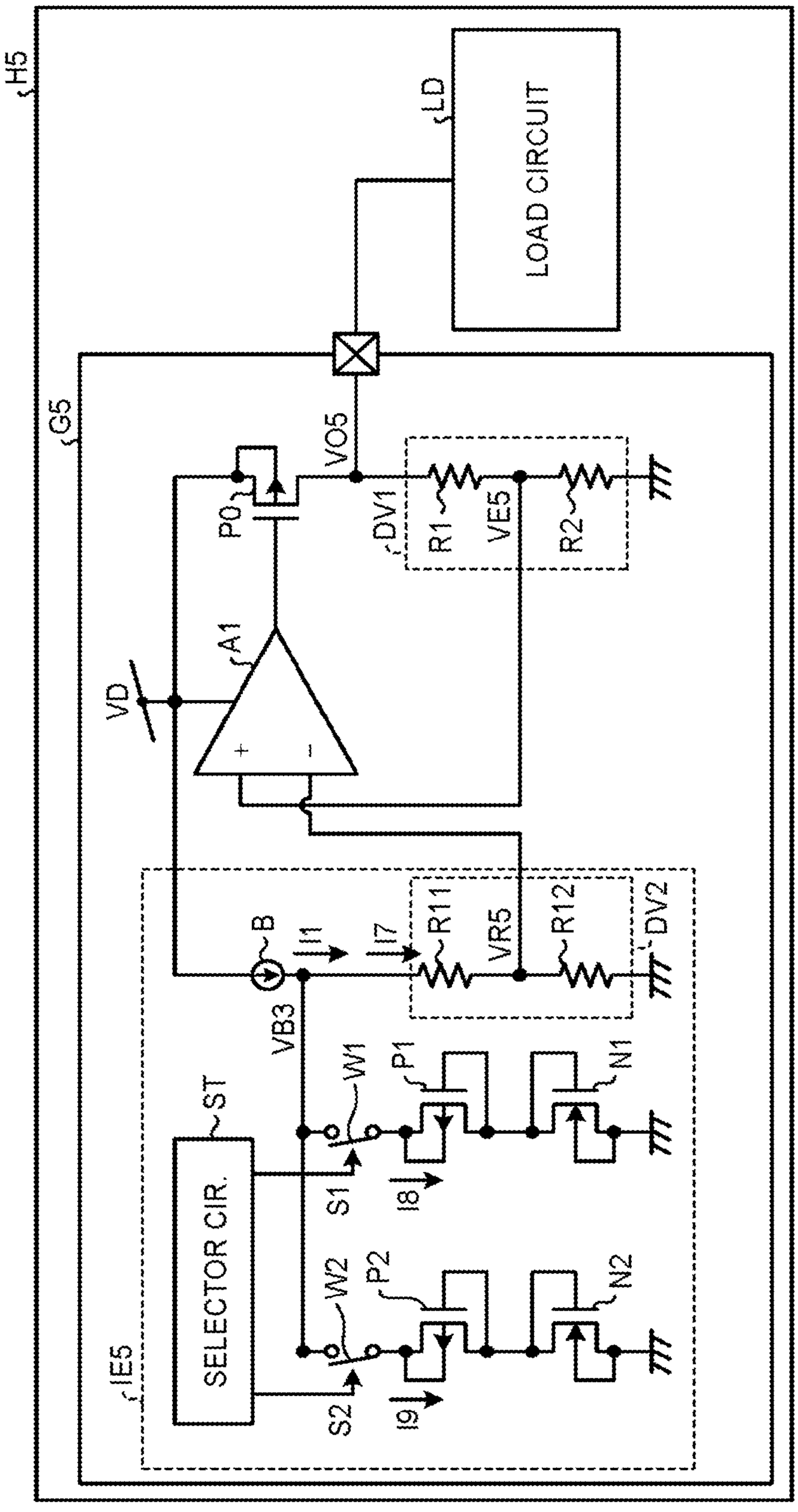


FIG.6


H5
LD
LOAD CIRCUIT
G5
VO5
P0
DV1
R1
VE5
R2
A1
VD
+
-
B
II1
II7
R11
VR5
R12
DV2
VB3
W1
P1
N1
ST
SELECTOR CIR.
S1
I8
W2
P2
N2
IE5
S2
I9

REGULATOR AND SEMICONDUCTOR INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from U.S. Provisional Application No. 62/133,125, filed on Mar. 13, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a regulator and semiconductor integrated circuit.

BACKGROUND

In regulators, in order to keep the output voltage constant, a reference voltage is generated by making a constant current flow through a resistor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram showing the configuration of a regulator according to a first embodiment;

FIG. **2** is a circuit diagram showing the configuration of a regulator according to a second embodiment;

FIG. **3** is a circuit diagram showing the configuration of a regulator according to a third embodiment;

FIG. **4** is a circuit diagram showing the configuration of a regulator according to a fourth embodiment;

FIG. **5** is a circuit diagram showing the configuration of the current source of FIG. **4**; and

FIG. **6** is a circuit diagram showing the configuration of a regulator according to a fifth embodiment.

DETAILED DESCRIPTION

In general, according to one embodiment, a regulator comprises a reference voltage generating circuit that generates a reference voltage, a first voltage dividing circuit that divides a regulator output in voltage, an error amplifier that compares a first divided voltage obtained by dividing the regulator output and the reference voltage, and an output transistor that generates the regulator output based on the output of the error amplifier. The reference voltage generating circuit comprises a constant current source that generates a constant current, and a diode-connected first transistor having the constant current supplied thereto. The reference voltage is generated based on a diode voltage generated by the first transistor.

The regulators and semiconductor integrated circuits according to embodiments will be described in detail below with reference to the accompanying drawings. The present invention is not limited to these embodiments.

First Embodiment

FIG. **1** is a circuit diagram showing the configuration of a regulator according to the first embodiment.

In FIG. **1**, on a semiconductor chip H**1**, there are provided a regulator G**1** and a load circuit LD. In the load circuit LD, there can be provided an integrated circuit including a CMOS circuit and the like. In the regulator G**1**, there are provided a reference voltage generating circuit IE**1** that generates a reference voltage VR**1**, an error amplifier A**1** that

compares a divided voltage VE**1** obtained by dividing a regulator output VO**1** and the reference voltage VR**1**, an output transistor P**0** that generates the regulator output VO**1** based on the output of the error amplifier A**1**, and a voltage dividing circuit DV**1** that divides the regulator output VO**1**. In the reference voltage generating circuit IE**1**, there are provided a constant current source B that generates a constant current I**1**, a diode-connected P-channel transistor P**1**, and a diode-connected N-channel transistor N**1**. Field-effect transistors can be used as the P-channel transistor P**1** and N-channel transistor N**1**. The P-channel transistor P**1** and N-channel transistor N**1** are connected in series. The threshold voltages of the P-channel transistor P**1** and N-channel transistor N**1** can be made to coincide with those of P-channel transistors and N-channel transistors used in the load circuit LD by using transistors having the same type of threshold voltage as transistors used in the load circuit LD. In this case, the dimensions of the P-channel transistor P**1** and N-channel transistor N**1** are preferably set to be equal to those of P-channel transistors and N-channel transistors used in the load circuit LD. As these dimensions, the gate length, gate width, gate insulating film thickness, and so on can be cited. Where P-channel transistors having threshold voltages different from each other are used in the load circuit LD or N-channel transistors having threshold voltages different from each other are used, the average of the threshold voltages of P-channel transistors in the load circuit LD may be used as the threshold voltage of the P-channel transistor P**1**, or the average of the threshold voltages of N-channel transistors in the load circuit LD may be used as the threshold voltage of the N-channel transistor N**1**. Resistors R**1**, R**2** are provided in the voltage dividing circuit DV**1**. The resistors R**1**, R**2** are connected in series. A P-channel field-effect transistor can be used as the output transistor P**0**.

A power supply voltage VD is supplied to the constant current source B, the source of the output transistor P**0**, and the error amplifier A**1**. The regulator output VO**1** is outputted via the drain of the output transistor P**0** and used as the power supply voltage of the load circuit LD. The regulator output VO**1** is divided by the resistors R**1**, R**2**, and the divided voltage VE**1** is outputted via the connection point of the resistors R**1**, R**2**. This divided voltage VE**1** is inputted to the non-inverting input terminal of the error amplifier A**1**. The constant current I**1** is supplied from the constant current source B to the P-channel transistor P**1** and N-channel transistor N**1**. The sum of the diode voltages of the P-channel transistor P**1** and N-channel transistor N**1** at this time is inputted as the reference voltage VR**1** to the inverting input terminal of the error amplifier A**1**. The gate of the output transistor P**0** is driven by the error amplifier A**1** according to the difference between the reference voltage VR**1** and the divided voltage VE**1**, and thus the output of the error amplifier A**1** is set such that the difference between the reference voltage VR**1** and the divided voltage VE**1** approaches zero. Hence, the regulator output VO**1** proportional to the reference voltage VR**1** can be obtained. The proportionality constant for this can be adjusted through the division ratio of the resistors R**1**, R**2**.

Here, in the manufacture process of the semiconductor chips H**1**, variations occur in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD. In this situation, where the regulator output VO**1** is constant, if the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD become higher, then the operation margin of the load circuit LD becomes smaller, so that the performance decreases. On the other hand, if the threshold voltages of

P-channel transistors and N-channel transistors used in the load circuit LD become lower, then the leakage current of the load circuit LD increases, so that the current consumption increases. The dimensions of the output transistor P0 are determined anticipating this increase in the current consumption when designing.

In contrast, by making the regulator output VO1 change according to variations in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD, a decrease in the operation margin of the load circuit LD and an increase in the current consumption can be suppressed. Since the regulator output VO1 is proportional to the reference voltage VR1, by making the reference voltage VR1 change according to variations in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD, the regulator output VO1 can be changed. In the configuration of FIG. 1, the reference voltage VR1 can be given by the sum of the diode voltages of the P-channel transistor P1 and N-channel transistor N1. The diode voltage of the P-channel transistor P1 depends on the threshold voltage of the P-channel transistor P1. The diode voltage of the N-channel transistor N1 depends on the threshold voltage of the N-channel transistor N1. By forming the regulator G1 and the load circuit LD on the same semiconductor chip H1, variations in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD can be reflected in the threshold voltages of the P-channel transistor P1 and N-channel transistor N1. Thus, the regulator output VO1 can be made to follow variations in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD so that the variations in the threshold voltages are absorbed, and hence a decrease in the operation margin of the load circuit LD and an increase in the current consumption can be suppressed. Further, because the dimensions of the output transistor P0 do not need to be increased anticipating an increase in the current consumption of the load circuit LD when the regulator output VO1 is constant, the dimensions of the output transistor P0 can be made smaller.

Second Embodiment

FIG. 2 is a circuit diagram showing the configuration of a regulator according to the second embodiment.

In FIG. 2, on a semiconductor chip H2, there are provided a regulator G2 and a load circuit LD. In the regulator G2, a reference voltage generating circuit IE2 is provided instead of the reference voltage generating circuit IE1 of the regulator G1 in FIG. 1. A voltage dividing circuit DV2 that divides a diode voltage VB1 is added to the reference voltage generating circuit IE2. Resistors R11, R12 are provided in the voltage dividing circuit DV2. The resistors R11, R12 are connected in series. Other than that, the regulator G2 can be configured in the same way as in FIG. 1.

A regulator output VO2 is outputted via the drain of the output transistor P0 and used as the power supply voltage of the load circuit LD. The regulator output VO2 is divided by the resistors R1, R2, and a divided voltage VE2 is outputted via the connection point of the resistors R1, R2. This divided voltage VE2 is inputted to the non-inverting input terminal of the error amplifier A1. The constant current I1 is outputted from the constant current source B, and a current I2 is supplied to the voltage dividing circuit DV2, and a current I3 is supplied to the P-channel transistor P1 and N-channel transistor N1. The diode voltage VB1 that is the sum of the diode voltages of the P-channel transistor P1 and N-channel transistor N1 at this time is divided by the resistors R11, R12, and a divided voltage outputted via the connection point of the resistors R11, R12 is inputted as a reference voltage VR2 to the inverting input terminal of the error amplifier A1. The gate of the output transistor P0 is driven by the error amplifier A1 according to the difference between the reference voltage VR2 and the divided voltage VE2, and thus the output of the error amplifier A1 is set such that the difference between the reference voltage VR2 and the divided voltage VE2 approaches zero.

Here, by connecting the resistors R11, R12 in parallel with the P-channel transistor P1 and N-channel transistor N1, the temperature dependence of the reference voltage VR2 can be made smaller than that of the reference voltage VR1, and thus the temperature dependence of the regulator output VO2 can be made smaller.

Third Embodiment

FIG. 3 is a circuit diagram showing the configuration of a regulator according to the third embodiment.

In FIG. 3, on a semiconductor chip H3, there are provided a regulator G3 and a load circuit LD. In the regulator G3, a reference voltage generating circuit IE3 is provided instead of the reference voltage generating circuit IE2 of the regulator G2 in FIG. 2. A diode-connected P-channel transistor P2 and a diode-connected N-channel transistor N2 is added to the reference voltage generating circuit IE3. The P-channel transistor P2 and N-channel transistor N2 are connected in series. The series circuit of the P-channel transistor P1 and N-channel transistor N1 can be connected in parallel with the series circuit of the P-channel transistor P2 and N-channel transistor N2. The threshold voltages of the P-channel transistor P2 and N-channel transistor N2 can be made different from the threshold voltages of the P-channel transistor P1 and N-channel transistor N1. Other than that, the regulator G3 can be configured in the same way as in FIG. 2.

A regulator output VO3 is outputted via the drain of the output transistor P0 and used as the power supply voltage of the load circuit LD. The regulator output VO3 is divided by the resistors R1, R2, and a divided voltage VE3 is outputted via the connection point of the resistors R1, R2. This divided voltage VE3 is inputted to the non-inverting input terminal of the error amplifier A1. The constant current I1 is outputted from the constant current source B; a current I4 is supplied to the voltage dividing circuit DV2; a current I5 is supplied to the P-channel transistor P1 and N-channel transistor N1; and a current I6 is supplied to the P-channel transistor P2 and N-channel transistor N2. The average VB2 of a diode voltage that is the sum of the diode voltages of the P-channel transistor P1 and N-channel transistor N1 at this time and of a diode voltage that is the sum of the diode voltages of the P-channel transistor P2 and N-channel transistor N2 at this time is divided by the resistors R11, R12, and a divided voltage outputted via the connection point of the resistors R11, R12 is inputted as a reference voltage VR3 to the inverting input terminal of the error amplifier A1. The gate of the output transistor P0 is driven by the error amplifier A1 according to the difference between the reference voltage VR3 and the divided voltage VE3, and thus the output of the error amplifier A1 is set such that the difference between the reference voltage VR3 and the divided voltage VE3 approaches zero.

Here, by using the average of the diode voltages of transistors having different threshold voltages as the reference voltage VR3, also where transistors having different

threshold voltages are used in the load circuit LD, the accuracy of the regulator output VO3 in following variations can be improved so that the variations in those threshold voltages are effectively absorbed.

Fourth Embodiment

FIG. **4** is a circuit diagram showing the configuration of a regulator according to the fourth embodiment.

In FIG. **4**, on a semiconductor chip H**4**, there are provided a regulator G**4** and a load circuit LD. In the regulator G**4**, a reference voltage generating circuit IE**4** is provided instead of the reference voltage generating circuit IE**1** of the regulator G**1** in FIG. **1**. In the reference voltage generating circuit IE**4**, a current source BU whose temperature characteristic is adjustable and a current mirror circuit CM that performs current mirror operation for a constant current I**22** generated by the current source BU are provided instead of the constant current source B of FIG. **1**. The current source BU can reduce the temperature dependence of a constant current I**21**. P-channel transistors P**32**, P**33** are provided in the current mirror circuit CM. The gates of the P-channel transistors P**32**, P**33** are connected to the drain of the P-channel transistor P**32**. The power supply voltage VD is supplied to the sources of the P-channel transistors P**32**, P**33**.

A regulator output VO**4** is outputted via the drain of the output transistor P**0** and used as the power supply voltage of the load circuit LD. The regulator output VO**4** is divided by the resistors R**1**, R**2**, and a divided voltage VE**4** is outputted via the connection point of the resistors R**1**, R**2**. This divided voltage VE**4** is inputted to the non-inverting input terminal of the error amplifier A**1**. The constant current I**22** is generated by the current source BU and inputted to the current mirror circuit CM. In the current mirror circuit CM, current mirror operation for a constant current I**22** is performed, so that the constant current I**21** is generated and supplied to the P-channel transistor P**1** and N-channel transistor N**1**. A diode voltage that is the sum of the diode voltages of the P-channel transistor P**1** and N-channel transistor N**1** at this time is inputted as a reference voltage VR**4** to the inverting input terminal of the error amplifier A**1**. The gate of the output transistor P**0** is driven by the error amplifier A**1** according to the difference between the reference voltage VR**4** and the divided voltage VE**4**, and thus the output of the error amplifier A**1** is set such that the difference between the reference voltage VR**4** and the divided voltage VE**4** approaches zero.

Here, by reducing the temperature dependence of a constant current I**21**, the temperature characteristic of only the P-channel transistor P**1** and N-channel transistor N**1** can be reflected in the reference voltage VR**4**. Thus, the correspondence between the temperature characteristic of the P-channel transistors and N-channel transistors used in the load circuit LD and the temperature characteristic of the reference voltage VR**4** can be made highly accurate, and therefore the accuracy of the regulator output VO**4** in following variations can be improved so that the variations in their threshold voltages are effectively absorbed.

Although the voltage dividing circuit DV**2** of FIG. **2** is not provided in the example of FIG. **4**, the voltage dividing circuit DV**2** of FIG. **2** may be provided.

FIG. **5** is a circuit diagram showing the configuration of the current source of FIG. **4**.

In FIG. **5**, in this current source BU, there are provided an error amplifier A**2**, P-channel transistors P**41** to P**45**, resistors R**41**, R**42**, and a variable resistor R**43**. Field-effect transistors can be used as the P-channel transistors P**41** to P**43**, and bipolar transistors can be used as the P-channel transistors P**44**, P**45**. The P-channel transistors P**41**, P**44** are connected in series, and the resistor R**41** and the P-channel transistors P**42**, P**45** are connected in series. The connection point of the P-channel transistors P**41**, P**44** is connected to the inverting input terminal of the error amplifier A**2**, and the connection point of the resistor R**41** and the P-channel transistor P**42** is connected to the non-inverting input terminal of the error amplifier A**2**. Further, the resistor R**42** is connected to the connection point of the resistor R**41** and the P-channel transistor P**42**, and the variable resistor R**43** is connected to the connection point of the resistor R**41** and the P-channel transistor P**45**. The output of the error amplifier A**2** is connected to the gates of the P-channel transistors P**41** to P**43**. The power supply voltage VD is supplied to the error amplifier A**2** and the sources of the P-channel transistors P**41** to P**43**.

The inverting input potential A of the error amplifier A**2** is set by a current I**23** flowing through the P-channel transistor P**44**, and the non-inverting input potential B of the error amplifier A**2** is set by a current I**24** flowing through the resistor R**41** and distributed to the P-channel transistor P**45** and the variable resistor R**43**. The output of the error amplifier A**2** is set according to the difference between the inverting input potential A and the non-inverting input potential B, and the gate of the P-channel transistor P**43** is driven by that output to generate the constant current I**22**. At this time, since the P-channel transistors P**44**, P**45** have a temperature characteristic, the inverting input potential A and the non-inverting input potential B vary due to temperature change. Because the variable resistor R**43** is connected in parallel with the P-channel transistor P**45**, a variation in the non-inverting input potential B due to the temperature characteristic of the P-channel transistor P**45** can be adjusted for by varying the variable resistor R**43**. At this time, by adjusting the variable resistor R**43**, the temperature characteristic curve of the P-channel transistor P**45** can be made to coincide with that of the P-channel transistor P**44**. Thus, in the error amplifier A**2**, a variation in the inverting input potential A and a variation in the non-inverting input potential B due to temperature change can be made to cancel out, so that the temperature dependence of the constant current I**22** can be reduced.

Fifth Embodiment

FIG. **6** is a circuit diagram showing the configuration of a regulator according to the fifth embodiment.

In FIG. **6**, on a semiconductor chip H**5**, there are provided a regulator G**5** and a load circuit LD. In the regulator G**5**, a reference voltage generating circuit IE**5** is provided instead of the reference voltage generating circuit IE**3** of the regulator G**3** in FIG. **3**. Switches W**1**, W**2** and a selector circuit ST are added to the reference voltage generating circuit IE**5**. The switch W**1** is provided between a series circuit of a P-channel transistor P**1** and N-channel transistor N**1** and a constant current source B. The switch W**2** is provided between a series circuit of a P-channel transistor P**2** and N-channel transistor N**2** and the constant current source B. The selector circuit ST outputs selecting signals S**1**, S**2** to the switches W**1**, W**2** to set the switches W**1**, W**2** to be on or off. The selector circuit ST may be constituted by fuses, an EEPROM, or a logic circuit.

The regulator G**5** and load circuit LD can be made to operate according to the on/off states of the switches W**1**,

W2, and the on/off states of the switches W1, W2 can be registered in the selector circuit ST so as to optimize a regulator output VO5.

The regulator output VO5 is outputted via the drain of the output transistor P0 and used as the power supply voltage of the load circuit LD. The regulator output VO5 is divided by the resistors R1, R2, and a divided voltage VE5 is outputted via the connection point of the resistors R1, R2. This divided voltage VE5 is inputted to the non-inverting input terminal of the error amplifier A1. A constant current I1 is outputted from the constant current source B, and a current I7 is supplied to a voltage dividing circuit DV2. If the switch W1 is turned on, a current I8 is supplied to the P-channel transistor P1 and N-channel transistor N1. If the switch W2 is turned on, a current I9 is supplied to the P-channel transistor P2 and N-channel transistor N2. A diode voltage that is the sum of the diode voltages of the P-channel transistor P1 and N-channel transistor N1 or a diode voltage that is the sum of the diode voltages of the P-channel transistor P2 and N-channel transistor N2 is divided by the resistors R11, R12 depending on the on/off of the switches W1, W2, and a divided voltage outputted via the connection point of the resistors R11, R12 is inputted as a reference voltage VR5 to the inverting input terminal of the error amplifier A1. The gate of the output transistor P0 is driven by the error amplifier A1 according to the difference between the reference voltage VR5 and the divided voltage VE5, and thus the output of the error amplifier A1 is set such that the difference between the reference voltage VR5 and the divided voltage VE5 approaches zero.

Here, by optimizing the regulator output VO5 based on the actual operation state of the regulator G5 and the load circuit LD, a decrease in the operation margin of the load circuit LD and an increase in the current consumption can be suppressed even if the load circuit LD operates in an unexpected manner according to variations in the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD. Further, also where the regulator G5 and the load circuit LD are incorporated in separate chips, or so on, so that the variation distribution of the threshold voltages of the P-channel transistor P1 and N-channel transistor N1 used in the regulator G5 and the variation distribution of the threshold voltages of P-channel transistors and N-channel transistors used in the load circuit LD are different, the regulator output VO5 can be optimized.

Although in the above embodiment the configuration is shown where only two series circuits of the diode-connected P-channel transistor and diode-connected N-channel transistor connected in series are connected in parallel, M number (M is an integer of two or greater) of series circuits of the diode-connected P-channel transistor and diode-connected N-channel transistor connected in series may be connected in parallel. In this case, the threshold voltages of the P-channel transistor and N-channel transistor can be set to be different for each series circuit. Further, the current source BU and the current mirror circuit CM of FIG. **4** may be used instead of the constant current source B of FIGS. **1**, **2**, **3**, and **6**.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A regulator comprising:

a reference voltage generating circuit that generates a reference voltage;

a first voltage dividing circuit that divides a regulator output in voltage;

an error amplifier that compares a first divided voltage obtained by dividing the regulator output and the reference voltage; and

an output transistor that generates the regulator output based on the output of the error amplifier,

wherein the reference voltage generating circuit comprises:

a constant current source that generates a constant current; and

a diode-connected first transistor having the constant current supplied thereto,

wherein the reference voltage is generated based on a diode voltage generated by the first transistor, the first transistor comprising:

a diode-connected P-channel transistor; and

a diode-connected N-channel transistor connected in series to the P-channel transistor, and

wherein the diode voltage of the first transistor is given by the sum of the diode voltage of the P-channel transistor and the diode voltage of the N-channel transistor.

2. The regulator according to claim **1**, wherein the first voltage dividing circuit comprises:

a first resistor; and

a second resistor connected in series to the first resistor, and

wherein the first divided voltage is outputted via the connection point of the first resistor and the second resistor.

3. The regulator according to claim **1**, comprising:

a second voltage dividing circuit that divides the diode voltage of the first transistor,

wherein the reference voltage is a second divided voltage obtained by dividing the diode voltage of the first transistor.

4. The regulator according to claim **3**, wherein the second voltage dividing circuit comprises:

a third resistor; and

a fourth resistor connected in series to the third resistor, and

wherein the second divided voltage is outputted via the connection point of the third resistor and the fourth resistor.

5. The regulator according to claim **1**, wherein the first transistor comprises:

M number (M is an integer of two or greater) of series circuits of a diode-connected P-channel transistor and a diode-connected N-channel transistor connected in series that are connected in parallel,

wherein the threshold voltages of the P-channel transistor and the N-channel transistor are set to be different for each of the series circuits, and

wherein the diode voltage of the first transistor is a voltage on a connection point of the parallel connection.

6. The regulator according to claim **5**, comprising a selector circuit that selects one or a number, no greater than M−1, of series circuits from the M number of series circuits.

7. The regulator according to claim **6**, wherein the selector circuit selects the series circuits according to thresholds of

P-channel transistors and N-channel transistors of a load circuit to which the regulator output is supplied.

8. The regulator according to claim **1**, wherein the constant current source comprises:

a current source whose temperature characteristic is adjustable; and

a current mirror circuit that performs current mirror operation for a current generated by the current source to generate the constant current.

9. The regulator according to claim **8**, wherein the current source comprises a variable resistor that can be adjusted to reduce the temperature dependence of the constant current.

10. A semiconductor integrated circuit comprising:

a reference voltage generating circuit that generates a reference voltage;

a first voltage dividing circuit that divides a regulator output in voltage;

an error amplifier that compares a first divided voltage obtained by dividing the regulator output and the reference voltage;

an output transistor that generates the regulator output based on the output of the error amplifier; and

a load circuit to which the regulator output is supplied,

wherein the reference voltage generating circuit comprises:

a constant current source that generates a constant current; and

a diode-connected first transistor having the constant current supplied thereto,

wherein the reference voltage is generated based on a diode voltage generated by the first transistor, the first transistor comprising:

a diode-connected P-channel transistor; and

a diode-connected N-channel transistor connected in series to the P-channel transistor, and

wherein the diode voltage of the first transistor is given by the sum of the diode voltage of the P-channel transistor and the diode voltage of the N-channel transistor.

11. The semiconductor integrated circuit according to claim **10**, wherein the reference voltage generating circuit, the first voltage dividing circuit, the error amplifier, the output transistor, and the load circuit are formed on the same semiconductor chip.

12. The semiconductor integrated circuit according to claim **11**, wherein the first voltage dividing circuit comprises:

a first resistor; and

a second resistor connected in series to the first resistor, and

wherein the first divided voltage is outputted via the connection point of the first resistor and the second resistor.

13. The semiconductor integrated circuit according to claim **11**, comprising:

a second voltage dividing circuit that divides the diode voltage of the first transistor,

wherein the reference voltage is a second divided voltage obtained by dividing the diode voltage of the first transistor.

14. The semiconductor integrated circuit according to claim **13**, wherein the second voltage dividing circuit comprises:

a third resistor; and

a fourth resistor connected in series to the third resistor, and

wherein the second divided voltage is outputted via the connection point of the third resistor and the fourth resistor.

15. The semiconductor integrated circuit according to claim **11**, wherein the constant current source comprises:

a current source whose temperature characteristic is adjustable; and

a current mirror circuit that performs current mirror operation for a current generated by the current source to generate the constant current.

16. The semiconductor integrated circuit according to claim **15**, wherein the current source comprises a variable resistor that can be adjusted to reduce the temperature dependence of the constant current.

17. The semiconductor integrated circuit according to claim **10**, wherein the first transistor comprises:

M number (M is an integer of two or greater) of series circuits of a diode-connected P-channel transistor and a diode-connected N-channel transistor connected in series that are connected in parallel,

wherein the threshold voltages of the P-channel transistor and the N-channel transistor are set to be different for each of the series circuits, and

wherein the diode voltage of the first transistor is a voltage on a connection point of the parallel connection.

18. The semiconductor integrated circuit according to claim **10**, comprising a selector circuit that selects one or a number, no greater than M−1, of series circuits from the M number of series circuits.

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