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(54) **TFD I/O PARTITION FOR HIGH-SPEED, HIGH-DENSITY APPLICATIONS**

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CPC ***G11C 5/02*** (2013.01); ***G11C 5/063*** (2013.01); ***G11C 11/408*** (2013.01); ***H01L 25/0652*** (2013.01); *G11C 5/06* (2013.01); *G11C 8/00* (2013.01); *H01L 2225/0651* (2013.01); *H01L 2225/06562* (2013.01)

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(57) **ABSTRACT**

A microelectronic package can include a substrate having first and second surfaces, first, second, and third microelectronic elements each having a surface facing the first surface, terminals exposed at the second surface, and leads electrically connected between contacts of each microelectronic element and the terminals. The substrate can have first, second, and third spaced-apart apertures having first, second, and third parallel axes extending in directions of the lengths of the apertures. The contacts of the first, second, and third microelectronic elements can be aligned with one of the first, second, or third apertures. The terminals can include first and second sets of first terminals configured to carry address information. The first set can be connected with the first and third microelectronic elements and not with the second microelectronic element, and the second set can be connected with the second microelectronic element and not with the first or third microelectronic elements.

9 Claims, 5 Drawing Sheets

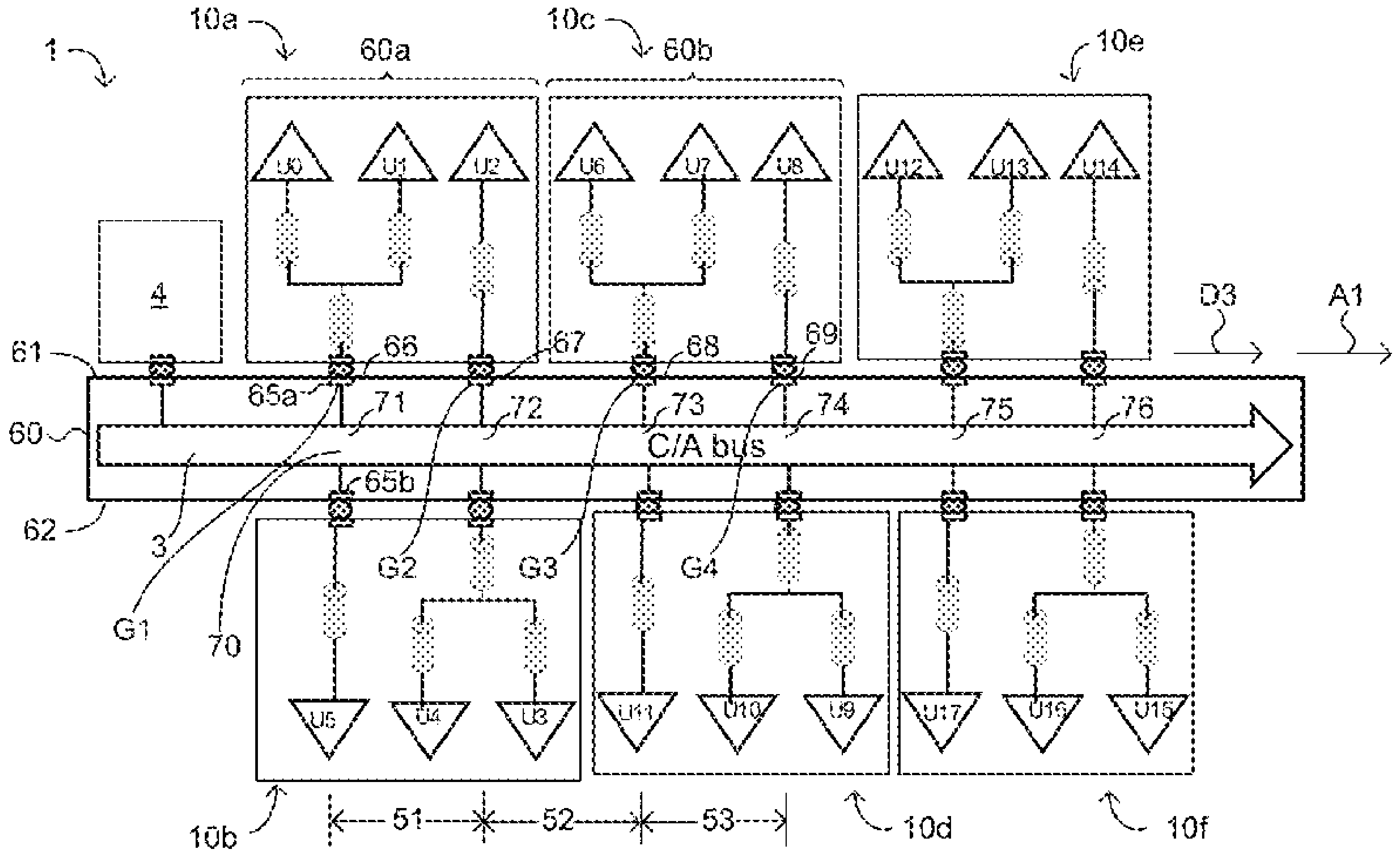

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FIG. 1A

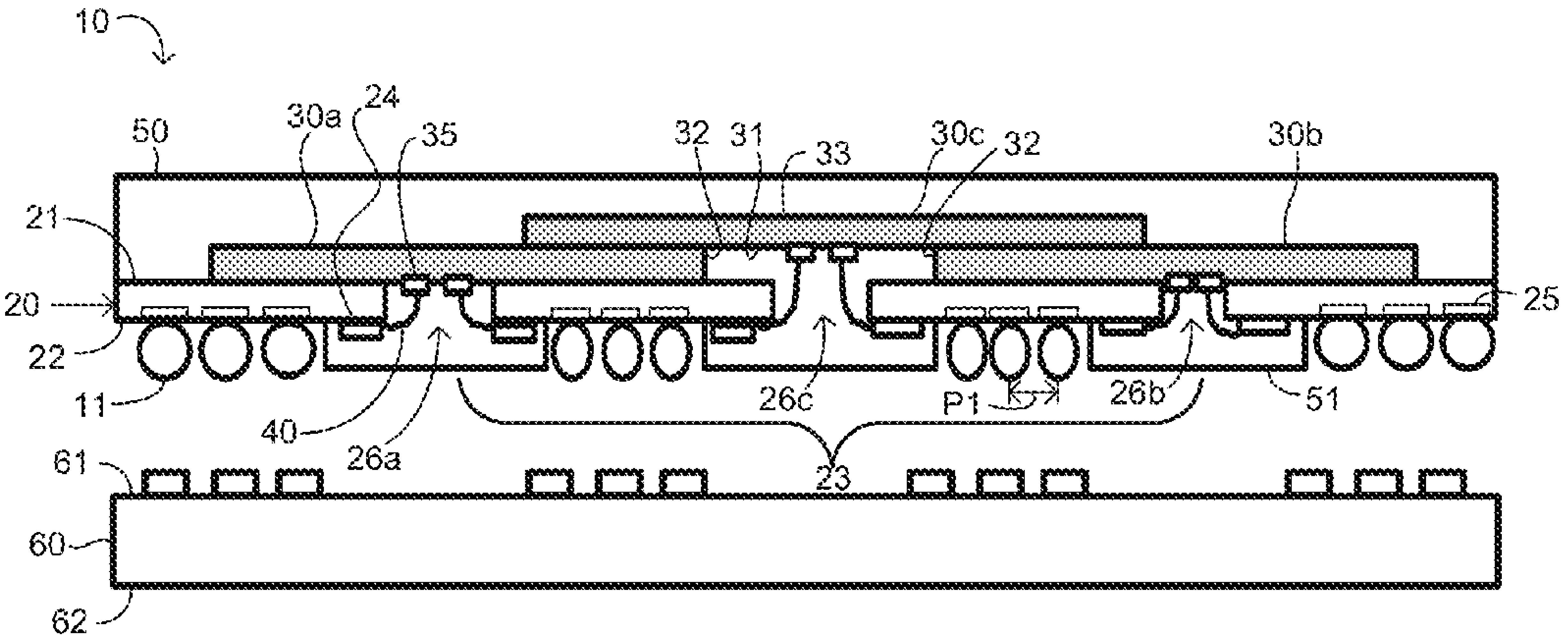

10
50
30a
24
35
32
31
33
30c
32
30b
21
20
25
22
11
40
26a
26c
P1
26b
51
23
61
60
62

FIG. 1B

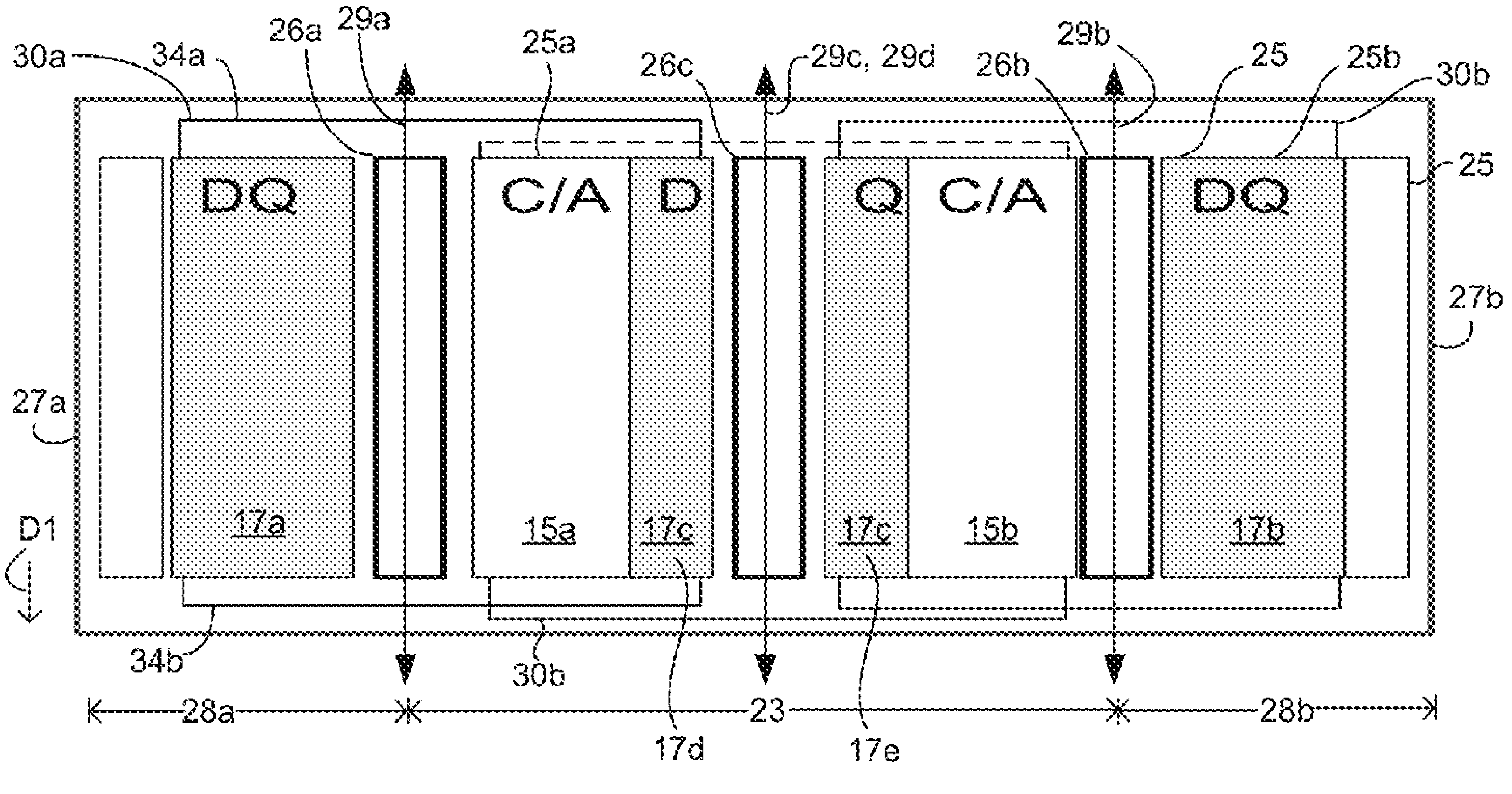

30a
34a
26a
29a
25a
26c
29c, 29d
26b
29b
25
25b
30b
25
DQ
C/A
D
Q
C/A
DQ
27b
27a
D1
17a
15a
17c
17c
15b
17b
34b
30b
28a
23
28b
17d
17e

FIG. 1C

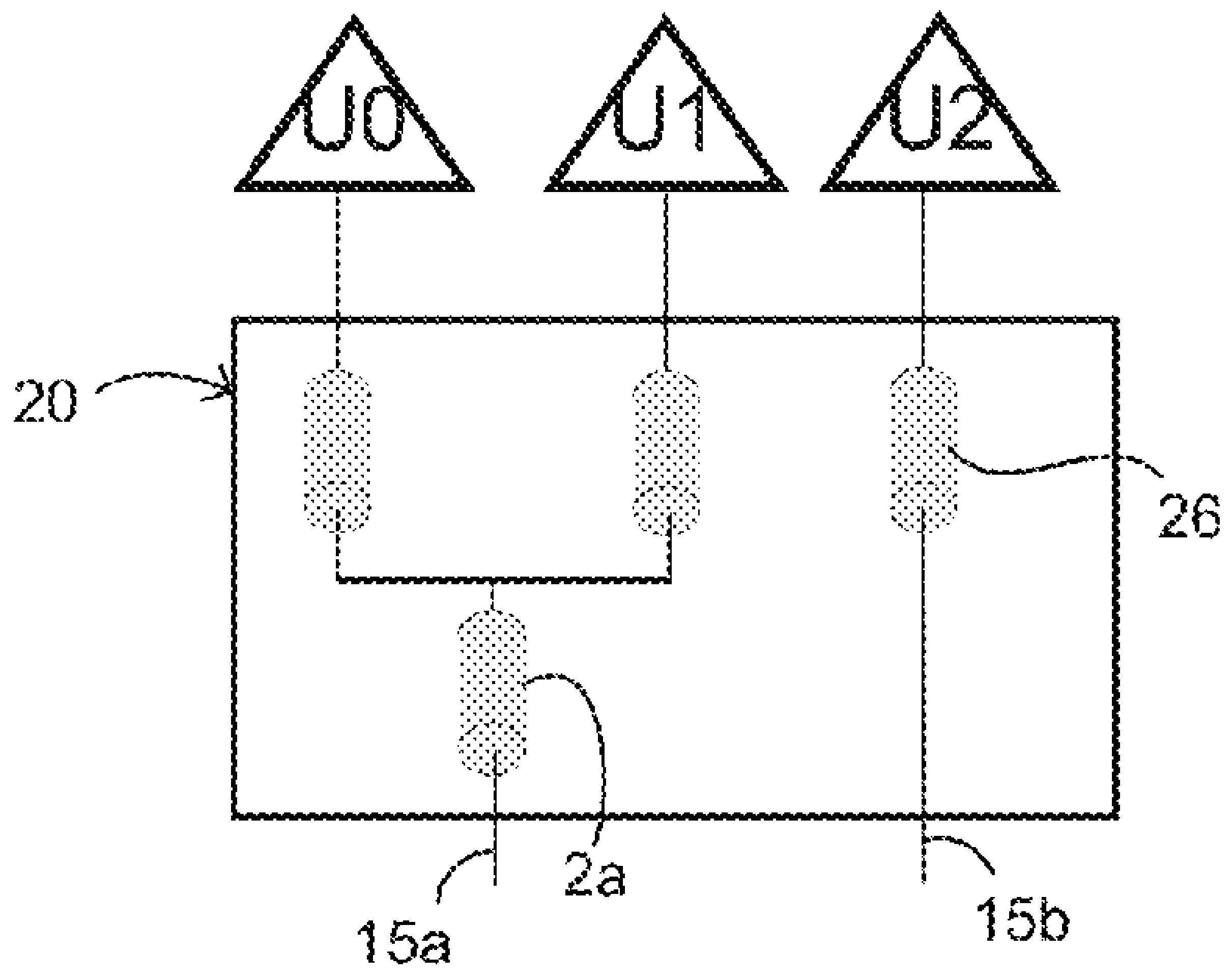


FIG. 1D

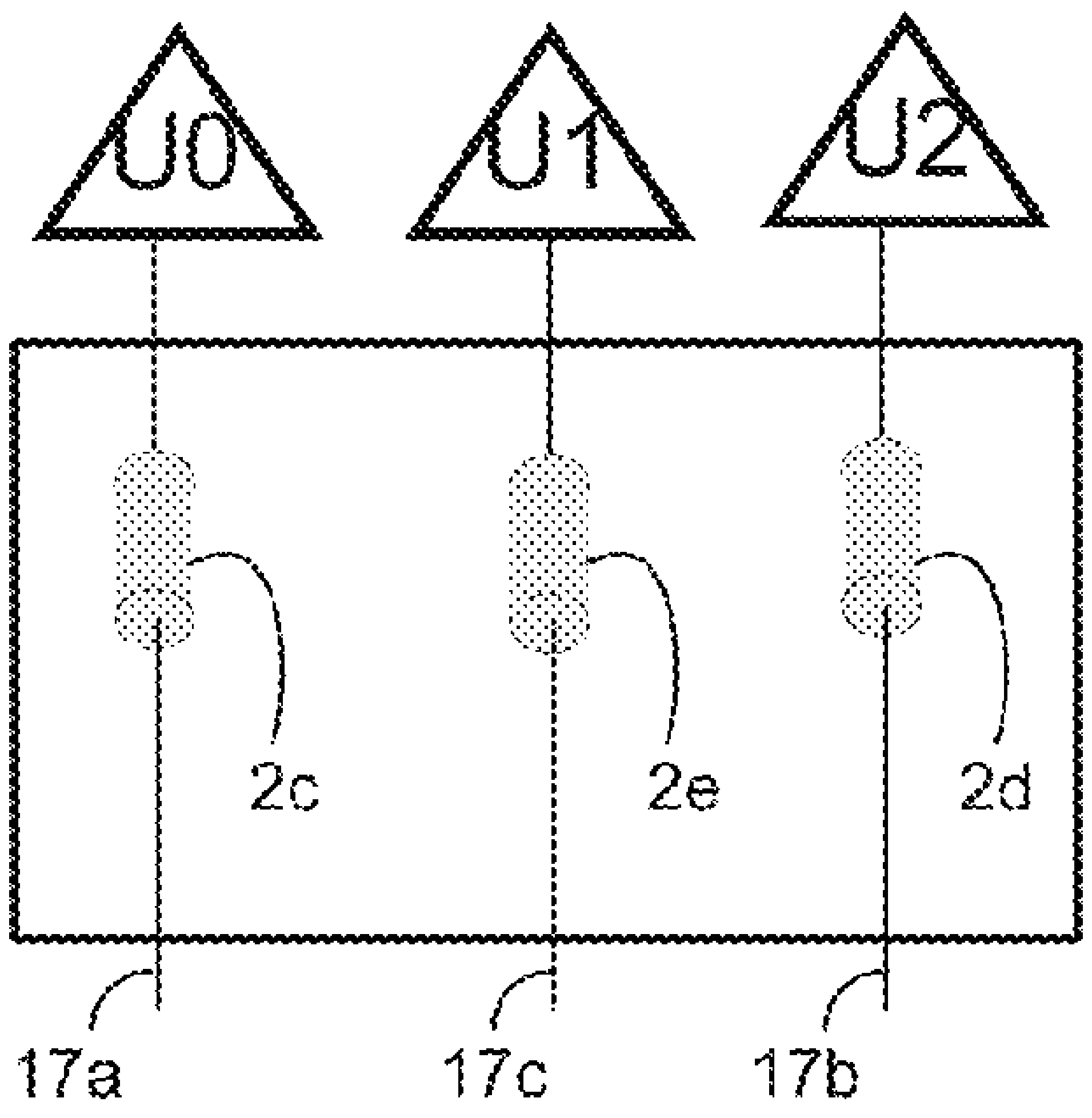


FIG. 1E

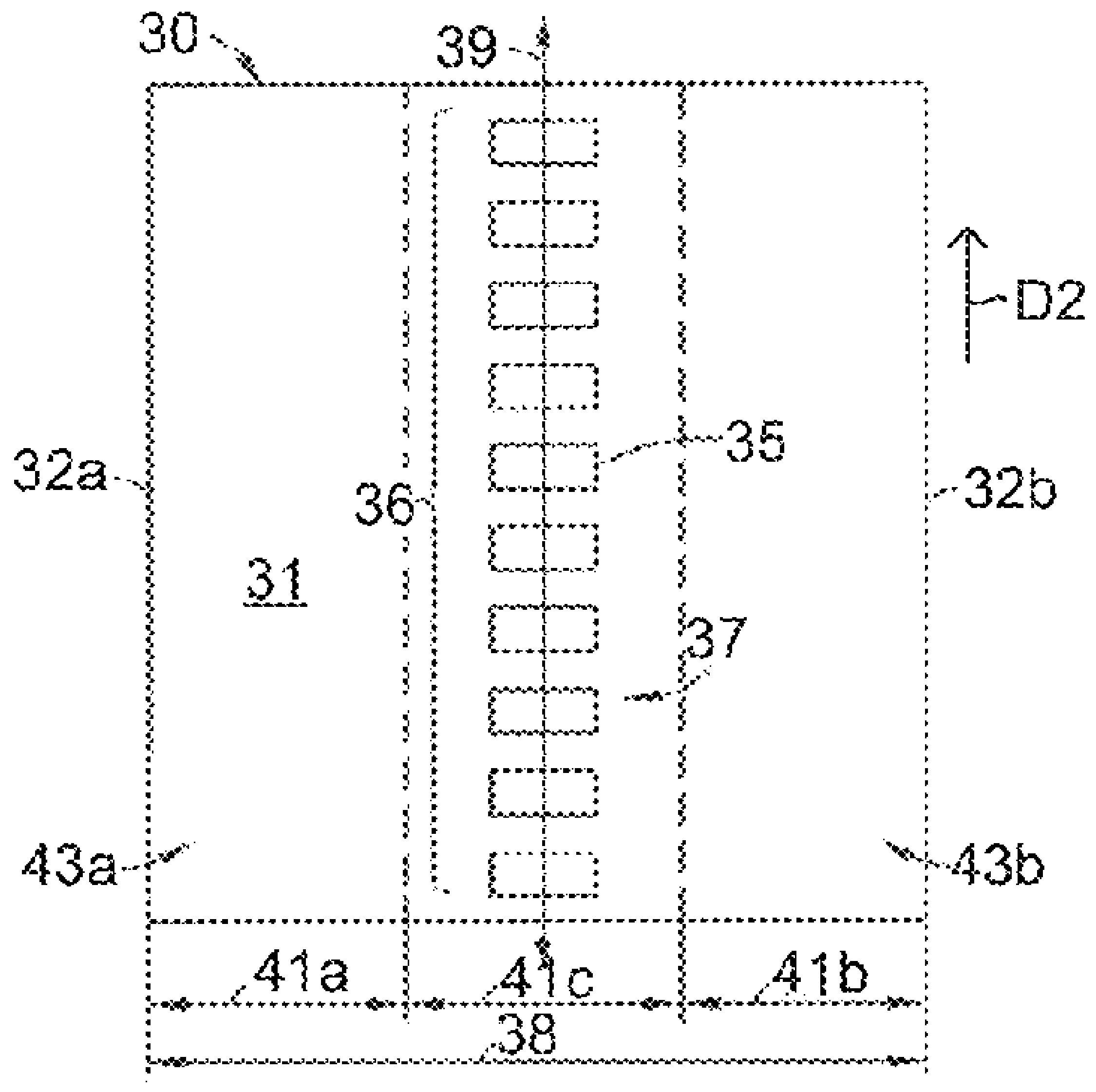
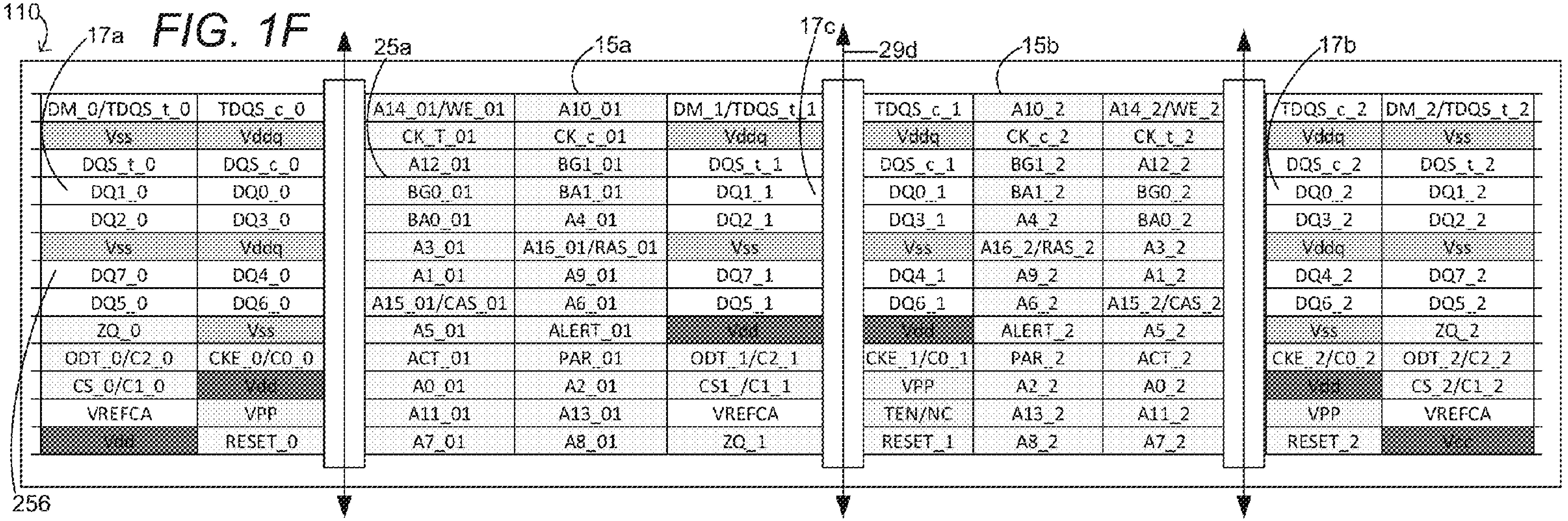
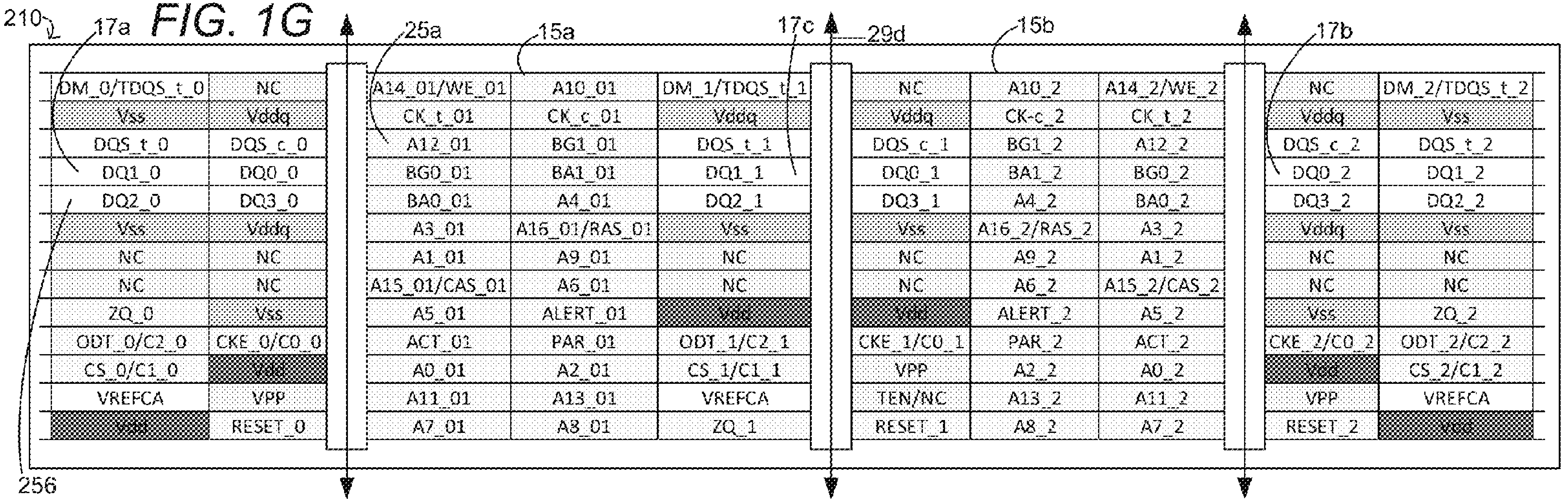


FIG. 1F



DM_0/TDQS_t_0	TDQS_c_0	A14_01/WE_01	A10_01	DM_1/TDQS_t_1	TDQS_c_1	A10_2	A14_2/WE_2	TDQS_c_2	DM_2/TDQS_t_2
Vss	Vddq	CK_T_01	CK_c_01	Vddq	Vddq	CK_c_2	CK_t_2	Vddq	Vss
DQS_t_0	DQS_c_0	A12_01	BG1_01	DQS_t_1	DQS_c_1	BG1_2	A12_2	DQS_c_2	DQS_t_2
DQ1_0	DQ0_0	BG0_01	BA1_01	DQ1_1	DQ0_1	BA1_2	BG0_2	DQ0_2	DQ1_2
DQ2_0	DQ3_0	BA0_01	A4_01	DQ2_1	DQ3_1	A4_2	BA0_2	DQ3_2	DQ2_2
Vss	Vddq	A3_01	A16_01/RAS_01	Vss	Vss	A16_2/RAS_2	A3_2	Vddq	Vss
DQ7_0	DQ4_0	A1_01	A9_01	DQ7_1	DQ4_1	A9_2	A1_2	DQ4_2	DQ7_2
DQ5_0	DQ6_0	A15_01/CAS_01	A6_01	DQ5_1	DQ6_1	A6_2	A15_2/CAS_2	DQ6_2	DQ5_2
ZQ_0	Vss	A5_01	ALERT_01	Vdd	Vdd	ALERT_2	A5_2	Vss	ZQ_2
ODT_0/C2_0	CKE_0/C0_0	ACT_01	PAR_01	ODT_1/C2_1	CKE_1/C0_1	PAR_2	ACT_2	CKE_2/C0_2	ODT_2/C2_2
CS_0/C1_0	Vdd	A0_01	A2_01	CS1_/C1_1	VPP	A2_2	A0_2	Vdd	CS_2/C1_2
VREFCA	VPP	A11_01	A13_01	VREFCA	TEN/NC	A13_2	A11_2	VPP	VREFCA
Vdd	RESET_0	A7_01	A8_01	ZQ_1	RESET_1	A8_2	A7_2	RESET_2	Vdd

FIG. 1G



DM_0/TDQS_t_0	NC	A14_01/WE_01	A10_01	DM_1/TDQS_t_1	NC	A10_2	A14_2/WE_2	NC	DM_2/TDQS_t_2
Vss	Vddq	CK_t_01	CK_c_01	Vddq	Vddq	CK-c_2	CK_t_2	Vddq	Vss
DQS_t_0	DQS_c_0	A12_01	BG1_01	DQS_t_1	DQS_c_1	BG1_2	A12_2	DQS_c_2	DQS_t_2
DQ1_0	DQ0_0	BG0_01	BA1_01	DQ1_1	DQ0_1	BA1_2	BG0_2	DQ0_2	DQ1_2
DQ2_0	DQ3_0	BA0_01	A4_01	DQ2_1	DQ3_1	A4_2	BA0_2	DQ3_2	DQ2_2
Vss	Vddq	A3_01	A16_01/RAS_01	Vss	Vss	A16_2/RAS_2	A3_2	Vddq	Vss
NC	NC	A1_01	A9_01	NC	NC	A9_2	A1_2	NC	NC
NC	NC	A15_01/CAS_01	A6_01	NC	NC	A6_2	A15_2/CAS_2	NC	NC
ZQ_0	Vss	A5_01	ALERT_01	Vdd	Vdd	ALERT_2	A5_2	Vss	ZQ_2
ODT_0/C2_0	CKE_0/C0_0	ACT_01	PAR_01	ODT_1/C2_1	CKE_1/C0_1	PAR_2	ACT_2	CKE_2/C0_2	ODT_2/C2_2
CS_0/C1_0	Vdd	A0_01	A2_01	CS_1/C1_1	VPP	A2_2	A0_2	Vdd	CS_2/C1_2
VREFCA	VPP	A11_01	A13_01	VREFCA	TEN/NC	A13_2	A11_2	VPP	VREFCA
Vdd	RESET_0	A7_01	A8_01	ZQ_1	RESET_1	A8_2	A7_2	RESET_2	Vdd

FIG. 1H

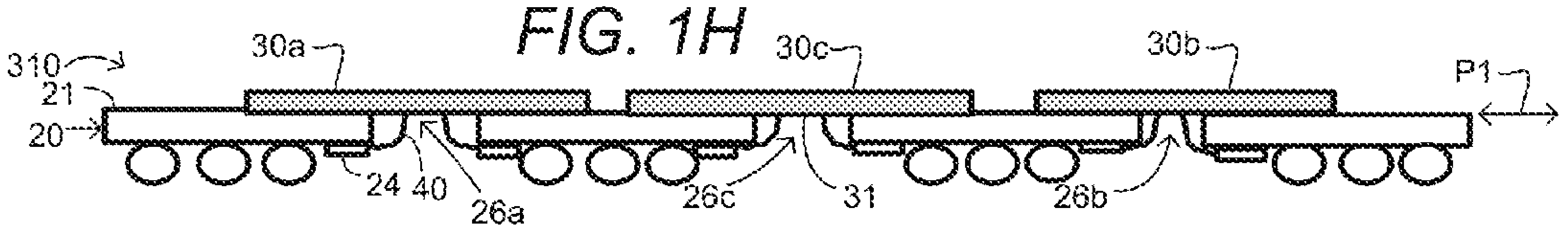


FIG. 2

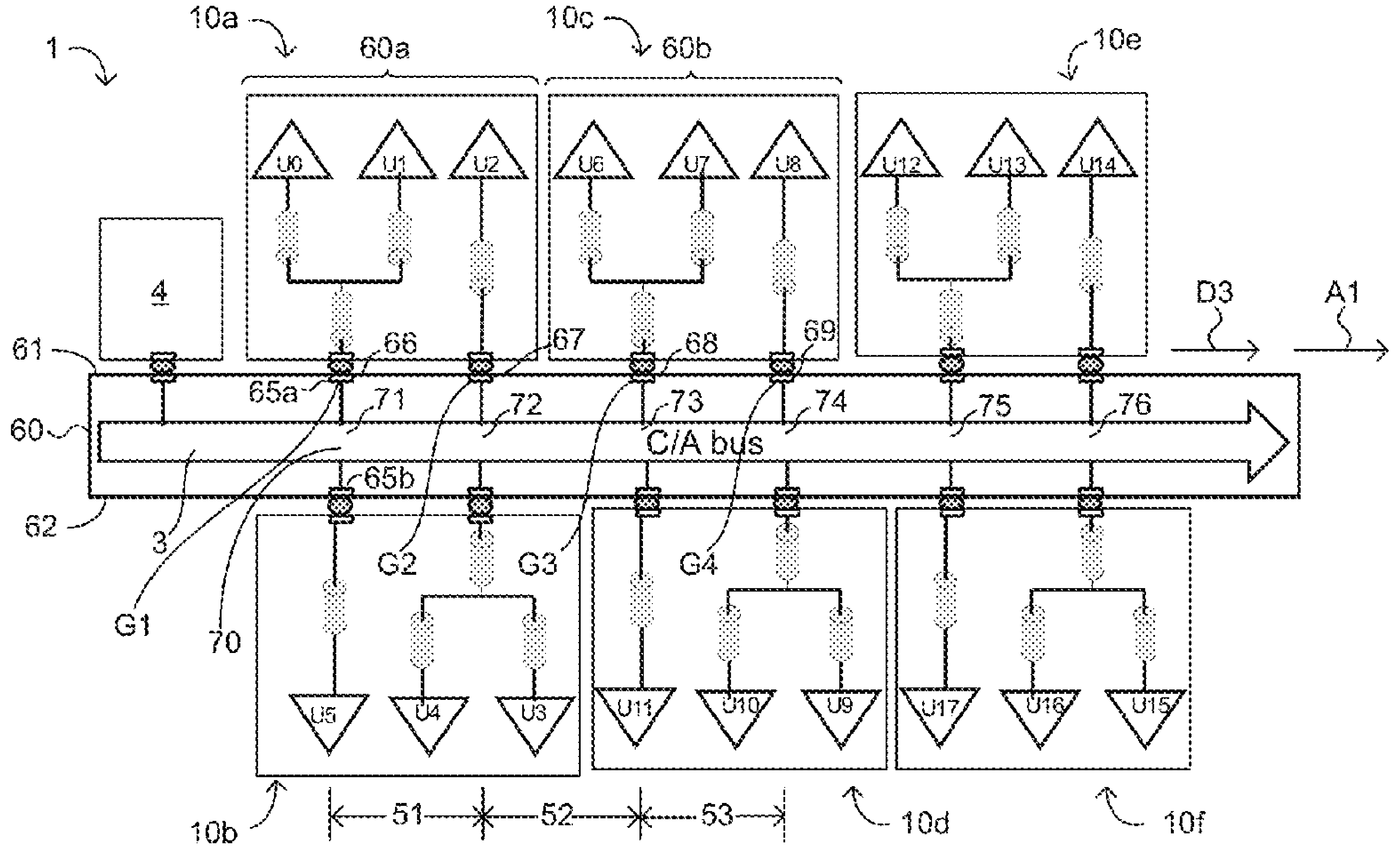


FIG. 3

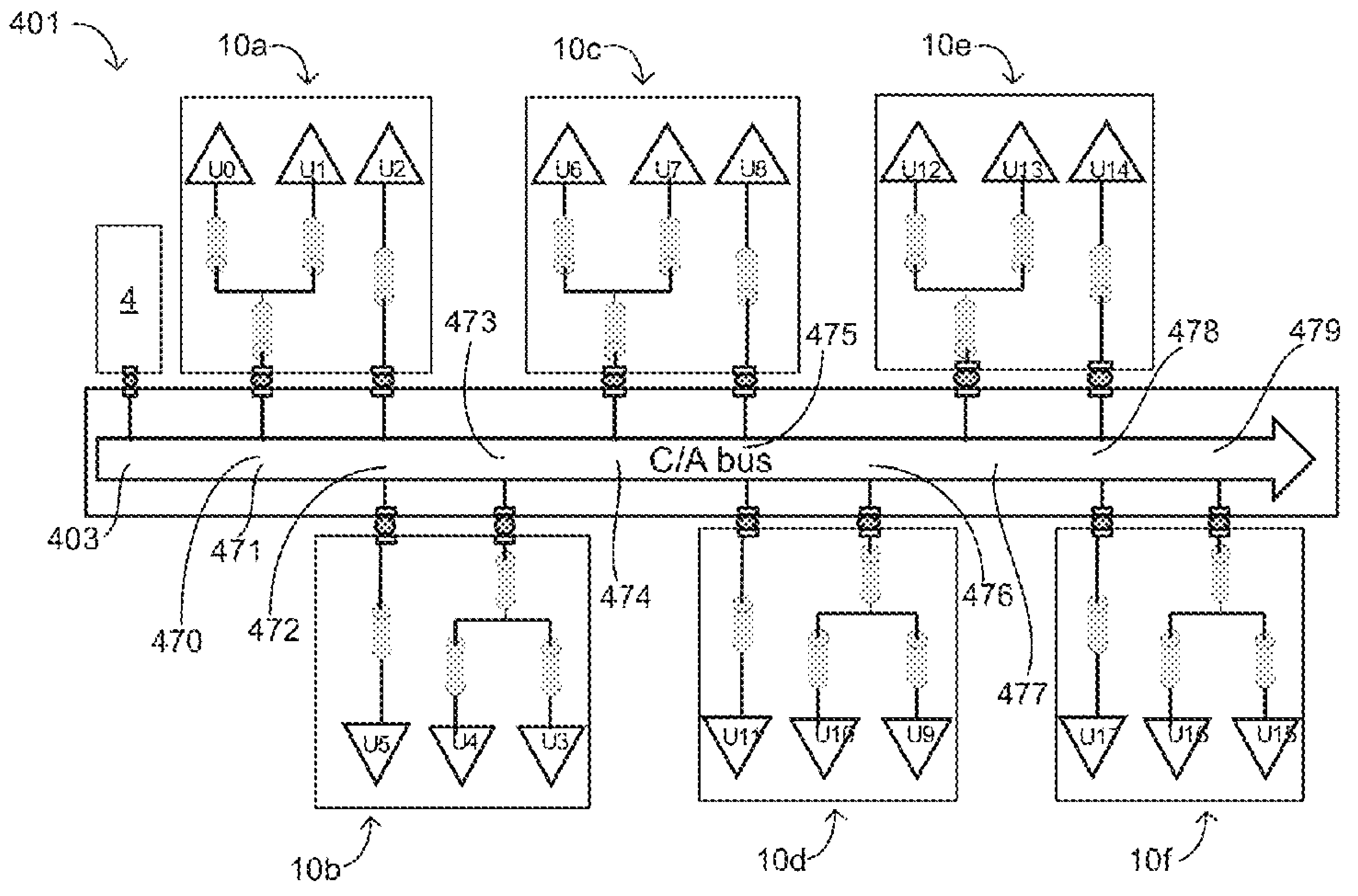


FIG. 4

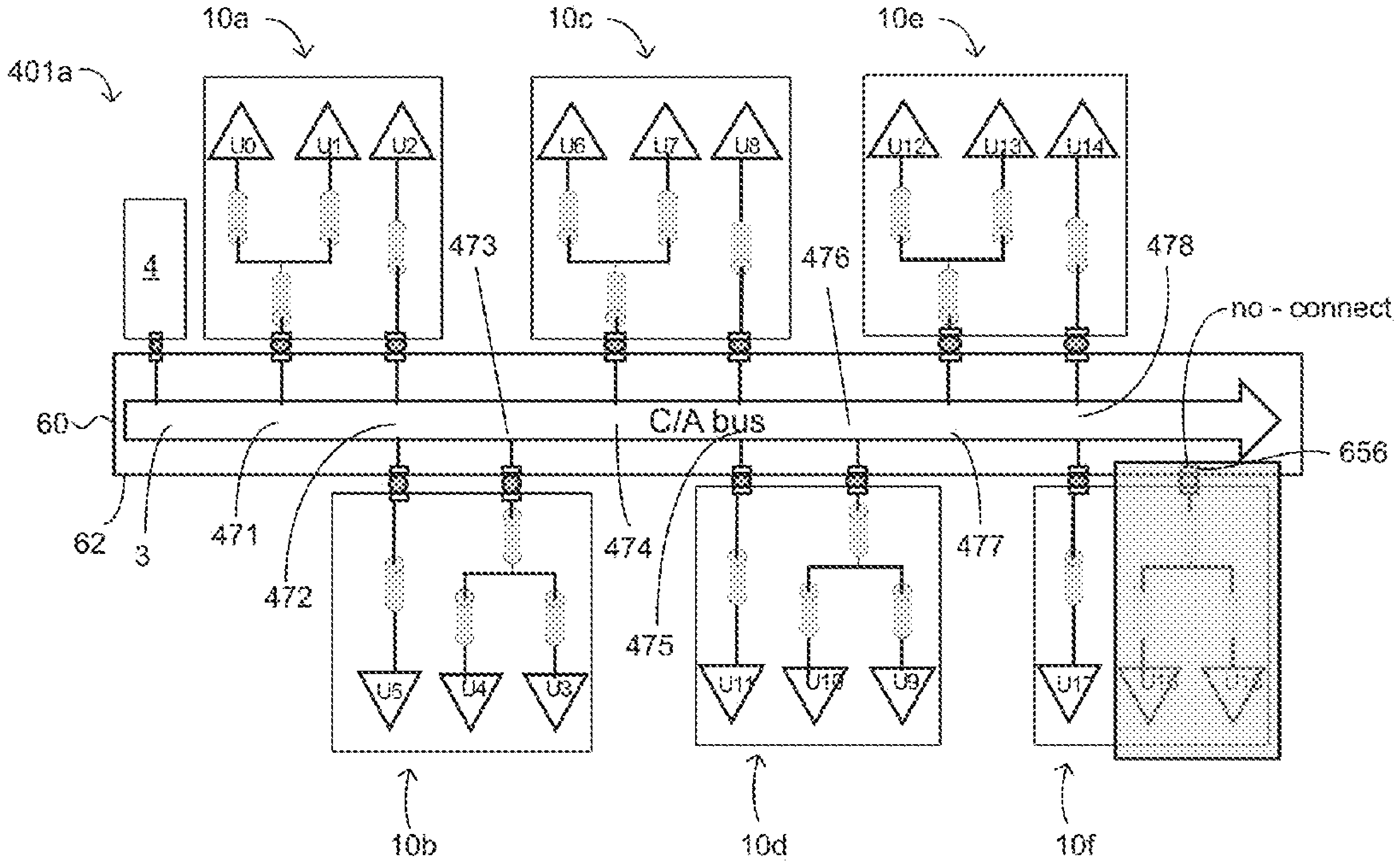
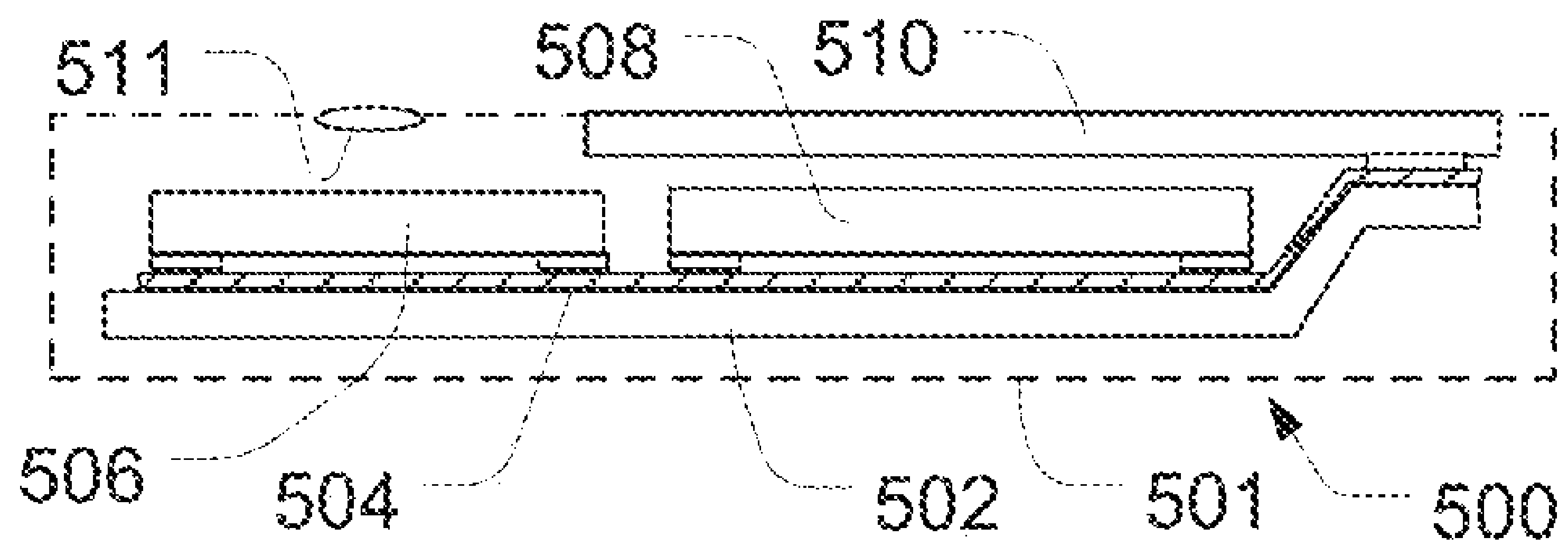

401a
10a
10c
10e
U0
U1
U2
U6
U7
U8
U12
U13
U14
4
473
476
478
no - connect
60
C/A bus
656
62
3
471
472
474
475
477
U5
U4
U3
U11
U10
U9
U17
10b
10d
10f

FIG. 5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TFD I/O PARTITION FOR HIGH-SPEED, HIGH-DENSITY APPLICATIONS

BACKGROUND OF THE INVENTION

The subject matter of the present application relates to microelectronic packages, circuit panels, and microelectronic assemblies incorporating one or more microelectronic package and a circuit panel.

Semiconductor chips are commonly provided as individual, prepackaged units. A standard chip has a flat, rectangular body with a large front face having contacts connected to the internal circuitry of the chip. Each individual chip typically is contained in a package having external terminals connected to the contacts of the chip. In turn, the terminals, i.e., the external connection points of the package, are configured to electrically connect to a circuit panel, such as a printed circuit board. In many conventional designs, the chip package occupies an area of the circuit panel considerably larger than the area of the chip itself. As used in this disclosure with reference to a flat chip having a front face, the "area of the chip" should be understood as referring to the area of the front face.

Size is a significant consideration in any physical arrangement of chips. The demand for more compact physical arrangements of chips has become even more intense with the rapid progress of portable electronic devices. Merely by way of example, devices commonly referred to as "smart phones" integrate the functions of a cellular telephone with powerful data processors, memory, and ancillary devices such as global positioning system receivers, electronic cameras, and local area network connections along with high-resolution displays and associated image processing chips. Such devices can provide capabilities such as full internet connectivity, entertainment including full-resolution video, navigation, electronic banking and more, all in a pocket-size device.

Complex portable devices require packing numerous chips into a small space. Moreover, some of the chips have many input and output connections, commonly referred to as "I/Os." These I/Os must be interconnected with the I/Os of other chips. The components that form the interconnections should not greatly increase the size of the assembly. Similar needs arise in other applications as, for example, in data servers such as those used in internet search engines where increased performance and size reduction are needed.

Semiconductor chips containing memory storage arrays, particularly dynamic random access memory chips (DRAMs) and flash memory chips, are commonly packaged in single- or multiple-chip packages and assemblies. Each package has many electrical connections for carrying signals, power, and ground between terminals and the chips therein. The electrical connections can include different kinds of conductors such as horizontal conductors, e.g., traces, beam leads, etc., that extend in a horizontal direction relative to a contact-bearing surface of a chip, vertical conductors such as vias, which extend in a vertical direction relative to the surface of the chip, and wire bonds that extend in both horizontal and vertical directions relative to the surface of the chip.

Conventional microelectronic packages can incorporate a microelectronic element that is configured to predominantly provide memory storage array function, i.e., a microelectronic element that embodies a greater number of active devices to provide memory storage array function than any other function. The microelectronic element may be or may

include a DRAM chip, or a stacked electrically interconnected assembly of such semiconductor chips.

In light of the foregoing, certain improvements in the design of microelectronic packages and microelectronic assemblies including circuit panels and/or other microelectronic components can be made in order to improve the functional flexibility or electrical performance thereof, particularly in microelectronic packages and microelectronic assemblies having circuit panels and/or other microelectronic components to which microelectronic packages can be mounted and electrically interconnected with one another.

BRIEF SUMMARY OF THE INVENTION

A microelectronic package can include, a substrate having first and second opposed surfaces, first, second, and third microelectronic elements each having a surface facing the first surface of the substrate, terminals exposed at the second surface and configured for connecting the microelectronic package to at least one component external to the microelectronic package, and leads electrically connected between contacts of each microelectronic element and the terminals. The substrate can have first and second opposed edges extending between the first and second surfaces, and first, second, and third spaced-apart apertures each extending between the first and second surfaces. The apertures can have first, second, and third parallel axes each extending in directions of the lengths of the apertures, respectively. The third axis can be disposed between the first and second axes. The second surface can have a central region between the first and second axes.

The first, second, and third microelectronic elements can each have contacts exposed at the surface of the respective microelectronic element and aligned with one of the first, second, or third apertures, respectively. Each microelectronic element can have memory storage array function. Each lead can have a portion aligned with at least one of the apertures. The terminals can include first terminals configured to carry address information. The first terminals can include first and second sets thereof. The first set of the first terminals can be electrically connected with the first and third microelectronic elements and not electrically connected with the second microelectronic element. The second set of the first terminals can be electrically connected with the second microelectronic element and not electrically connected with the first or third microelectronic elements.

In one embodiment, the terminals can include second terminals configured to carry second information. The second information can be other than the information carried by the first terminals. The second information can include data signals. The second terminals can include first, second, and third sets thereof each connected to only one of the first, second, and third microelectronic elements. In a particular example, the third set of the second terminals can be electrically connected with the third microelectronic element. The third set of the second terminals can include first and second groups disposed in the central region on first and second opposite sides of the third aperture. In an exemplary embodiment, the second surface of the substrate can have first and second peripheral regions between the central region and the respective first and second edges. The first and second sets of second terminals can be electrically connected with the respective first and second microelectronic elements and can be disposed in the respective first and second peripheral regions.

In one example, the signal assignments of corresponding ones of the second terminals in the first and second sets can be symmetric about a theoretical fourth axis between the first and second sets. The fourth axis can be parallel to the first, second, and third axes. In a particular embodiment, the fourth axis can be located within one ball pitch of the terminals of a centerline of the substrate located equidistant between the first and second opposed edges. In one embodiment, the first and second sets of the second terminals can be disposed at positions within respective first and second grids, and columns of the second terminals in the first and second grids can extend in a direction parallel to the first and second opposed edges of the substrate. In a particular example, the first terminals can be configured to carry all of the address information usable by circuitry within the microelectronic package. In an exemplary embodiment, the first set of first terminals and the second set of first terminals can each be configured to carry all of the same signals.

In one example, the signal assignments of corresponding ones of the first terminals in the first and second sets can be symmetric about a theoretical fourth axis between the first and second sets. The fourth axis can be parallel to the first, second, and third axes. In a particular embodiment, the fourth axis can be located within one ball pitch of the terminals of a centerline of the substrate located equidistant between the first and second opposed edges. In one embodiment, the first and second sets of the first terminals can be disposed at positions within respective first and second grids, and columns of the first terminals in the first and second grids can extend in a direction parallel to the first and second opposed edges of the substrate. In a particular example, each of the microelectronic elements can embody a greater number of active devices to provide memory storage array function than any other function.

In an exemplary embodiment, the surface of each of the first and second microelectronic elements can confront the first surface of the substrate, and the surface of the third microelectronic element can at least partially overlie a rear surface of at least one of the first and second microelectronic elements. In one example, the surfaces of all of the microelectronic elements can be arranged in a single plane parallel to the first surface of the substrate. In a particular embodiment, at least some of the leads can include wire bonds extending through at least one of the apertures. In one embodiment, a system can include a microelectronic package as described above and one or more other electronic components electrically connected to the microelectronic package. In a particular example, the system can also include a housing, the microelectronic package and the one or more other electronic components being assembled with the housing.

A microelectronic assembly can include a circuit panel having first and second opposed surfaces and an address bus comprising a plurality of signal conductors electrically connected with a plurality of mutually exclusive connection regions. Each connection region can include first panel contacts and second panel contacts electrically coupled with the first panel contacts disposed at the first and second surfaces, respectively. The microelectronic assembly can also include first and second microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively. Each microelectronic package can have first, second, and third microelectronic elements therein.

Each microelectronic element may be electrically coupled to the address bus via only one of the connection regions. The first and third microelectronic elements of the first microelectronic package and the second microelectronic element of the second microelectronic package may be electrically coupled to the address bus only at a first one of the connection regions. The second microelectronic elements of the first microelectronic package and the first and third microelectronic elements of the second microelectronic package may be electrically coupled to the address bus only at a second one of the connection regions.

In one embodiment, the address bus can be configured to carry all address signals usable by circuitry within the first and second microelectronic packages. In a particular example, each of the microelectronic elements can embody a greater number of active devices to provide memory storage array function than any other function. In an exemplary embodiment, the first terminals of the first and second microelectronic packages can be arranged at positions of first and second grids, and the first and second grids can be aligned with one another in x and y orthogonal directions parallel to the first and second surfaces of the circuit panel. The alignment can be within a distance equal to a minimum pitch between adjacent terminals of the grids.

In one example, the microelectronic assembly can also include third and fourth microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively. Each of the third and fourth microelectronic packages can have first, second, and third microelectronic elements therein. Each microelectronic element can be electrically coupled to the address bus via only one of the connection regions. The first and third microelectronic elements of the third microelectronic package and the second microelectronic element of the fourth microelectronic package can be electrically coupled to the address bus only at a third one of the connection regions. The second microelectronic element of the third microelectronic package and the first and third microelectronic elements of the fourth microelectronic package can be electrically coupled to the address bus only at a fourth one of the connection regions.

An electrical characteristic between the first and second connection regions can be within a same tolerance of the electrical characteristic between the second and third connection regions. In a particular embodiment, the electrical characteristic can be an electrical trace length. In one embodiment, the electrical characteristic can be an electrical propagation delay. In a particular example, the electrical characteristic can be a characteristic impedance of the signal conductors. In an exemplary embodiment, the electrical characteristic can be a difference in an electrical load applied to the address bus from the microelectronic elements connected with the respective connection region.

A microelectronic assembly can include a circuit panel having first and second opposed surfaces and an address bus comprising a plurality of signal conductors electrically connected with a plurality of mutually exclusive connection regions. Each connection region can include either or both of first panel contacts and second panel contacts electrically coupled with at least some of the plurality of signal conductors and disposed at the first and second surfaces, respectively. The microelectronic assembly can also include first and second microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively. Each microelectronic package can have first, second, and third microelectronic elements therein.

Each microelectronic element may be electrically coupled to the address bus via only one of the connection regions. The first and third microelectronic elements of the first microelectronic package may be electrically coupled to the address bus only at a first one of the connection regions. The second microelectronic element of the first microelectronic package and the second microelectronic element of the second microelectronic package may be electrically coupled to the address bus only at a second one of the connection regions. The first and third microelectronic elements of the second microelectronic package may be electrically coupled to the address bus only at a third one of the connection regions.

In one embodiment, the address bus can be configured to carry all address signals usable by circuitry within the first and second microelectronic packages. In a particular example, each of the microelectronic elements can embody a greater number of active devices to provide memory storage array function than any other function. In an exemplary embodiment, an electrical characteristic between the first and second connection regions can be within a same tolerance of the electrical characteristic between the second and third connection regions. In one example, the electrical characteristic can be an electrical trace length. In a particular embodiment, the electrical characteristic can be an electrical propagation delay. In one embodiment, the electrical characteristic can be a characteristic impedance of the signal conductors. In a particular example, the electrical characteristic can be a difference in an electrical load applied to the address bus from the microelectronic elements connected with the respective connection region.

In an exemplary embodiment, the microelectronic assembly can also include third and fourth microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively. Each of the third and fourth microelectronic packages can have first, second, and third microelectronic elements therein. Each microelectronic element can be electrically coupled to the address bus via only one of the connection regions. The first and third microelectronic elements of the third microelectronic package can be electrically coupled to the address bus only at a fourth one of the connection regions. The second microelectronic element of the third microelectronic package and the second microelectronic element of the fourth microelectronic package can be electrically coupled to the address bus only at a fifth one of the connection regions. The first and third microelectronic elements of the fourth microelectronic package may not be electrically coupled to the address bus. In one example, the first and third microelectronic elements of the fourth microelectronic package can be electrically coupled to third panel contacts disposed at the second surface of the circuit panel, and the third panel contacts may not be connected in any electrical path to the address bus within the microelectronic assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a sectional view of a microelectronic assembly including a microelectronic package and a circuit panel according to an embodiment of the present invention.

FIG. **1**B is a diagrammatic plan view of the microelectronic package shown in FIG. **1**A.

FIG. **1**C is a diagrammatic representation of the electrical connections for address signals within the microelectronic package shown in FIG. **1**A.

FIG. **1**D is a diagrammatic representation of the electrical connections for data signals within the microelectronic package shown in FIG. **1**A.

FIG. **1**E is a diagrammatic plan view a microelectronic element suitable for use in the microelectronic package shown in FIG. **1**A.

FIG. **1**F is a diagrammatic plan view showing potential signal assignments of a portion of the diagrammatic plan view shown in FIG. **1**B, according to one embodiment.

FIG. **1**G is a diagrammatic plan view showing potential signal assignments of a portion of the diagrammatic plan view shown in FIG. **1**B, according to another embodiment.

FIG. **1**H is a sectional view of an alternative configurations of microelectronic elements of the microelectronic package shown in FIG. **1**A.

FIG. **2** is a diagrammatic representation of the electrical connections for address signals within a microelectronic assembly including the microelectronic package shown in FIG. **1**A.

FIG. **3** is a diagrammatic representation of the electrical connections for address signals within a microelectronic assembly including the microelectronic package shown in FIG. **1**A, which is a variation of the microelectronic assembly of FIG. **2**.

FIG. **4** is a diagrammatic representation of the electrical connections for address signals within a microelectronic assembly including the microelectronic package shown in FIG. **1**A, which is a variation of the microelectronic assembly of FIG. **3**.

FIG. **5** is a schematic depiction of a system according to one embodiment of the invention.

DETAILED DESCRIPTION

FIGS. **1**A and **1**B illustrate a particular type of microelectronic package **10**. As seen in FIGS. **1**A and **1**B, the microelectronic package **10** can include packaging structure, for example, a dielectric element or substrate **20**, e.g., a support element that includes or consists essentially of dielectric material, e.g., organic or inorganic dielectric material such as, without limitation, oxides, nitrides, or combinations thereof, epoxies, polyimides, thermoset materials or thermoplastics, or other polymeric materials, or composite materials such as epoxy-glass, which can be FR-4 or BT resin structures, or which can be a portion of a tape utilized in tape-automated bonding ("TAB"), for example. The dielectric element **20** has first and second oppositely facing surfaces **21** and **22**.

In some cases, the dielectric element **20** can consist essentially of a material having a low coefficient of thermal expansion ("CTE") in a plane of the substrate (in a direction parallel to the first surface **21** of the substrate), i.e., a CTE of less than 12 parts per million per degree Celsius (hereinafter, "ppm/° C."), such as a semiconductor material e.g., silicon, or a dielectric material such as ceramic material or silicon dioxide, e.g., glass. Alternatively, the substrate **20** may include a sheet-like substrate that can consist essentially of a polymeric material such as polyimide, epoxy, thermoplastic, thermoset plastic, or other suitable polymeric material or that includes or consists essentially of composite polymeric-inorganic material such as a glass reinforced structure of BT resin (bismaleimide triazine) or epoxy-glass, such as FR-4, among others. In one example, such a substrate **20** can consist essentially of a material having a CTE of less than 30 ppm/° C. in the plane of the dielectric element, i.e., in a direction along its surface.

In FIGS. **1**A and **1**B, the directions parallel to the first surface **21** of the dielectric element **20** are referred to herein as "horizontal" or "lateral" directions, whereas the directions perpendicular to the first surface are referred to herein as upward or downward directions and are also referred to herein as the "vertical" directions. The directions referred to herein are in the frame of reference of the structures referred to. Thus, these directions may lie at any orientation to the normal "up" or "down" directions in a gravitational frame of reference.

A statement that one feature is disposed at a greater height "above a surface" than another feature means that the one feature is at a greater distance in the same orthogonal direction away from the surface than the other feature. Conversely, a statement that one feature is disposed at a lesser height "above a surface" than another feature means that the one feature is at a smaller distance in the same orthogonal direction away from the surface than the other feature.

First, second, and third apertures **26***a*, **26***b*, and **26***c* can extend between the first and second surfaces **21**, **22** of the dielectric element **20**. As can be seen in FIG. **1**A, the dielectric element **20** can have two three apertures **26***a*, **26***b*, and **26***c* extending therethrough. The longest dimensions of the apertures **26***a*, **26***b*, and **26***c* can define first, second, and third parallel axes **29***a*, **29***b*, and **29***c* (collectively axes **29**). The first and second parallel axes **29***a* and **29***b* can define a central region **23** of the second surface **22** of the dielectric element **20** located between the axes **29***a* and **29***b*. A first peripheral region **28***a* of the second surface is disposed between axis **29***a* and the peripheral edge **27***a* of the dielectric element. A second peripheral region **28***b* of the second surface is disposed between axis **29***b* and a peripheral edge **27***b* of the dielectric element opposite from peripheral edge **27***a*. Hereinafter, a statement that a terminal is disposed between an aperture of a substrate and a given feature of a substrate or package such as a peripheral edge thereof shall mean that the terminal is disposed between an axis of the aperture and the given feature.

The dielectric element **20** can have a plurality of terminals **25**, e.g., conductive pads, lands, or conductive posts at the second surface **22** of the dielectric element **20**. As used in this disclosure with reference to a component, e.g., an interposer, microelectronic element, circuit panel, substrate, etc., a statement that an electrically conductive element is "at" a surface of a component indicates that, when the component is not assembled with any other element, the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to the surface of the component toward the surface of the component from outside the component. Thus, a terminal or other conductive element which is at a surface of a substrate may project from such surface; may be flush with such surface; or may be recessed relative to such surface in a hole or depression in the substrate.

The terminals **25** can be configured for connecting the microelectronic package **10** to at least one component external to the microelectronic package. The terminals **25** can function as endpoints for the connection of the microelectronic package **10** with corresponding electrically conductive elements of an external component such as the contacts of a circuit panel **60**, e.g., printed wiring board, flexible circuit panel, socket, other microelectronic assembly or package, interposer, or passive component assembly, among others. In one example, such a circuit panel can be a motherboard or DIMM module board. In a particular example, the circuit panel **60** can include an element having a CTE less than 30 ppm/° C. In one embodiment, such an element can consist essentially of semiconductor, glass, ceramic or liquid crystal polymer material.

In one example, terminals **25***a* that are disposed in the central region **23** of the second surface **22** of the dielectric element **20** can be configured to carry address signals. These terminals are referred to herein as "first terminals." The first terminals **25***a* comprise terminals configured to carry address information. For example, when the microelectronic elements **30***a*, **30***b*, **30***c* include or are DRAM semiconductor chips, each set **15***a*, **15***b* of first terminals **25***a* can be configured to carry sufficient address information transferred to the microelectronic package **10** that is usable by circuitry within the package, e.g., row address and column address decoders, and bank selection circuitry of one or more of the microelectronic elements **30** to determine an addressable memory location from among all the available addressable memory locations of a memory storage array within a microelectronic element in the package. In a particular embodiment, the first terminals **25***a* can be configured to carry all the address information used by such circuitry within the microelectronic package **10** to determine an addressable memory location within such memory storage array. In one example, the first terminals **25***a* can be configured to carry all of the address information usable by circuitry within the microelectronic package **10**.

In one example, the first terminals **25***a* can be configured to carry each of a group of signals of a command-address bus of the microelectronic element; i.e., command signals, address signals, bank address signals, and clock signals that are transferred to the microelectronic package, wherein the command signals include write enable, row address strobe, and column address strobe signals, and the clock signals are clocks used for sampling the address signals. While the clock signals can be of various types, in one embodiment, the clock signals carried by these terminals can be one or more pairs of differential clock signals received as differential or true and complement clock signals.

In a particular example in which the microelectronic elements **30***a*, **30***b*, and **30***c* include DDR3 type chips, the command signals transferred to the microelectronic elements can include write enable ("WE"), row address strobe ("RAS"), and column address strobe signals ("CAS"). In one example in which the microelectronic elements **30***a*, **30***b*, and **30***c* include DDR4 type chips, the command signals transferred to the microelectronic elements can include write enable, row address strobe, column address strobe, activate ("ACT"), and parity ("PAR") signals. Such contacts and/or terminals in packages containing DDR3 or DDR4 chips that are configured to receive the aforementioned command signals can be included in any of the embodiments described herein.

In a particular embodiment, the first set **15***a* of first terminals **25***a* can be configured to carry all the address information used by the circuitry within the microelectronic package **10** to determine an addressable memory location within the first and third microelectronic elements **30***a*, **30***c* and the second set **15***b* of first terminals **25***a* can be configured to carry all the address information used by the circuitry within the microelectronic package **10** to determine an addressable memory location within the second microelectronic element **30***b*. In one example, each set **15***a*, **15***b* of first terminals **125***a* can be configured to carry each of a group of signals of a command-address bus of the corresponding microelectronic elements; i.e., command signals, address signals, bank address signals, and clock signals that are transferred to the microelectronic package **10**. In some examples (e.g., FIGS. **1**F and **1**G), the first set **15***a* of first terminals **25***a* and the second set **15***b* of first terminals can each be configured to carry all of the same signals (e.g., having the same numerical weight).

In one example, as can also be seen in FIGS. **1**F and **1**G, the signal assignments of corresponding ones of the first terminals **25***a* in the first and second sets **15***a*, **15***b* can be symmetric about a theoretical fourth axis **29***d* between the first and second sets, the fourth axis being parallel to the first, second, and third axes **29***a*, **29***b*, **29***c*. In one embodiment, such a fourth axis **29***d* can be located within one ball pitch of the terminals of a centerline of the substrate **20** located equidistant between the first and second opposed edges **27***a*, **27***b*. As shown in FIGS. **1**B, **1**F, and **1**G, the first and second sets **15***a*, **15***b* of the first terminals **25***b* can be disposed at positions within respective first and second grids, and columns of the first terminals in the first and second grids can extend in a direction D**1** parallel to the first and second opposed edges **27***a*, **27***b* of the substrate **20**.

As further seen in FIG. **1**B, in addition to first terminals **25***a*, second terminals **25***b* can be disposed at the second surface **22** of the substrate **20**. As can be seen in FIG. **1**B, a first set **17***a* of the second terminals **25***b* can be disposed in the first peripheral region **28***a* of the second surface **22** of the substrate **20**, a second set **17***b* of the second terminals **25***b* can be disposed in the second peripheral region **28***b* of the second surface of the substrate, and a third set **17***c* of the second terminals **25***b* can be disposed in the central region **23** of the second surface of the substrate.

In one example, as can be seen in FIG. **1**D, each of the memory arrays U**0**, U**1**, U**2** of the microelectronic elements **30***a*, **30***b*, **30***c* can have an independent electrical connection **2***c*, **2***d*, **2***e* to a corresponding first, second, or third set **17***a*, **17***b*, **17***c* of second terminals **25***b*, respectively. Stated another way, in the microelectronic package **10**, the first, second, and third sets **17***a*, **17***b*, **17***c* of second terminals **25***b* are each connected to only one of the first, second, and third microelectronic elements **30***a*, **30***b*, **30***c*, respectively.

In one embodiment, the first and second sets **17***a*, **17***b* of second terminals **25***b* can be electrically connected with the respective first and second microelectronic elements **30***a*, **30***b*, and can be disposed in the respective first and second peripheral regions **28***a*, **28***b*. In one example, the third set **17***c* of the second terminals **25***b* can be electrically connected with the third microelectronic element **30***c*, and the third set of second terminals can include first and second groups **17***d* and **17***e* disposed in the central region **23** of the second surface **22** of the substrate **20** on first and second opposite sides of the third aperture **26***c*.

In one example, as can also be seen in FIGS. **1**F and **1**G, the signal assignments of corresponding ones of the second terminals **25***b* in the first and second sets **17***a*, **17***b* can be symmetric about a theoretical fourth axis **29***d* between the first and second sets, the fourth axis being parallel to the first, second, and third axes **29***a*, **29***b*, **29***c*. In one embodiment, such a fourth axis **29***d* can be located within one ball pitch of the terminals of a centerline of the substrate **20** located equidistant between the first and second opposed edges **27***a*, **27***b*. As shown in FIGS. **1**B, **1**F, and **1**G, the first and second sets **17***a*, **17***b* of the second terminals **25***b* can be disposed at positions within respective first and second grids, and columns of the second terminals in the first and second grids extend in a direction D**1** parallel to the first and second opposed edges **27***a*, **27***b* of the substrate **20**.

Typically, the second terminals are configured to carry all bi-directional data signals for writing of data to and for reading of data from random access addressable locations of at least a main memory storage array within each DRAM microelectronic element. However, in some cases, some of the second terminals can carry uni-directional data signals for input to a microelectronic element for writing of data to a memory storage array, and some of the first terminals can carry uni-directional data signals output from a microelectronic element based on data read from a memory storage array.

In one example, the second terminals **25***b* can be configured to carry one or more of data strobe signals, or other signals or reference potentials such as chip select, reset, power supply voltages, e.g., Vdd, Vddq, and ground, e.g., Vss and Vssq. The second terminals **25***b* may include terminals assigned to carry data signals and also data masks and "on die termination" (ODT) signals used to turn on or off parallel terminations to termination resistors.

The microelectronic package **10** can include joining elements **11** attached to the terminals **25** for connection with an external component. The joining elements **11** can be, for example, masses of a bond metal such as solder, tin, indium, a eutectic composition or combination thereof, or another joining material such as an electrically conductive paste, an electrically conductive adhesive or electrically conductive matrix material or a combination of any or all of such bond metals or electrically conductive materials. In a particular embodiment, the joints between the terminals **25** and contacts of an external component (e.g., the circuit panel **60**) can include an electrically conductive matrix material such as described in U.S. Pat. Nos. 8,890,304 and 9,117,811, the disclosures of which are hereby incorporated herein by reference. In a particular embodiment, the joints can have a similar structure or be formed in a manner as described therein.

The microelectronic package **10** can comprise a plurality of microelectronic elements **30** (e.g., **30***a*, **30***b*, and **30***c*) each having a front face **31** facing the first surface **21** of the dielectric element **20**. Although the microelectronic elements **30** are shown in FIG. **1**B as being offset from one another in a direction parallel to the axes **29**, that need not be the case. Such an offset of the microelectronic elements **30** is shown in the figures for improved clarity of the overlying location of the microelectronic elements with respect to one another. In a particular embodiment, peripheral edges **34***a* of each of the microelectronic elements **30** can lie in a first common plane, and peripheral edges **34***b* opposite the peripheral edges **34***a* of each of the microelectronic elements can lie in a second common plane.

The front surfaces **31** of the first and second microelectronic elements **30***a*, **30***b* can confront the first surface **21** of the substrate **20**, and the front surface of the third microelectronic element **30***c* can at least partially overlie a rear surface **33** of at least one of the first and second microelectronic elements. In the example shown in FIG. **1**A, the front surface **31** of the third microelectronic element **30***c* at least partially overlies the rear surface **33** of each of the first and second microelectronic elements **30***a*, **30***b*. At least a portion of the central region **37** (FIG. **1**E) of the front surface **31** of the third microelectronic element **30***c* can project beyond a lateral edge **32** of each of the first and second microelectronic elements **30***a*, **30***b*. Accordingly, the contacts **35** of the third microelectronic element **30***c* can be positioned in a location projecting beyond the lateral edge **32** of each of the first and second microelectronic elements **30***a*, **30***b*. In other examples (e.g., FIG. **1**H), the front surfaces **31** of all of the microelectronic elements **30***a*, **30***b*, **30***c* can be arranged in a single plane parallel to the first surface **21** of the substrate **20**.

One or more adhesive layers can be positioned between the front surface **31** of the first microelectronic element **30***a* and the first surface **21** of the dielectric element **20**, between the front surface of the second microelectronic element **30***b* and the first surface of the dielectric element, and/or between the front surface of the third microelectronic element **30***c* and the rear surface **33** of one or both of the first and second microelectronic elements.

In one example, the microelectronic elements **30** can each comprise a memory storage element such as a dynamic random access memory ("DRAM") storage array or that is configured to predominantly function as a DRAM storage array (e.g., a DRAM integrated circuit chip). As used herein, a "memory storage element" refers to a multiplicity of memory cells arranged in an array, together with circuitry usable to store and retrieve data therefrom, such as for transport of the data over an electrical interface. In one example, each of the microelectronic elements **30** can have memory storage array function. In a particular embodiment, each microelectronic element **30** can embody a greater number of active devices to provide memory storage array function than any other function.

As further seen in FIG. **1**E, each microelectronic element **30** can have a plurality of electrically conductive element contacts **35** exposed at the front surface **31** thereof. The contacts **35** of each microelectronic element **30** can be arranged in one (e.g., FIG. **1**E) or in two or more (e.g., FIG. **1**A) columns **36** disposed in a central region **37** of the front face **31** that occupies a central portion of an area of the front face. As used herein with respect to a face (e.g., a front face, a rear face) of a microelectronic element, "central region" means an area, such as region **37**, occupying a middle third **41***c* of a distance **38** between opposite peripheral edges **32***a*, **32***b* of the microelectronic element **30** in a direction orthogonal to the edges **32***a*, **32***b*.

The central region **37** is disposed between peripheral regions **43***a*, and **43***b*, each of which lies between the central region **37** and a respective peripheral edge **32***a* or **32***b*, and each peripheral region also occupying an area covering a respective third **41***a* or **41***b* of the distance **38** between the opposite peripheral edges **32***a*, **32***b*. In the particular example shown in FIG. **1**E, when the contacts **35** of each microelectronic element **30** are arranged in a central region **37** of the microelectronic element, the contacts can be arranged along an axis **39** that bisects the microelectronic element. As shown in FIG. **1**A, the contacts **35** of each microelectronic element **30** can be aligned with at least one of the apertures **26**. In one example, the contacts of microelectronic element **30***a* can be aligned only with one of the apertures **26***a*, the contacts of microelectronic element **30***b* can be aligned only with another one of the apertures **26***b*, and the contacts of microelectronic element **30***c* can be aligned only with yet another one of the apertures **26***c*.

The microelectronic elements **30** in a microelectronic package **10** can be configured in accordance with one of several different standards, e.g., standards of JEDEC, which specify the type of signaling that semiconductor chips (such as the microelectronic elements **30**) transmit and receive through the contacts **35** thereof.

Thus, in one example, each of the microelectronic elements **30** can be of DDRx type, i.e., configured in accordance with one of the JEDEC double data rate DRAM standards DDR3, DDR4, or one or more of their follow-on standards (collectively, "DDRx"). Each DDRx type microelectronic element can be configured to sample the command and address information coupled to the contacts thereof at a first sampling rate, such as once per clock cycle (e.g., on the rising edge of the clock cycle). In particular examples, the DDRx type microelectronic elements can have four, eight or sixteen contacts used for transmitting and receiving bi-directional data signals, each such bi-directional signal referred to as a "DQ" signal. Alternatively, the first terminals of a package can be configured to carry uni-directional data signals such as data signals or "D" signals input to the package and data signals "Q" output from the package, or can be configured to carry a combination of bi-directional and uni-directional data signals.

In another example, each of the microelectronic elements **30** can be of LPDDRx type, i.e., configured in accordance with one of the JEDEC low power double data rate DRAM standards LPDDR3 or one or more of its follow-on standards (collectively, "LPDDRx"). LPDDRx type DRAM chips are available which have 32 contacts assigned to carry DQ signals. There are other differences as well. Each contact **35** on an LPDDRx type DRAM chip may be used to simultaneously carry two different signals in interleaved fashion. For example, each contact **35** on such DRAM chip can be assigned to carry one signal which is sampled on the rising edge of the clock cycle and can also be assigned to carry another signal that is sampled on the falling edge of the clock cycle.

Thus, in LPDDRx type chips, each microelectronic element **30***a*, **30***b*, **30***c* can be configured to sample the command and address information input to the contacts thereof at a second sampling rate, such as twice per clock cycle (e.g., on both the rising edge and on the falling edge of the clock cycle). Accordingly, the number of contacts on the LPDDRx DRAM chip that carry address information or command-address bus information can also be reduced. In a particular example of LPDDRx type chips, one or more of the contacts **35** of each microelectronic element **30***a*, **30***b*, **30***c* can be configured to carry address information at one edge of the clock cycle and command information at another edge of the clock cycle, such that a single contact can be used to alternatingly receive command and address information. Such contacts and/or terminals that are configured to alternatingly receive command and address information can be included in any of the embodiments described herein.

Electrical connections between the contacts **35** and the terminals **25** can include leads, e.g., wire bonds **40**, or other possible structure in which at least portions of the leads are aligned with at least one of the apertures **26**. For example, as seen in FIG. **1**A, at least some of the electrical connections can include a wire bond **40** that extends beyond an edge of an aperture **26** in the dielectric element **20**, and is joined at one end to the contact **35** of a microelectronic element and to a conductive element **24** of the dielectric element **20** at another end. In one example, at least some of the leads can include wire bonds **40** extending through at least one of the apertures **26***a*, **26***b*, **26***c*. In one embodiment, at least some of the electrical connections between the dielectric element and the contacts of the microelectronic element can be through lead bonds, i.e., leads that are integral with other conductive elements on the dielectric element and which extend in a lateral direction along one or both of the first and second surfaces **21**, **22** of the dielectric element **20** and are bonded to contacts of one or more of the microelectronic elements, each lead having a portion aligned with at least one of the apertures **26**.

The microelectronic package **10** can also include an encapsulant **50** that can optionally cover, partially cover, or leave uncovered the rear surfaces **33** of the microelectronic elements **30**. For example, in the microelectronic package **10** shown in FIG. **1**A, an encapsulant can be flowed, stenciled, screened or dispensed onto the rear surfaces **33** of the microelectronic elements **30**. The microelectronic package

10 can further include an encapsulant **51** that can optionally cover the wire bonds **40** and the conductive elements **24** of the dielectric element **20**. Such an encapsulant can also optionally extend into the apertures **26**, and it can cover the contacts **35** of the microelectronic elements **30**.

In the embodiment of FIGS. **1**A and **1**B, at least some signals that pass through at least some of the first terminals **25***a* of the package can be common to at least two of the microelectronic elements **30**, while other signals that pass through at least some of the first terminals of the package may only be electrically connected with one of the microelectronic elements. These signals can be routed through connections such as conductive traces extending on or within the dielectric element **20** in directions parallel to the first and second surfaces **21**, **22** of the dielectric element from the terminals **25** to the corresponding contacts **35** of the microelectronic elements **30**.

For example, a first terminal **25***a* in a first set **15***a* of the first terminals disposed in the central region **23** of the second surface **22** of the dielectric element **20** can be electrically coupled with a conductive contact **35** of each of the first and third microelectronic elements **30***a* and **30***c* through conductive traces, conductive elements **24**, e.g., bond pads, and wire bonds **40** joined to corresponding ones of the conductive elements and the contacts. A first terminal **25***a* in a second set **15***b* of the first terminals disposed in the central region **23** of the second surface **22** of the dielectric element **20** can be electrically coupled with a conductive contact **35** of only the second microelectronic element **30***b* through conductive traces, a conductive element **24**, e.g., a bond pad, and a wire bond **40** joined to corresponding ones of the conductive elements and the contacts.

In one example, the first group **15***a* of first terminals **25***a* disposed on a first side of a theoretical axis **29***d* can have signal assignments that are symmetric about the axis **29***d* with the signal assignments of the second group **15***b* of first terminals that are disposed on a second side of the axis **29***d*. The theoretical axis **29***d* can extend parallel to the longitudinal axis **29** of each of the apertures **26** and is disposed between the proximate edges of the respective apertures. In the example shown in FIG. **1**B, the theoretical axis **29***d* can be coincident with the third axis **29***c*, although that need not always be the case. In each of the examples shown in FIGS. **1**F and **1**G, the first group **15***a* of first terminals **25***a* disposed on a first side of the theoretical axis **29***d* has signal assignments that are symmetric about the axis **29***d* with the signal assignments of the second group **15***b* of first terminals that are disposed on a second side of the axis **29***d*. In particular embodiments (not shown), the first group **15***a* of first terminals **25***a* may have signal assignments that are not symmetric about a theoretical axis with the signal assignments of the second group **15***b* of first terminals.

Typically, the theoretical axis **29***d* is disposed at or near the median distance between the proximate edges of the first and second apertures **26***a*, **26***b*. "Symmetric" as used herein in connection with signal assignments of terminals for carrying address information means that the signal assignment of a terminal on a first side of the theoretical axis has a name and numerical weight which are the same as that of another terminal on an opposite side of the axis at a position symmetric about the axis from the terminal on the first side. The "numerical weight" of the address information assigned to a given terminal refers to the place of that address information within the places of an address that is specified by the address information. For example, an address can be specified by 20 address bits A**0** . . . A**19**. Each bit has a numerical weight, from the highest-ordered address information bit A**19**, which has a numerical weight of 19 representing 2^19 (2 to the power of 19), to the lowest-ordered address information bit A**0**, which has a numerical weight of zero representing 2^0 (2 to the power of zero), which is the 1's place of the address.

In a particular embodiment, the first and second groups **15***a*, **15***b* of first terminals **25***a* of the microelectronic package **10** can be configured to have modulo-X symmetry about the theoretical axis **29***d*. Microelectronic packages having groups of address and/or data terminals having modulo-X symmetry are shown and described in U.S. Pat. Nos. 8,441,111 and 9,123,555, which are hereby incorporated by reference herein in their entireties.

As can be seen in FIG. **1**C, such an example can have two independent sets of electrical connections between the microelectronic package **10** and a signal bus (e.g., the address bus or command/address bus **3** on the circuit panel **60** in FIG. **2**). As shown in FIG. **1**C, two of the memory arrays U**0**, U**1** of the microelectronic elements **30***a*, **30***c*, respectively, can have a shared electrical connection **2***a* to a first set **15***a* of first terminals **25***a* on the second surface **22** of the substrate **20**, while a third memory array U**2** of the microelectronic element **30***b* can have an independent electrical connection **2***b* to a second set **15***b* of the first terminals on the second surface of the substrate.

Stated another way, in the microelectronic package **10**, the first set **15***a* of the first terminals **25***a* are electrically connected with the first and third microelectronic elements **30***a*, **30***c* and not electrically connected with the second microelectronic element **30***b*, and the second set **15***b* of the first terminals are electrically connected with the second microelectronic element and not electrically connected with the first or third microelectronic elements. In this way, the first and third microelectronic elements **30***a*, **30***c* share an electrical connection **2***a* to the first set **15***a* of the first terminals **25***a*, and the second microelectronic element **30***b* has an unshared independent electrical connection **2***b* to a second set **15***b* of the first terminals.

In one potential example of the terminal configuration of the microelectronic package **10** described above, FIG. **1**F shows a microelectronic package **110** having a ball map that can apply to the microelectronic package **10** depicted in FIGS. **1**A and **1**B. The microelectronic package **110** has an exemplary ballout map of terminals **25** on the second surface **22** of the substrate **20**, wherein terminals A**0**-A**16** are address terminals that can be first terminals **25***a*. The first terminals **25***a* can include first and second sets **15***a*, **15***b* that can each have an independent electrical connection to an address bus or command/address bus of a circuit panel such as the circuit panel **60**. The terminals DQ**0**-DQ**7** are data terminals that can be second terminals **25***b*. The second terminals **25***b* can include first, second, and third sets **17***a*, **17***b*, **17***c* that can each have an independent electrical connection to a data bus of a circuit panel such as the circuit panel **60**. Other terminals **25** on the ballout map can be as shown in FIG. **1**F. In one example, the microelectronic elements **30** in the microelectronic package **110** can be configured in accordance with one of the JEDEC double data rate DRAM standard DDR4.

In another potential example of the terminal configuration of the microelectronic package **10** described above, FIG. **1**G shows a microelectronic package **210** having a ball map that can apply to the microelectronic package **10** depicted in FIGS. **1**A and **1**B. The microelectronic package **210** has an exemplary ballout map of terminals **25** on the second surface **22** of the substrate **20**, wherein terminals A**0**-A**16** are address terminals that can be first terminals **25***a*. The first terminals **25***a* can include first and second sets **15***a*, **15***b* that can each have an independent electrical connection to an address bus or command/address bus of a circuit panel such as the circuit panel **60**. Terminals DQ**0**-DQ**3** are data terminals that can be second terminals **25***b*. The second terminals **25***b* can include first, second, and third sets **17***a*, **17***b*, **17***c* that can each have an independent electrical connection to a data bus of a circuit panel such as the circuit panel **60**. Other terminals **25** on the ballout map can be as shown in FIG. **1**G. In one example, the microelectronic elements **30** in the microelectronic package **210** can be configured in accordance with one of the JEDEC double data rate DRAM standard DDR4.

FIG. **1**H shows a microelectronic package **310** that is a variation of the embodiment of FIGS. **1**A and **1**B. Each feature or element of the microelectronic package **310** can be the same as a corresponding feature or element of the microelectronic package **10**, except as otherwise described below. In FIG. **1**H, the microelectronic elements **30***a*, **30***b*, **30***c* can be disposed adjacent to one another, with the front faces **31** facing toward the first surface **21** of the substrate **20** and arranged in a single plane P parallel to the first surface of the substrate. In this variation, similar to the embodiment of FIGS. **1**A and **1**B, each of the microelectronic elements **30** can be electrically connected to substrate contacts **24** by leads (e.g., wire bonds **40**) aligned with apertures **26***a*, **26***b*, **26***c* extending through the substrate **20**.

Although the microelectronic elements **30** are shown in FIGS. **1**A and **1**H as being wire bonded to contacts of the substrate with their front faces facing the first surface of the package substrate, that need not be the case. For example, in other embodiments, a variation of the microelectronic package **10** can have microelectronic elements each bearing element contacts at a front face thereof, the front faces facing away from the first surface of the substrate. The microelectronic elements can each be electrically connected with conductive elements of the substrate by electrically conductive structure such as wire bonds extending above the front face between the element contacts and substrate contacts at the first surface of the substrate. The substrate contacts can be electrically connected with the terminals at the second surface of the substrate. In some variations, the front faces of the microelectronic elements can be arranged in a single plane parallel to the first surface of the substrate, or alternatively, the microelectronic elements can be arranged in a vertical stack above the first surface of the substrate.

In another embodiment, a variation of the microelectronic package **10** can have microelectronic elements each bearing element contacts a front face thereof, the front faces facing toward the first surface of the substrate, with the element contacts facing and joined to substrate contacts at the first surface of the substrate by conductive joining material extending therebetween. The substrate contacts can be electrically connected with the terminals at the second surface of the substrate.

In yet another variation of the of the microelectronic package **10**, the substrate can be omitted, such that the microelectronic package **10** can be in form of microelectronic elements **30** having packaging structure that includes an electrically conductive redistribution layer overlying the front face **31** of one or more of the microelectronic elements. The redistribution layer has electrically conductive metallized vias extending through a dielectric layer of the package to the element contacts **35** of the microelectronic elements **30**. The redistribution layer may include the terminals **25** and traces electrically connected with the terminals, such that the terminals are electrically connected with the element contacts, such as through the metallized vias or through metallized vias and electrically conductive traces. In this case, the package can be referred to as a "wafer-level package having a redistribution layer thereon." In an additional variation, such a microelectronic package having a redistribution layer thereon as described above can have one or more columns of the terminals **25** disposed on areas of the dielectric layer that extend laterally beyond one or more edges of the microelectronic elements. In this case, the package can be referred to as a "fan-out wafer-level package having a redistribution layer thereon."

Referring to FIG. **2**, in accordance with an aspect of the invention, a microelectronic assembly **1** can include first, second, third, fourth, fifth, and sixth microelectronic packages **10***a*, **10***b*, **10***c*, **10***d*, **10***e*, and **10***f* (collectively, the microelectronic packages **10**) assembled with a circuit panel **60** in a clamshell arrangement, with the first, third, and fifth microelectronic elements mounted to the first surface **61** of the circuit panel, and with the second, fourth, and sixth microelectronic elements mounted to the second surface **62** of the circuit panel. Specifically, as seen in FIG. **2**, the packages **10***a*, **10***b* can be mounted opposite one another to respective panel contacts at the first and second surfaces **61**, **62** of the circuit panel **60**, such that the first package **10***a* occupies the same or substantially the same area of the circuit panel as the second package **10***b*.

Each of the microelectronic packages **10** of the microelectronic assembly **1** can have a similar structure that includes first, second, and third microelectronic elements **30** as described above with reference to FIGS. **1**A and **1**B. As can be seen in FIG. **2**, each of the memory arrays U**0** through U**17** of the microelectronic elements **30** within the microelectronic packages **10** can be electrically connected to a connection region **70** of an address bus or command/address bus **3** on the circuit panel **60**, via a shared electrical connection **2***a* or an independent electrical connection **2***b*. In the examples herein, each memory array U**0** through U**17** is located within a corresponding microelectronic element **30**.

In the examples of FIGS. **2**-**4**, the first, second, and third microelectronic elements **30***a*, **30***b*, and **30***c* of the first microelectronic package **10***a* contain memory arrays U**0**, U**1**, and U**2**, respectively, and the first, second, and third microelectronic elements of the second microelectronic package **10***b* contain memory arrays U**3**-U**5**, respectively. In similar fashion, the first, second, and third microelectronic elements **30***a*, **30***b*, and **30***c* of the third microelectronic package **10***c* contain memory arrays U**6**-U**8**, respectively, the first, second, and third microelectronic elements of the fourth microelectronic package **10***d* contain memory arrays U**9**-U**11**, respectively, the first, second, and third microelectronic elements of the fifth microelectronic package **10***e* contain memory arrays U**12**-U**14**, respectively, and the first, second, and third microelectronic elements of the sixth microelectronic package **10***f* contain memory arrays U**15**-U**17**, respectively.

The microelectronic assembly **1** can include an address bus or command-address bus **3** that can comprise a plurality of signal conductors each passing sequentially through connection regions **70** of the circuit panel **60** such as first, second, third, fourth, fifth, and sixth connection regions **71**, **72**, **73**, **74**, **75**, and **76**. The bus **3** can extend within or on a support, which may be a portion of the circuit panel **60**. The bus **3** can comprise a plurality of signal conductors for transmitting address signals or address and command signals. The circuit panel **60** can have conductive panel contacts **65** at a surface of the support, such as the first panel contacts **65***a* at the first surface **61** of the circuit panel and the second panel contacts **65***b* at the second surface **62** of the circuit panel. The microelectronic packages **10** can be mounted to the panel contacts **65**, for example, by joining elements **11** that can extend between the terminals **25** and the panel contacts.

The address bus or command-address bus **3** can comprise a plurality of signal conductors electrically connected with a plurality of mutually exclusive connection regions **71-76**. As used herein, "mutually exclusive" connection regions are not electrically connected to one another within the circuit panel **60**. In the example shown in FIG. **2**, each connection region **70** can include first panel contacts **65***a* disposed at the first surface **61** and second panel contacts **65***b* disposed at the second surface **62**, and the first and second panel contacts in a particular connection region can be electrically coupled with one another. Thus, at least some first terminals **25***a* of both a first microelectronic package **10***a* and a second microelectronic package **10***b* can be electrically coupled with one another through a particular connection region (e.g., the first connection region **71**).

In one example, the address bus **3** can be configured to carry all address signals usable by circuitry within the microelectronic packages **30**. In a particular example (e.g., DDR3 chips), the address bus **3** can be configured to carry all command signals transferred to each of the microelectronic packages **30**, the command signals being write enable, row address strobe, and column address strobe signals. In one embodiment (e.g., DDR4 chips), all of the command signals transferred to each of the microelectronic packages **30** can be write enable, row address strobe, column address strobe, activate, and parity signals. The first terminals **25***a* of each of the microelectronic packages **30** can be configured to carry all of the address signals usable by circuitry within the respective microelectronic package.

On the circuit panel **60**, e.g., a printed circuit board, module card, etc., these above-noted signals of the command-address bus: i.e., command signals, address signals, bank address signals, and clock signals, can be bussed to multiple microelectronic packages **10** that are connected thereto in parallel, for example, to first and second microelectronic packages **10***a*, **10***b* mounted to opposite surfaces of the circuit panel in a clamshell configuration.

In one embodiment, the first terminals **25***a* of the respective microelectronic packages **10** can be functionally and mechanically matched, such that each microelectronic package can have the same pattern of first terminals at the second surface **22** of the substrate **20** of the respective microelectronic package with the same function, although the particular dimensions of the length, width, and height of each microelectronic package can be different than that of the other microelectronic packages.

In one example, each of the sets or groups **15***a* and **15***b* of the first terminals **25***a* of each microelectronic package **30** can be configured to carry all of the same address signals. As can be seen in FIG. **2**, in a particular embodiment, each of the sets or groups **15***a* and **15***b* of the first terminals **25***a* of each microelectronic package **30** can be disposed in respective first and second opposite sides of a theoretical axis **29***d* extending along the second surface **22** of the respective substrate **20**. In one example, the first terminals **25***a* of the first and second microelectronic packages **10***a*, **10***b* can be arranged at positions of first and second grids, and the first and second grids can be aligned with one another in x and y orthogonal directions parallel to the first and second surfaces **61**, **62** of the circuit panel **60**, the alignment being within a distance equal to a minimum pitch **P1** (FIG. **1**A) between adjacent terminals of the grids.

As can be seen in FIG. **2**, each of the connection regions **71-76** of the address bus **3** is electrically connected with three corresponding ones of the microelectronic elements **30** containing three corresponding ones of the memory arrays **U0**-**U17**. Also in this example, each microelectronic element **30** in the microelectronic assembly **1** may be electrically coupled to the address bus **3** via only one of the connection regions **71-76**. Therefore, although both of the first and second microelectronic packages **10***a* and **10***b* are electrically connected with both the first and second connection regions **71**, **72**, each of the first and second connection regions is electrically connected with only one of the sets **15** of the first terminals **25***a* of each of the first and second microelectronic packages.

For example, as shown in FIG. **2**, the first connection region **71** is electrically connected only with memory arrays **U0** and **U1** of the first microelectronic package **10***a* (via the first set **15***a* of the first terminals **25***a*) and with memory array **U5** of the second microelectronic package **10***b* (via the second set **15***b* of the first terminals). Therefore, the first connection region **71** is electrically connected only with the first and third microelectronic elements **30***a*, **30***c* of the first microelectronic package **10***a* and with the second microelectronic element **30***b* of the second microelectronic package **10***b*.

Likewise, the second connection region **72** is electrically connected only with memory array **U2** of the first microelectronic package **10***a* (via the second set **15***b* of the first terminals **25***a*) and with memory arrays **U3** and **U4** of the second microelectronic package **10***b* (via the first set **15***a* of the first terminals). Therefore, the second connection region **72** is electrically connected only with the second microelectronic element **30***b* of the first microelectronic package **10***a* and with the first and third microelectronic elements **30***a*, **30***c* of the second microelectronic package **10***b*.

Stated another way, the first and third microelectronic elements **30***a*, **30***c* of the first microelectronic package **10***a* and the second microelectronic element **30***b* of the second microelectronic package **10***b* can be electrically coupled to the address bus **3** only at a first one of the connection regions **71**, and the second microelectronic element **30***b* of the first microelectronic package **10***a* and the first and third microelectronic elements **30***a*, **30***c* of the second microelectronic package **10***b* are electrically coupled to the address bus only at a second one of the connection regions **72**. In one example, the first and third microelectronic elements **30***a*, **30***c* of the third microelectronic package **10***c* and the second microelectronic element **30***b* of the fourth microelectronic package **10***d* can be electrically coupled to the address bus **3** only at a third one of the connection regions **73**, and the second microelectronic element **30***b* of the third microelectronic package **10***c* and the first and third microelectronic elements **30***a*, **30***c* of the fourth microelectronic package **10***d* are electrically coupled to the address bus only at a fourth one of the connection regions **74**.

In some examples, the microelectronic assembly **1** can further include an optional controller package **4** electrically coupled to the address bus or command-address bus **3**. The controller package **4** can include a controller element configured to control generation of address signals for transmission on the bus **3**. In one example, first and second microelectronic packages **10***a*, **10***b* can overlie respective first and second areas of a same surface of the support or circuit panel **60**, and the controller package **4** can overlie a third area of the circuit panel. Such a controller package **4** may be included in embodiments of the microelectronic assembly **1** where the assembly is a registered DIMM. In other embodiments, the microelectronic assembly may not include the controller package **4** where the assembly is a DIMM without registers, e.g., UDIMM (unregistered DIMM).

As illustrated in FIG. **2**, signals transported by the address bus or command-address bus **3** can be routed in at least one direction D**3** between connection sites on a circuit panel such as the circuit panel **60** at which a plurality of microelectronic packages **10** are connected, such that signals of the bus reach each connection region **70** at different times.

The at least one direction D**3** can be transverse or orthogonal to a direction D**2** (FIG. **1**E) in which at least one column **36** of a plurality of contacts **35** on at least one microelectronic element **30** extends. In such a way, the signal conductors of the command-address bus **3** on (i.e., on or within) the circuit panel **60** can in some cases be spaced apart from one another in the direction D**2** that is parallel to the at least one column **36** of contacts **35** on a microelectronic element **30** within a microelectronic package **10** connected to, or to be connected to the circuit panel **60**.

In the embodiment shown in FIG. **2**, the microelectronic packages **10***a* and **10***c* can be first and third microelectronic packages each joined to the panel contacts **65***a* at respective first and second different areas **60***a*, **60***b* of the first surface **61** of the circuit panel **60**. The first microelectronic package **10***a* can include first, second, and third microelectronic elements **30***a*, **30***b*, **30***c* having memory arrays U**0**, U**1**, and U**2**, and the third microelectronic package **10***c* can include first, second, and third microelectronic elements **30***a*, **30***b*, **30***c* having memory arrays U**6**, U**7**, and U**8**.

The first terminals **25***a* of the microelectronic packages **10***a* and **10***c* can be electrically coupled to first, second, third, and fourth sets **66**, **67**, **68**, and **69** of the first panel contacts **65***a*. In turn, the first, second, third, and fourth sets **66**, **67**, **68**, and **69** of the first panel contacts **65***a* can be electrically coupled to the signal conductors of the bus **3**. In one example (e.g., DDR3 chips), each of the first, second, third, and fourth sets **66**, **67**, **68**, and **69** of first panel contacts **65***a* can be configured to carry address information usable by circuitry within the microelectronic packages **10** and command signals transferred to the microelectronic packages, the command signals being write enable, row address strobe, and column address strobe signals. In one embodiment (e.g., DDR4 chips), the command signals transferred to the microelectronic packages can be write enable, row address strobe, column address strobe, activate, and parity signals.

Each of the memory arrays U**0**, U**1**, U**2**, U**6**, U**7**, and U**8** of the microelectronic packages **10***a*, **10***c* can be electrically coupled to the signal conductors of the bus **3** at one of the connection regions **71**, **72**, **73**, **74** via a set **66**, **67**, **68**, **69** of the first panel contacts **65***a* and via packaging structure (e.g., first terminals **25***a*) of the respective microelectronic package for receiving address signals or address and command signals.

In the embodiment shown in FIG. **2**, each of the memory arrays U**0**, U**1**, U**2**, U**6**, U**7**, and U**8** of the microelectronic packages **10***a*, **10***c* can be electrically coupled to the bus **3** at only one of the first, second, third, and fourth connection regions **71**, **72**, **73**, **74**. In a particular example, a memory array U**0** of a first microelectronic package **10***a* can have address inputs coupled only to the first set **66** of first panel contacts **65***a*, and a memory array U**2** of the first microelectronic package **10***a* can have address inputs coupled only to the second set **67** of first panel contacts **65***a*.

In the example shown in FIG. **2**, geometric centers G**1**, G**2**, and G**3** of the respective first, second, and third sets **66**, **67**, **68** of the first panel contacts **65***a* have first, second, and third substantially equal relative separation distances S**1**, S**2**, and S**3** from the geometric centers G**2**, G**3**, and G**4** of the second, third, and fourth sets **66**, **67**, **68** of the panel contacts, respectively. In one example, any difference among the first, second, and third substantially equal relative separation distances S**1**, S**2**, and S**3** can fall within a same tolerance, for example, a same tolerance of ±0.5 mm, or in a particular embodiment, a same tolerance of ±1% of any one of the separation distances.

In one embodiment, the geometric centers G**1**, G**2**, G**3**, and G**4** of the respective first, second, third, and fourth sets **66**, **67**, **68**, **69** of the first panel contacts **65***a* can be equally spaced from one another along a common theoretical axis A**1** extending parallel to the first surface **61** of the circuit panel **60**. As used herein, a statement that elements are "equally spaced" with respect one another along a common theoretical axis means that the actual difference in spacing between adjacent ones of the elements is within a typical manufacturing tolerance known to one skilled in the relevant art.

In the embodiment of FIG. **2**, an electrical characteristic between the first and second connection regions **71**, **72** can be within a same tolerance of the electrical characteristic between the second and third connection regions **72**, **73**. The electrical characteristic can be, for example, an electrical trace length, an electrical propagation delay, a characteristic impedance of the signal conductors, or a difference in electrical load applied to the address bus from the microelectronic element connected with the respective connection region.

In one embodiment, each of the first, second, and third connection regions **71**, **72**, **73** can have respective first, second, and third relative electrical lengths (i.e., electrical trace lengths) from the respective second, third, and fourth connection regions **72**, **73**, **74**, and any difference among the first, second, and third relative electrical lengths can fall within a same tolerance, for example, a same tolerance of ±0.5 mm, or in a particular embodiment, a same tolerance of ±1% of any one of the relative electrical lengths. In a particular embodiment, an electrical trace length between the first and second connection regions **71**, **72** can be within a same tolerance of the electrical trace length between the second and third connection regions **72**, **73**.

In a particular embodiment, each of the second, third, and fourth connection regions **72**, **73**, and **74** can be configured to receive address signals from the bus **3** at respective first, second, and third relative delays (i.e., electrical propagation delays) from the respective first, second, and third connection regions **71**, **72**, and **73**, and any difference among the first, second, and third relative delays can fall within a same tolerance, for example, a same tolerance of ±1% of any one of the relative delays. In a particular embodiment, an electrical propagation delay between the first and second connection regions **71**, **72** can be within a same tolerance of the electrical propagation delay between the second and third connection regions **72**, **73**.

In one example, a characteristic impedance of the signal conductors of the bus **3** between the first and second connection regions **71** and **72**, and the characteristic impedance of the signal conductors between the second and third connection regions **72** and **73** can fall within a same tolerance, for example, a same tolerance of ±5 ohms. Likewise, a characteristic impedance of the signal conductors of the bus **3** between the first and second connection regions **71** and

72, the characteristic impedance of the signal conductors of the bus **3** between the second and third connection regions **72** and **73**, and the characteristic impedance of the signal conductors between the third and fourth connection regions **73** and **74** can fall within a same tolerance, for example, a same tolerance of ±5 ohms.

In one example, each of the groups of microelectronic elements **30** electrically connected to a particular one of the connection regions **71-76** can be configured to apply substantially a same load (i.e., electrical load) to the bus **3** as any other of the groups of microelectronic elements **30** electrically connected to another one of the connection regions **71-76**, for example, within a tolerance of ±5 ohms In a particular embodiment, a difference in electrical load applied to the address bus **3** via the first and second connection regions **71**, **72** can be within a same tolerance of the difference in electrical load applied to the address bus via the second and third connection regions **72**, **73**. For example, the same tolerance of the difference in electrical load applied to the address bus can be within a tolerance of ±5 ohms.

FIG. **3** illustrates a microelectronic assembly **401** that is a variation of the microelectronic assembly **1** of FIG. **2**. Each feature or element of the microelectronic assembly **401** can be the same as a corresponding feature or element of the microelectronic assembly **1**, except as otherwise described below. As can be seen in FIG. **3**, each of the connection regions **471-479** (collectively **470**) of the address bus **403** is electrically connected with two corresponding ones of the microelectronic elements **30** containing two corresponding ones of the memory arrays U**0**-U**17**. Also in this example, each microelectronic element **30** in the microelectronic assembly **401** may be electrically coupled to the address bus **3** via only one of the connection regions **471-479**. Therefore, although both of the first and second microelectronic packages **10***a* and **10***b* are electrically connected with two of the connection regions **470**, each of the connection regions is electrically connected with only two of the memory arrays U**0**-U**17**.

In the example of FIG. **3**, the microelectronic packages **10** are in a staggered clamshell configuration. For example, the packages **10***a*, **10***b* can be mounted opposite one another to respective panel contacts at the first and second surfaces **61**, **62** of the circuit panel **60**, but the first package **10***a* only occupies a portion of the same area of the circuit panel as the second package **10***b*, and another portion of the first package does not occupy the same area as the second package.

Since each connection region is electrically connected with only two of the memory arrays U**0**-U**17**, the first set **15***a* of the first terminals **25***a* of each microelectronic package **10**, through which the first and third microelectronic elements **30***a*, **30***c* have a shared electrical connection **2***a* to the address bus or command/address bus **3**, does not share a connection region **470** with any other microelectronic package. However, the second set **15***b* of the first terminals **25***a* of each microelectronic package **10**, through which the second microelectronic element **30***b* has an independent electrical connection **2***b* to the address bus or command/address bus **3**, shares its connection region with a corresponding second set of first terminals of another microelectronic package mounted to the opposite side of the circuit panel **60**.

Therefore, in the example shown in FIG. **3**, the odd connection regions **471**, **473**, **475**, **477**, and **479** are only connected with a first set **15***a* of first terminals **25***a* of a single corresponding microelectronic package **10**, while even connection regions **472**, **474**, **476**, and **479** are connected with a second set **15***b* of first terminals of two microelectronic packages **10** at opposite sides of the circuit panel. Similar to the example of FIG. **2**, each microelectronic element **30** (and each memory array U**0**-U**17**) of the microelectronic assembly **401** is electrically coupled to the address bus **3** via only one of the connection regions **470**.

More specifically, in the microelectronic assembly **401**, the first and third microelectronic elements **30***a*, **30***c* of the first microelectronic package **10***a* are electrically coupled to the address bus **3** only at a first one of the connection regions **471**, the second microelectronic element **30***b* of the first microelectronic package and the second microelectronic element of the second microelectronic package **10***b* are electrically coupled to the address bus only at a second one of the connection regions **472**, and the first and third microelectronic elements of the second microelectronic package are electrically coupled to the address bus only at a third one of the connection regions **473**. This pattern is repeated for the third through sixth microelectronic packages **10***c*-**10***f*.

In the embodiment of FIGS. **2** and **3**, when each microelectronic element **30** is configured to carry 4 bi-directional data signals DQ**0** . . . DQ**3** (e.g., FIG. **1**G), the microelectronic assemblies **1** or **401** can each be configured to transmit 72 bi-directional data signals in tandem to support 72-bit single-rank memory access, including 8 bits for error correction. Alternatively, the embodiments of FIGS. **2** and **3** could be expanded to include 12 microelectronic packages containing 36 microelectronic elements total, each microelectronic element configured to carry 4 bi-directional data signals. In such embodiments, the microelectronic assemblies **1** or **401** can each be configured to transmit 72 bi-directional data signals in tandem to support 72-bit dual-rank memory access, including 8 bits for error correction per rank. When each microelectronic element **30** is configured to carry 8 bi-directional data signals DQ**0** . . . DQ**7** (e.g., FIG. **1**F), the microelectronic assemblies **1** or **401** can each be configured to transmit 72 bi-directional data signals in tandem to support 72-bit dual-rank memory access, including 8 bits for error correction per rank.

FIG. **4** illustrates a microelectronic assembly **401***a* that is a variation of the microelectronic assembly **401** of FIG. **3**. Each feature or element of the microelectronic assembly **401***a* can be the same as a corresponding feature or element of the microelectronic assembly **401**, except as otherwise described below. The microelectronic assembly **401***a* is the same as the microelectronic assembly **401**, except that the ninth connection region **479** is omitted, leaving eight connection regions **471-478** on the address bus **3**. This reduction of connection regions can be accomplished by using no-connect panel contacts as the second panel contacts **65***b* that are electrically connected with the first set **15***a* of first terminals **25***a*, which are electrically connected with the memory arrays U**16** and U**15**. As used herein, a "no-connect" panel contacts not connected in any electrical path to the address bus within the microelectronic assembly. By removing the electrical connections between the address bus **3** and two of the eighteen microelectronic elements **30** within the microelectronic assembly **401***a*, that can remove the error-correction feature of the microelectronic assembly **401***a*.

In the embodiment of FIG. **4**, when each microelectronic element **30** is configured to carry 4 bi-directional data signals DQ**0** . . . DQ**3** (e.g., FIG. **1**G), the microelectronic assembly **401***a* can be configured to transmit 64 bi-directional data signals in tandem to support 64-bit single-rank memory access, without error correction. Alternatively, the embodiment of FIG. **4** could be expanded to include 11 or

12 microelectronic packages **10** containing 33 or 36 microelectronic elements total, each microelectronic element configured to carry 4 bi-directional data signals. In such embodiments, if only 32 of the microelectronic elements are electrically connected to the address bus, the microelectronic assembly **401***a* can be configured to transmit 64 bi-directional data signals in tandem to support 64-bit dual-rank memory access, without error correction. When each microelectronic element **30** is configured to carry 8 bi-directional data signals DQ**0** . . . DQ**7** (e.g., FIG. **1**F), the microelectronic assembly **401***a* can each be configured to transmit 64 bi-directional data signals in tandem to support 64-bit dual-rank memory access, without error correction.

In the example of FIG. **4**, the electrical connections between the microelectronic packages **10** and the address bus **3** are the same as with the microelectronic assembly **401**, except for the sixth microelectronic package **10***f*. In this example, the first and third microelectronic elements **30***a*, **30***c* of the fifth microelectronic package **10***e* are electrically coupled to the address bus only at a seventh one of the connection regions **477**, the second microelectronic element **30***b* of the fifth microelectronic package and the second microelectronic element of the sixth microelectronic package **10***f* are electrically coupled to the address bus only at an eighth one of the connection regions **478**, and the first and third microelectronic elements of the sixth microelectronic package are not electrically coupled to the address bus **3**. To accomplish this, the first and third microelectronic elements **30***a*, **30***c* of the sixth microelectronic package can be electrically coupled to second panel contacts **65***b* disposed at the second surface **62** of the circuit panel **60**, but the such panel contacts are not connected in any electrical path to the address bus **3** within the microelectronic assembly **401***a*.

In the examples of the microelectronic assemblies **1**, **401**, **401***a* described herein having microelectronic packages **10** configured to apply balanced electrical connections to the address bus or command/address bus **3** (through independent groups **15***a*, **15***b* of first terminals each connected to only one of the connection regions **70**), the electrical loads may be distributed more evenly distributed along the signal conductors of the fly-by bus **3** compared to conventional microelectronic assemblies.

Such microelectronic assemblies **1**, **401**, **401***a* may result in better impedance matching between adjacent connection regions along the bus **3**, and more bandwidth capability along the bus to handle higher frequency signals, compared to conventional microelectronic assemblies. The inventors have found that in use, the structure of the microelectronic assemblies **1**, **401**, **401***a* may produce significantly lower reflection compared to conventional microelectronic assemblies, thereby permitting the assembly to operate at a higher bandwidth with better signal transmission than conventional microelectronic assemblies.

In one embodiment, the connection regions **71**, **72**, **73**, and **74** need not all be disposed on a single circuit panel. For example, connection regions **71**, **72** to which the microelectronic elements of a first package **10***a* are coupled can be disposed on a circuit panel other than the circuit panel on which the connection regions **73**, **74** coupled to the second package **10***c* are disposed.

Although in the embodiments described herein, the first terminals **25***a* of the microelectronic packages **30** were disposed in the central region **23** of the second surface **22** of the substrate **20**, in other examples, the first terminals can be disposed anywhere on the substrate. Although in the embodiments described herein, the first and second sets **17***a*, **17***b* of the second terminals **25***b* of the microelectronic packages **30** were disposed in the peripheral regions **28** of the second surface **22** of the substrate **20**, in other examples, the first and second sets of the second terminals can be disposed anywhere on the substrate. Although in the embodiments described herein, the third set **17***c* of the second terminals **25***b* of the microelectronic packages **30** were disposed in the central region **23** of the second surface **22** of the substrate **20**, on both sides of the third aperture **26***c*, in other examples, the third set of the second terminals can be disposed anywhere on the substrate, and the third set of the second terminals need not be distributed on both sides of the third aperture.

The microelectronic packages and microelectronic assemblies described above with reference to FIGS. **1**A through **4** above can be utilized in construction of diverse electronic systems, such as the system **500** shown in FIG. **5**. For example, the system **500** in accordance with a further embodiment of the invention includes a plurality of modules or components **506** such as the microelectronic packages and microelectronic assemblies as described above, in conjunction with other electronic components **508**, **510** and **511**.

In the exemplary system **500** shown, the system can include a circuit panel, motherboard, or riser panel **502** such as a flexible printed circuit board, and the circuit panel can include numerous conductors **504**, of which only one is depicted in FIG. **5**, interconnecting the modules or components **506**, **508**, **510** with one another. Such a circuit panel **502** can transport signals to and from each of the microelectronic packages and/or microelectronic assemblies included in the system **500**. However, this is merely exemplary; any suitable structure for making electrical connections between the modules or components **506** can be used.

In a particular embodiment, the system **500** can also include a processor such as the semiconductor chip **508**, such that each module or component **506** can be configured to transfer a number N of data bits in parallel in a clock cycle, and the processor can be configured to transfer a number M of data bits in parallel in a clock cycle, M being greater than or equal to N.

In the example depicted in FIG. **5**, the component **508** is a semiconductor chip and component **510** is a display screen, but any other components can be used in the system **500**. Of course, although only two additional components **508** and **511** are depicted in FIG. **5** for clarity of illustration, the system **500** can include any number of such components.

Modules or components **506** and components **508** and **511** can be mounted in a common housing **501**, schematically depicted in broken lines, and can be electrically interconnected with one another as necessary to form the desired circuit. The housing **501** is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen **510** can be exposed at the surface of the housing. In embodiments where a structure **506** includes a light-sensitive element such as an imaging chip, a lens **511** or other optical device also can be provided for routing light to the structure. Again, the simplified system shown in FIG. **5** is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like can be made using the structures discussed above.

It will be appreciated that the various dependent claims and the features set forth therein can be combined in different ways than presented in the initial claims. It will also be appreciated that the features described in connection with individual embodiments may be shared with others of the described embodiments. Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

The invention claimed is:

1. A microelectronic assembly, comprising:

a circuit panel having first and second opposed surfaces and an address bus comprising a plurality of signal conductors electrically connected with a plurality of mutually exclusive connection regions, each connection region including first panel contacts and second panel contacts electrically coupled with the first panel contacts disposed at the first and second surfaces, respectively; and

first and second microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively, each microelectronic package having first, second, and third microelectronic elements therein, each microelectronic element electrically coupled to the address bus via only one of the connection regions,

wherein the first and third microelectronic elements of the first microelectronic package and the second microelectronic element of the second microelectronic package are electrically coupled to the address bus only at a first one of the connection regions, and

wherein the second microelectronic element of the first microelectronic package and the first and third microelectronic elements of the second microelectronic package are electrically coupled to the address bus only at a second one of the connection regions.

2. The microelectronic assembly as claimed in claim **1**, wherein the address bus is configured to carry all address signals usable by circuitry within the first and second microelectronic packages.

3. The microelectronic assembly as claimed in claim **1**, wherein each of the microelectronic elements embodies a greater number of active devices to provide memory storage array function than any other function.

4. The microelectronic assembly as claimed in claim **1**, wherein the first terminals of the first and second microelectronic packages are arranged at positions of first and second grids, and wherein the first and second grids are aligned with one another in x and y orthogonal directions parallel to the first and second surfaces of the circuit panel, the alignment being within a distance equal to a minimum pitch between adjacent terminals of the grids.

5. The microelectronic assembly as claimed in claim **1**, further comprising third and fourth microelectronic packages having first terminals mounted to the first panel contacts and the second panel contacts, respectively, each of the third and fourth microelectronic packages having first, second, and third microelectronic elements therein, each microelectronic element electrically coupled to the address bus via only one of the connection regions,

wherein the first and third microelectronic elements of the third microelectronic package and the second microelectronic element of the fourth microelectronic package are electrically coupled to the address bus only at a third one of the connection regions,

wherein the second microelectronic element of the third microelectronic package and the first and third microelectronic elements of the fourth microelectronic package are electrically coupled to the address bus only at a fourth one of the connection regions, and

wherein an electrical characteristic between the first and second connection regions is within a same tolerance of the electrical characteristic between the second and third connection regions.

6. The microelectronic assembly as claimed in claim **5**, wherein the electrical characteristic is an electrical trace length.

7. The microelectronic assembly as claimed in claim **5**, wherein the electrical characteristic is an electrical propagation delay.

8. The microelectronic assembly as claimed in claim **5**, wherein the electrical characteristic is a characteristic impedance of the signal conductors.

9. The microelectronic assembly as claimed in claim **5**, wherein the electrical characteristic is a difference in an electrical load applied to the address bus from the microelectronic elements connected with the respective connection region.

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