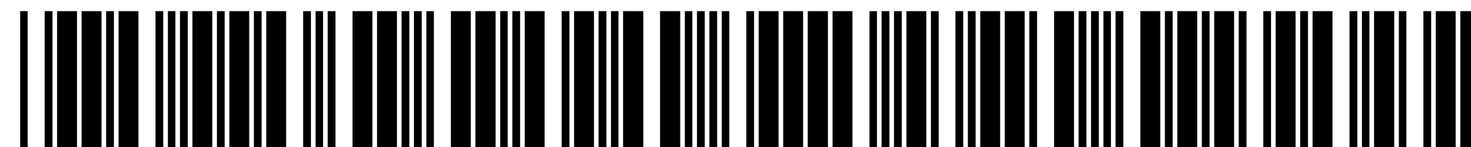

US009673154B2

(12) **United States Patent**
Tsutsue et al.

(10) **Patent No.: US 9,673,154 B2**
(45) **Date of Patent: Jun. 6, 2017**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **PANASONIC CORPORATION**, Osaka (JP)

(72) Inventors: **Makoto Tsutsue**, Shiga (JP); **Masaki Utsumi**, Kyoto (JP)

(73) Assignee: **PANASONIC CORPORATION**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/147,606**

(22) Filed: **May 5, 2016**

(65) **Prior Publication Data**

US 2016/0247771 A1 Aug. 25, 2016

Related U.S. Application Data

(60) Continuation of application No. 14/663,436, filed on Mar. 19, 2015, now abandoned, which is a division of
(Continued)

(30) **Foreign Application Priority Data**

Nov. 10, 2003 (JP) 2003-379754

(51) **Int. Cl.**
H01L 29/66 (2006.01)
H01L 23/58 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 23/585*** (2013.01); ***H01L 23/3171*** (2013.01); ***H01L 23/3192*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 23/585; H01L 23/3171; H01L 23/3192; H01L 23/5226; H01L 23/528; H01L 23/562; H01L 23/564; H01L 23/522
(Continued)

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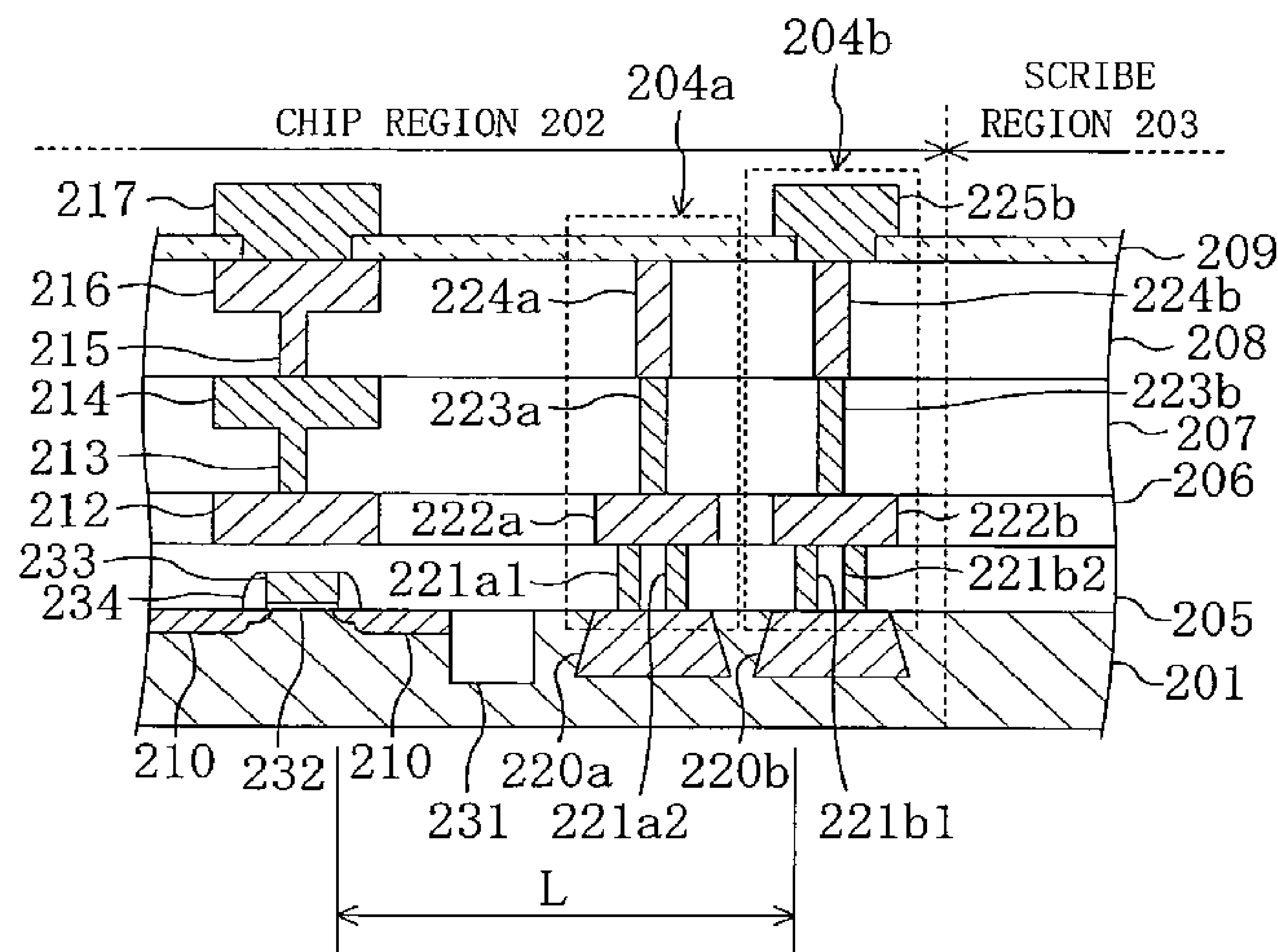
Primary Examiner — Tu-Tu Ho
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A seal ring structure is formed through a multilayer structure of a plurality of dielectric films in a peripheral part of a chip region to surround the chip region. A dual damascene interconnect in which an interconnect and a plug connected to the interconnect are integrated is formed in at least one of the dielectric films in the chip region. Part of the seal ring structure formed in the dielectric film in which the dual damascene interconnect is formed is continuous. A protection film formed on the multilayer structure has an opening on the seal ring. A cap layer connected to the seal ring is formed in the opening.

20 Claims, 19 Drawing Sheets



Related U.S. Application Data

application No. 14/231,150, filed on Mar. 31, 2014, now Pat. No. 9,082,779, which is a continuation of application No. 13/941,156, filed on Jul. 12, 2013, now Pat. No. 8,710,595, which is a continuation of application No. 13/551,425, filed on Jul. 17, 2012, now Pat. No. 8,618,618, which is a division of application No. 13/171,181, filed on Jun. 28, 2011, now Pat. No. 8,247,876, which is a division of application No. 12/858,942, filed on Aug. 18, 2010, now Pat. No. 7,994,589, which is a division of application No. 12/264,675, filed on Nov. 4, 2008, now Pat. No. 7,948,039, which is a division of application No. 10/983,760, filed on Nov. 9, 2004, now Pat. No. 7,453,128.

(51) **Int. Cl.**
H01L 23/00 (2006.01)
H01L 23/31 (2006.01)
H01L 23/528 (2006.01)
H01L 23/522 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/528*** (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 23/562*** (2013.01); ***H01L 23/564*** (2013.01); *H01L 23/522* (2013.01); *H01L 2924/0002* (2013.01); *H01L 2924/12044* (2013.01)

(58) **Field of Classification Search**
USPC 257/409
See application file for complete search history.

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FIG. 1

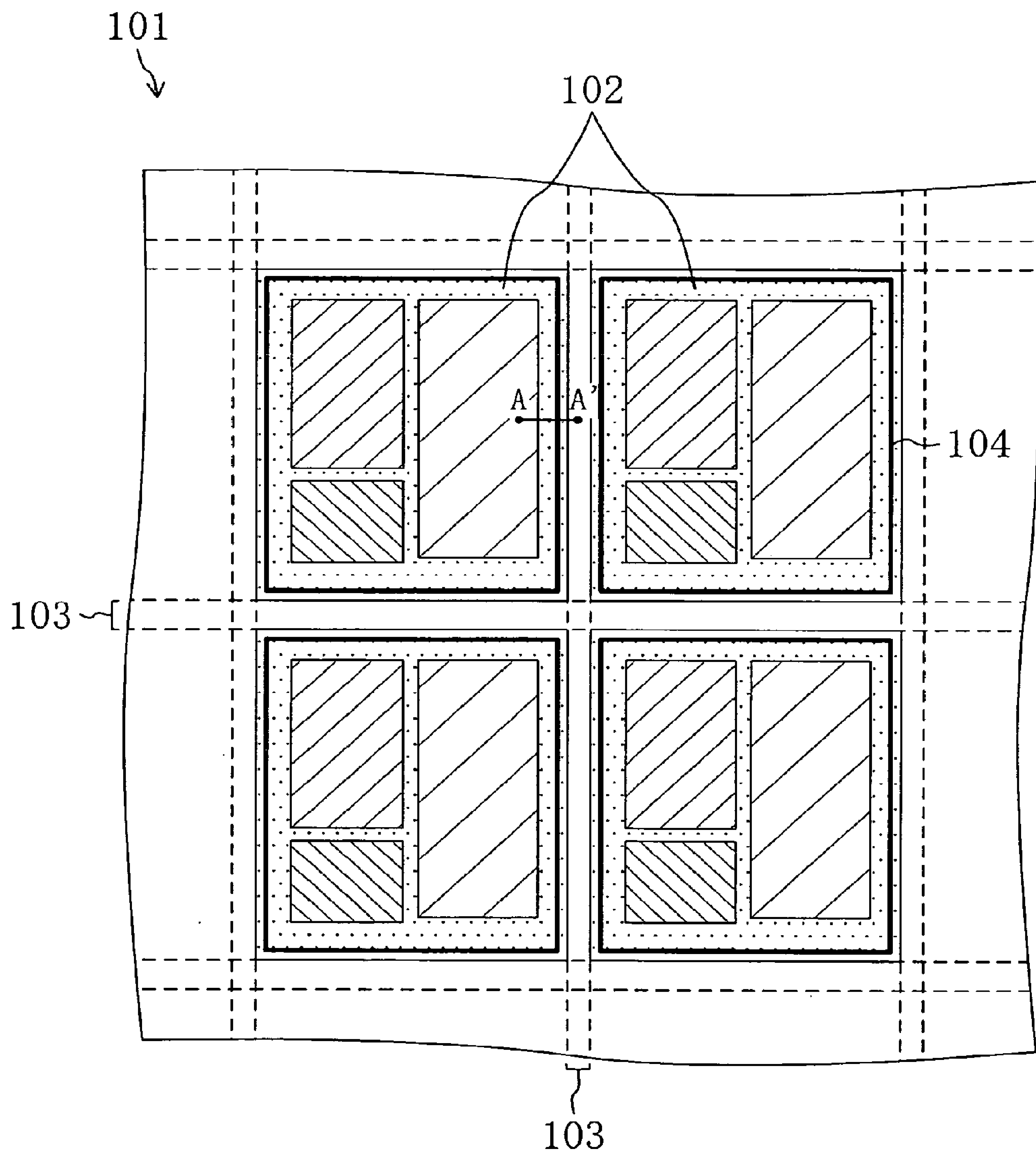


FIG. 2A

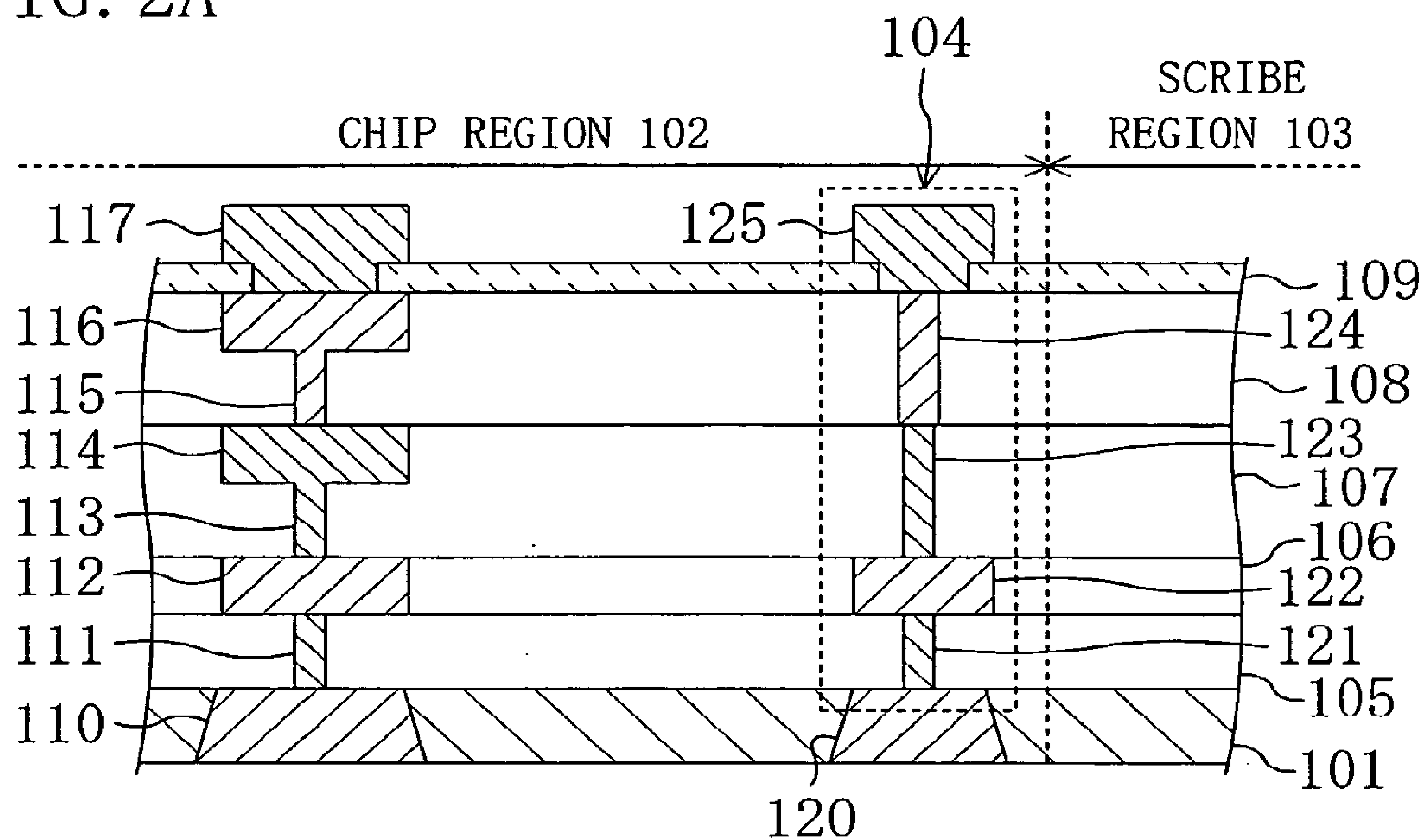


FIG. 2B

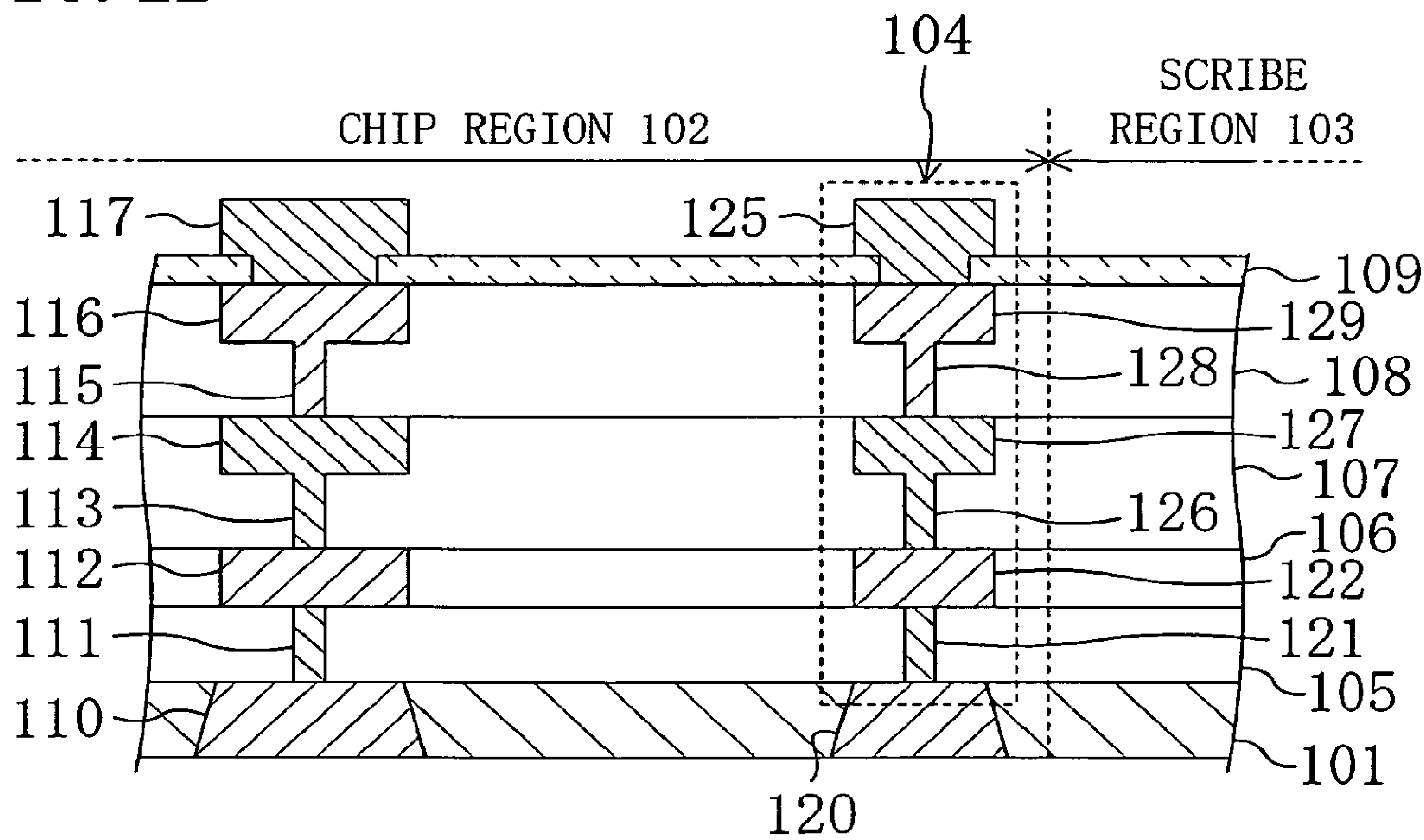


FIG. 3A

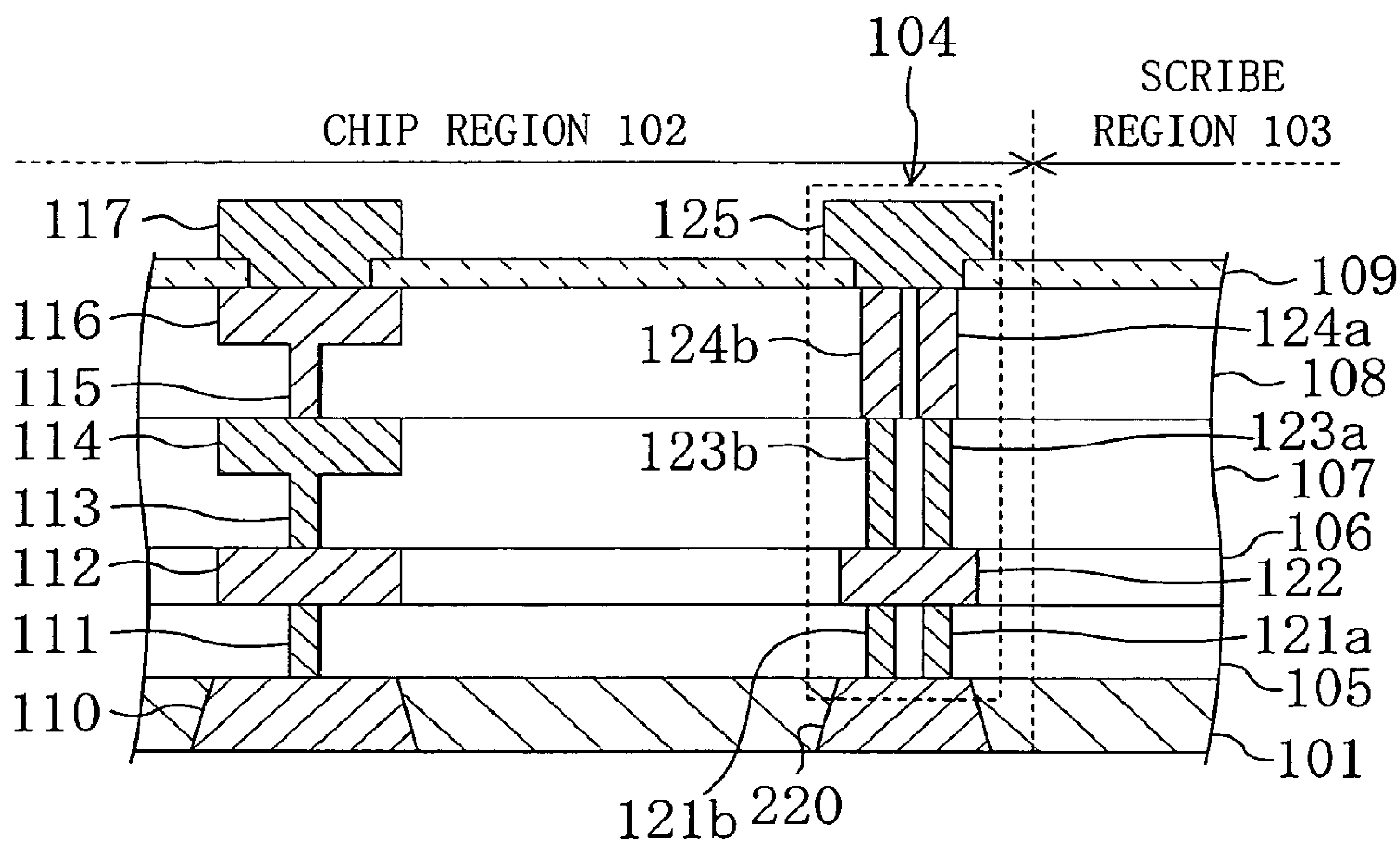


FIG. 3B

FIG. 4A

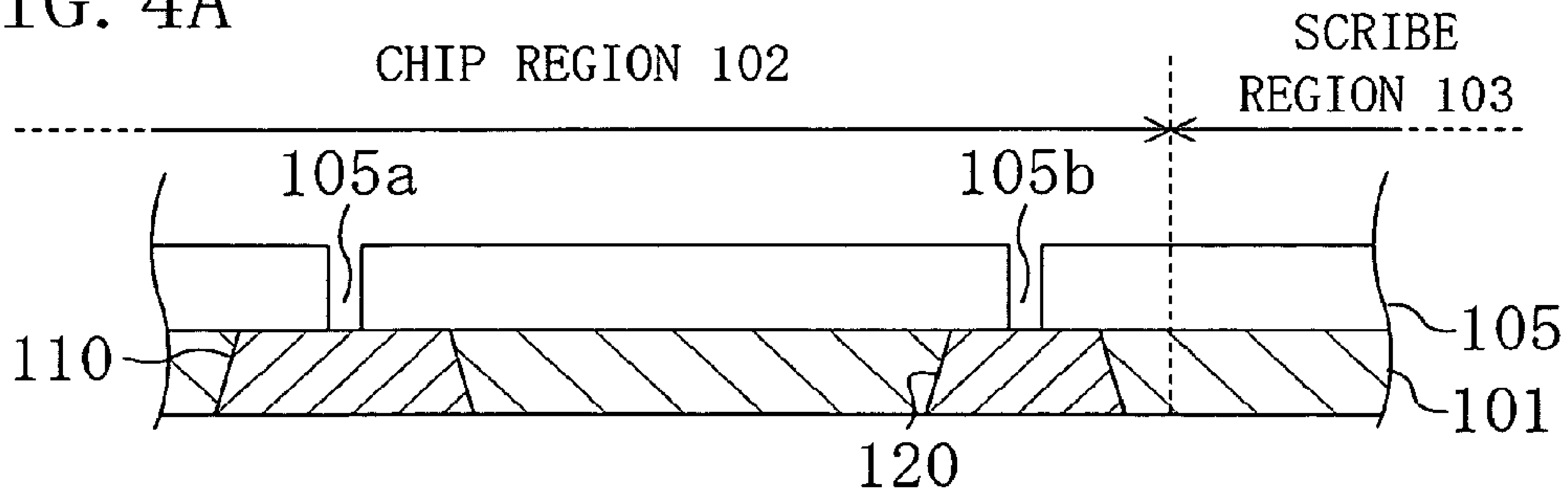


FIG. 4B

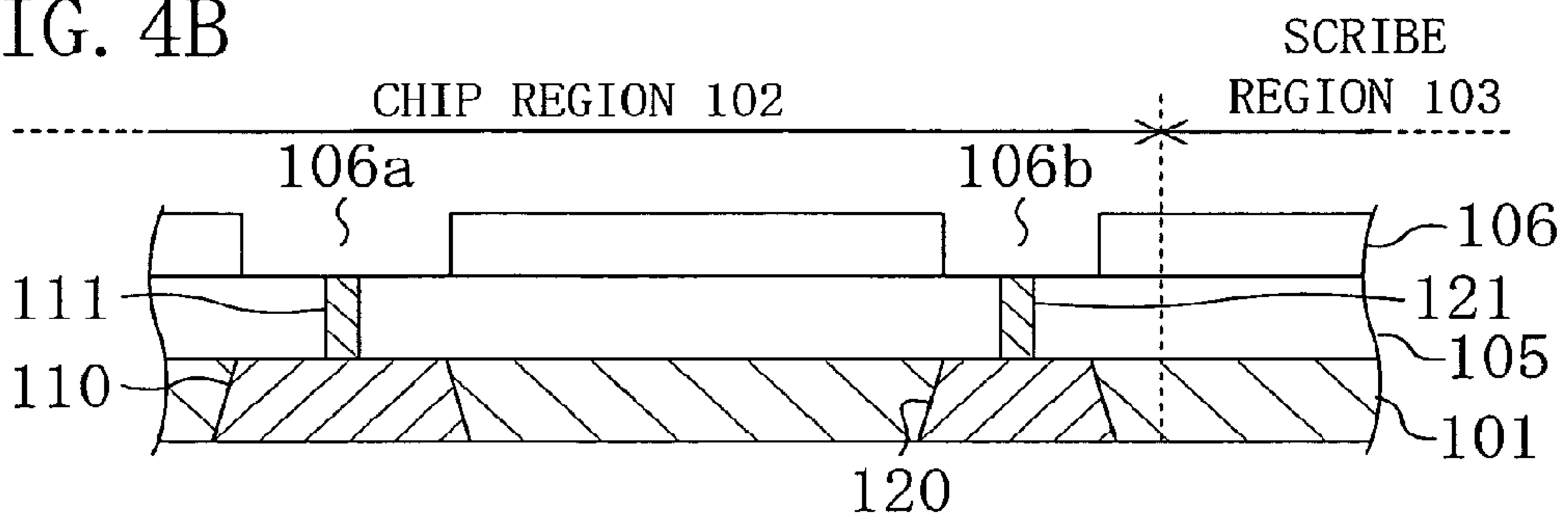


FIG. 4C

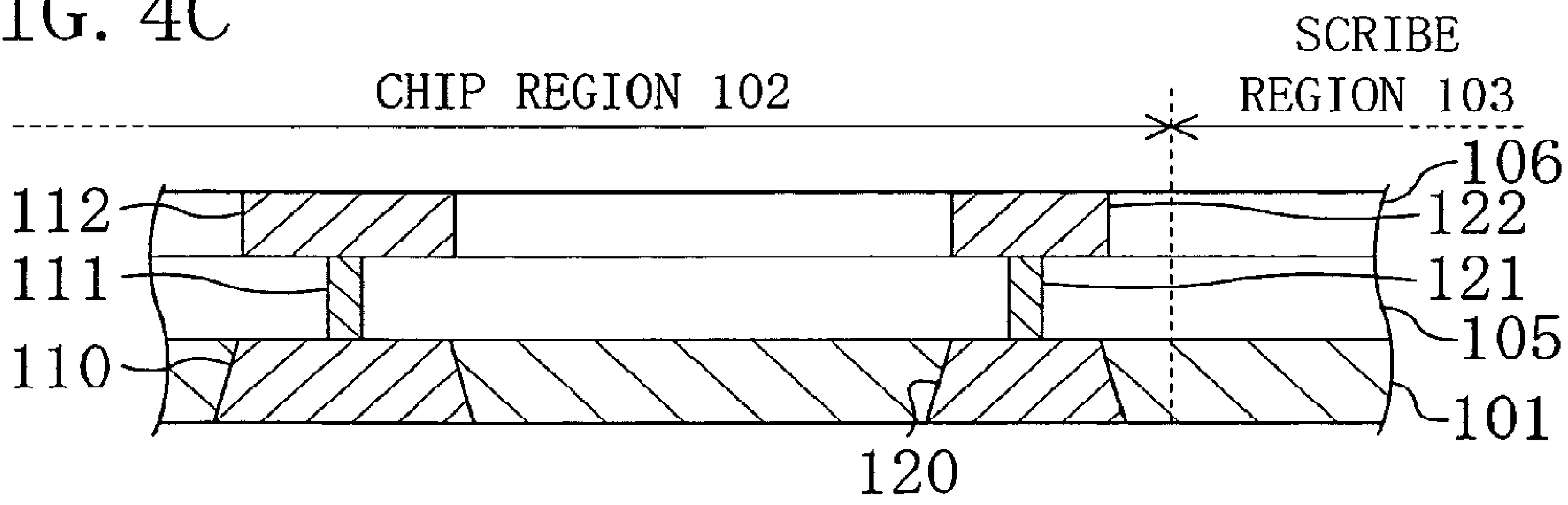


FIG. 4D

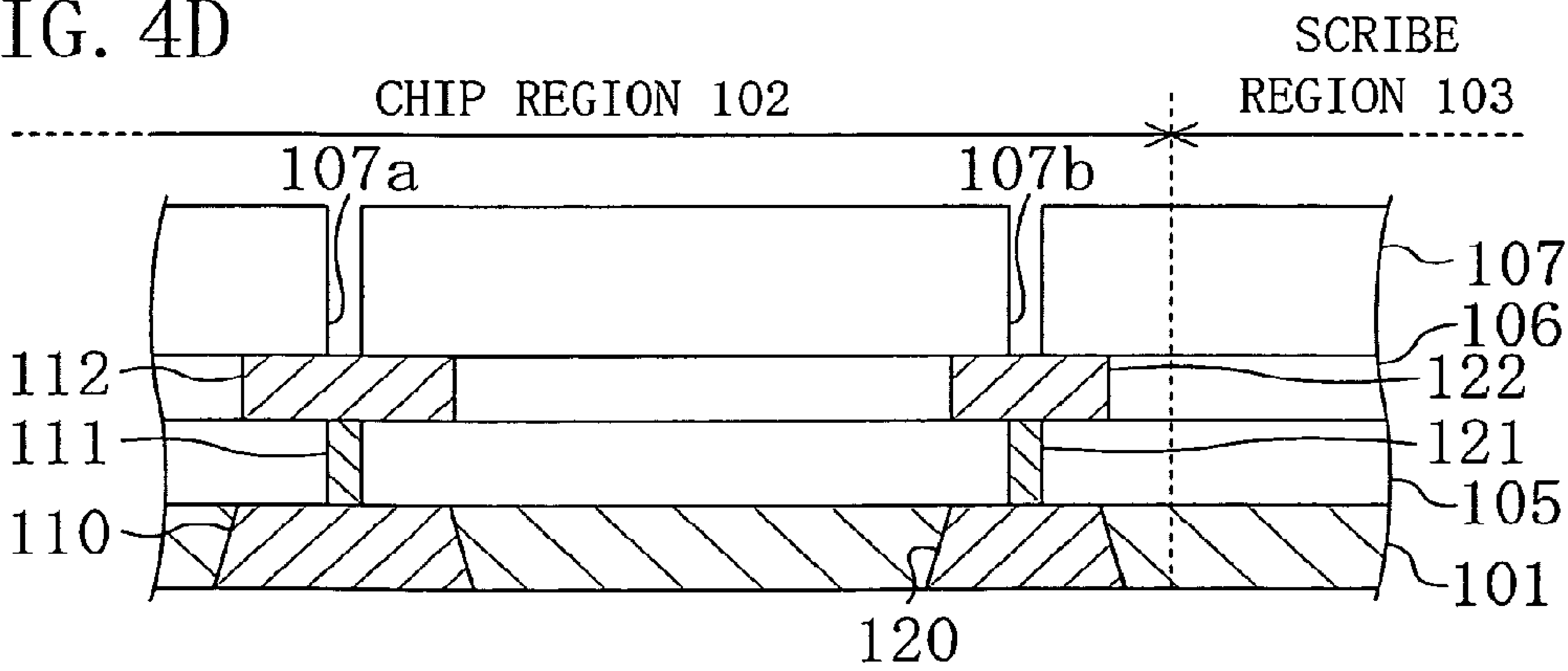


FIG. 5A

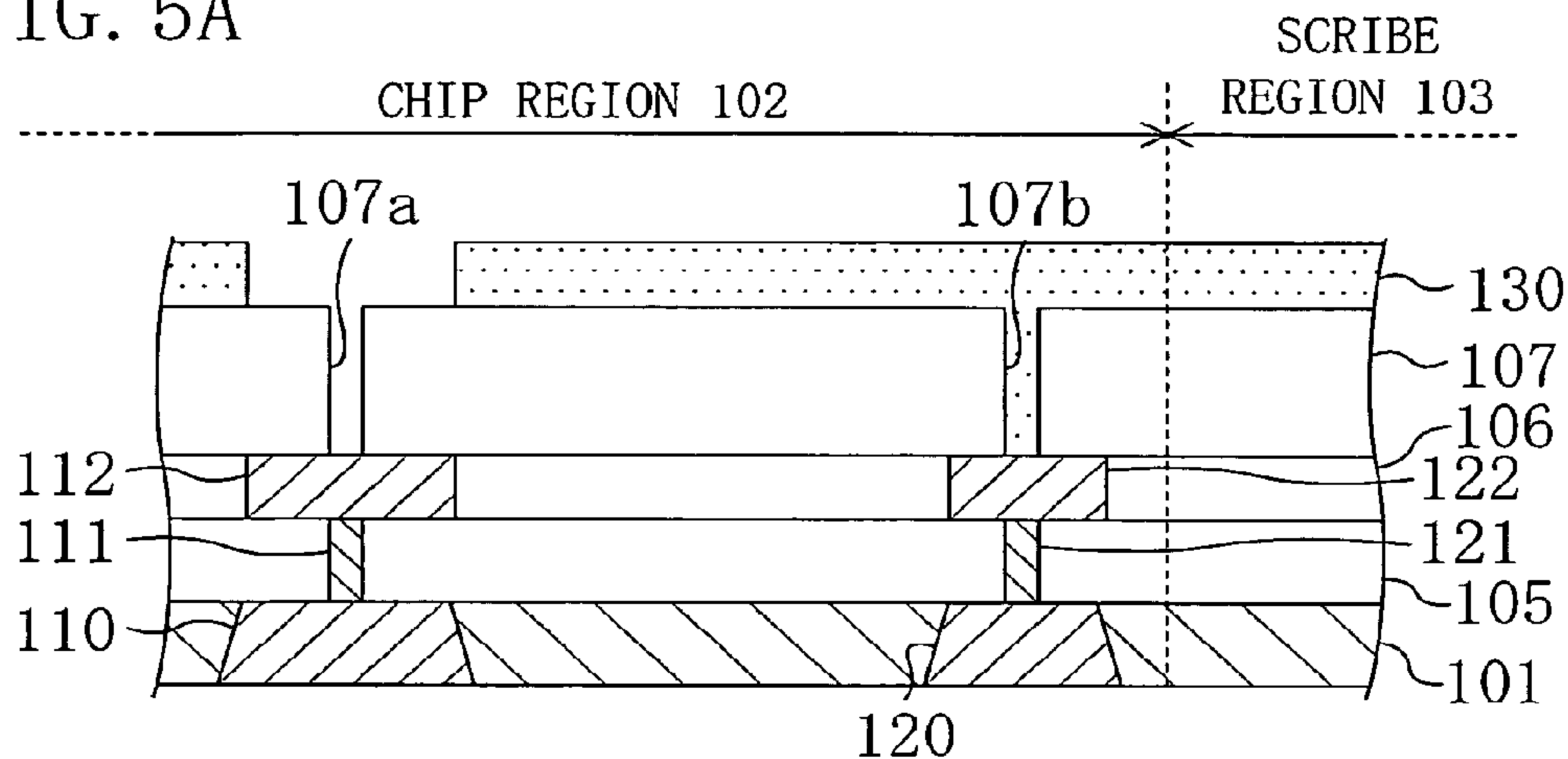


FIG. 5B

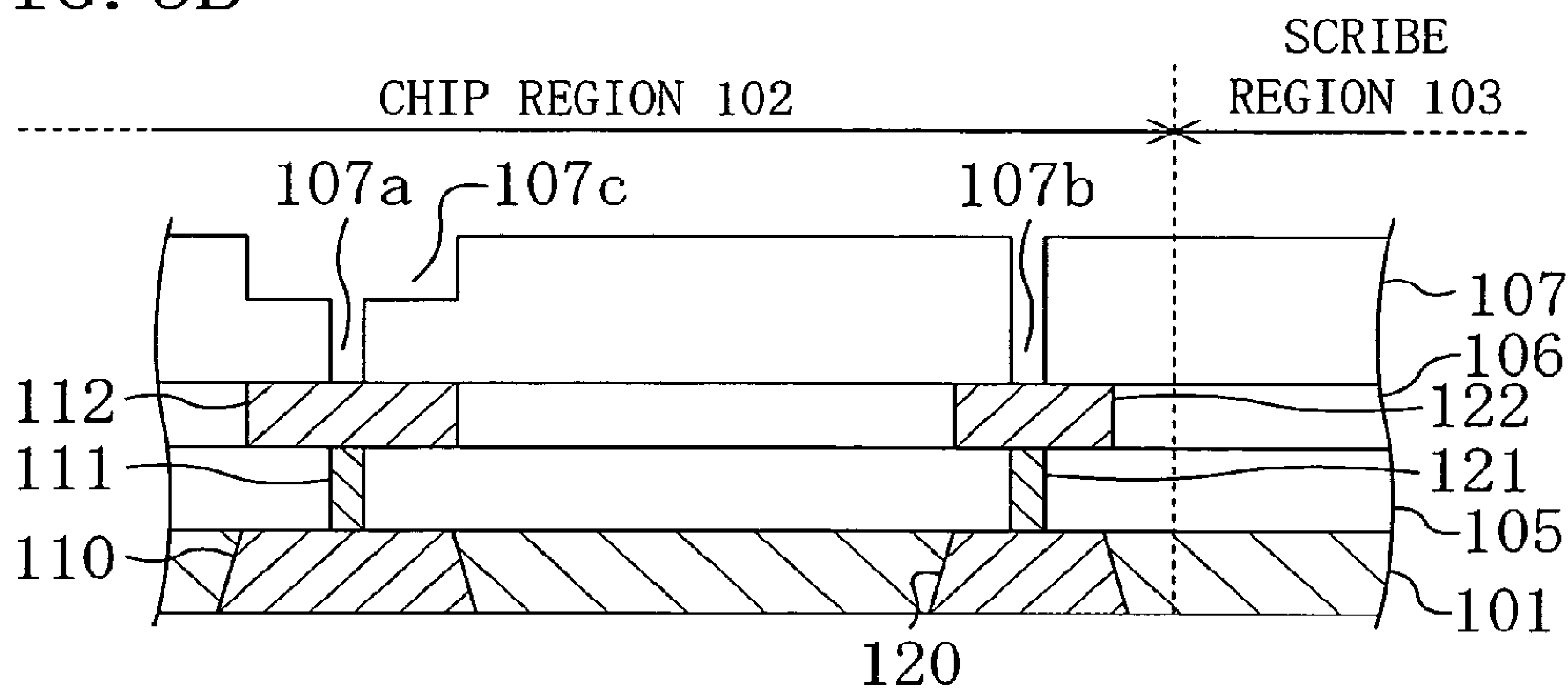


FIG. 5C

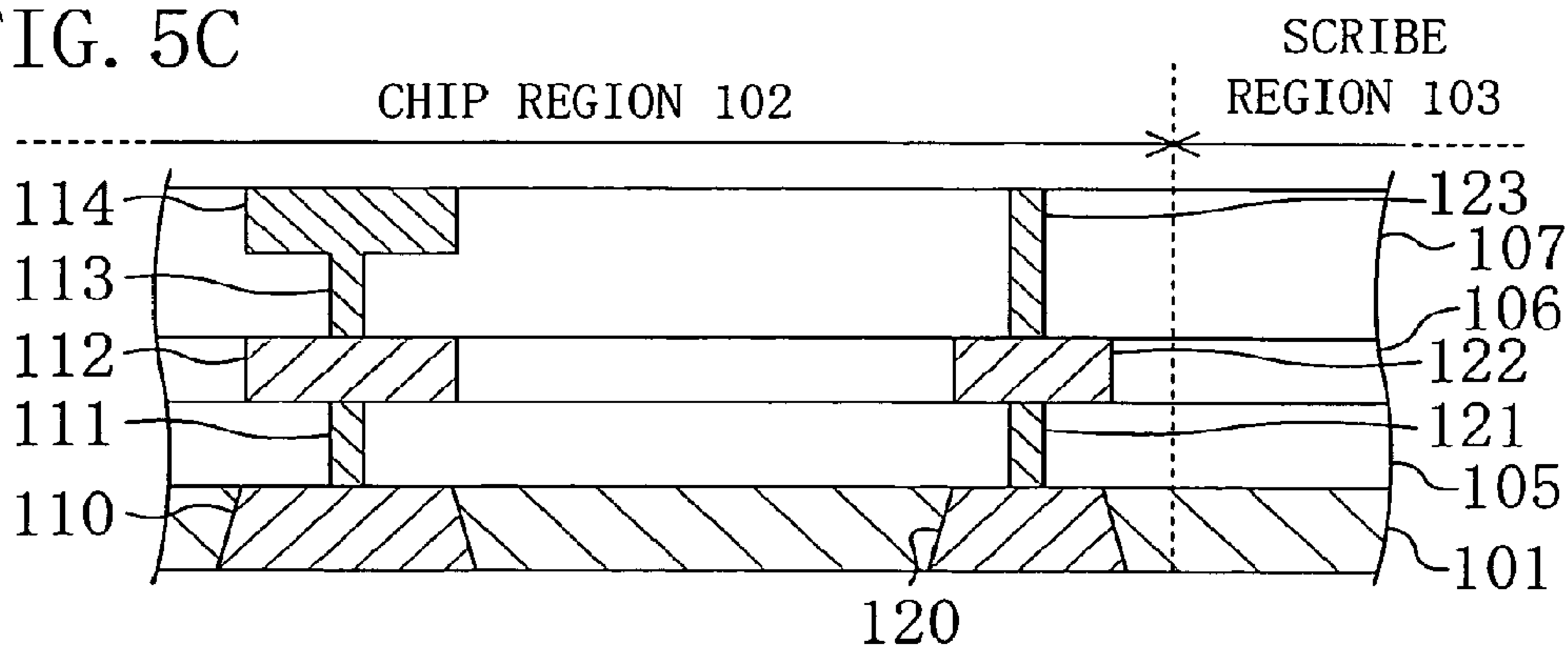


FIG. 6A

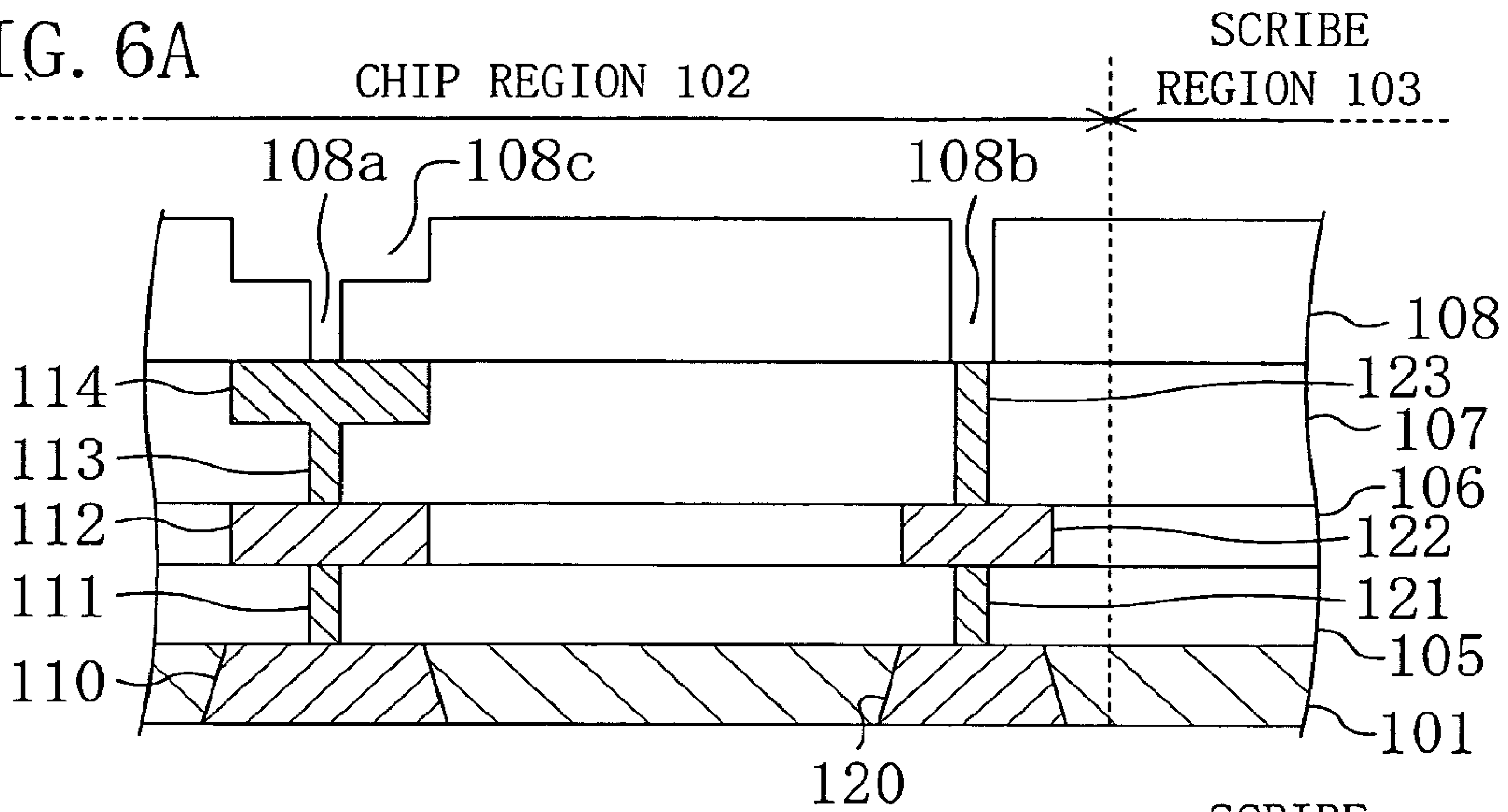


FIG. 6B

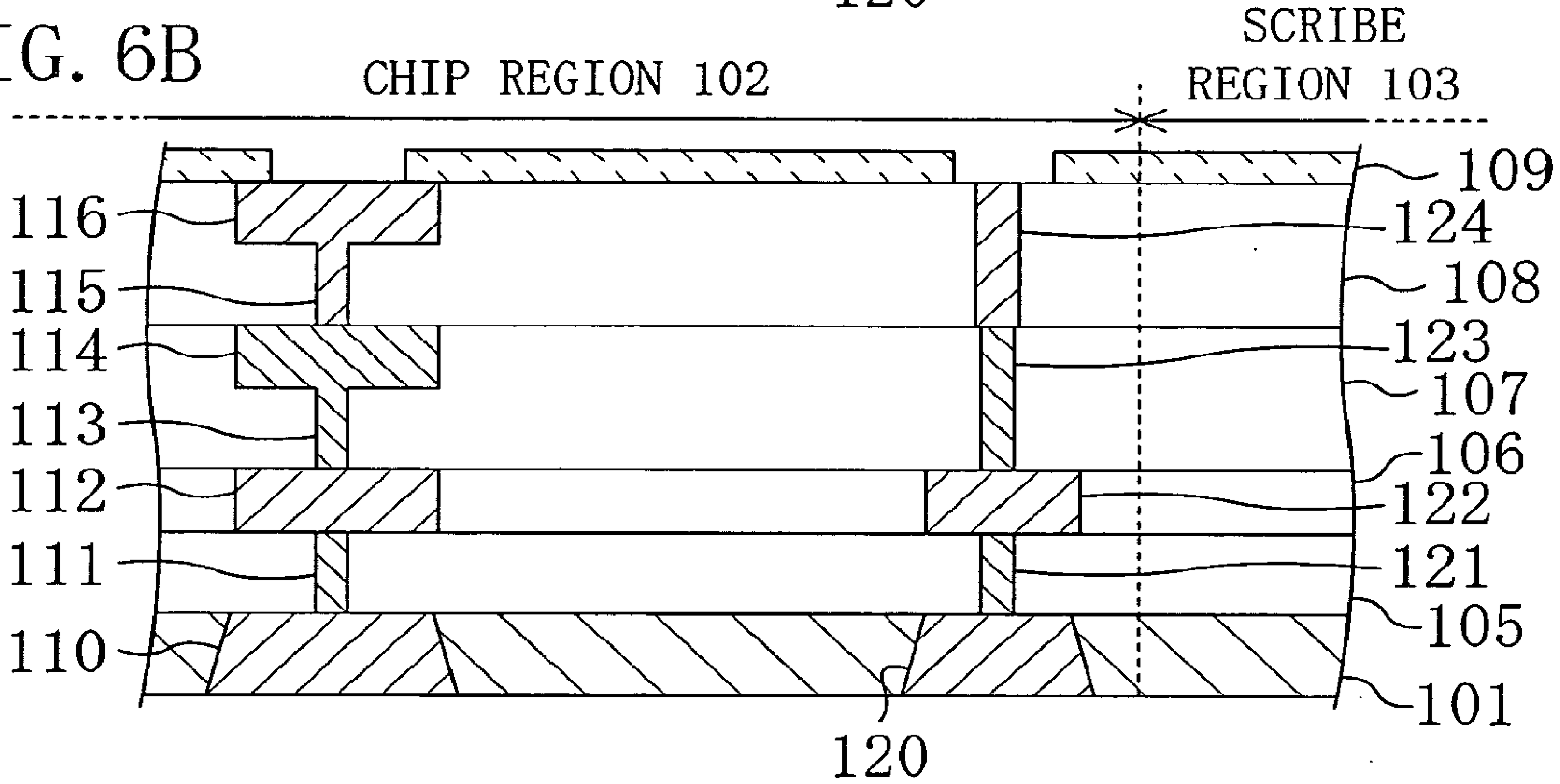


FIG. 6C

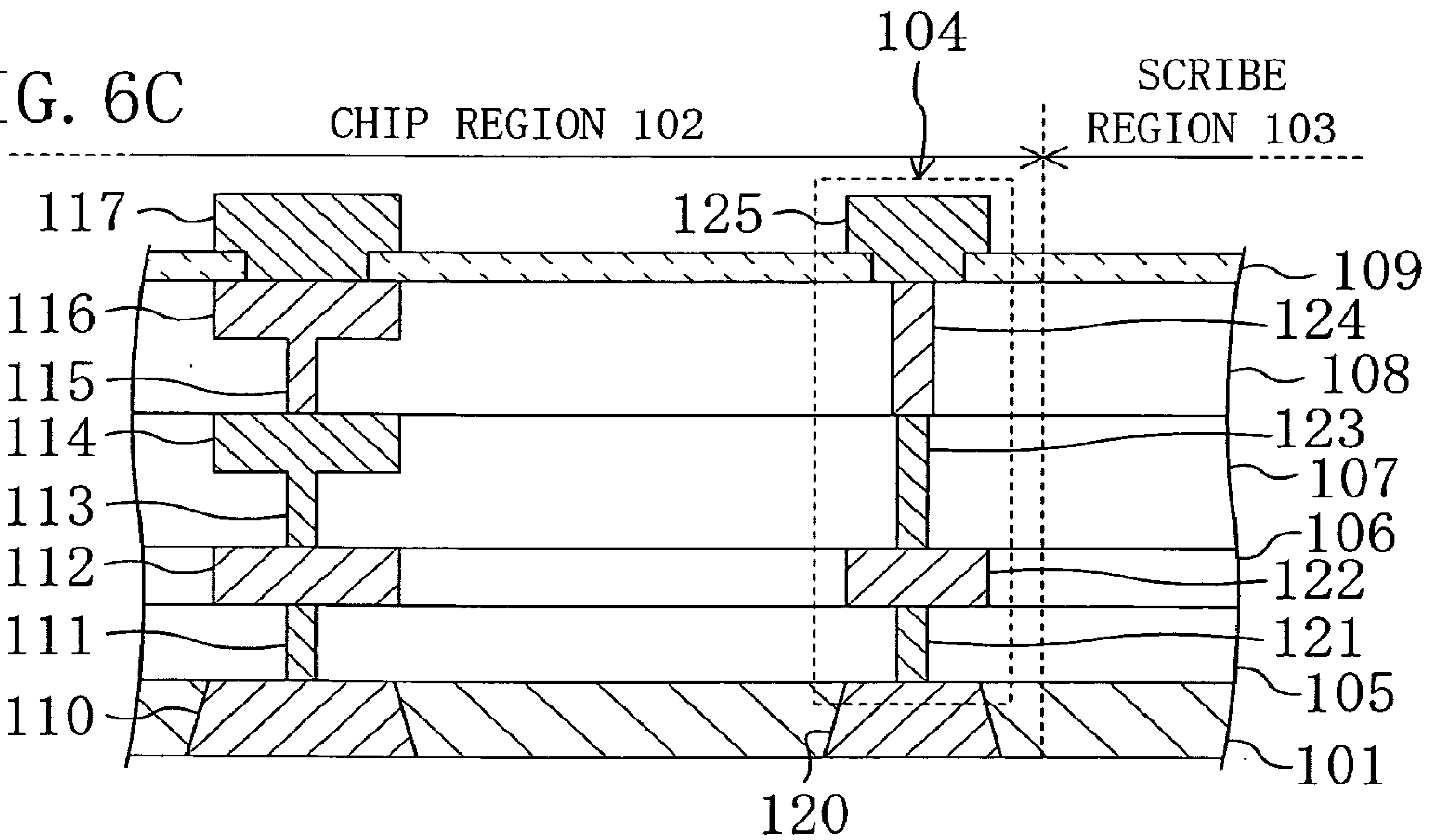


FIG. 7

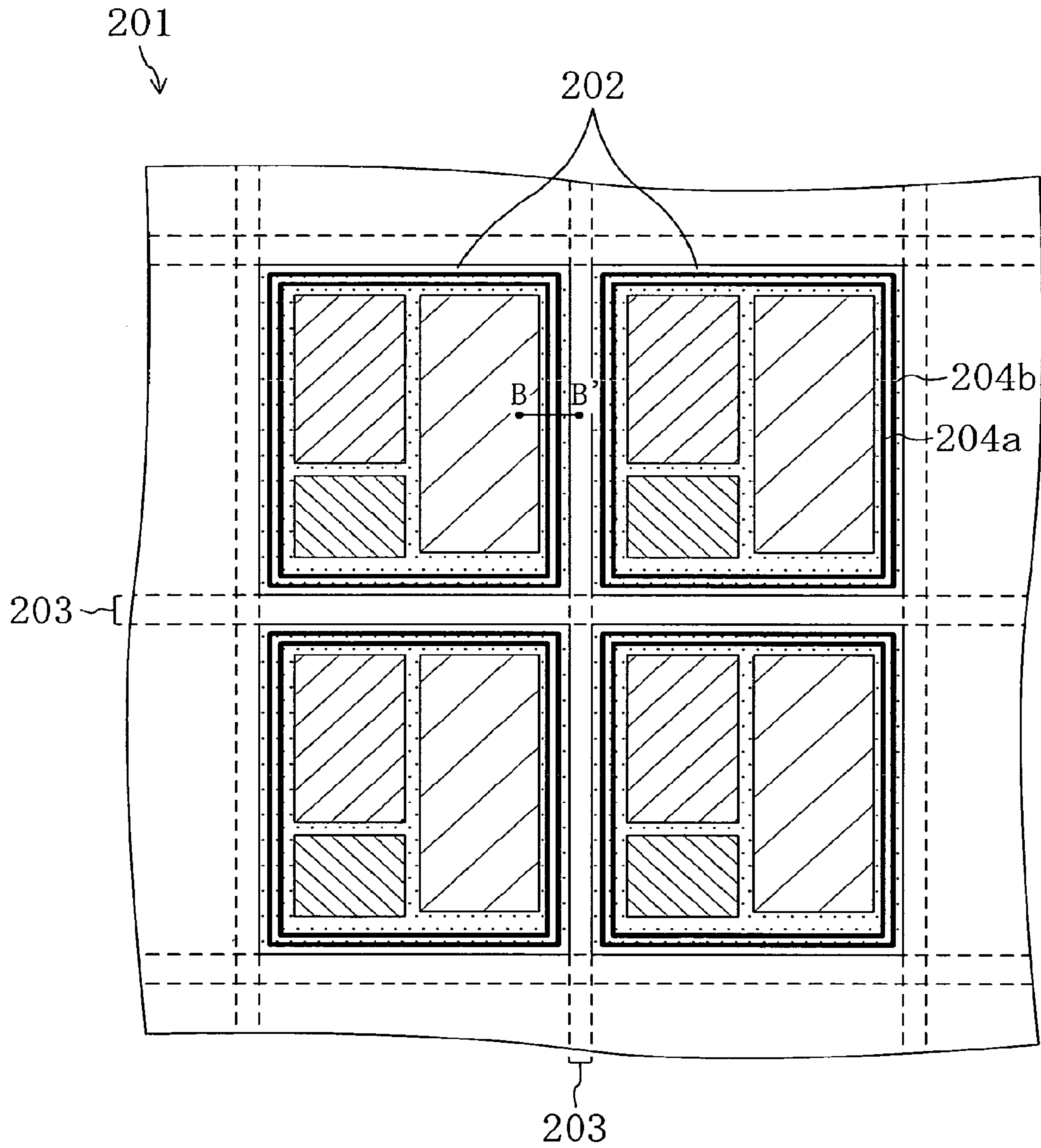


FIG. 8A

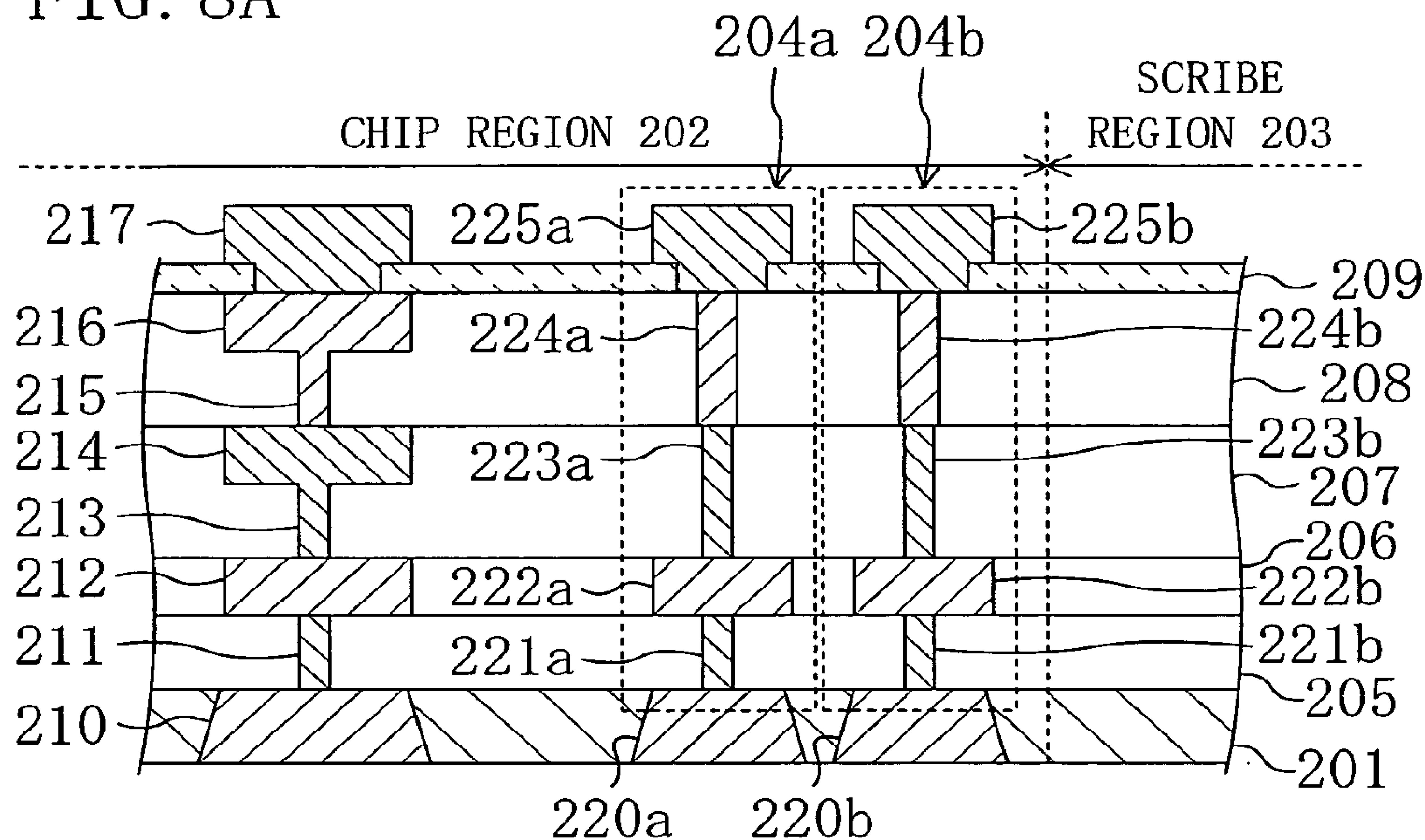


FIG. 8B

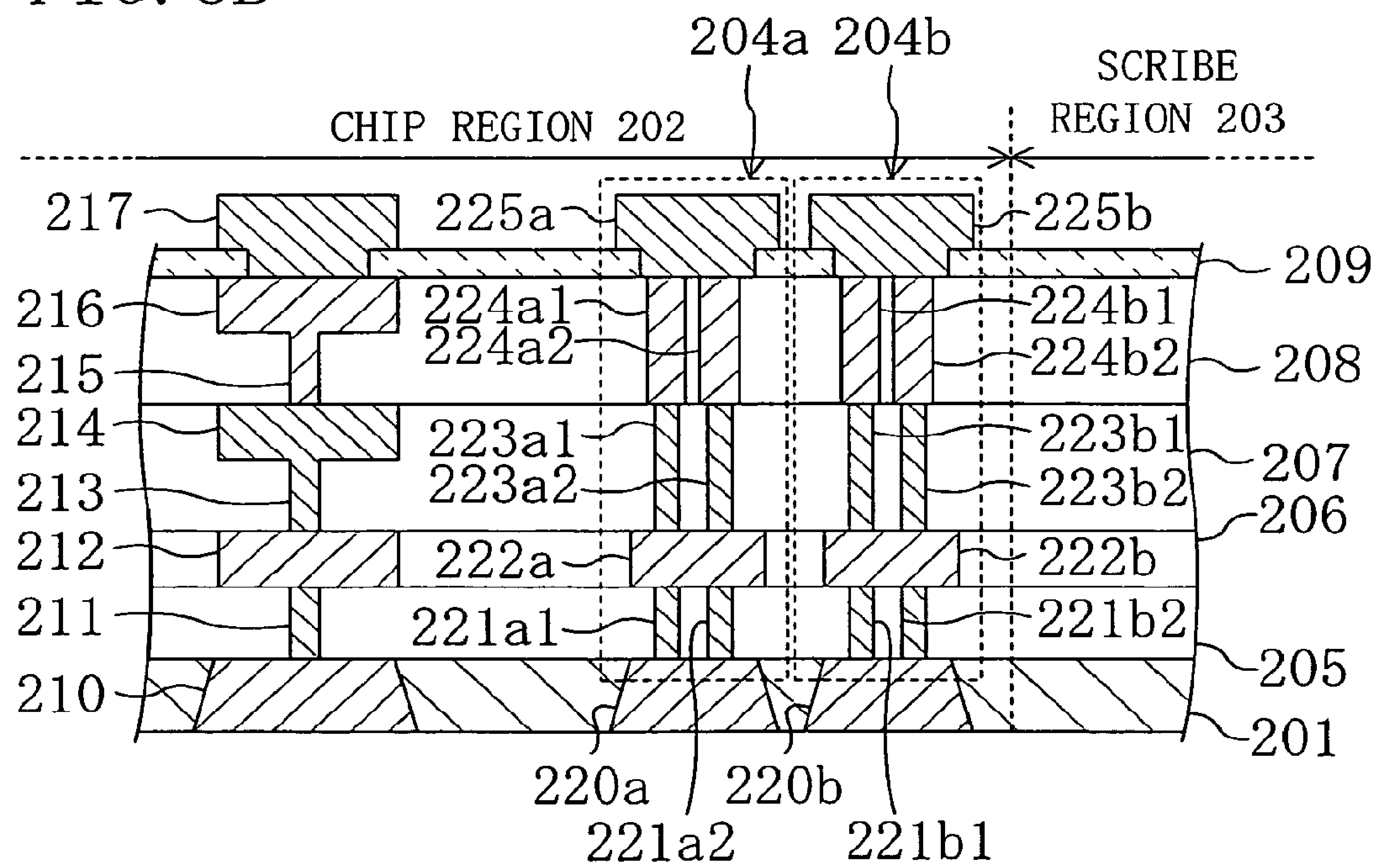


FIG. 9A

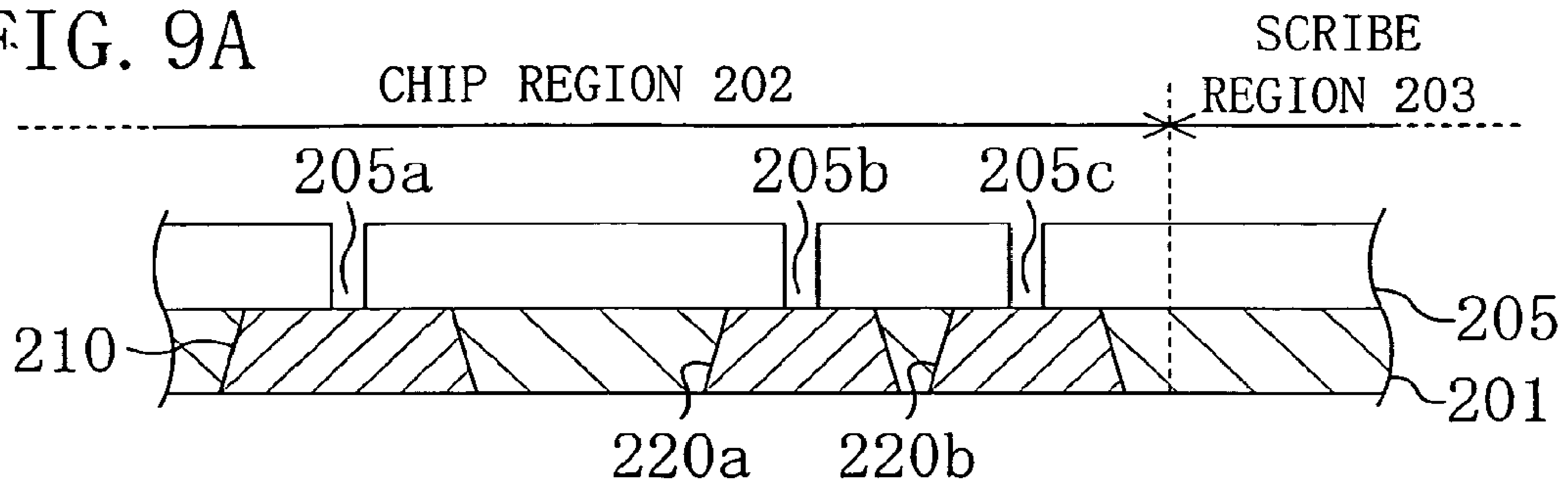


FIG. 9B

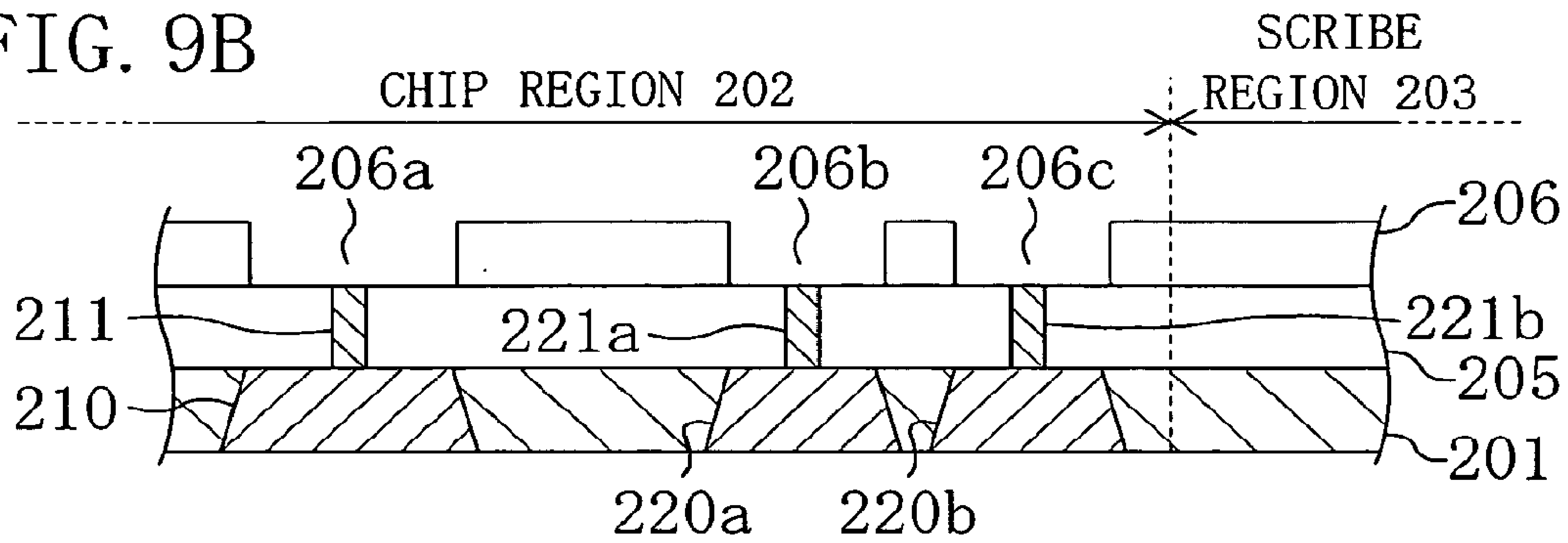


FIG. 9C

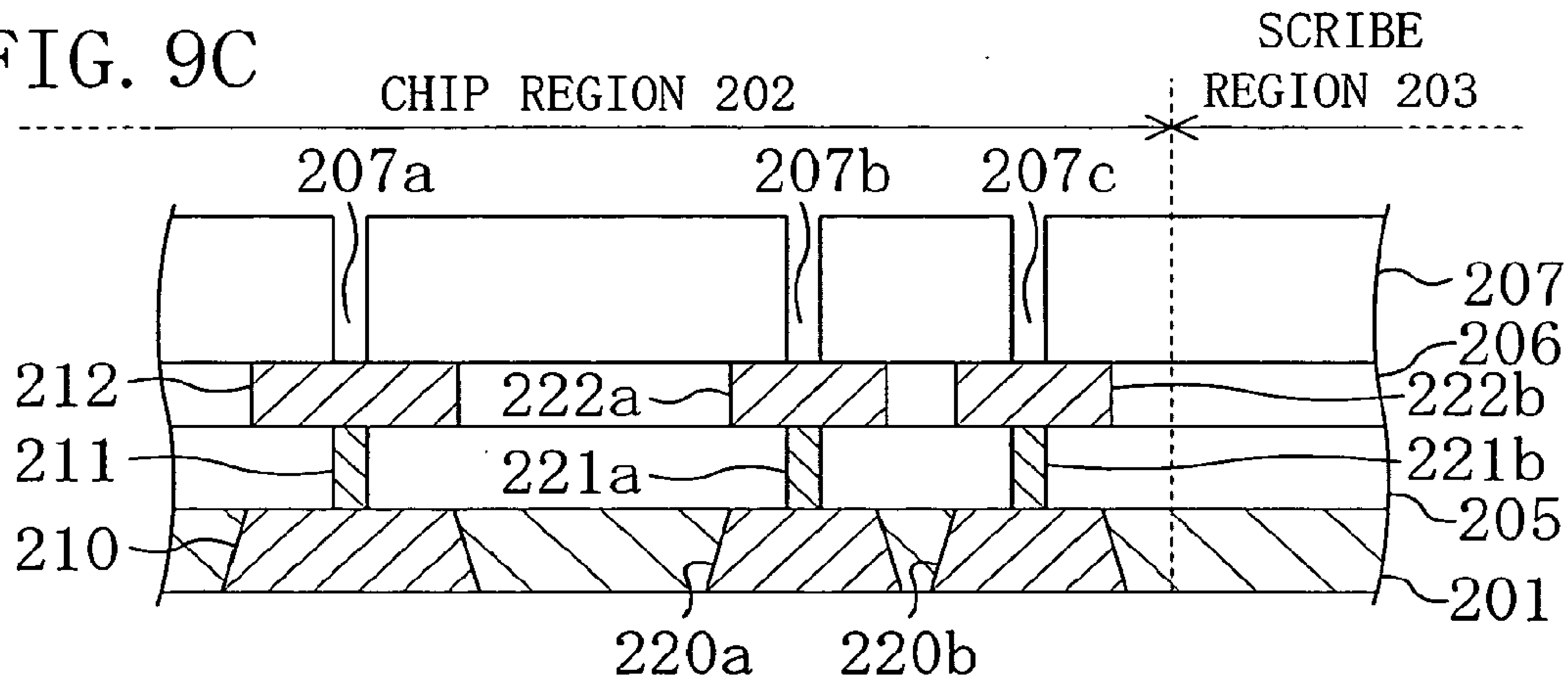


FIG. 9D

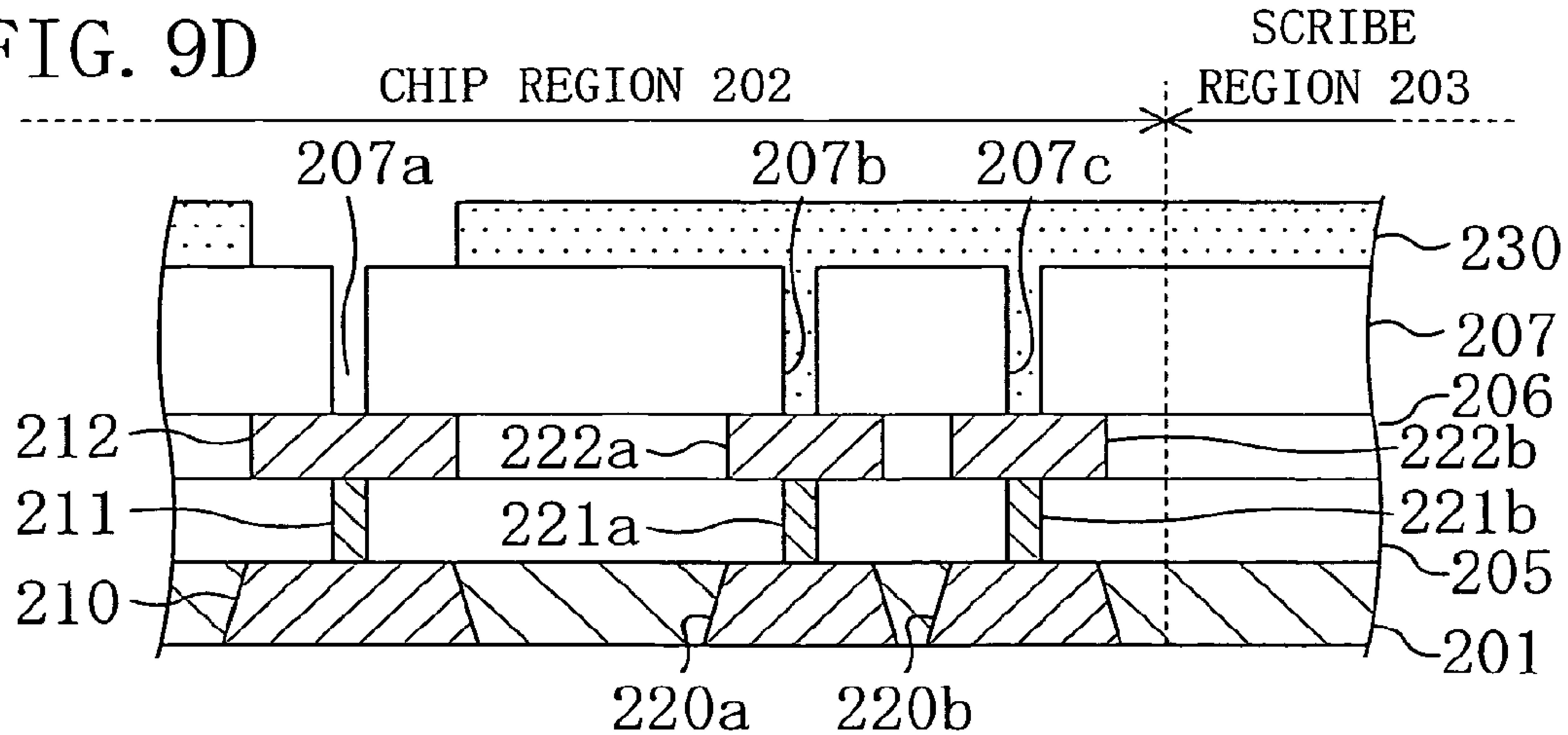


FIG. 10A

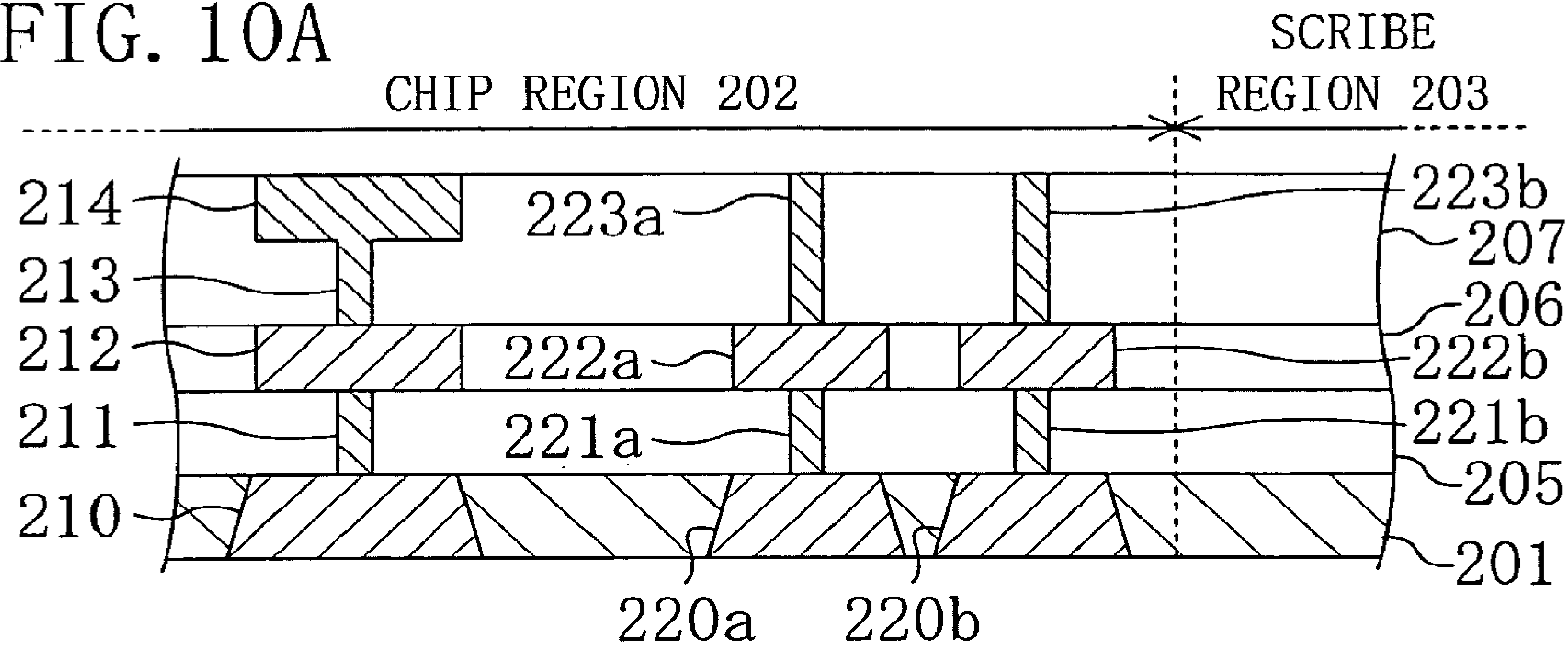


FIG. 10B

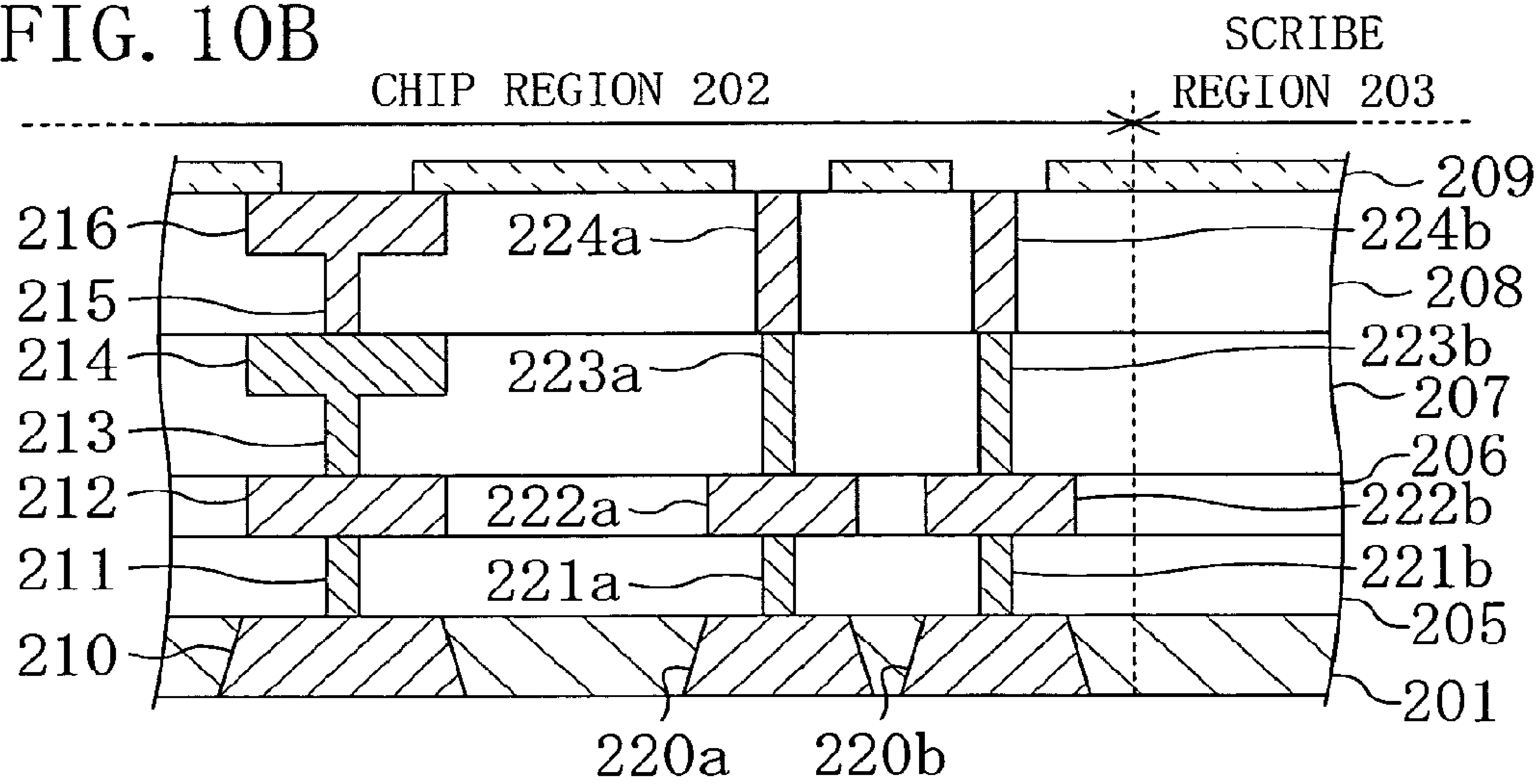


FIG. 10C

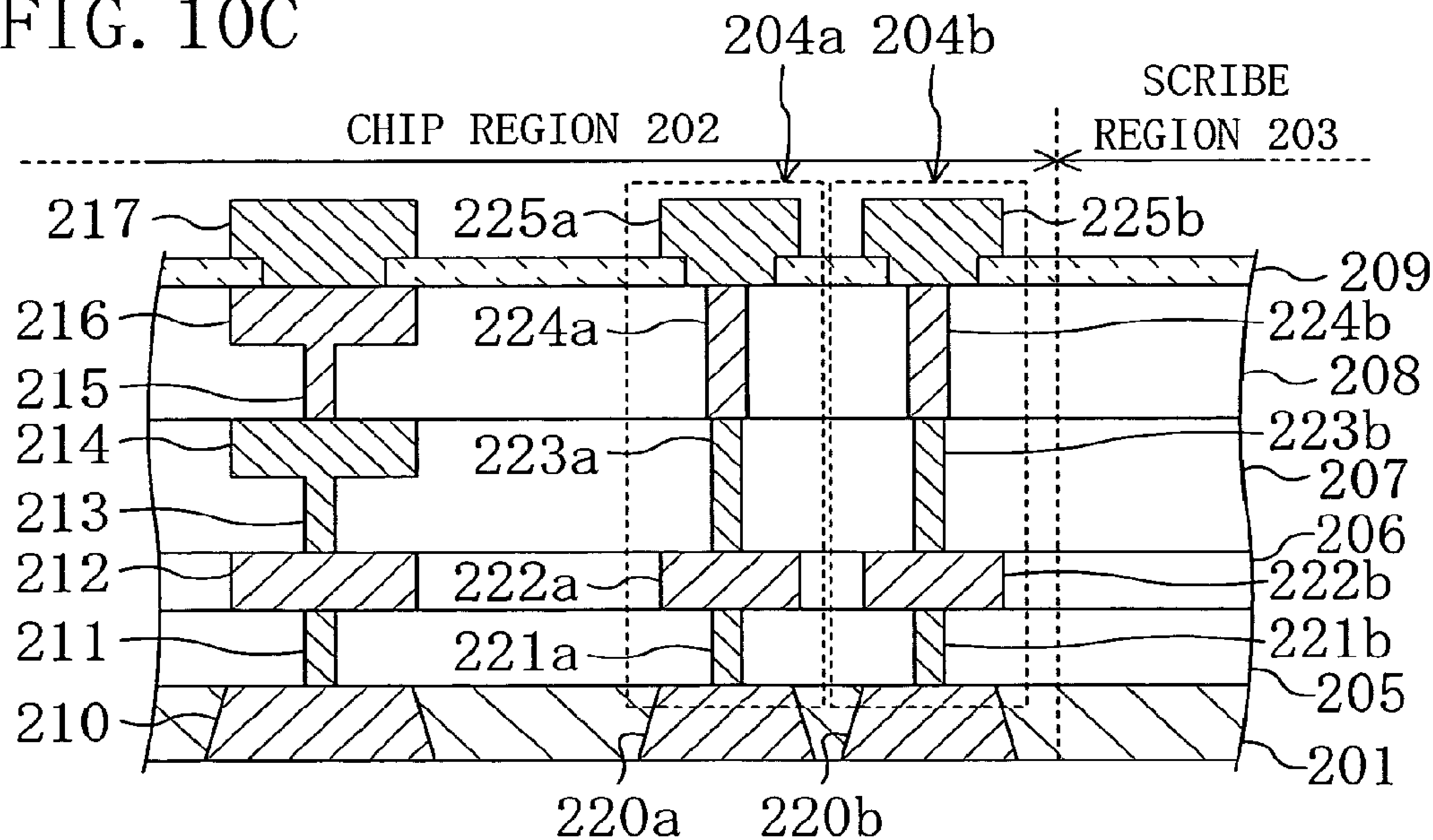


FIG. 11A

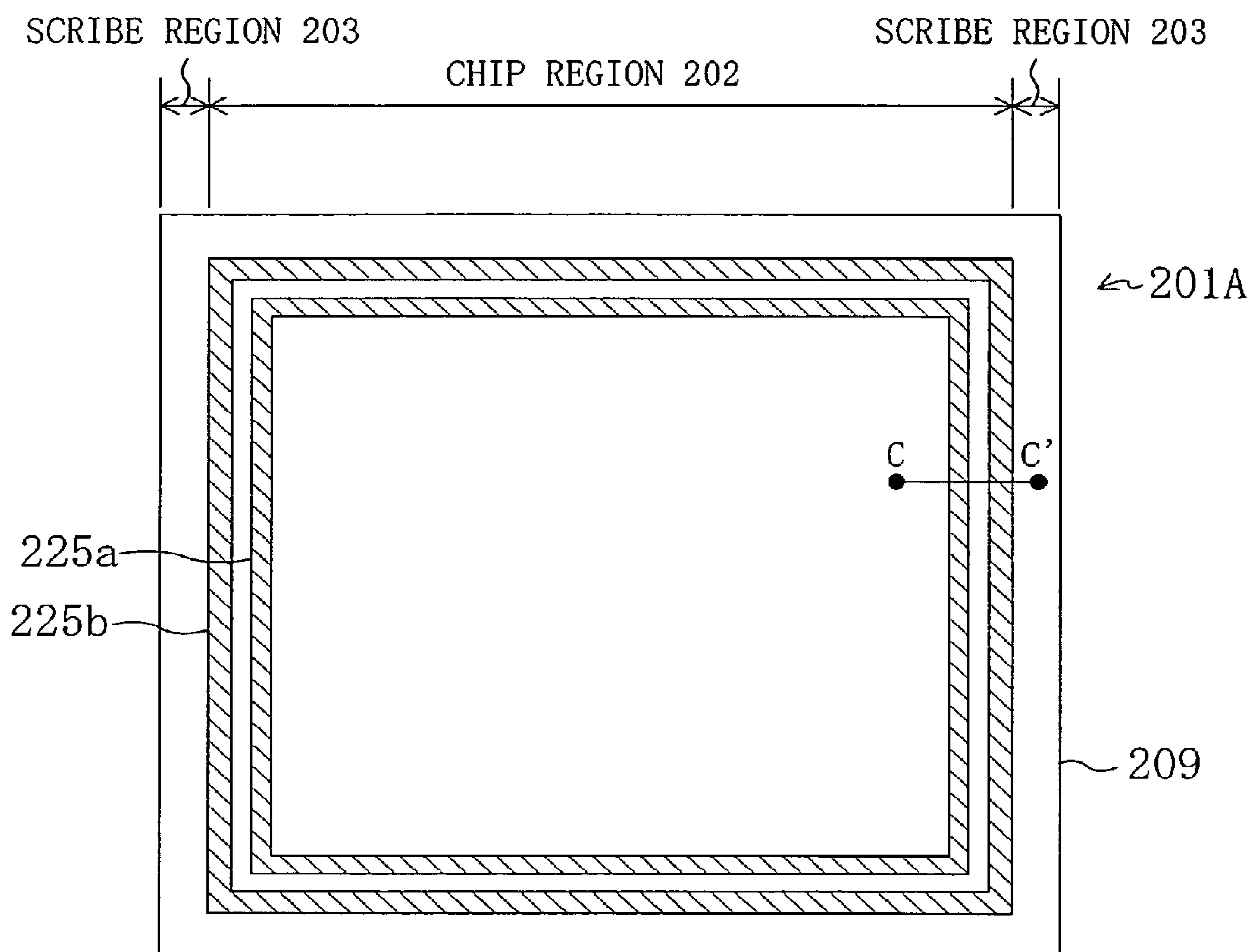


FIG. 11B

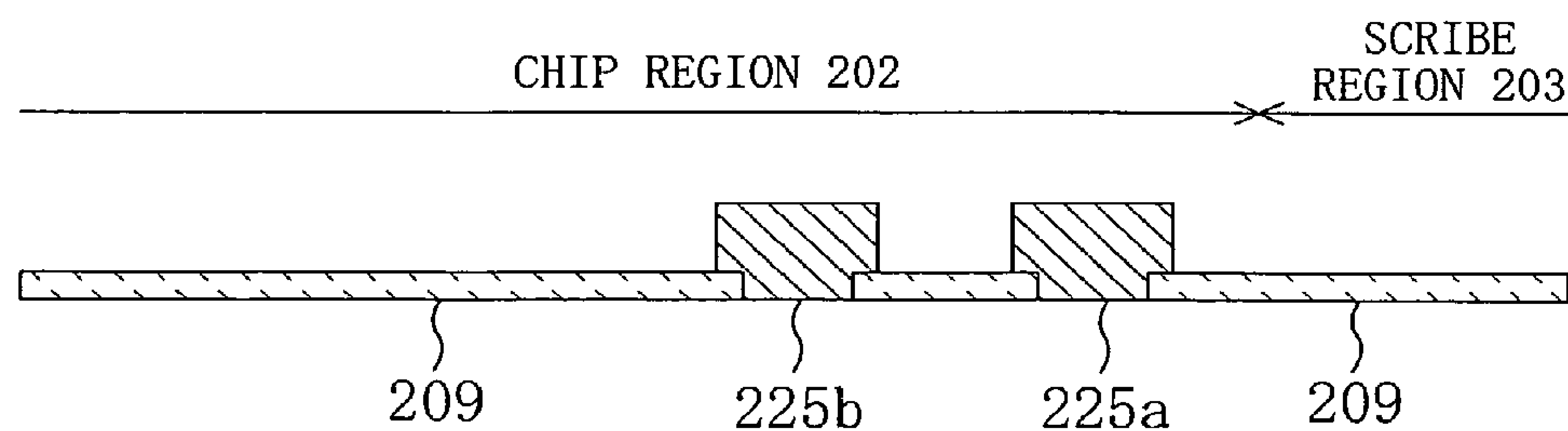


FIG. 12A

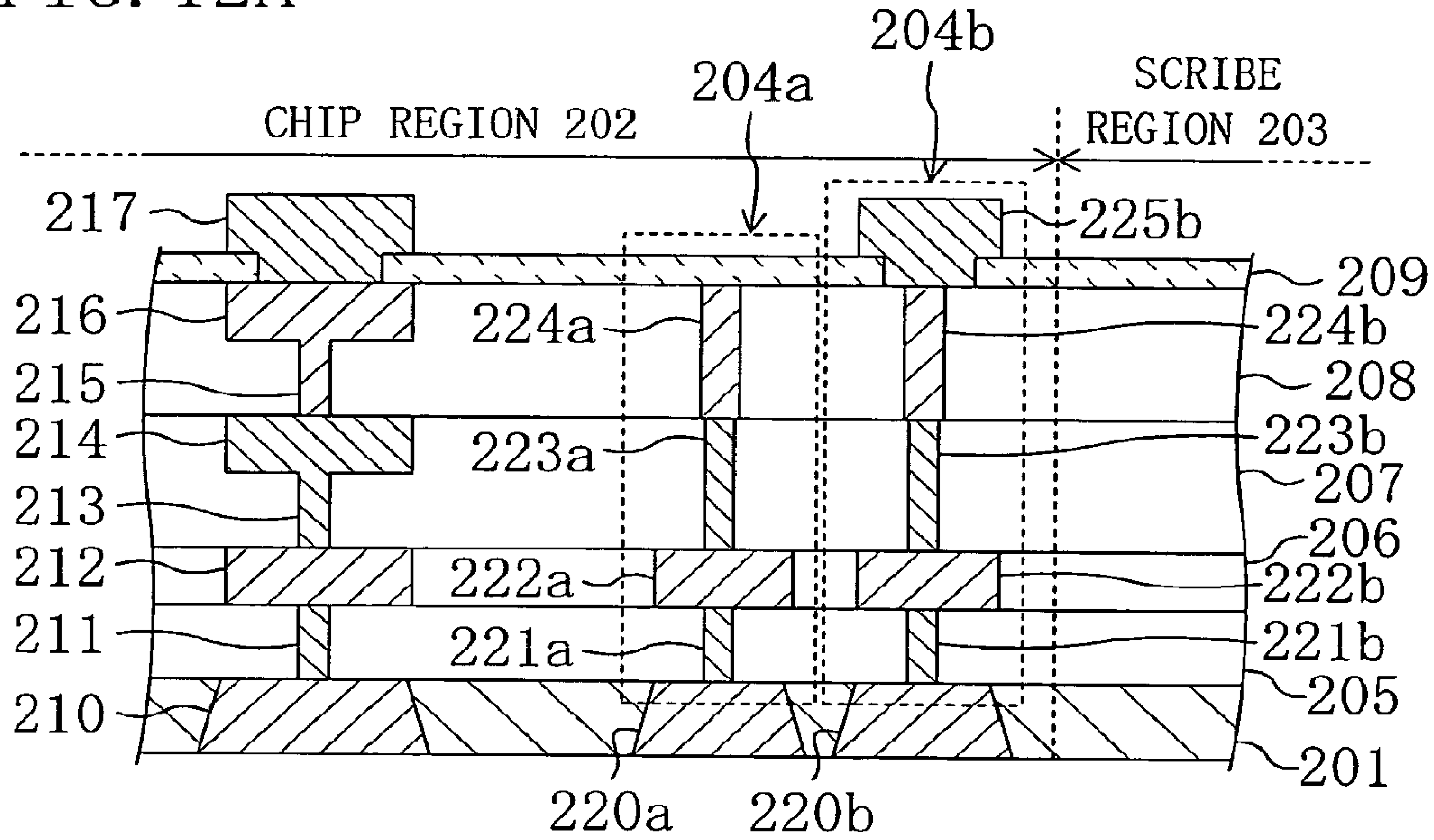


FIG. 12B

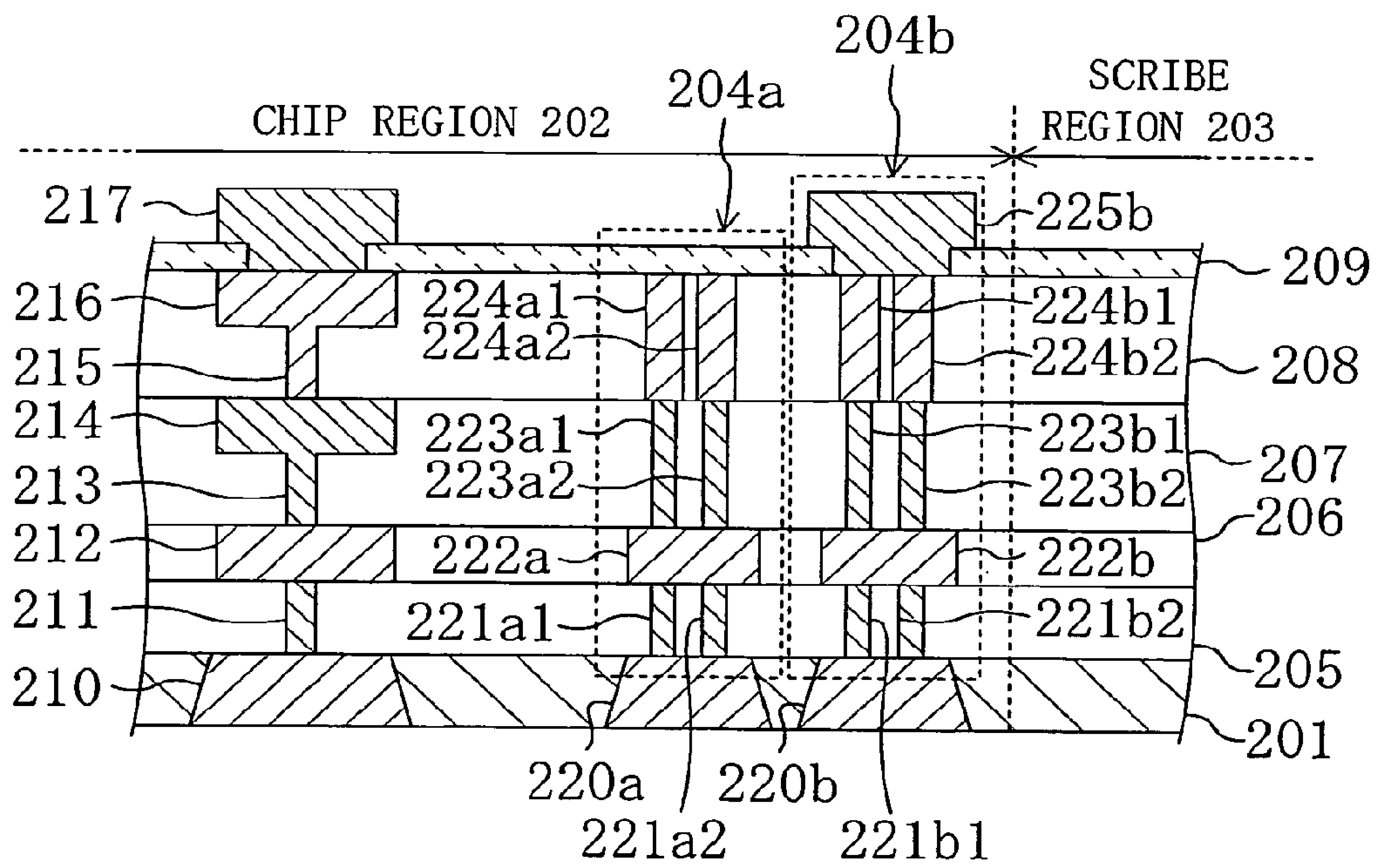


FIG. 13

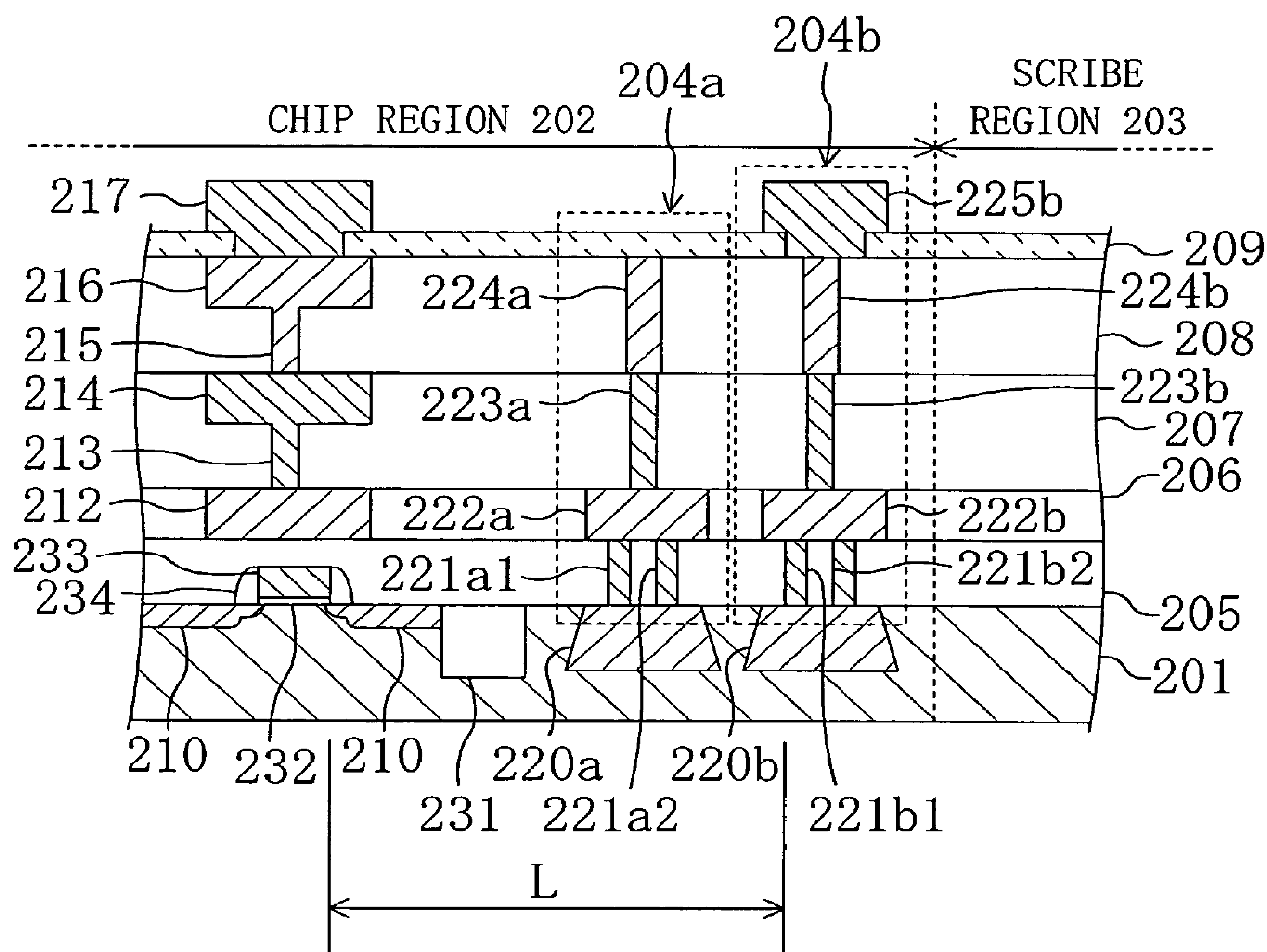


FIG. 14A
PRIOR ART

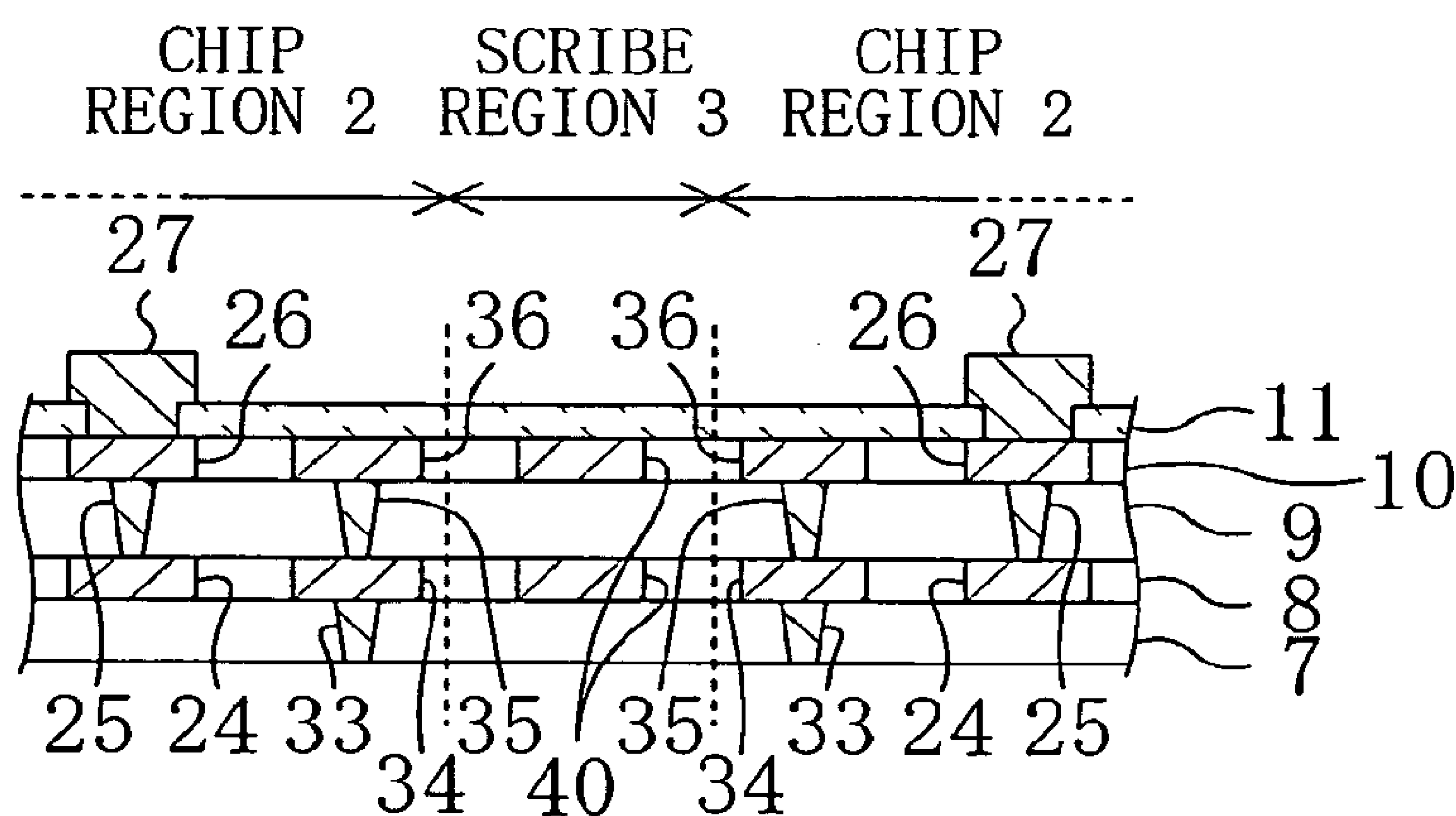


FIG. 14B
PRIOR ART

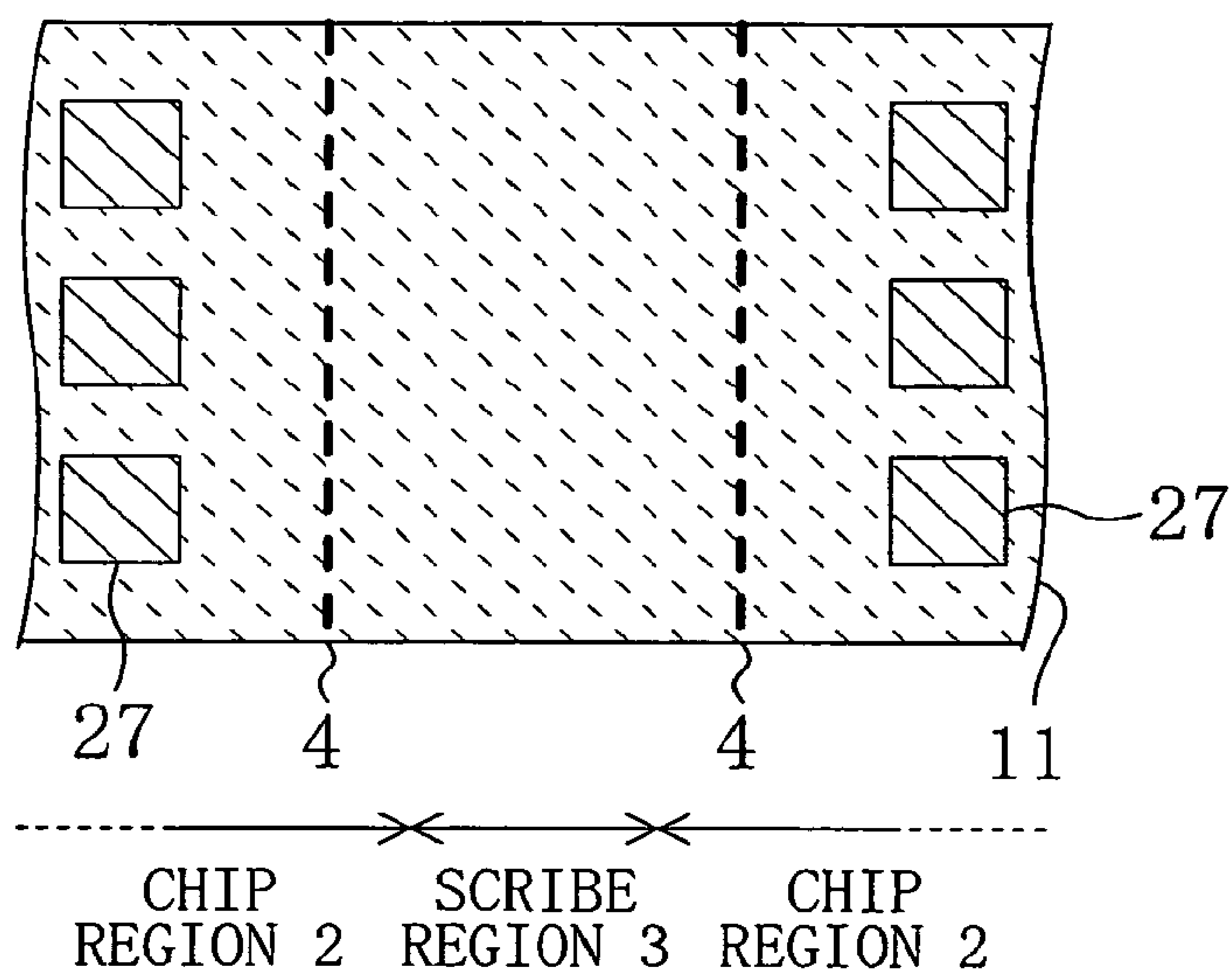


FIG. 15A

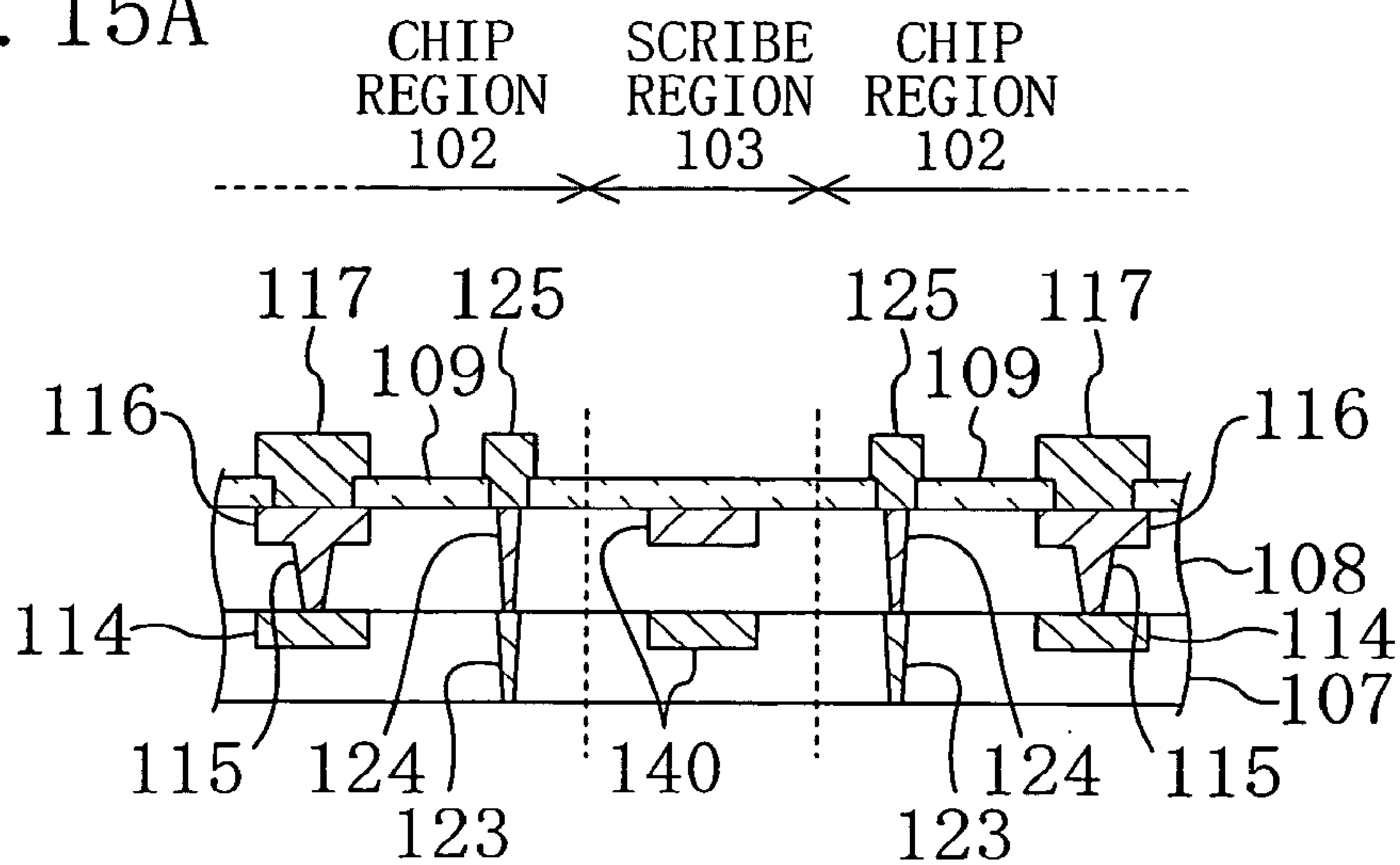


FIG. 15B

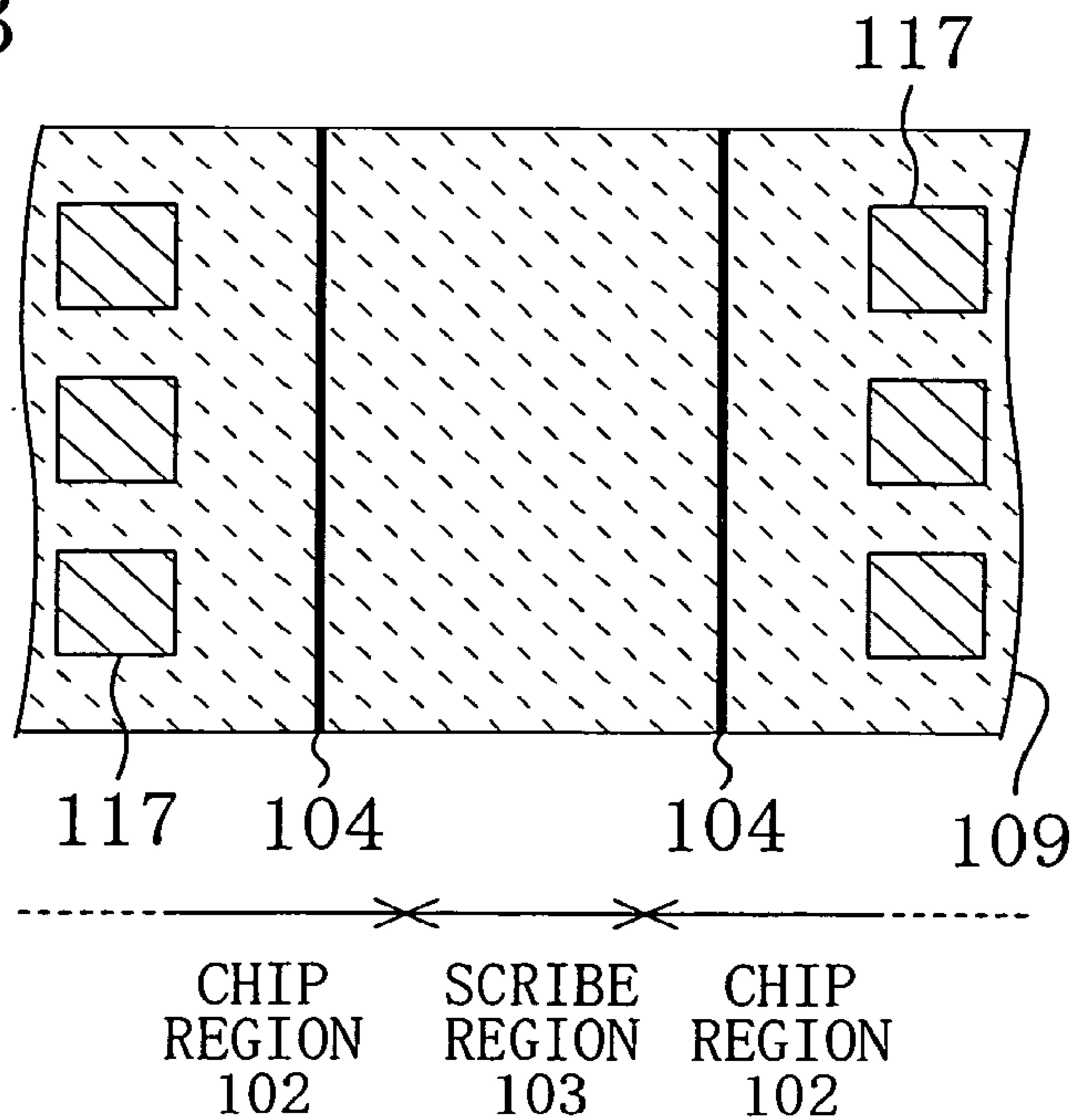


FIG. 16A

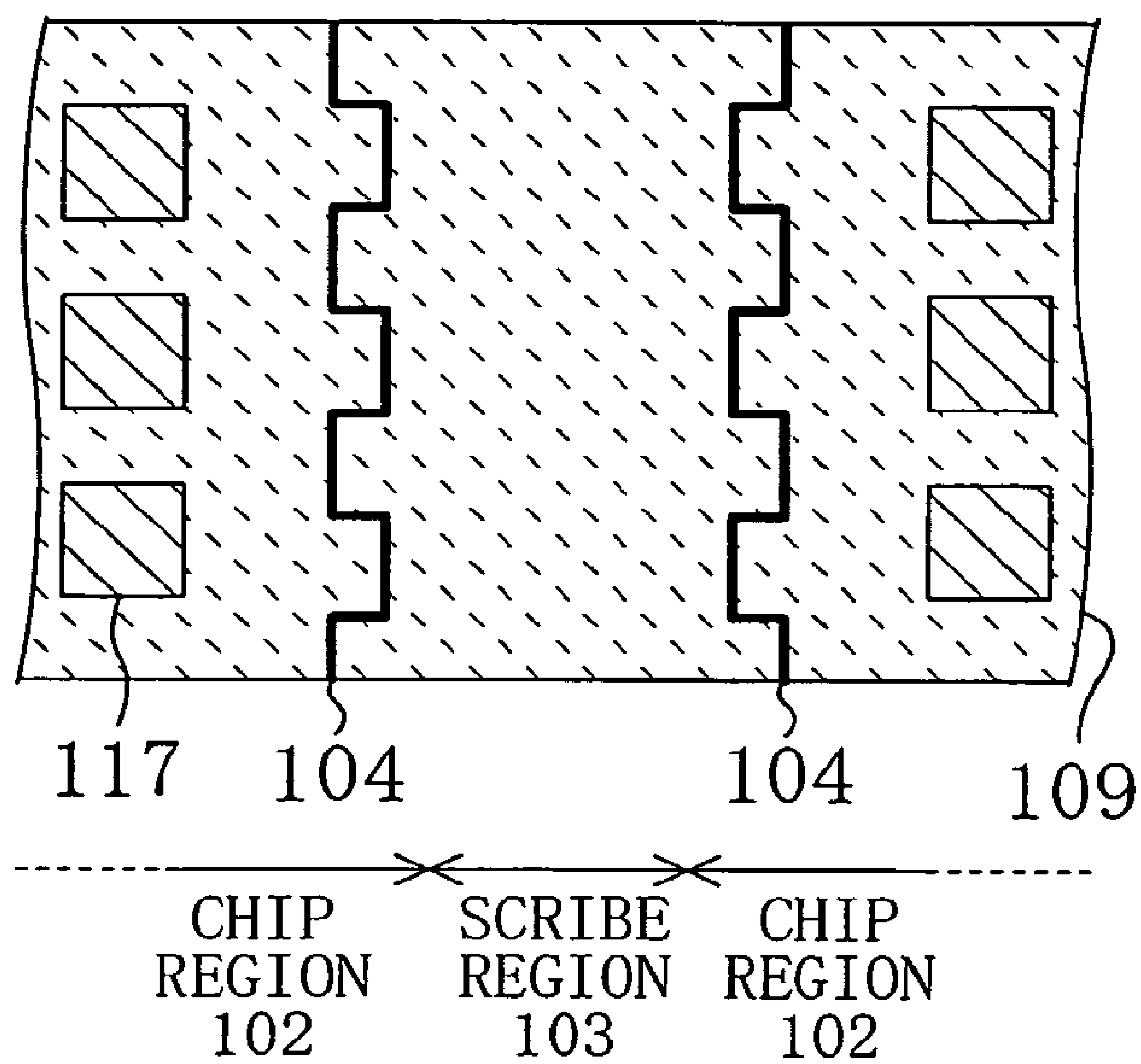


FIG. 16B

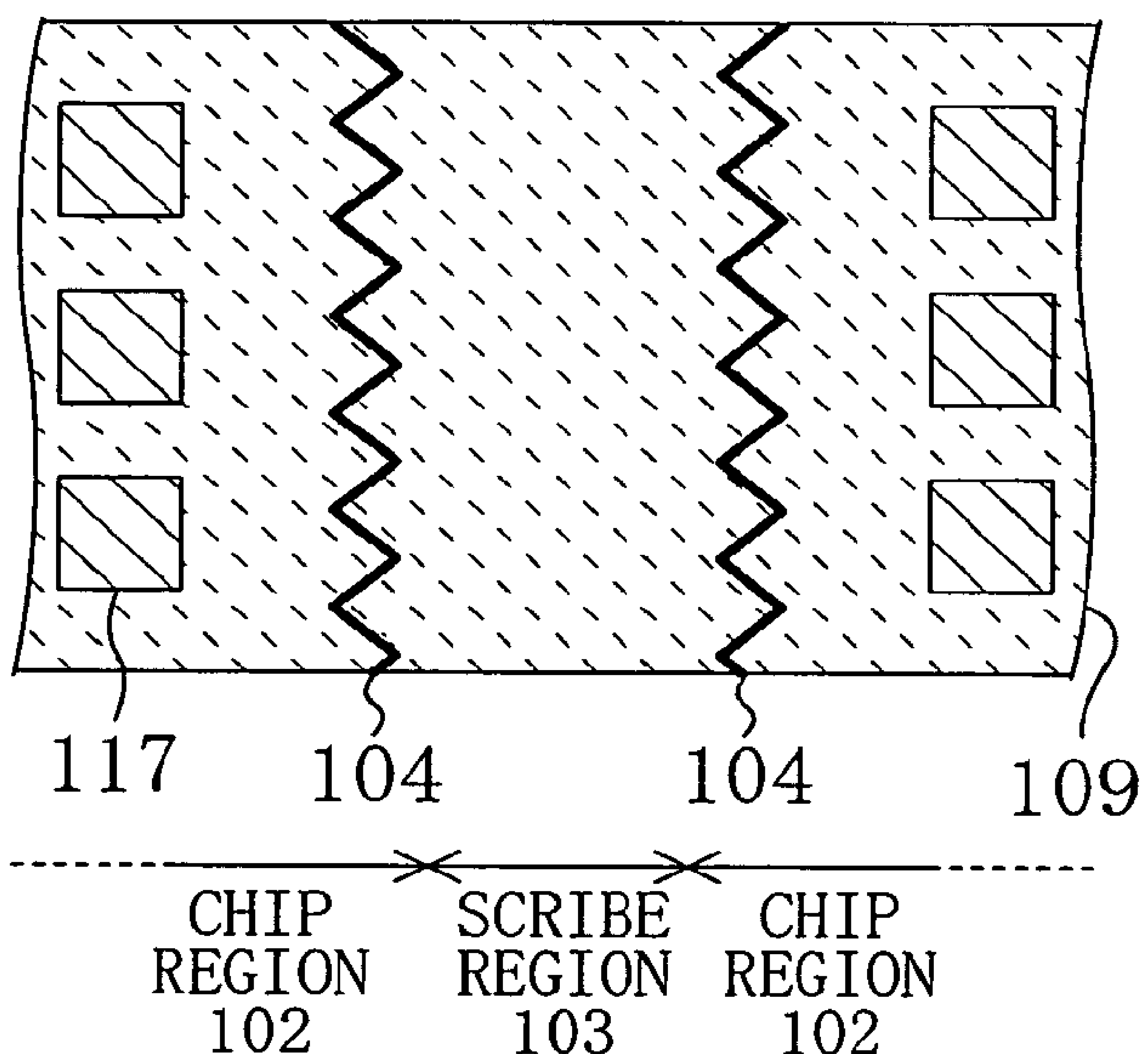


FIG. 16C

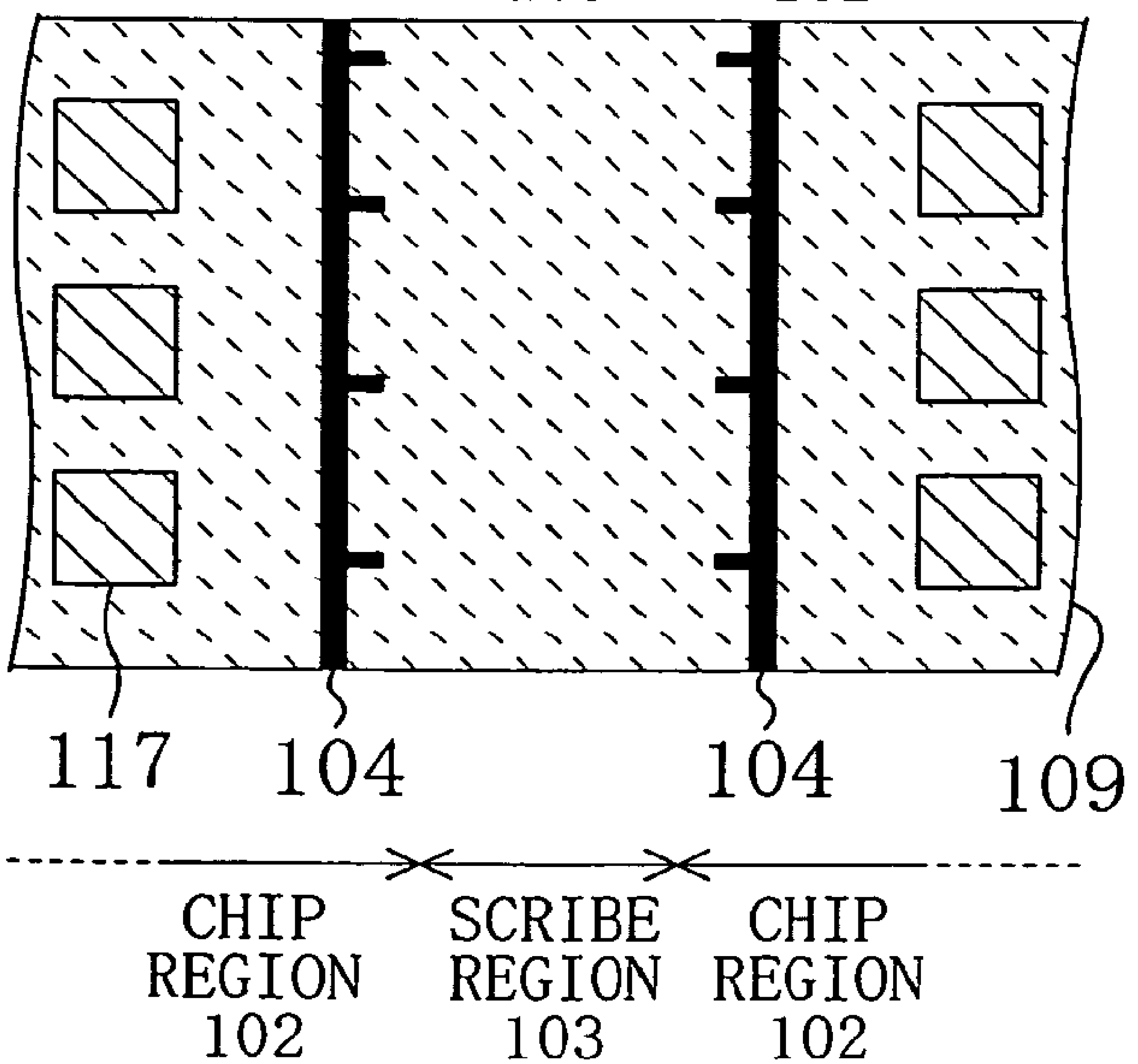


FIG. 17A

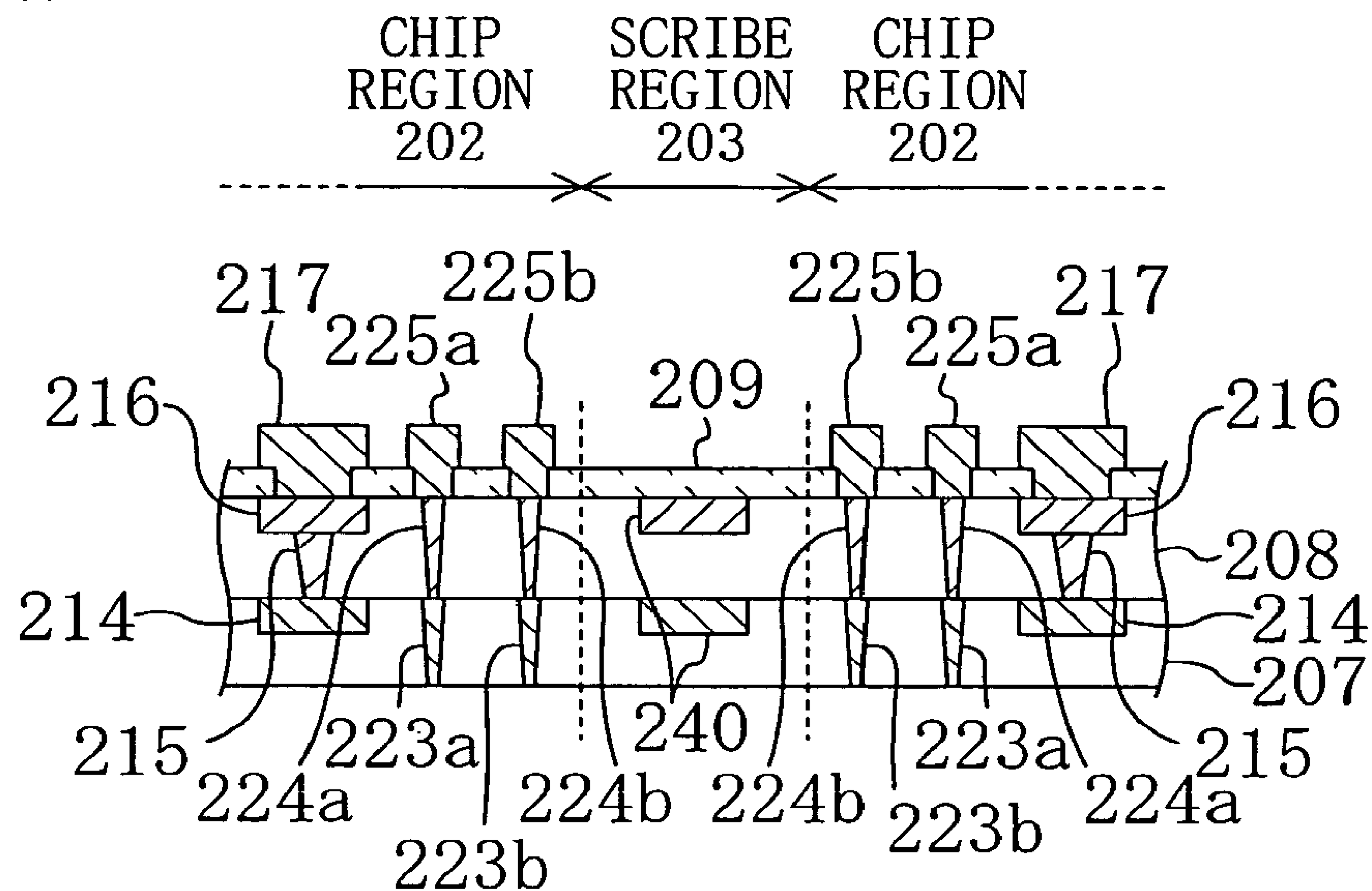


FIG. 17B

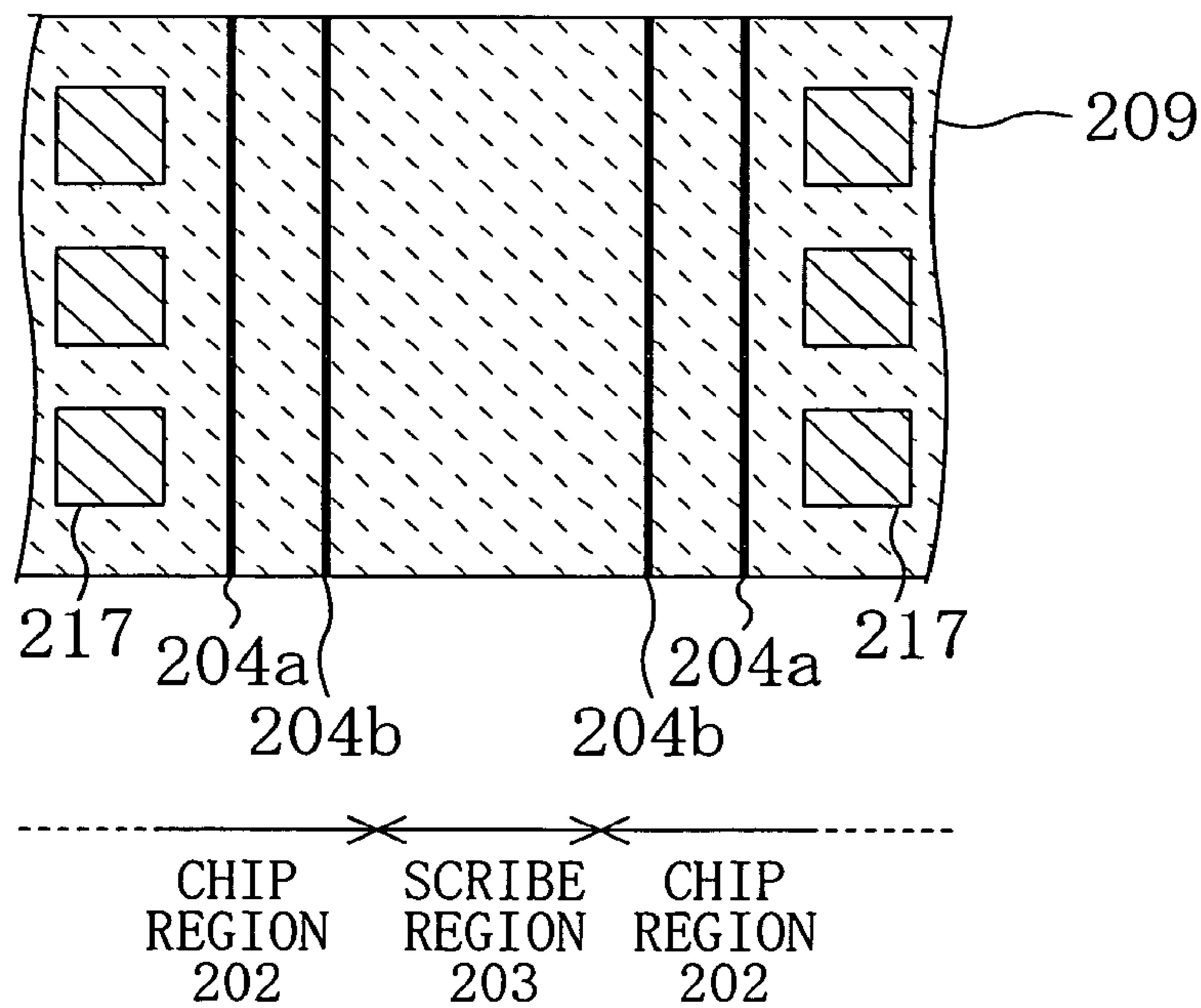


FIG. 18A

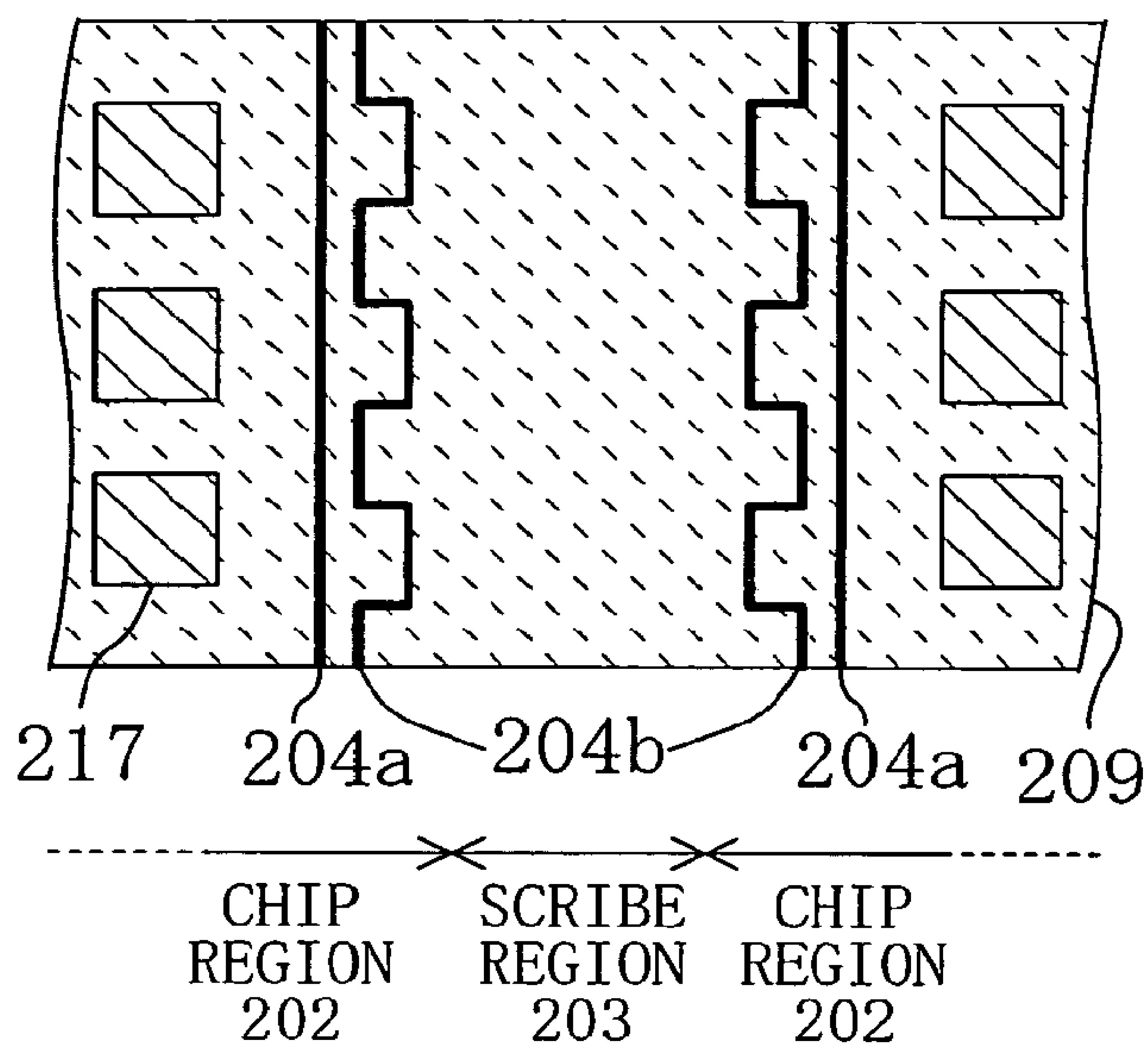


FIG. 18B

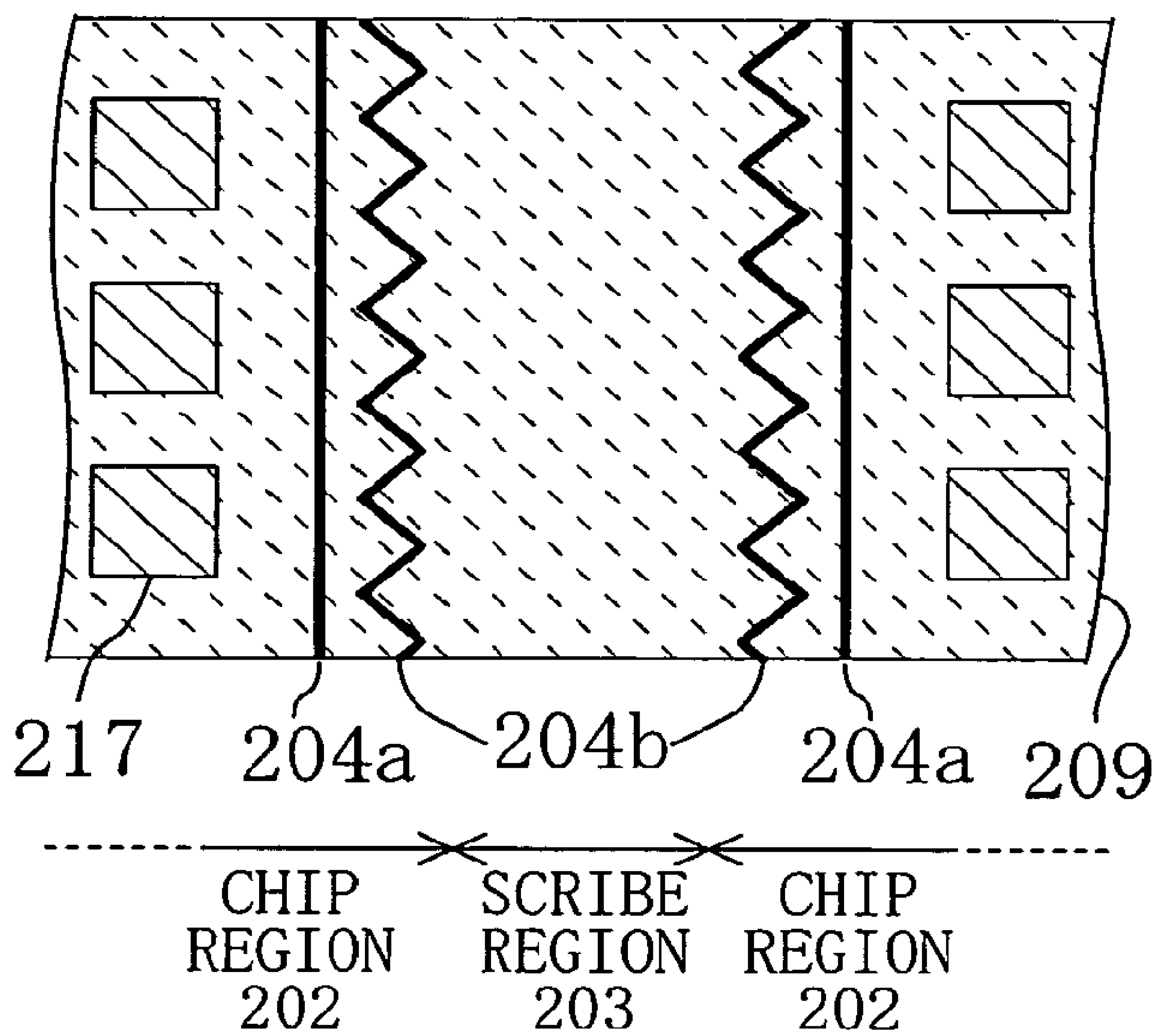


FIG. 18C

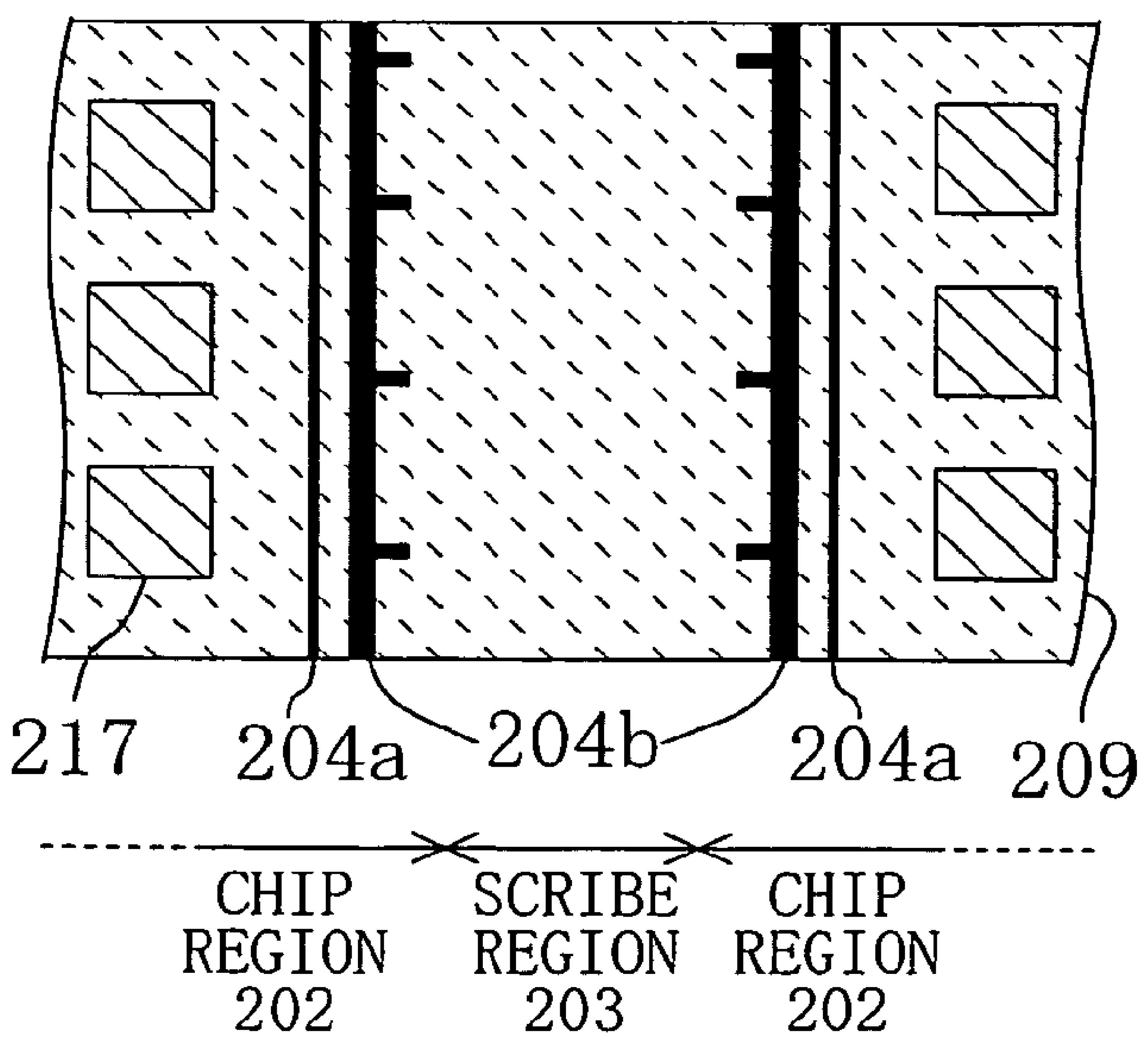
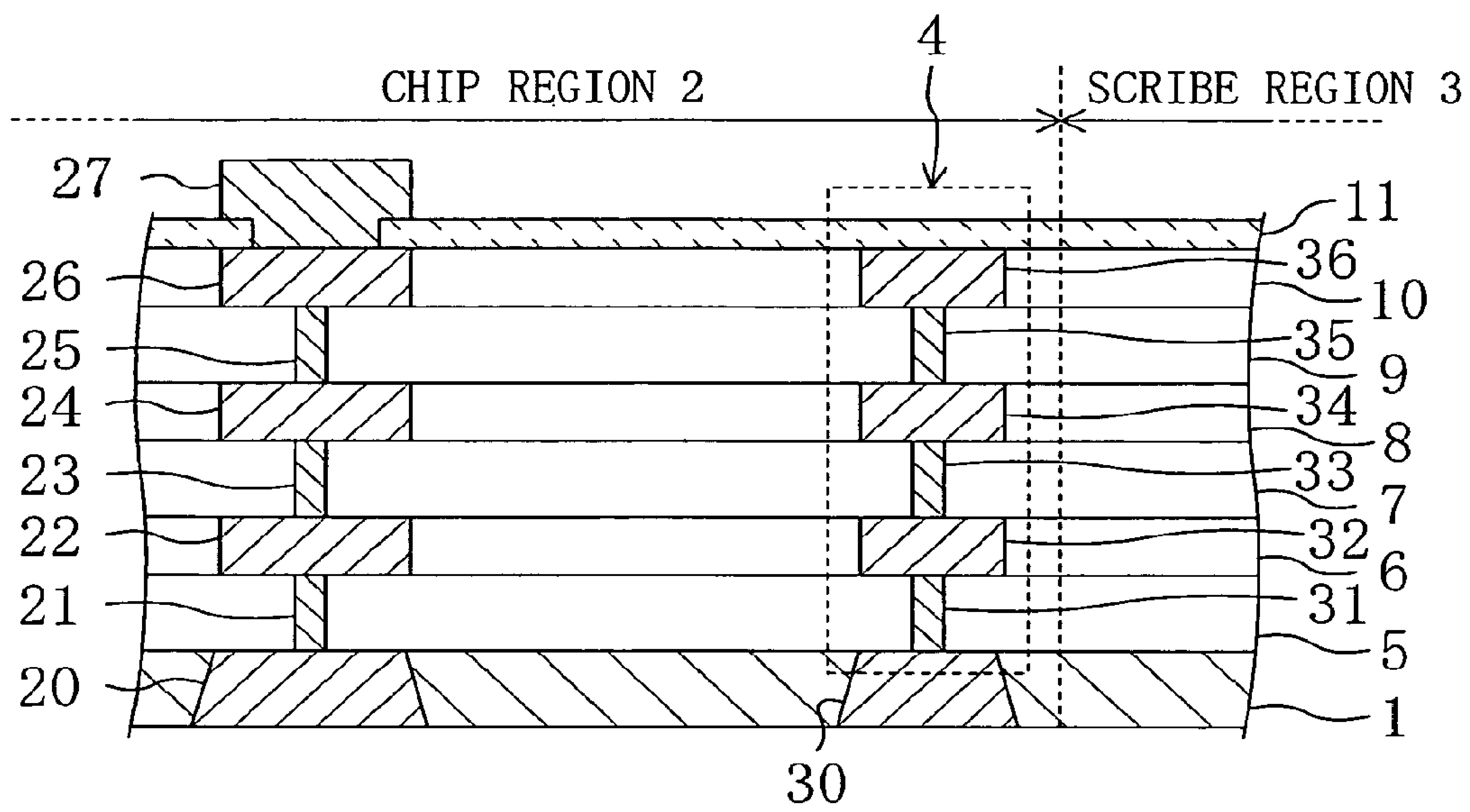


FIG. 19
PRIOR ART



SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a Continuation of U.S. patent application Ser. No. 14/663,436, filed on Mar. 19, 2015, which is a Divisional of U.S. patent application Ser. No. 14/231,150, filed on Mar. 31, 2014, now U.S. Pat. No. 9,082,779, which is a Continuation of U.S. patent application Ser. No. 13/941,156, filed on Jul. 12, 2013, now U.S. Pat. No. 8,710,595, which is a Continuation of U.S. patent application Ser. No. 13/551,425, filed on Jul. 17, 2012, now U.S. Pat. No. 8,618,618, which is a Divisional of U.S. patent application Ser. No. 13/171,181, filed on Jun. 28, 2011, now U.S. Pat. No. 8,247,876, which is a Divisional of U.S. patent application Ser. No. 12/858,942, filed on Aug. 18, 2010, now U.S. Pat. No. 7,994,589, which is a Divisional of U.S. patent application Ser. No. 12/264,675, filed on Nov. 4, 2008, now U.S. Pat. No. 7,948,039, which is a Divisional of U.S. patent application Ser. No. 10/983,760, filed on Nov. 9, 2004, now U.S. Pat. No. 7,453,128, claiming priority of Japanese Patent Application No. 2003-379754 filed on Nov. 10, 2003, whose priority is claimed under 35 USC §119, the disclosures of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device having a seal ring structure surrounding a chip region and to a method for fabricating the device.

A semiconductor device is generally fabricated by arranging a large number of integrated circuits (ICs) constituted by a plurality of elements and provided with given functions on a semiconductor wafer of, for example, silicon.

A large number of chip regions arranged on a wafer are separated from each other by a scribe region (scribe line) having a lattice pattern. After the large number of chip regions have been formed on a wafer through a semiconductor fabrication process, the wafer is diced into chips along the scribe region, thereby forming semiconductor devices.

However, when the wafer is diced into chips, chip regions near the scribe line might suffer mechanical damage, resulting in occurrence of cracks or chipping in part of the diced cross sections of the separated chips, i.e., semiconductor devices.

To solve this problem, in Japanese Unexamined Patent Publication (Kokai) No. 2001-23937 (hereinafter, referred to as reference **1**), proposed is a technique for preventing crack propagation in chip regions during dicing by providing a seal ring serving as a ring-shaped protection wall around the chip regions.

FIG. **19** is a cross-sectional view showing a conventional semiconductor device (formed in a wafer) having a seal ring.

As shown in FIG. **19**, a chip region **2** is defined in a of a wafer by a scribe region **3**. A multilayer structure made of a plurality of interlayer dielectric films **5** through **10** is formed on the substrate **1**. An active layer **20** constituting an element is formed in the substrate **1** in the chip region **2**. A plug (via) **21** is formed through the interlayer dielectric film **5** to be connected to the active layer **20**. An interconnect **22** is formed through the interlayer dielectric film **6** to be connected to the plug **21**. A plug **23** is formed through the interlayer dielectric film **7** to be connected to the interconnect **22**. An interconnect **24** is formed through the interlayer dielectric film **8** to be connected to the plug **23**. A plug **25** is formed through the interlayer dielectric film **9** to be connected to the interconnect **24**. An interconnect **26** is formed through the interlayer dielectric film **10** to be connected to the plug **25**.

As shown in FIG. **19**, in part of the multilayer structure of the interlayer dielectric films **5** through **10** located in a peripheral part of the chip region **2**, a seal ring **4** is formed through the multilayer structure to completely surround the chip region **2**. As shown in reference **1**, for example, the seal ring **4** is formed by alternately using masks for forming interconnects and masks for forming vias. Specifically, the seal ring **4** includes: a conductive layer **30** formed in the substrate **1**; a seal via **31** formed through the interlayer dielectric film **5** to be connected to the conductive layer **30**; a seal interconnect **32** formed through the interlayer dielectric film **6** to be connected to the seal via **31**; a seal via **33** formed through the interlayer dielectric film **7** to be connected to the seal interconnect **32**; a seal interconnect **34** formed through the interlayer dielectric film **8** to be connected to the seal via **33**; a seal via **35** formed through the interlayer dielectric film **9** to be connected to the seal interconnect **34**; and a seal interconnect **36** formed through the interlayer dielectric film **10** to be connected to the seal via **35**. Parts of the seal ring formed by using masks for forming interconnects will be hereinafter referred to as seal interconnects, and parts of the seal ring formed by using masks for forming vias will be hereinafter referred to as seal vias.

As shown in FIG. **19**, a passivation film **11** is formed on the multilayer structure of the interlayer dielectric films **5** through **10** in which interconnects (**22**, **24**, **26**), vias (**21**, **23**, **25**) and the seal ring **4** are provided. The passivation film **11** has an opening on the interconnect **26**, and a pad **27** connected to the interconnect **26** is formed in the opening.

SUMMARY OF THE INVENTION

However, the conventional semiconductor device has the problem that the passivation film peels off by impact caused during dicing of a wafer or the problem that the impact propagates through the passivation film to reach the inside of the chip region.

If the passivation film has an opening on the seal ring and the upper part of the seal ring is exposed in the opening as in the semiconductor device disclosed in reference **1**, it is impossible to sufficiently prevent moisture or the like from entering a region surrounded by the seal ring from the outside.

To prevent increase in capacitance between interconnects involved in miniaturization of semiconductor elements and of interconnects connected thereto, i.e., to prevent decrease in processing speed of semiconductor devices, a technique for preventing the increase in capacitance between interconnects by using interlayer dielectric films with low dielectric constants (low-κ interlayer dielectric films) has been developed.

However, the low-κ interlayer dielectric films generally have low mechanical strength, so that the low-κ interlayer dielectric films exhibit insufficient durability against stress occurring during dicing, as compared to interlayer dielectric films made of conventional materials. Therefore, the low-κ interlayer dielectric films are susceptible to damage during dicing. Accordingly, even if a seal ring is formed by alternately using masks for vias and masks for interconnects in a peripheral part of a chip region in a semiconductor device using such low-κ interlayer dielectric films as in the conventional device, damage during dicing is not sufficiently

prevented. Specifically, the conventional seal ring formed by alternately using masks for vias and masks for interconnects includes a large number of components, so that the seal ring has a large number of junctions between components (e.g., a junction between a seal via and a seal interconnect). As the number of junctions between components increases, the number of portions where components are not connected is likely to increase. As a result, such junctions (or portions where components are not connected) act as paths through which impact propagates, so that it is impossible to prevent cracks or the like occurring during dicing from propagating into chip regions.

It is therefore an object of the present invention to prevent degradation of moisture resistance and reliability of a semiconductor device by preventing propagation of chipping, cracks and the like caused during dicing, which is performed to divide a wafer into chips, from a side of a chip (semiconductor device) into a chip region.

In order to obtain the object, a semiconductor device according to the present invention includes: an element formed on a substrate in a chip region; a multilayer structure including a plurality of interlayer dielectric films formed on the substrate; an interconnect formed in at least one of the interlayer dielectric films in the chip region; a plug formed in at least one of the interlayer dielectric films in the chip region and connecting either the element and the interconnect or the interconnect and another interconnect; a seal ring structure formed through the multilayer structure in a peripheral part of the chip region and surrounding the chip region (without interruption); and a protection film formed on the multilayer structure in which the interconnect, the plug and the seal ring structure are provided. In this device, a dual damascene interconnect in which the interconnect and the plug connected to the interconnect are integrated is formed in at least one of the interlayer dielectric films in the chip region, part of the seal ring structure located in the interlayer dielectric film in which the dual damascene interconnect is formed is continuous, and the protection film has an opening on the seal ring structure, and a cap layer connected to the seal ring structure is formed in the opening.

In the semiconductor device of the present invention, the protection film such as a passivation film has an opening on the seal ring structure. In other words, the protection film is partially discontinuous in a peripheral part of the chip region. Accordingly, it is possible to prevent peeling of the protection film in the chip region caused by impact on a wafer during dicing. It is also possible to prevent impact on the protection film outside the chip region from propagating through the protection film and reaching the inside of the chip region.

In addition, at least part of the seal ring structure is continuous in the interlayer dielectric film in which the dual damascene structure is provided. In other words, this part of the seal ring structure has no "junction." Accordingly, the number of "junctions" between components in the entire seal ring structure is reduced. As a result, it is possible to prevent cracks or the like occurring during dicing from propagating into the chip region through "junctions." It is also possible to prevent an impurity or the like from entering the chip region from the outside of the seal ring structure.

Moreover, the cap layer (e.g., a cap layer made of a conductor) is buried in the opening of the protection film formed on the seal ring structure such that this cap layer and the body of the seal ring structure are continuous. Accordingly, unlike a case where no cap layer is provided, it is possible to prevent moisture or an impurity which has entered from the scribe region during dicing from entering the chip region via the peripheral part of the chip region, i.e., the opening of the protection film near the scribe region.

In the device of the present invention, at least part of the seal ring structure is preferably buried in a concave portion formed in one of the interlayer dielectric films or in at least two successive interlayer dielectric films out of the plurality of interlayer dielectric films, and the concave portion preferably has an aspect ratio of three or more.

This ensures reduction of the number of "junctions" between components in the entire seal ring structure.

In the device of the present invention, the seal ring structure is preferably divided into at least two branches in at least one of the interlayer dielectric films.

Then, a structure in which components of the seal ring structure are connected to each other via two or more branches (which are also components of the seal ring structure) is implemented. Specifically, the chip region is surrounded by this partial structure including two (or three or more) seal ring branches in a film. In this film, the seal ring structure is composed of a plurality of branches, so that the seal ring structure has high mechanical strength. Accordingly, even if an interlayer dielectric film in the scribe region is damaged by stress occurring during dicing, the seal ring structure serves as a protection wall and prevents propagation of the damage to the interlayer dielectric film in the scribe region toward the chip region or prevents propagation of impact during dicing through the interlayer dielectric film in the chip region.

In the device of the present invention, the seal ring structure preferably includes at least two seal rings surrounding the chip region.

Then, a first seal ring (inner seal ring) which surrounds the chip region and at least one seal ring (outer seal ring) which surrounds the first seal ring and is electrically insulated from the first seal ring are formed between the chip region and the scribe region surrounding the chip region. With this structure, even if a seal ring located outside the first seal ring is damaged, e.g., suffered from breaking or cracks, by the stress from a dicing blade during dicing, the first seal ring prevents impact from propagating into the chip region. Even if the seal ring outside the first seal ring is damaged, the first seal ring prevents moisture or a contaminant from entering the chip region because the first seal ring is formed independently of this outer seal ring.

If the chip region is surrounded by at least two seal rings, the opening of the protection film may be located only on an outermost seal ring out of the seal rings, and the cap layer may be formed in the opening to be connected to the outermost seal ring. Alternatively, each of the seal rings may be divided into at least two branches in at least one of the interlayer dielectric films.

In the device of the present invention, a plurality of projections are preferably provided on a side of the seal ring structure.

Then, it is possible to prevent impact and stress caused by contact of a dicing blade with a film such as a protection film during dicing of a wafer and cracks and the like occurring in the wafer resulting from the impact and stress, from propagating along the side (the side facing the scribe region) of the seal ring structure.

In the device of the present invention, the seal ring structure preferably has a waved-shaped periphery when viewed from above the substrate.

Then, it is possible to prevent impact and stress caused by contact of a dicing blade with a film such as a protection film during dicing of a wafer and cracks and the like occurring in

the wafer resulting from the impact and stress, from propagating along the side of the seal ring structure.

In the device of the present invention, the seal ring structure may include at least one material selected from the group consisting of W, Al and Cu.

In the semiconductor device of the present invention, if the cap layer includes Al, prevention of erosion of the seal ring structure (especially a seal ring structure made of Cu) is ensured.

A method for fabricating a semiconductor device according to the present invention is a method for fabricating a semiconductor device including: an element formed on a substrate in a chip region; a multilayer structure including a plurality of interlayer dielectric films formed on the substrate; an interconnect formed in at least one of the interlayer dielectric films in the chip region; a plug formed in at least one of the interlayer dielectric films in the chip region and connecting either the element and the interconnect or the interconnect and another interconnect; and a seal ring structure formed through the multilayer structure in a peripheral part of the chip region and surrounding the chip region. Specifically, the method includes the steps of: forming, through one of the interlayer dielectric films, a first concave portion in which the plug is to be buried and a second concave portion in which part of the seal ring structure is to be buried; forming a third concave portion in which the interconnect is to be buried in an upper part of said one of the interlayer dielectric films such that the third concave portion is connected to the first concave portion; burying a conductive film in the first, second and third concave portions, thereby forming a dual damascene interconnect in which the plug and the interconnect are integrated and said part of the seal ring structure; forming a protection film on the multilayer structure in which the interconnect, the plug and the seal ring structure are provided; and forming an opening in part of the protection film on the seal ring structure and forming a cap layer in the opening such that the cap layer is connected to the seal ring structure.

That is, the method for fabricating a semiconductor device according to the present invention is a method for fabricating the above-described semiconductor device. Therefore, the same advantages are obtained.

In the method of the present invention, if the aspect ratio of the second concave portion is three or more, reduction of the number of "junctions" between components in the entire seal ring structure is ensured.

The method of the present invention may further include the step of forming a fourth concave portion in which another part of the seal ring structure is to be buried in another interlayer dielectric film stacked on said one of the interlayer dielectric films such that the fourth concave portion is connected to the second concave portion.

As described above, according to the present invention, in a semiconductor device including a chip region and a seal ring structure provided in a peripheral part of the chip region and surrounding an element, interconnect layers and others in the chip region, a seal ring structure including a small number of "junctions" between its components is provided, a protection film has an opening on the seal ring structure, and a cap layer is formed in the opening. This seal ring structure may partially include branches (e.g., at least two conductors serving as bridges in part of the seal ring structure) or may include two or more seal rings surrounding the chip region (e.g., a first seal ring formed in a peripheral part of the chip region and at least one seal ring surrounding the first seal ring.)

With the foregoing features of the present invention, it is possible to prevent chipping, breaking and the like caused by dicing a wafer into chips (semiconductor devices) from reaching chip regions. Accordingly, it is also possible to prevent degradation of the moisture resistance and reliability of the semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view showing part of a wafer on which a semiconductor device according to a first embodiment of the present invention is provided.

FIGS. **2**A and **2**B are views respectively showing variations of the cross-sectional structure taken along the line A-A' in FIG. **1** (i.e., cross-sectional structure of an end of a semiconductor device including a seal ring portion located in a peripheral part of a chip region.)

FIG. **3**A is a view showing a variation of the cross-sectional structure taken along the line A-A' in FIG. **1** (i.e., a cross-sectional structure of an end of a semiconductor device including a seal ring portion located in a peripheral part of a chip region.) FIG. **3**B schematically shows planar structures of a via and a seal via provided in a film where the via is formed in the structure shown in FIG. **2**A or **2**B.

FIGS. **4**A through **4**D are cross-sectional views showing respective process steps of a method for fabricating a semiconductor device according to the first embodiment.

FIGS. **5**A through **5**C are cross-sectional views showing respective process steps of the method for fabricating the semiconductor device of the first embodiment.

FIGS. **6**A through **6**C are cross-sectional views showing respective process steps of the method for fabricating the semiconductor device of the first embodiment.

FIG. **7** is a plan view showing part of a wafer on which a semiconductor device according to a second embodiment of the present invention is provided.

FIGS. **8**A and **8**B are views respectively showing variations of the cross-sectional structure taken along the line B-B' in FIG. **7** (i.e., cross-sectional structure of an end of a semiconductor device including a seal ring portion located in a peripheral part of a chip region.)

FIGS. **9**A through **9**D are cross-sectional views showing respective process steps of a method for fabricating a semiconductor device according to the second embodiment.

FIGS. **10**A through **10**C are cross-sectional views showing respective process steps of the method for fabricating the semiconductor device of the second embodiment.

FIG. **11**A is a plan view of the semiconductor device of the second embodiment when viewed from above. FIG. **11**B is a cross-sectional view of a chip surface taken along the line C-C' in FIG. **11**A.

FIG. **12**A is a cross-sectional view showing a semiconductor device according to a first modified example of the second embodiment. FIG. **12**B is a cross-sectional view showing a semiconductor device according to a second modified example of the second embodiment.

FIG. **13** is a cross-sectional view showing a semiconductor device according to a third modified example of the second embodiment.

FIG. **14**A is a view schematically showing a cross-sectional structure of a conventional semiconductor device shown in FIG. **19**. FIG. **14**B is a plan view corresponding to the structure shown in FIG. **14**A.

FIG. **15**A is a view schematically showing a cross-sectional structure of the semiconductor device of the first embodiment shown in FIG. **2**A. FIG. **15**B is a plan view corresponding to the structure shown in FIG. **15**A.

FIGS. **16**A through **16**C are plan views respectively showing variations of a semiconductor device according to a third embodiment of the present invention.

FIG. **17**A is a view schematically showing a cross-sectional structure of the semiconductor device of the second embodiment shown in FIG. **8**A. FIG. **17**B is a plan view corresponding to the structure shown in FIG. **17**A.

FIGS. **18**A through **18**C are plan views respectively showing variations of the semiconductor device of the third embodiment.

FIG. **19** is a cross-sectional view showing the conventional semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be described with reference to the drawings.

A first feature of the present invention is that a seal ring and an interconnect structure are formed by the same process and a dual damascene process is adopted to form the seal ring. Accordingly, the resultant seal ring includes a small number of "junctions" between its components, as compared to the case of adopting a single damascene process. In this description, a structure in which an interconnect and a plug (for connecting interconnects or an interconnect and an element) are stacked is referred to as an interconnect structure.

A second feature of the present invention is that an opening is formed in part of a passivation film (e.g., a SiN film) covering the top of the seal ring and a cap is provided in the opening. This prevents impact on the passivation film during dicing from propagating into a chip region (see first embodiment.)

A third feature of the present invention is that the seal ring is partially divided into two or more branches and these branches serve as an integrated unit. This enhances the mechanical strength of the seal ring itself, thereby preventing impact from a scribe line during dicing from propagating into a chip region.

A fourth feature of the present invention is that at least two seal rings surround a chip region. Accordingly, the seal ring structure is stronger than a seal ring structure in which a single seal ring surrounds the chip region (see second embodiment.)

The other embodiments of the present invention will be specifically described in the following description.

Embodiment 1

Hereinafter, a semiconductor device and a method for fabricating the device according to a first embodiment of the present invention will be described with reference to drawings.

FIG. **1** is a plan view showing part of a wafer on which the semiconductor device of the first embodiment (i.e., a semiconductor device in which one seal ring surrounds a chip region) is provided.

As shown in FIG. **1**, on a wafer **101** to be a semiconductor substrate, which is typically a silicon substrate, for example, a plurality of chip regions **102** to be semiconductor devices are provided. In each of the chip regions **102**, an integrated circuit (IC) made of a plurality of elements and provided with a given function is formed. The chip regions **102** are defined by a scribe region **103** having a lattice pattern.

A semiconductor device (i.e., a semiconductor chip) includes: a chip region **102** on which an IC made of a plurality of elements and provided with a given function is formed; and a seal ring **104** provided in a peripheral part of the chip region **102** to surround the chip region **102**. The wafer **101** on which a plurality of such semiconductor devices are formed is diced along the scribe region **103**, thereby separating the semiconductor devices.

FIGS. **2**A, **2**B and **3**A show variations of the cross-sectional structure taken along the line A-A' in FIG. **1** (i.e., a cross-sectional structure of an end of a semiconductor device including a seal ring portion located in a peripheral part of the chip region **102**.) FIG. **3**B schematically shows planar structures of a via and a seal via which are provided in the same film in the structure shown in FIG. **2**A or **2**B.

FIGS. **2**A, **2**B and **3**A show cross-sectional structures of interconnect structures and seal rings in the chip region **102**.

As shown in FIGS. **1**, **2**A, **2**B and **3**A, a semiconductor device before dicing includes the chip regions **102** and the scribe region **103**, and the seal ring **104** is formed in each of the chip regions **102** near the boundary between the chip region **102** and the scribe region **103**.

Now, features of the respective structures shown in FIGS. **2**A, **2**B and **3**A will be described specifically.

First, the structure shown in FIG. **2**A has a feature in which seal vias constituting the seal ring **104** are continuously formed through at least two films.

Next, the structure shown in FIG. **2**B has a feature in which seal vias and seal interconnects constituting the seal ring **104** are alternately provided.

Then, the structure shown in FIG. **3**A has a feature in which a seal via constituting the seal ring **104** is divided into at least two branches in the same interlayer dielectric film.

On the other hand, the structures shown in FIGS. **2**A, **2**B and **3**A have a common feature in which a seal ring cap (a cap layer **125**) is provided at the top of the seal ring **104**.

Hereinafter, a method for fabricating a semiconductor device having the structure shown in FIG. **2**A will be described with reference to FIGS. **4**A through **4**D, **5**A through **5**C and **6**A through **6**C.

First, as shown in FIG. **4**A, an active layer **110** constituting an element such as a transistor is formed in a wafer **101** (hereinafter, referred to as a substrate **101**) in a chip region **102**. At the same time, a conductive layer **120** configured in the same manner as the active layer **110** is formed in the substrate **101** in a peripheral part of the chip region **102** (i.e., in a region to be a seal ring, which will be hereinafter referred to as a seal ring region, near a scribe region **103**.)

Then, a first interlayer dielectric film **105** is deposited on the substrate **101**. Thereafter, through a lithography process and a dry etching process, a via hole **105***a* for forming a first via **111** (see FIG. **4**B) is formed through the first interlayer dielectric film **105** in the chip region **102** and, at the same time, a trench concave portion **105***b* for forming a first seal via **121** (see FIG. **4**B) is formed through the first interlayer dielectric film **105** in the seal ring region. The seal via is a component constituting a seal ring and is formed by filling the trench concave portion with a conductive material. That is, a seal via has a line structure having substantially the same width as that of a via in the chip region (see FIG. **3**B.)

In this embodiment, the aspect ratio of the seal via (i.e., the ratio of the depth to the width in the concave portion in which the seal via is buried) is preferably one or more.

In this embodiment, the via hole **105***a* and the trench concave portion **105***b* for forming the first seal via **121** are formed at the same time in the first interlayer dielectric film **105** in the chip region **102**. Alternatively, the via hole **105***a* and the trench concave portion **105***b* may of course be formed individually.

Next, as shown in FIG. **4**B, the via hole **105***a* and the trench concave portion **105***b* formed through the first interlayer dielectric film **105** are filled with a conductive film made of, for example, W (tungsten) by, for example, a chemical vapor deposition (CVD) process. Then, an unnecessary part of the conductive film extending off the via hole **105***a* and the trench concave portion **105***b* is removed by, for example, a chemical/mechanical polishing (CMP) process, thereby forming a first via **111** connected to the active layer **110** and a first seal via **121** connected to the conductive layer **120**.

Thereafter, a second interlayer dielectric film **106** is deposited on the first interlayer dielectric film **105**. Then, through a lithography process and a dry etching process, an interconnect trench **106***a* for forming a first interconnect **112** (see FIG. **4**C) is formed through the second interlayer dielectric film **106** in the chip region **102**, and at the same time, an interconnect trench **106***b* for forming a first seal interconnect **122** (see FIG. **4**C) is formed through the second interlayer dielectric film **106** in the seal ring region.

Then, as shown in FIG. **4**C, the interconnect trenches **106***a* and **106***b* formed through the second interlayer dielectric film **106** are filled with a conductive film of, for example, Cu (copper) by, for example, an electroplating process. Then, part of the conductive film extending off the interconnect trenches **106***a* and **106***b* is removed by, for example, a CMP process, thereby forming a first interconnect **112** connected to the first via **111** and a first seal interconnect **122** connected to the first seal via **121**.

Thereafter, as shown in FIG. **4**D, a third interlayer dielectric film **107** is deposited on the second interlayer dielectric film **106**, and then a via hole **107***a* for forming a second via **113** (see FIG. **5**C) is formed through the third interlayer dielectric film **107** in the chip region **102**. At the same time, a trench concave portion **107***b* for forming a second seal via **123** (see FIG. **5**C) is formed through the third interlayer dielectric film **107** in the seal ring region. In this embodiment, a premium is placed on efficiency, and the via hole **107***a* for forming the second via **113** to be a plug for connecting interconnects and the trench concave portion **107***b* for forming the second seal via **123** to be a part of the seal ring **104** are formed by the same process. Alternatively, the via hole **107***a* and the trench concave portion **107***b* may be formed by different processes.

Subsequently, as shown in FIG. **5**A, a resist film **130** for forming an interconnect trench in which a second interconnect **114** (see FIG. **5**C) is to be buried is formed on the third interlayer dielectric film **107** using a lithography process. This resist film **130** has an opening in a region where an interconnect is to be formed (hereinafter, referred to as an interconnect region) including the via hole **107***a*. The resist film **130** is also buried in the trench concave portion **107***b*.

Then, as shown in FIG. **5**B, through a dry etching process using the resist film **130** as a mask, an interconnect trench **107***c* for forming the second interconnect **114** is formed in an upper part of the third interlayer dielectric film **107** in the chip region **102** to be connected to the via hole **107***a*. Thereafter, the remaining resist film **130** is removed by ashing.

Subsequently, as shown in FIG. **5**C, a conductive film made of, for example, Cu is buried in the via hole **107***a*, the interconnect trench **107***c* and the trench concave portion **107***b* formed in the third interlayer dielectric film **107**. Then, part of the conductive film extending off the interconnect trench **107***c* and the trench concave portion **107***b* (i.e., part of the conductive film located above the third interlayer dielectric film **107**) is removed by, for example, a CMP process. In this manner, a second via **113** connected to the first interconnect **112** and a second interconnect **114** connected to the second via **113** are formed (i.e., a dual damascene interconnect constituted by the second via **113** and the second interconnect **114** is formed) in the third interlayer dielectric film **107** in the chip region **102**. At the same time, a second seal via **123** connected to the first seal interconnect **122** is formed through the third interlayer dielectric film **107** in the seal ring region. The process of forming a via and an interconnect by burying a conductive film in a concave portion as described above is generally called a dual damascene process.

In the case of forming the second via **113** and the second interconnect **114** by a single damascene process, different conductive films are buried in the via hole **107***a* for forming the second via **113** and the interconnect trench **107***c* for forming the second interconnect **114**, respectively. Therefore, two processes of burying the conductive films are also performed on the trench concave portion **107***b*. These two burying processes cause a "junction" inside the second seal via **123**.

However, in this embodiment, the second seal via **123** is formed by burying a conductive film only once simultaneously with the formation of an interconnect with a dual damascene structure, so that no junction between conductive films occurs inside the second seal via **123**.

In the case where an interconnect with a dual damascene structure is formed in an interlayer dielectric film in the chip region **102** and a seal via constituting the seal ring **104** is formed in this interlayer dielectric film as in this embodiment, the seal via has an aspect ratio of three or more. Accordingly, the number of junctions between components of the seal ring **104** is reduced, so that the seal ring further ensures prevention of contamination of the chip region **102** from the outside.

Subsequently, as shown in FIG. **6**A, a fourth interlayer dielectric film **108** is deposited on the third interlayer dielectric film **107**, and then a dual damascene interconnect structure and a seal ring are formed in the fourth interlayer dielectric film **108** by a dual damascene process, in the same manner as the process steps shown in FIGS. **4**D through **5**C.

Specifically, as shown in FIG. **6**A, through a lithography process and a dry etching process, a via hole **108***a* for forming a third via **115** (see FIG. **6**B) is formed through the fourth interlayer dielectric film **108** in the chip region **102** and, at the same time, a trench concave portion **108***b* for forming a third seal via **124** is formed through the fourth interlayer dielectric film **108** in the seal ring region. Thereafter, a resist film (not shown) for forming an interconnect trench in which a third interconnect **116** (see FIG. **6**B) is to be buried is formed on the fourth interlayer dielectric film **108** using a lithography process. This resist film has an opening on the interconnect region including the via hole **108***a*. The resist film is also buried in the trench concave portion **108***b*. Then, through a dry etching process using the resist film as a mask, an interconnect trench **108***c* for forming the third interconnect **116** is formed in an upper part of the fourth interlayer dielectric film **108** in the chip region **102** to be connected to the via hole **108***a*. Then, the remaining resist film is removed by ashing. In this manner, a concave portion (i.e., the via hole **108***a* and the interconnect trench **108***c*) for forming a dual damascene interconnect and a trench concave portion **108***b* for forming the third seal via **124** are formed in the fourth interlayer dielectric film **108**.

Subsequently, as shown in FIG. **6**B, a conductive film made of, for example, Cu is buried in a concave portion with the dual damascene structure in which the via hole **108***a* for

forming the third via **115** and the interconnect trench **108***c* for forming the third interconnect **116** are integrated and also buried in the trench concave portion **108***b* for forming the third seal via **124**. Then, part of the conductive film extending off the interconnect trench **108***c* and the trench concave portion **108***b* (i.e., part of the conductive film located above the fourth interlayer dielectric film **108**) is removed by, for example, a CMP process. In this manner, a third via **115** connected to the second interconnect **114** and a third interconnect **116** connected to the third via **115** are formed (i.e., a dual damascene interconnect constituted by the third via **115** and the third interconnect **116** is formed) in the fourth interlayer dielectric film **108** in the chip region **102**. At the same time, a third seal via **124** connected to the second seal via **123** is formed through the fourth interlayer dielectric film **108** in the seal ring region.

Thereafter, as shown in FIG. **6**B, on the fourth interlayer dielectric film **108**, which is the uppermost interconnect layer, a passivation film **109** serving as a protection film of this uppermost interconnect layer is deposited. Then, parts of the passivation film **109** on the third interconnect **116** and the third seal via **124**, respectively, are removed by a lithography process and a dry etching process, thereby forming openings. The opening of the passivation film **109** on the third seal via **124** is in the shape of a trench completely surrounding the chip region **102**.

Thereafter, as shown in FIG. **6**C, an Al (aluminum) film, for example, is deposited by, for example, a spattering process over the entire surface of the passivation film **109** including the openings on the third interconnect **116** and the third seal via **124**, respectively, and then this Al film is patterned into a predetermined shape by a lithography process and a dry etching process. Specifically, an unnecessary part of the Al film on the region except for the openings and their neighboring portions is removed. In this manner, a pad electrode **117** connected to the third interconnect **116** is formed in the opening of the passivation film **109** on the third interconnect **116** and a cap layer **125** connected to the third seal via **124**, i.e., the seal ring **104**, is formed in the opening of the passivation film **109** on the third seal via **124**. In this manner, an interconnect structure and a bonding pad (pad electrode **117**) for connecting the interconnect structure to an external electrode are formed in the chip region **102**, whereas the seal ring **104** including the cap layer **125** at its top is formed in the seal ring region, i.e., in a peripheral part of the chip region **102**.

As described above, in this embodiment, an interconnect structure is formed by using a dual damascene process with which a conductive film is buried in a hole for forming a via and a trench for forming an interconnect at the same time. This interconnect structure and a seal via constituting a seal ring are formed in the same process. Specifically, simultaneously with burying of a conductive film in an interconnect trench having a dual damascene structure in which a concave portion for forming a via and an interconnect trench for forming an interconnect are integrated, the conductive film is also buried in a concave portion for forming a seal via. Accordingly, a seal via having a sufficient height, i.e., a seal via whose aspect ratio of the depth (height) to the width, for example, is one or more (preferably three or more), is formed through one burying process.

Therefore, in this embodiment, the resultant seal ring has a smaller number of "junctions" originating from burying of conductive films, as compared to the case of forming an interconnect by a single damascene process. Specifically, a merit of a small number of processes of burying conductive films is that the number of interfaces between the conductive films constituting a seal ring is reduced. That is, discontinuous portions due to poor burying of conductive films are less likely to occur between components of a seal ring, resulting in that the resultant seal ring has higher reliability than that obtained through a large number of burying processes.

In this embodiment, the cap layer **125** connected to the top of the seal ring **104** is formed simultaneously with the formation of a pad (pad electrode **117**) for supplying power from the outside to interconnect layers in the chip region **102** or for taking a signal from the interconnect layers to the outside. This makes it possible to form the cap layer **125** at the top of the seal ring **104** without an additional process for forming the cap layer.

Hereinafter, a seal ring structure of this embodiment shown in FIG. **2**A will be described specifically.

As shown in FIG. **2**A (or FIG. **6**C), the seal ring of this embodiment is formed in the chip region **102** near the boundary between the chip region **102** and the scribe region **103**. An element (not shown) such as a transistor is formed on the substrate **101** in the chip region **102**, and a plurality of interconnect layers are formed over the element such as a transistor.

As shown in FIG. **2**A, in the peripheral part of the chip region **102** as described above, the seal ring **104** as a combination of the conductive layer **120**, the seal vias **121**, **123** and **124** and the seal interconnect **122** is formed to surround the inside of the chip region **102**, i.e., the above-mentioned element and interconnect layers and to penetrate the multilayer structure made of a plurality of interlayer dielectric films **105** through **108**. Specifically, the seal ring **104** is made of a conductor (e.g., Cu) continuously buried from the lowermost interlayer dielectric film through the uppermost interlayer dielectric film without interruption (without gaps) in the multilayer structure in the peripheral part of the chip region **102** (i.e., in the chip region **102** near the boundary between the chip region **102** and the scribe region **103**.) This seal ring **104** serves as a barricade for blocking the passage of entering of an impurity and the like from the outside into the chip region **102**.

In this embodiment, at least one conductor (component) out of stacked conductors constituting the seal ring **104** and an interconnect with a dual damascene structure are formed by the same process as described above. Accordingly, this conductor serves as a seal via penetrating at least one interlayer dielectric film without a "junction". That is, the seal ring **104** is formed in the process for forming a dual damascene interconnect in the entire chip region **102** in which a seal ring, an element such as a transistor, an interconnect and others are formed, so that the number of "junctions" in the seal ring **104** is reduced. If a "junction", i.e., an interface between conductive films serving as components, is present in the seal ring, this "junction" serves as a path through which impact caused during, for example, dicing of the substrate (wafer) **101** along the scribe region **103** or moisture entering from the outside easily propagates into the chip region **102**. However, in this embodiment, the number of "junctions" between components of the seal ring **104** is reduced, so that it is possible to prevent impact during wafer dicing or moisture from the outside from entering the chip region **102**.

In this embodiment, the seal ring **104** is formed in the peripheral part of the chip region **102** (in the chip region **102** near the boundary between the chip region **102** and the scribe region **103**). Accordingly, when the substrate (wafer) **101** on which a plurality of semiconductor devices are formed is diced along the scribe region **103** so as to obtain the individual semiconductor devices as chips, it is possible

to prevent mechanical impact or stress on the scribe region **103** during the dicing from propagating into the chip region **102**.

In the seal ring structure shown in FIG. **2**A, the cap layer **125** of, for example, Al on the third seal via **124** formed on the uppermost interlayer dielectric film (i.e., fourth interlayer dielectric film **108**) is formed in an opening provided in part of the protection film (passivation film **109**) on the third seal via **124**, i.e., is formed in a trench provided in the passivation film **109** to completely surround an interconnect layer and others formed in the chip region **102**. Specifically, the cap layer **125** connected to the top of the seal ring **104** is formed to protrude from the surface of the passivation film **109**. Accordingly, the passivation film **109** partially opens to be discontinuous.

In this embodiment, part of the passivation film **109** located in the chip region **102** and part of the passivation film **109** located outside the seal ring region (including the scribe region **103**) are discontinuous, so that mechanical impact on the passivation film **109** near the scribe region **103** during dicing is less likely to propagate into films such as the passivation film **109** deposited in the chip region **102**. That is, the passivation film **109** is partially discontinuous in the chip region **102** near the boundary between the chip region **102** and the scribe region **103**, so that it is possible to prevent impact during dicing of the wafer from reaching the chip region **102**.

Accordingly, it is possible to prevent the phenomenon that impact during dicing causes cracks or the like in part of the passivation film **109** located in the scribe region **103** to make the passivation film **109** and others peel off in the chip region **102**. This avoids occurrence of cracks in the chip region **102**. As a result, it is possible to prevent a contaminant such as moisture or mobile ions from entering the chip from the chip surface, thus enhancing the reliability of semiconductor devices.

In addition, the cap layer **125** is buried in the opening of the passivation film **109** on the seal ring **104** so that the cap layer **125** and the body of the seal ring **104** are continuous. Accordingly, unlike a case where the cap layer **125** is not provided, it is possible to prevent moisture or an impurity which has entered from the scribe region **103** during dicing from penetrating into the chip region **102** via the peripheral part of the chip region **102**, i.e., the opening of the passivation film **109** near the scribe region **103**.

In the seal ring structure of this embodiment shown in FIG. **2**A, the seal ring **104** is preferably narrow in part (specifically, the seal vias **121**, **123** and **124**). Specifically, the aspect ratio (the ratio of the height to the width) of this part is preferably one or more. In particular, the aspect ratio of a seal via formed without "junctions" through an interlayer dielectric film in which a dual damascene interconnect is formed is preferably three or more. Alternatively, in a case where seal vias (e.g., the seal vias **123** and **124**) are respectively formed through two or more successive interlayer dielectric films, the aspect ratio of the structure of these stacked seal vias is preferably three or more. In this manner, if seal vias are used as conductors which are components of the seal ring **104**, a margin for disposing the seal ring can be adjusted to some degree in accordance with an interconnect layout in interlayer dielectric films by utilizing the fact that the widths of vias are smaller than those of interconnects. That is, in an interlayer dielectric film in which a wide range of the chip region **102** needs to be used to dispose an interconnect layer and others, a seal via is preferably used as a component of the seal ring **104**.

On the other hand, if the space for forming a seal ring therein in a target interlayer dielectric film has a margin in consideration of an interconnect layout of the chip region **102** and others, a seal interconnect having substantially the same width as an interconnect can be used. That is, a seal ring is formed by using a mask provided with a seal interconnect pattern having substantially the same width as an interconnect pattern.

As described above, in this embodiment, the width of each component of a seal ring is selected for each dielectric film under consideration of an interconnect layout of the chip region **102**. Accordingly, the width (thickness) of each dielectric film for the seal ring is controlled as necessary.

In this embodiment, instead of the seal ring structure shown in FIG. **2**A, i.e., a seal ring structure in which at least two seal vias are continuously stacked, a seal ring **104** in which seal vias and seal interconnects are alternately stacked in the same manner as in the seal ring structure shown in FIG. **2**B, i.e., an interconnect structure in which vias and interconnects are alternately stacked in the chip region **102** where an element and others are formed, may be used.

Hereinafter, the seal ring structure shown in FIG. **2**B will be described specifically. In FIG. **2**B, components already shown in FIG. **2**A are denoted by the same reference numerals, and thus the description thereof will be omitted.

As shown in FIG. **2**B, the seal ring **104** is formed simultaneously with the formation of an interconnect structure in the chip region **102**. Specifically, a first seal via **121** is formed through a first interlayer dielectric film **105** on a conductive layer **120**. A first seal interconnect **122** is formed through a second interlayer dielectric film **106** on the first interlayer dielectric film **105** to be connected to the first seal via **121**. In a third interlayer dielectric film **107** deposited on the second interlayer dielectric film **106**, an interconnect (seal portion) with a dual damascene structure in which a second seal via **126** connected to the first seal interconnect **122** and a second seal interconnect **127** connected to the second seal via **126** are integrated is formed. In a fourth interlayer dielectric film **108** on the third interlayer dielectric film **107**, a seal portion with a dual damascene structure in which a third seal via **128** connected to the second seal interconnect **127** and a third seal interconnect **129** connected to the third seal via **128** are integrated is formed. A passivation film **109** formed on the fourth interlayer dielectric film **108** has an opening on top of the third seal interconnect **129**. A cap layer **125** connected to the third seal interconnect **129** is formed in this opening.

In this manner, the semiconductor device of this embodiment shown in FIG. **2**B includes the seal ring **104** with a structure similar to that of an interconnect structure formed in the chip region **102**, so that the seal ring **104** and the interconnect are formed by the same process.

In addition, in the semiconductor device of this embodiment shown in FIG. **2**B, an interconnect structure, e.g., the second via **113** and the second interconnect **114**, and components of the seal ring **104**, e.g., the second seal via **126** and the second seal interconnect **127**, are formed by the same dual damascene process. Accordingly, a concave portion for forming the second seal via **126** and a trench for forming the second seal interconnect **127** are integrated, so that the concave portion and the trench are filled with a conductive film at the same time. As a result, no "junction" is present between the second seal via **126** and the second seal interconnect **127**. Specifically, if an interconnect structure and a seal ring **104** are formed by a dual damascene process in the manner as in this embodiment, the number of "junctions" in the seal ring **104** is reduced, thereby forming the seal ring

104 capable of preventing moisture or an impurity from entering the chip region 102 from the outside of the scribe region 103 and others. As a result, the moisture resistance of semiconductor chips (semiconductor devices) is enhanced and the semiconductor chips are manufactured with high yield.

The seal ring structure shown in FIG. 2B is formed using photo masks in which a mask pattern for forming an interconnect structure in the chip region 102 and a mask pattern for forming a seal ring coincide with each other with respect to the same interlayer dielectric film. For example, when an interconnect with a dual damascene structure in which a via (plug) and an interconnect are integrated is formed in the interlayer dielectric film 107 in the chip region 102, a dual damascene process is also employed to form a component of the seal ring 104 in this interlayer dielectric film 107. Specifically, the component of the seal ring 104 formed in the interlayer dielectric film 107 is constituted by the second seal via 126 having substantially the same width as the second via 113 and the second seal interconnect 127 having substantially the same width as the second interconnect 114. In the interlayer dielectric film 107, the multilayer structure made of the second seal via 126 and the second seal interconnect 127 is formed to vertically penetrate the interlayer dielectric film 107 and completely surround (without an interruption) the chip region 102.

The seal ring 104 shown in FIG. 2B is formed by alternately stacking seal interconnects and seal vias and the width of a seal interconnect is larger than that of the associated seal via. Accordingly, the strength of the seal ring is enhanced, as compared to a seal ring formed by stacking only seal vias or stacking seal vias for the most part.

The method for fabricating a semiconductor device with the structure shown in FIG. 2B is different from that for fabricating a semiconductor device with the structure shown in FIG. 2A only in mask patterns for forming the seal ring in respective photo masks. Specifically, in forming the seal ring 104 shown in FIG. 2A, for example, mask patterns for forming the seal ring in respective masks which have been predetermined so as to form the third seal via 124 on the second seal via 123 are altered in the formation of the seal ring 104 shown in FIG. 2B. More specifically, mask patterns for forming a seal ring in respective masks are defined such that the second seal interconnect 127 is formed on the second seal via 126 and the third seal interconnect 129 is formed on the third seal via 128, i.e., such that seal vias and seal interconnects are alternately formed.

Hereinafter, the seal ring structure shown in FIG. 3A, i.e., a seal ring 104 in which a seal via is divided into at least two branches in an interlayer dielectric film, will be described specifically. In FIG. 3A, components already shown in FIG. 2A are denoted by the same reference numerals, and thus the description thereof will be omitted.

The seal ring structure shown in FIG. 3A is different from that shown in FIG. 2A in the following aspects. First, instead of the first seal via 121, seal vias 121*a* and 121*b* connected to the conductive layer 120 are provided through the first interlayer dielectric film 105. Second, instead of the second seal via 123, seal vias 123*a* and 123*b* connected to the first seal interconnect 122 are provided through the third interlayer dielectric film 107. Third, instead of the third seal via 124, seal vias 124*a* and 124*b* connected to the respective seal vias 123*a* and 123*b* are provided through the fourth interlayer dielectric film 108. The tops of the respective seal vias 121*a* and 121*b* are connected to the first seal interconnect 122, and the tops of the respective seal vias 124*a* and 124*b* are connected to the cap layer 125.

That is, the method for fabricating a semiconductor device with the structure shown in FIG. 3A is different from that for fabricating a semiconductor device with the structure shown in FIG. 2A in that mask patterns for forming two seal vias are provided in photo masks for use in etching of an interlayer dielectric film, and a conductive film is buried in a pair of parallel trench concave portions formed by using these mask patterns.

In addition to the advantages obtained by the seal ring structure shown in FIG. 2A, the seal ring structure shown in FIG. 3A has the following advantages. Since a seal via is narrower than a seal interconnect, the strength of the seal via is relatively lower than that of the seal interconnect. On the other hand, if a seal via divided into at least two branches is used instead of a single seal via as a component of a seal ring as in the seal ring structure shown in FIG. 3A, the seal ring partially has a multiplex structure (i.e., a structure in which the chip region 102 is surrounded by multiple seal ring branches) in an interlayer dielectric film in which the seal via is divided into the branches. Accordingly, as compared to a seal ring which is not divided into branches in an interlayer dielectric film (i.e., which has a single structure), the strength of the seal ring with the multiplex structure shown in FIG. 3A is enhanced. It should be noted that in terms of processing, the seal ring structure shown in FIG. 2A is more easily implemented than the seal ring structure shown in FIG. 3A.

With the seal ring structure shown in FIG. 3A, even if the seal ring 104 is damaged in part by impact involved in dicing of a wafer (substrate 101) into chips along the scribe region 103, it is possible to prevent the chip region 102 inside the scribe region 103 from being affected by the impact as long as the seal ring 104 in this damaged part has a multiplex structure including two or more branches. Specifically, it is possible to suppress entering of moisture from the scribe region 103 into the chip region 102 or propagation of the impact during dicing of the wafer along the scribe region 103 into the chip region 102.

The seal ring 104 shown in FIG. 3A has a structure in which a seal via is divided into two branches connected to one seal interconnect. Alternatively, a seal via may be divided into three or more branches connected to one seal interconnect. In the seal ring 104 shown in FIG. 3A, each of the seal vias is divided into a plurality of branches in a film. Alternatively, the seal via may be selectively divided into branches in each film, depending on a margin on a layout necessary for an interconnect layer formed in the chip region 102, or the strength of a film (interlayer dielectric film), for example.

In this embodiment, an interconnect structure is formed in four stacked interlayer dielectric films. However, the number of interlayer dielectric films is not limited to four and may of course be smaller or greater than four depending on the structure of a chip.

In this embodiment, Cu is used as a conductive material constituting the seal ring 104. However, the present invention is not limited to this, and the seal ring 104 may be made of at least one of W, Al and Cu. Then, the seal ring 104 is formed out of the same material as interconnects and vias formed in the chip region 102 of a semiconductor device.

In this embodiment, the conductive material constituting the cap layer 125 is not specifically limited. However, use of Al as the conductive material ensures prevention of erosion of the seal ring 104 (especially a seal ring made of Cu.)

In this embodiment, in a case where a plurality of seal vias are continuously stacked as in the seal ring structure shown in FIG. 2A or 3A, for example, the contact surface of an

upper seal via or a lower seal via is preferably larger than that of the other seal via. Then, the contact margin is enhanced.

Embodiment 2

Hereinafter, a semiconductor device and a method for fabricating the device according to a second embodiment of the present invention will be described with reference to drawings.

FIG. **7** is a plan view showing part of a wafer on which a semiconductor device of the second embodiment (i.e., a semiconductor device in which a chip region is surrounded by two seal rings) is provided. Hereinafter, a seal ring structure including two or more seal rings surrounding a chip region will be also referred to as a multi-seal ring structure.

As shown in FIG. **7**, on a wafer **201** to be a semiconductor substrate, typically a silicon substrate, for example, a plurality of chip regions **202** to be semiconductor devices, are provided. In each of the chip regions **202**, an IC made of a plurality of elements and provided with a given function is formed. The chip regions **202** are defined by a scribe region **203** having a lattice pattern.

A semiconductor device (i.e., a semiconductor chip) includes: an IC (located in the chip region **202**) made of a plurality of elements and provided with a given function; and seal rings **204***a* and **204***b* provided in a peripheral part of the chip region **202** to surround the chip region **202**. In this embodiment, a multi-seal ring structure including two seal rings is used. Alternatively, a multi-seal ring including three, four or more seal rings may be used depending on a margin on a layout.

After formation of chips has been completed, the wafer **201** on which a plurality of semiconductor devices each having its chip region **202** surrounded by the multi-seal ring structure **204** are formed is diced along the scribe region **203**, thereby separating the semiconductor devices from each other.

In this embodiment, the seal ring structure **204** having at least two seal rings is formed in the chip region **202** near the scribe region **203**. Accordingly, even if one of the seal rings (e.g., the outermost seal ring) is damaged during dicing of the wafer **201**, damage to an element, an active region and others in the chip region **202** is prevented by the other inner seal ring(s). This eliminates degradation of performance of a semiconductor chip caused by occurrence of a crack in the chip region **202**, including an element, an active region and others, during dicing of the wafer **201** into chips.

FIGS. **8**A and **8**B show variations of the cross-sectional structure taken along the line B-B' in FIG. **7** (the cross-sectional structure of an end of a semiconductor device including a seal ring portion located in a peripheral part of the chip region **202**.)

As shown in FIGS. **7**, **8**A and **8**B, a semiconductor device before dicing includes the chip regions **202** and the scribe region **203**, and the seal rings **204***a* and **204***b* are formed in the chip region **202** near the boundary between the chip region **202** and the scribe region **203**.

Now, features of the respective structures shown in FIGS. **8**A and **8**B will be described specifically.

First, the structure shown in FIG. **8**A has a feature in which seal vias constituting each of the seal rings **204***a* and **204***b* are continuously formed through at least two successive films.

Next, the structure shown in FIG. **8**B has a feature in which seal vias constituting each of the seal rings **204***a* and **204***b* are continuously formed through at least two successive films, two or more adjacent seal vias are formed in the same interlayer dielectric film, and these two or more adjacent seal vias are connected to one seal interconnect formed in a dielectric film located on top or bottom of the film in which the seal vias are formed. That is, each seal via constituting the seal ring structure **204** shown in FIG. **8**B is divided into two or more branches in the same interlayer dielectric film.

On the other hand, the structures shown in FIGS. **8**A and **8**B have a common feature in which the seal ring structure **204** includes at least two seal rings and seal ring caps (cap layers **225***a* and **226***b*) are provided at the tops of the respective seal rings **204***a* and **204***b*.

Hereinafter, a method for fabricating a semiconductor device having the structure shown in FIG. **8**A will be described with reference to FIGS. **9**A through **9**D and **10**A through **10**C.

First, as shown in FIG. **9**A, an active layer **210** constituting an element such as a transistor is formed in a wafer **201** (hereinafter, referred to as a substrate **201**) in a chip region **202**. At the same time, two adjacent conductive layers **220***a* and **220***b* are formed in the substrate **201** in a peripheral part of the chip region **202** (a seal ring region near a scribe region **203**.) The conductive layers **220***a* and **220***b* have similar configuration as that of the active layer **210**.

Then, a first interlayer dielectric film **205** is deposited on the substrate **201**. Subsequently, through a lithography process and a dry etching process, a via hole **205***a* for forming a first via **211** (see FIG. **9**B) is formed through the first interlayer dielectric film **205** in the chip region **202** and, at the same time, trench concave portions **205***b* and **205***c* for forming first seal vias **221***a* and **221***b* (see FIG. **9**B) on the respective adjacent conductive layers **220***a* and **220***b* are formed through the first interlayer dielectric film **205** in the seal ring region. The seal vias are components of seal rings and are formed by filling the trench concave portions with a conductive material. Specifically, each seal via has a line structure having substantially the same width as a via in the chip region.

In this embodiment, the aspect ratio of a seal via (i.e., the ratio of the depth to the width in a concave portion in which the seal via is buried) is preferably one or more. In particular, in the case where seal vias are formed simultaneously with an interconnect layer as in this embodiment, the aspect ratio of each seal via is preferably set at three or more in accordance with the degree of miniaturization of interconnects.

In this embodiment, the trench concave portions **205***b* and **205***c* for forming the first seal vias **221***a* and **221***b* and the via hole **205***a* are formed at the same time in the first interlayer dielectric film **205** in the chip region **202**. Alternatively, the via hole **205***a* and the trench concave portions **205***b* and **205***c* may of course be formed individually.

Next, as shown in FIG. **9**B, the via hole **205***a* and the trench concave portions **205***b* and **205***c* formed through the first interlayer dielectric film **205** are filled with a conductive film made of, for example, W by, for example, a CVD process. Then, an unnecessary part of the conductive film extending off the via hole **205***a* and the trench concave portions **205***b* and **205***c* is removed by, for example, a CMP process, thereby forming a first via **211** connected to the active layer **210** and adjacent first seal vias **221***a* and **221***b* connected to the respective conductive layers **220***a* and **220***b*.

Thereafter, a second interlayer dielectric film **206** is deposited on the first interlayer dielectric film **205**. Then,

through a lithography process and a dry etching process, an interconnect trench **206**a for forming a first interconnect **212** (see FIG. **9**C) is formed through the second interlayer dielectric film **206** in the chip region **202**, and at the same time, interconnect trenches **206**b and **206**c for forming adjacent first seal interconnects **222**a and **222**b (see FIG. **9**C) are formed through the second interlayer dielectric film **206** in the seal ring region.

Then, as shown in FIG. **9**C, the interconnect trenches **206**a, **206**b and **206**c formed through the second interlayer dielectric film **206** are filled with a conductive film of, for example, Cu by, for example, an electroplating process. Thereafter, part of the conductive film extending off the interconnect trenches **206**a, **206**b and **206**c is removed by, for example, a CMP process, thereby forming a first interconnect **212** connected to the first via **211** and adjacent first seal interconnects **222**a and **222**b connected to the respective first seal vias **221**a and **221**b.

Subsequently, a third interlayer dielectric film **207** is deposited on the second interlayer dielectric film **206**, and then a via hole **207**a for forming a second via **213** (see FIG. **10**A) is formed through the third interlayer dielectric film **207** in the chip region **202**. At the same time, trench concave portions **207**b and **207**c for forming adjacent second seal vias **223**a and **223**b (see FIG. **10**A) are formed through the third interlayer dielectric film **207** in the seal ring region.

Then, as shown in FIG. **9**D, a resist film **230** for forming an interconnect trench in which a second interconnect **214** (see FIG. **10**A) is to be buried is formed on the third interlayer dielectric film **207** using a lithography process. This resist film **230** has an opening on an interconnect region including the via hole **207**a. The resist film **230** is also buried in the trench concave portions **207**b and **207**c.

Thereafter, through a dry etching process using the resist film **230** as a mask, an interconnect trench connected to the via hole **207**a and used for forming the second interconnect **214** is formed in an upper part of the third interlayer dielectric film **207** in the chip region **202**. Then, the remaining resist film **230** is removed by ashing. Thereafter, a conductive film made of, for example, Cu is buried in the via hole **207**a, the interconnect trench integrated with the via hole **207**a to form a concave portion with a dual damascene structure, and the trench concave portions **207**b and **207**c formed in the third interlayer dielectric film **207** by the previous process steps. Then, part of the conductive film extending off the interconnect trench and the trench concave portions **207**b and **207**c (i.e., part of the conductive film located above the third interlayer dielectric film **207**) is removed by, for example, a CMP process. In this manner, as shown in FIG. **10**A, a second via **213** connected to the first interconnect **212** and a second interconnect **214** connected to the second via **213** are formed (i.e., a dual damascene interconnect constituted by the second via **213** and the second interconnect **214** is formed) in the third interlayer dielectric film **207** in the chip region **202**. At the same time, two adjacent second seal vias **223**a and **223**b connected to the respective first seal interconnects **222**a and **222**b are formed through the third interlayer dielectric film **207** in the seal ring region. The process of simultaneously forming a via and an interconnect by burying a conductive film in a concave portion as described above is generally called a dual damascene process.

If the second via **213** and the second interconnect **214** are formed by a single damascene process, different conductive films are buried in the via hole **207**a for forming the second via **213** and the interconnect trench for forming the second interconnect **214**, respectively. Therefore, since this interconnect structure and the second seal vias **223**a and **223**b are formed by the same process, two burying processes of the conductive films are also performed on the trench concave portions **207**b and **207**c. In this case, "junctions" created by these two burying processes occur inside the second seal vias **223**a and **223**b.

However, in this embodiment, the second seal vias **223**a and **223**b are formed by burying a conductive film only once in the process for forming an interconnect with a dual damascene structure, so that no junction is created between conductive films in the seal vias.

In the case where an interconnect with a dual damascene structure is formed in an interlayer dielectric film in the chip region **202** and seal vias constituting the seal ring structure **204** are formed in this interlayer dielectric film as in this embodiment, each of the resultant seal vias has an aspect ratio of three or more. Accordingly, the number of junctions between components of the seal ring structure **204** is reduced, so that a seal ring structure which further ensures prevention of contamination of the chip region **202** from the outside.

Subsequently, as shown in FIG. **10**B, a fourth interlayer dielectric film **208** is deposited on the third interlayer dielectric film **207**, and then an interconnect structure with a dual damascene and a seal ring are formed in the fourth interlayer dielectric film **208** by a dual damascene process, in the same manner as in the process steps shown in FIGS. **9**C through **10**A.

Specifically, as shown in FIG. **10**B, through a lithography process and a dry etching process, a via hole for forming a third via **215** is formed through the fourth interlayer dielectric film **208** in the chip region **202** and, at the same time, two trench concave portions for forming adjacent third seal vias **224**a and **224**b are formed through the fourth interlayer dielectric film **208** in the seal ring region. Thereafter, a resist film (not shown) for forming an interconnect trench in which a third interconnect **216** is to be buried is formed on the fourth interlayer dielectric film **208** using a lithography process. This resist film has an opening on the interconnect region including the via hole. The resist film is also buried in the trench concave portions. Then, through a dry etching process using the resist film as a mask, an interconnect trench connected to the via hole and used for forming the third interconnect **216** is formed in an upper part of the fourth interlayer dielectric film **208** in the chip region **202**. Then, the remaining resist film is removed by ashing. In this manner, a concave portion (i.e., the via hole and the interconnect trench) for forming a dual damascene interconnect and two trench concave portions for forming the third seal vias **224**a and **224**b are formed in the fourth interlayer dielectric film **208**.

Subsequently, as shown in FIG. **10**B, a conductive film made of, for example, Cu is buried in a concave portion with the dual damascene structure in which the via hole for forming the third via **215** and the interconnect trench for forming the third interconnect **216** are integrated and also buried in the trench concave portions for forming the respective third seal vias **224**a and **224**b, in the fourth interlayer dielectric film **208**. Then, part of the conductive film extending off the interconnect trench and the trench concave portions (i.e., part of the conductive film located above the fourth interlayer dielectric film **208**) is removed by, for example, a CMP process. In this manner, a third via **215** connected to the second interconnect **214** and a third interconnect **216** connected to the third via **215** are formed (i.e., a dual damascene interconnect constituted by the third via **215** and the third interconnect **216** is formed) in the

fourth interlayer dielectric film **208** in the chip region **202**. At the same time, third seal vias **224***a* and **224***b* connected to the respective second seal vias **223***a* and **223***b* are formed through the fourth interlayer dielectric film **208** in the seal ring region.

Thereafter, as shown in FIG. **10**B, on the fourth interlayer dielectric film **208**, which is the uppermost interconnect layer, a passivation film **209** serving as a protection film of this uppermost interconnect layer is deposited. Then, parts of the passivation film **209** on the third interconnect **216** and the adjacent third seal vias **224***a* and **224***b* are removed by a lithography process and a dry etching process, thereby forming openings. In this manner, the upper surfaces of the respective third interconnect **216** and the third seal vias **224***a* and **224***b* are exposed.

Thereafter, as shown in FIG. **10**C, an Al film, for example, is deposited by, for example, a spattering process over the entire surface of the passivation film **209** including the openings on the third interconnect **216** and the third seal vias **224***a* and **224***b*. Then, this Al film is patterned into a predetermined shape by a lithography process and a dry etching process. Specifically, an unnecessary part of the Al film on the region except for the openings and their neighboring regions is removed. In this manner, a pad electrode **217** connected to the third interconnect **216** is formed in the opening of the passivation film **209** on the third interconnect **216**, and cap layers **225***a* and **225***b* connected to the respective third seal vias **224***a* and **224***b*, i.e., the respective seal rings **204***a* and **204***b*, are formed in the openings of the passivation film **209** on the respective third seal vias **224***a* and **224***b*.

In this manner, an interconnect structure and a bonding pad (pad electrode **217**) for connecting the interconnect structure to an external electrode are formed in the chip region **202**, whereas the seal rings **204***a* and **204***b* and the cap layers **225***a* and **225***b*, which are connected to the respective seal rings **204***a* and **204***b* through the protection film (passivation film **209**) deposited on the seal rings **204***a* and **204***b*, are formed in the seal ring region, i.e., in the peripheral part of the chip region **202** (near the boundary between the chip region **202** and the scribe region **203**.)

As described above, in this embodiment, an interconnect structure is formed by using a dual damascene process with which a conductive film is buried in a hole for forming a via and a trench for forming an interconnect at the same time. Seal vias constituting seal rings are also formed by the process for forming the interconnect structure. Specifically, an interconnect trench with a dual damascene structure in which a concave portion for forming a via and an interconnect trench for forming an interconnect are integrated is filled simultaneously with concave portions for forming seal vias at the same time. Accordingly, the concave portions for forming seal vias having sufficient heights, i.e., concave portions for forming seal vias whose aspect ratio of the depth to the width, for example, is one or more (preferably three or more), are filled by single burying process.

Therefore, in this embodiment, the resultant seal ring structure has a smaller number of "junctions" originating from burying of conductive films, as compared to the case of forming an interconnect by a single damascene process. Specifically, a merit of a small number of burying processes of conductive films is that the number of interfaces between conductive films constituting a seal ring is reduced. That is, discontinuous portions due to poor burying of conductive films are less likely to occur between components of a seal ring, resulting in that the resultant seal ring structure exhibits higher reliability than a seal ring structure obtained through a large number of burying processes (i.e., a seal ring structure formed by a single damascene process.)

In this embodiment, the cap layers **225***a* and **225***b* connected to the tops of the respective seal rings **204***a* and **204***b* are formed simultaneously with the formation of a pad (pad electrode **217**) for supplying power from the outside to an IC and others in the chip region **202** or for taking a signal from the IC and others to the outside. This allows the seal rings **204***a* and **204***b* including the cap layers **225***a* and **225***b* at their respective tops to be formed without an additional process for forming the cap layers.

In addition to the advantages obtained by the first embodiment, the second embodiment has the following advantages.

Specifically, in the second embodiment, the seal ring structure **204** including two seal rings completely surrounding the chip region **202** is formed in the peripheral part of the chip region **202**. Accordingly, when the semiconductor wafer (substrate) **201** is diced along the scribe region **203** so as to obtain individual completed semiconductor chips (semiconductor devices), prevention of propagation, into the chip region **202**, of mechanical impact caused by contact of a dicing blade with the scribe line (scribe region) **203** during dicing or prevention of damage to the chip region **202** due to the propagation is further ensured.

In addition, in the second embodiment, the two cap layers **225***a* and **225***b* are formed at the tops of the respective seal rings **204***a* and **204***b*, so that the following advantages are obtained.

FIG. **11**A is a plan view showing a structure of the semiconductor device (semiconductor chip) shown in FIG. **10**C (or FIG. **8**A) when viewed from above (from above the passivation film (protection film) **209** formed on the uppermost interconnect layer). FIG. **11**A shows one of semiconductor chips **201**A formed on the wafer (substrate) **201**.

As shown in FIG. **11**A, the scribe region **203** is provided to surround the chip region **202**, and the two seal rings **204***a* and **204***b* (not shown because these rings are formed under the cap layers **225***a* and **225***b*) are formed in the chip region **202** near the boundary between the chip region **202** and the scribe region **203**. The cap layers **225***a* and **225***b* formed at the tops of the respective seal rings **204***a* and **204***b* are provided in the openings (formed by partly removing the passivation film **209**) of the passivation film **209** completely surrounding the chip region **202**. Accordingly, part of the passivation film **209** in the chip region **202** and part of the passivation film **209** in the scribe region **203** are separated from each other by these two cap layers **225***a* and **225***b*. That is, connection between the scribe region **203** and the chip region **202** via the passivation film **209** is not established, so that impact on part of the passivation film **209** in the scribe region **203** during dicing hardly propagates through the passivation film **209** into the chip region **202**.

FIG. **11**B is a cross-sectional view showing the surface of a chip taken along the line C-C' in FIG. **11**A.

As shown in FIG. **11**B, the two cap layers **225***a* and **225***b* are formed through the passivation film **209** in the peripheral part of the chip region **202**. Accordingly, it is possible to prevent impact, stress or the like on the passivation film **209** in the scribe region **203** caused by contact with a dicing blade during dicing from affecting a circuit, an interconnect structure and others inside the chip region **202**.

Hereinafter, the seal ring structure shown in FIG. **8**B, i.e., a structure in which each of the seal vias constituting the seal rings **204***a* and **204***b* is divided into at least two branches in an interlayer dielectric film, will be described specifically. In

FIG. **8**B, components also shown in FIG. **8**A are denoted by the same reference numerals, and thus the description thereof will be omitted.

The seal ring structure shown in FIG. **8**B is different from that of the seal ring structure shown in FIG. **8**A in that each of the seal vias constituting the seal rings **204***a* and **204***b* is divided into at least two in an interlayer dielectric film.

Specifically, for the inner seal ring (first seal ring) **204***a* in the double structure including the first seal ring **204***a* and the outer seal ring (second seal ring) **204***b*, seal vias **221***a***1** and **221***a***2** connected to the conductive layer **220***a* are provided instead of the first seal via **221***a* in the first interlayer dielectric film **205**, seal vias **223***a***1** and **223***a***2** connected to the first seal interconnect **222***a* are provided instead of the second seal via **223***a* in the third interlayer dielectric film **207**, and seal vias **224***a***1** and **224***a***2** connected to the respective seal vias **223***a***1** and **223***a***2** are provided instead of the third seal via **224***a* in the fourth interlayer dielectric film **208**. The tops of the respective seal vias **221***a***1** and **221***a***2** are connected to the first seal interconnect **222***a*, and the tops of the respective seal vias **224***a***1** and **224***a***2** are connected to the cap layer (first cap layer) **225***a*.

For the second seal ring **204***b* located adjacent to the first seal ring **204***a* and outside the first seal ring **204***a*, seal vias **221***b***1** and **221***b***2** connected to the conductive layer **220***b* are provided instead of the first seal via **221***b* in the first interlayer dielectric film **205**, seal vias **223***b***1** and **223***b***2** connected to the first seal interconnect **222***b* are provided instead of the second seal via **223***b* in the third interlayer dielectric film **207**, and seal vias **224***b***1** and **224***b***2** connected to the respective seal vias **223***b***1** and **223***b***2** are provided instead of the third seal via **224***b* in the fourth interlayer dielectric film **208**. The tops of the respective seal vias **221***b***1** and **221***b***2** are connected to the first seal interconnect **222***b*, and the tops of the respective seal vias **224***b***1** and **224***b***2** are connected to the cap layer (second cap layer) **225***b*.

As described above, the seal rings **204***a* and **204***b* shown in FIG. **8**B have a structure in which a plurality of branches of a seal via (or a multilayer structure of such branches) are bundled by at least one seal interconnect. Accordingly, even if the width (thickness) of each seal via is small, the bundle of the branches provides the seal rings with high strength as a whole. Therefore, even if mechanical impact or stress is applied to the scribe region **203** during dicing, it is possible to prevent the seal ring **204***a* or **204***b* from being damaged or prevent damage to part of the seal ring **204***a* or **204***b* (i.e., one of the branches of seal vias) from affecting the chip region **202**.

In the seal ring structure shown in FIG. **8**B, each of the seal vias constituting the seal rings **204***a* and **204***b* is selectively divided into two, three, four or more in an interlayer dielectric film, thus enhancing protection of the chip region **202**. That is, prevention of propagation of impact or stress during dicing into the chip region **202** is further ensured.

In the seal ring structure shown in FIG. **8**B, as in the seal ring structure shown in FIG. **8**A, even if the outer second seal ring **204***b* is damaged, it is still possible to prevent a contaminant such as moisture or mobile ions from entering the chip region **202** and thereby degradation of the reliability of a semiconductor device is avoided, as long as the first seal ring **204***a*, which is electrically insulated from the second seal ring **204***b*, is not damaged and has its shape maintained.

In the seal ring structure shown in FIG. **8**B, a seal via is divided into two branches connected to one seal interconnect. Alternatively, the seal via may be divided into three or more branches connected to one seal interconnect. That is, the number of branches of a seal via may be appropriately selected in accordance with a margin on the layout of the chip region **202** or the strength of the film (interlayer dielectric film.)

In the seal rings **204***a* and **204***b* shown in FIGS. **8**A and **8**B, instead of the structure in which two or more seal vias are continuously stacked, a structure in which seal vias and seal interconnects are alternately stacked, e.g., an interconnect structure in which vias and interconnects are alternately stacked in the chip region **202** including an element and others are formed, may be used. In such a case, the same advantages as those obtained in this embodiment are obtained. It should be noted that a seal ring using a seal interconnect has a larger width than that using a seal via. Therefore, it is preferable to determine whether a seal interconnect is used or not in consideration of layouts of respective interconnect layers.

In this embodiment, an interconnect structure is formed in four successive interlayer dielectric films. However, the number of such interlayer dielectric films is not limited to four and may of course be smaller or larger than four, depending on the structure of the chip.

In this embodiment, Cu is used as a conductive material constituting the seal rings **204***a* and **204***b*. However, the present invention is not limited to this, and the seal rings **204***a* and **204***b* may be made of at least one of W, Al and Cu. Then, the seal rings **204***a* and **204***b* are formed out of the same material as that constituting interconnects and vias formed in the chip region **202** of a semiconductor device.

In addition, in this embodiment, the conductive material constituting the cap layers **225***a* and **225***b* is not specifically limited. However, if the conductive material is Al, prevention of erosion of the seal rings **204***a* and **204***b* (especially seal rings made of Cu) is ensured.

Moreover, in this embodiment, if a plurality of seal vias are continuously stacked as in the seal ring structures shown in FIGS. **8**A and **8**B, for example, the contact surface of an upper seal via or a lower seal via is preferably larger than that of the other seal via. Then, the contact margin is increased.

Modified Example 1 of Embodiment 2

Hereinafter, a semiconductor device and a method for fabricating the device according to a first modified example of the second embodiment will be described with reference to drawings.

FIG. **12**A is a cross-sectional view (a view showing the cross-sectional structure taken along the line B-B' in FIG. **7**) of a semiconductor device according to this modified example.

The seal ring structure of this modified example shown in FIG. **12**A is different from that of the second embodiment shown in FIG. **8**A in that the cap layer (first cap layer) **225***a* is not provided at the top of the inner seal ring (first seal ring) **204***a*. In other words, the passivation film **209** has no opening on the first seal ring **204***a*.

Specifically, as shown in FIG. **12**A, the semiconductor device of this modified example has a double seal ring structure as in the second embodiment. An outer second seal ring **204***b* in this structure includes a cap layer (second cap layer) **225***b* at its top as in the seal ring structure of the first embodiment shown in FIG. 2A, whereas an inner first seal ring **204***a* does not include a cap layer at its top.

As in the seal ring structure of the second embodiment shown in FIG. **8**A, the first and second seal rings **204***a* and

204*b* of this modified example are formed in a multilayer structure made of a plurality of interlayer dielectric films **205** through **209**. More specifically, first seal vias **221***a* and **221***b* are formed on respective conductive layers **220***a* and **220***b* provided in a substrate **201**, and first seal interconnects **222***a* and **222***b* are formed on the respective first seal vias **221***a* and **221***b*. Second seal vias **223***a* and **223***b* are formed on the respective first seal interconnects **222***a* and **222***b*, and third seal vias **224***a* and **224***b* are formed on the respective second seal vias **223***a* and **223***b*. A passivation film **209** is formed on the third seal via **224***a* and has an opening on the third seal via **224***b*, which is located at the top of the outer second seal ring **204***b*. A cap layer **225***b* connected to the third seal via **224***b* is formed in the opening.

In this modified example, the two seal rings **204***a* and **204***b* are formed to completely surround the chip region **202**. Accordingly, when the semiconductor wafer (substrate) **201** is diced along a scribe region **203** to obtain individual completed semiconductor chips (semiconductor devices), prevention of propagation, to the chip region **202**, of mechanical impact or stress caused by contact of a dicing blade with the scribe line (scribe region) **203** during dicing or prevention of damage to the chip region **202** due to the propagation is further ensured.

In this modified example, the cap layer **225***b* is formed at the top of the outer second seal ring **204***b* and penetrates the passivation film **209**. Accordingly, part of the passivation film **209** in the chip region **202** and part of the passivation film **209** in the scribe region **203** are completely separated from each other by the cap layer **225***b* to be discontinuous. As a result, it is possible to prevent impact on the scribe region **203** during dicing from propagating to the chip region **202**.

Modified Example 2 of Embodiment 2

Hereinafter, a semiconductor device and a method for fabricating the device according to a second modified example of the second embodiment will be described with reference to drawings.

FIG. **12**B is a cross-sectional view (a view showing the cross-sectional structure taken along the line B-B' in FIG. **7**) of a semiconductor device according to this modified example.

The seal ring structure of this modified example shown in FIG. **12**B is different from that of the second embodiment shown in FIG. **8**B in that the cap layer (first cap layer) **225***a* is not provided at the top of the inner seal ring (first seal ring) **204***a*. In other words, the passivation film **209** has no opening on the first seal ring **204***a*. Specifically, the semiconductor device of this modified example has a double seal ring structure as in the second embodiment. An outer second seal ring **204***b* in the structure of this modified example includes a cap layer (second cap layer) **225***b* at its top as in the seal ring structure of the first embodiment shown in FIG. **3**A, whereas an inner first seal ring **204***a* does not include a cap layer at its top.

The seal ring structure of this modified example shown in FIG. **12**B is different from that of the first modified example of the second embodiment shown in FIG. **12**A in that each seal via constituting the seal rings **204***a* and **204***b* has branches.

Specifically, each of first seal vias **221***a* and **221***b* in the first interlayer dielectric film **205** is divided into two branches, i.e., first seal vias **221***a***1** and **221***a***2** or first seal vias **221***b***1** and **221***b***2**, respectively. Likewise, each of second seal vias **223***a* and **223***b* in the third interlayer dielectric film **207** is divided into two branches, i.e., second seal vias **223***a***1** and **223***a***2** or second seal vias **223***b***1** and **223***b***2**, respectively. Each of third seal vias **224***a* and **224***b* in the fourth interlayer dielectric film **208** is divided into two branches, i.e., third seal vias **224***a***1** and **224***a***2** or third seal vias **224***b***1** and **224***b***2**, respectively. A passivation film **209** is formed over the third seal vias **224***a***1** and **224***a***2** whereas the passivation film **209** has an opening on the third seal vias **224***b***1** and **224***b***2**, which are located at the top of the outer second seal ring **204***b*. A cap layer **225***b* connected to the third seal vias **224***b***1** and **224***b***2** is formed in the opening.

In addition to the advantages obtained in the first modified example of the second embodiment shown in FIG. **12**A, the following advantage is obtained in this modified example. That is, since seal vias constituting the seal rings **204***a* and **204***b* have branches, the strength of the seal rings **204***a* and **204***b* is enhanced and the seal rings **204***a* and **204***b* prevent an impurity or moisture from entering the chip region **202** from the outside.

Modified Example 3 of Embodiment 2

Hereinafter, a semiconductor device and a method for fabricating the device according to a third modified example of the second embodiment will be described with reference to drawings.

FIG. **13** is a cross-sectional view (a view showing the cross-sectional structure taken along the line B-B' in FIG. **7**) of a semiconductor device according to this modified example.

The semiconductor device of this modified example shown in FIG. **13** is different from that of the second embodiment shown in FIG. **8**B in that a transistor is provided in part of the substrate **201** in the chip region **202** near the seal rings **204***a* and **204***b*. Specifically, a gate electrode **233** is formed over an area of the substrate **201** surrounded by an isolation **231** with a gate insulating film **232** interposed therebetween. An insulating sidewall **234** is formed on side faces of the gate electrode **233**. An active layer **210** to be source/drain regions is defined in parts of the substrate **201** below the sides of the gate electrode **233**.

The seal ring structure of this modified example shown in FIG. **13** is different from that of the second embodiment shown in FIG. **8**B in that each of the first seal vias **221***a* and **221***b* in the first interlayer dielectric film **205** in which the transistor is formed is divided into two first seal vias **221***a***1** and **221***a***2** or two first seal vias **221***b***1** an **221***b***2**, respectively. As in the seal ring structure of the first modified example of the second embodiment shown in FIG. **12**A, the cap layer (first cap layer) **225***a* is not provided on an inner seal ring (first seal ring) **204***a*. In other words, a passivation film **209** does not have an opening on the first seal ring **204***a*.

With recent reduction in chip size, the distance from a portion of a wafer at which the wafer is diced (i.e., a scribe region) to the transistor closest to this portion (hereinafter, referred to as a nearest transistor) has decreased. Specifically, in a conventional device in which no element is provided under a pad, the distance from a seal ring to the nearest transistor (corresponding to distance L in FIG. **13**) is approximately 100 μm. On the other hand, such a layout that an element is provided under a pad has been employed in recent years, and the distance L from a seal ring to the nearest transistor has been reduced to approximately 10 μm accordingly. As a result, impact during dicing easily propagates to the transistor so that the transistor is readily damaged. On the other hand, since the transistor has a miniaturized structure including a thin gate oxide film and others,

the transistor is vulnerable to impact. Therefore, transistors need to have protection especially against damage during dicing.

In view of this, in this modified example, the "seal via structure having two or more branches" described above is employed to enhance the strength of the seal ring structure of a transistor layer. Specifically, each of the first seal vias **221***a* and **221***b* constituting the seal rings **204***a* and **204***b* is divided into two branches in the dielectric film as the bottom layer on the substrate **201**, i.e., the first interlayer dielectric film **205** as a transistor layer including the gate electrode **233** and others, so that each of the branches, i.e., the seal vias **221***a***1**, **221***a***2**, **221***b***1** and **221***b***2**, serves as a barrier against impact on the bottom layer in the chip region **202**. In this manner, damage to a transistor during dicing is prevented, thus enhancing the yield in manufacturing semiconductor devices.

In this modified example, the "seal via structure having two or more branches" is used in a layer in which a miniaturized transistor is provided. Alternatively, the "seal via structure having two or more branches" may be used in a miniaturized layer or a layer having a miniaturized structure.

Embodiment 3

Hereinafter, a semiconductor device and a method for fabricating the device according to a third embodiment of the present invention will be described with reference to drawings. In this embodiment, variations of the first and second embodiments will be described.

FIG. **14**A is a view schematically showing a cross-sectional structure of the conventional semiconductor device shown in FIG. **19**. FIG. **14**A shows peripheral parts of two chip regions **2** sandwiching the scribe region **3**. In FIG. **14**A, some components are not shown and components also shown in FIG. **19** are denoted by the same reference numerals, and the description thereof will be omitted. As shown in FIG. **14**A, accessory interconnects **40** are provided in the interlayer dielectric films **8** and **10** in the scribe region **3**.

FIG. **14**B is a plan view corresponding to the structure shown in FIG. **14**A. In FIG. **14**B, seal rings **4** under the passivation film **11** are schematically represented by bold broken lines. As shown in FIG. **14**B, in the conventional semiconductor device, the seal rings **4** are provided in the shape of lines along the scribe region **3**.

FIG. **15**A is a view schematically showing a cross-sectional structure of the semiconductor device of the first embodiment shown in FIG. **2**A. FIG. **15**A shows peripheral parts of two chip regions **102** sandwiching the scribe region **103**. In FIG. **15**A, some components are not shown and components also shown in FIG. **2**A are denoted by the same reference numerals, and the description thereof will be omitted. As shown in FIG. **15**A, accessory interconnects **140** are provided in the interlayer dielectric films **107** and **108** in the scribe region **103**.

FIG. **15**B is a plan view corresponding to the structure shown in FIG. **15**A. In FIG. **15**B, the seal rings **104** including the cap layers **125** at their tops are schematically represented by bold solid lines. As shown in FIG. **15**B, in the semiconductor device of the first embodiment, the seal rings **104** are provided in the shape of lines along the scribe region **103**.

FIGS. **16**A through **16**C show planar structures of variations of the semiconductor device of the third embodiment, in comparison with the planar structure of the conventional semiconductor device shown in FIG. **14**B and the planar structure of the semiconductor device of the first embodiment shown in FIG. **15**B. In FIGS. **16**A through **16**C, the seal rings **104** are also schematically represented by bold solid lines.

The planar structure shown in FIG. **16**A is characterized in that each of the seal rings **104** is in the shape of a rectangular wave when viewed from above the substrate **101** (i.e., the passivation film **109**).

The planar structure shown in FIG. **16**B is characterized in that each of the seal rings **104** is in the shape of a triangular wave when viewed from above the substrate **101**.

The planar structure shown in FIG. **16**C is characterized in that a plurality of projections extend toward the scribe region **103** from a side of each of the seal rings **104**. Specifically, each of the seal rings **104** has a plurality of projections extending vertically to the direction in which the scribe region **103** runs.

The cross-sectional structures of the semiconductor devices associated with the respective structures shown in FIGS. **16**A through **16**C are similar to that of the first embodiment shown in FIG. **15**A or **2**A except that the position of the seal rings **104** shifts horizontally or the width of the seal rings **104** changes depending on the position at which the cross-sectional structure is observed.

Methods for fabricating the respective semiconductor devices associated with FIGS. **16**A through **16**C are similar to that of the first embodiment (shown in FIGS. **4**A through **4**D, **5**A through **5**C and **6**A through **6**C) except that mask patterns for forming seal rings differ among FIGS. **16**A through **16**C.

In the semiconductor device having a seal ring structure of this embodiment shown in any one of FIGS. **16**A through **16**C, the seal rings **104** serving as barriers for protecting the chip regions **102** are provided not only in the direction parallel to the direction in which the scribe region **103** runs but also in a direction vertical or diagonal to that direction. Accordingly, it is possible to prevent impact and stress caused by contact of a dicing blade with a film such as the passivation film **109** during dicing and cracks and the like occurring in the wafer (substrate **101**) by the impact and stress, from propagating along the sides (the sides facing the scribe region **103**) of the seal rings **104**.

FIG. **17**A is a view schematically showing a cross-sectional structure of the semiconductor device of the second embodiment shown in FIG. **8**A. FIG. **17**A shows peripheral parts of two chip regions **202** sandwiching the scribe region **203**. In FIG. **17**A, some components are not shown and components also shown in FIG. **8**A are denoted by the same reference numerals, and the description thereof will be omitted. As shown in FIG. **17**A, accessory interconnects **240** are provided in the interlayer dielectric films **207** and **208** in the scribe region **203**.

FIG. **17**B is a plan view corresponding to the structure shown in FIG. **17**A. In FIG. **17**B, the seal rings **204***a* and **204***b* including the cap layers **225***a* and **225***b* at their tops are schematically represented by bold solid lines. As shown in FIG. **17**B, in the semiconductor device of the second embodiment, the seal rings **204***a* and **204***b* are provided in the shape of two lines along the scribe region **203**.

FIGS. **18**A through **18**C show planar structures of variations of the semiconductor device of this embodiment, in comparison with the planar structure of the semiconductor device of the second embodiment shown in FIG. **17**B. In FIGS. **18**A through **18**C, the seal rings **204***a* and **204***b* are also schematically represented by bold solid lines.

The planar structure shown in FIG. **18**A is characterized in that each of the seal rings **204***b* near the scribe region **203** is in shape of a rectangular wave when viewed from above the substrate **201** (i.e., the passivation film **209**).

The planar structure shown in FIG. **18**B is characterized in that each of the seal rings **204***b* near the scribe region **203** is in the shape of a triangular wave when viewed from above the substrate **201**.

The planar structure shown in FIG. **18**C is characterized in that a plurality of projections extend toward the scribe region **203** from a side of each of the seal rings **204***b* near the scribe region **203**. Specifically, each of the seal rings **204***b* has a plurality of projections extending vertically to the direction in which the scribe region **203** runs.

The cross-sectional structures of the semiconductor devices associated with the respective structures shown in FIGS. **18**A through **18**C are similar to that of the second embodiment shown in FIG. **17**A or **8**A except that the position of the seal rings **204***b* shifts horizontally or the width of the seal rings **204***b* changes depending on the position at which the cross-sectional structure is observed.

Methods for fabricating the respective semiconductor devices associated with FIGS. **18**A through **18**C are similar to that of the second embodiment (shown in FIGS. **9**A through **9**D and **10**A through **10**C) except that mask patterns for forming seal rings differ among FIGS. **18**A through **18**C.

In the semiconductor device with a seal ring structure of this embodiment shown in any one of FIGS. **18**A through **18**C, the following advantage is obtained in addition to the advantages of the second embodiment obtained by the double seal ring structure. That is, the seal rings **204***b* near the scribe region **203** out of the seal rings **204***a* and **204***b* serving as barriers for protecting the chip regions **202** are provided not only in the direction parallel to the direction in which the scribe region **203** runs but also in a direction vertical or diagonal to that direction. Accordingly, it is possible to prevent impact and stress caused by contact of a dicing blade with a film such as the passivation film **209** during dicing and cracks and the like occurring in the wafer (substrate **201**) by the impact and stress, from propagating along the sides (the sides facing the scribe region **203**) of the respective seal rings **204***b*.

In the seal ring structures (double structures) of this embodiment shown in FIGS. **18**A through **18**C, the seal rings **204***a* in the shape of lines in a plan view and the seal rings **204***b* in a shape other than the line shape in the plan view are combined. Alternatively, the seal rings **204***a* and **204***b* may be in the same shape or in different shapes other than the line shape in a plan view. Alternatively, a seal ring structure which includes three or more seal rings and in which at least the outermost seal ring is in a shape other than the line shape in a plan view may be used. However, if the seal ring structure includes seal rings in a shape/shapes other than the line shape in a plan view or includes three or more seal rings, the widths of the seal rings occupy a large part of the width of a semiconductor device (i.e., semiconductor chip), so that this structure might be disadvantageous in miniaturization of semiconductor devices. Therefore, it is preferable to use a double seal ring structure in which a seal ring in the shape of a line in a plan view and a seal ring in a shape other than the line shape in the plan view are combined, as the seal ring structures of this embodiment shown in FIGS. **18**A through **18**C, respectively.

As described above, in the foregoing embodiments of the present invention, a seal via constituting a seal ring and a dual damascene interconnect structure in a chip region are formed through an interlayer dielectric film by the same process and the seal via is continuous in the film. Therefore, the seal via penetrates the interlayer dielectric film without a "junction". Accordingly, the number of "junctions" is reduced in the entire seal ring structure. This further prevents an impurity or the like from entering through "junctions", as compared to a seal ring structure including a large number of "junctions". As a result, the strength of the seal ring structure is enhanced. That is, it is possible to prevent impact from propagating into a chip region during dicing. In addition, it is also possible to prevent an impurity or the like from entering the chip region from the outside.

In the foregoing embodiments of the present invention, the structure in which a cap layer is provided at the top of a seal ring, the structure in which a seal via constituting a seal ring is divided into branches, the structure in which a seal via is formed simultaneously with formation of a dual damascene structure in a chip region, and the structure in which a plurality of seal rings surround a chip region, are used. These structures further ensure prevention of damage to a chip region or prevention of damage to part of the chip region when a wafer is diced into chips along a scribe region. Accordingly, it is possible to prevent impact on the scribe region during dicing from propagating into the chip region, so that an IC, interconnect layers and others in the chip region are not damaged. As a result, the yield in manufacturing semiconductor devices (chips) is enhanced and high-precision chips are obtained.

In the foregoing embodiments of the present invention, a seal ring structure is provided in a peripheral part of a chip region (part of the chip region near the boundary between the chip region and the scribed region.) Alternatively, the seal ring structure may be provided in part of the scribed region (part of the scribe region near the boundary between the scribed region and the chip region) which will remain as an end portion of a semiconductor device (semiconductor chip) after dicing.

What is claimed is:

1. A semiconductor device, comprising:
- a substrate including a chip region;
- a plurality of dielectric films formed on the substrate;
- seal rings formed in a peripheral part of a chip region, the seal rings including a first seal ring and a second seal ring, the first seal ring surrounding the second seal ring, the first seal ring and the second seal ring both provided through at least one of the plurality of dielectric films in the peripheral part of the chip region;
- a protection film formed on a first dielectric film, the first dielectric film being an uppermost film among the plurality of dielectric films;
- a cap layer having a convex shape, the cap layer having an upper portion and a lower portion which is narrower than the upper portion; and
- an interconnect formed in the first dielectric film in the chip region, wherein
- the first seal ring has a plurality of seal components, an uppermost seal component among the plurality of seal components disposed in the first dielectric film, the uppermost seal component having a first side surface and a second side surface which is located outside the first side surface when viewed from above,
- the cap layer disposed on the uppermost seal component, the upper portion of the cap layer has a first bottom surface and a second bottom surface which is located outside the first bottom surface when viewed from above,

the lower portion of the cap layer has a first side surface and a second side surface which is located outside the first side surface when viewed from above, and

a connecting point which connects the second bottom surface of the upper portion and the second side surface of the lower portion is located outside the second side surface of the uppermost seal component when viewed from above.

2. The semiconductor device of claim **1**, wherein the upper portion of the cap layer has a first side surface and a second side surface which is located outside the first side surface of the upper portion when viewed from above, and

the first and second side surfaces of the upper portion are not covered by the protection film.

3. The semiconductor device of claim **1**, wherein the second seal ring has a plurality of seal components, an uppermost seal component among the plurality of seal components disposed in the first dielectric film, the uppermost seal component of the second seal ring having a top surface which is entirely covered by the protection film.

4. The semiconductor device of claim **3**, wherein any other seal ring is not disposed between the first seal ring and the second seal ring.

5. The semiconductor device of claim **1**, wherein the second bottom surface of the upper portion is located outside the second side surface of the uppermost seal component when viewed from above.

6. The semiconductor device of claim **1**, wherein a distance from an upper surface of the uppermost seal component to the substrate is substantially equal to a distance from an upper surface of the interconnect to the substrate.

7. The semiconductor device of claim **1**, wherein a thickness of the cap layer in a depth direction at a center of the cap layer is larger than a thickness of the protection film in the depth direction.

8. The semiconductor device of claim **1**, wherein a thickness of the lower portion of the cap layer, in a depth direction, is equal to or greater than a thickness of the protection film in the depth direction.

9. The semiconductor device of claim **1**, wherein the uppermost seal component is made of at least one of W, Al and Cu.

10. The semiconductor device of claim **9**, wherein the uppermost seal component is made of Cu.

11. The semiconductor device of claim **1**, wherein the cap layer is made of Al.

12. A semiconductor device, comprising:

a substrate including a chip region;

a plurality of dielectric films formed on the substrate;

seal rings formed in a peripheral part of a chip region, the seal rings including a first seal ring and a second seal ring, the first seal ring surrounding the second seal ring, the first seal ring and the second seal ring both provided through at least one of the plurality of dielectric films in the peripheral part of the chip region;

a protection film formed on a first dielectric film, the first dielectric film being an uppermost film among the plurality of dielectric films;

a cap layer having a convex shape, the cap layer having an upper portion and a lower portion which is narrower than the upper portion; and

an interconnect formed in the first dielectric film in the chip region, wherein

the first seal ring has a plurality of seal components, an uppermost seal component among the plurality of seal components disposed in the first dielectric film, the uppermost seal component having a first side surface and a second side surface which is located outside the first side surface when viewed from above,

the cap layer disposed on the uppermost seal component, the upper portion of the cap layer has a first side surface and a second side surface which is located outside the first side surface when viewed from above,

the second side surface of the upper portion is located outside the second side surface of the uppermost seal component when viewed from above,

the uppermost seal component is made of Cu and,

the cap layer is made of Al.

13. The semiconductor device of claim **12**, wherein the lower portion of the cap layer has a bottom surface, and

the second side surface of the uppermost seal component is covered by the bottom surface of the lower portion.

14. The semiconductor device of claim **12**, wherein the first and second side surfaces of the upper portion are not covered by the protection film.

15. The semiconductor device of claim **12**, wherein the second seal ring has a plurality of seal components, an uppermost seal component among the plurality of seal components disposed in the first dielectric film, the uppermost seal component of the second seal ring having a top surface which is entirely covered by the protection film.

16. The semiconductor device of claim **15**, wherein any other seal ring is not disposed between the first seal ring and the second seal ring.

17. The semiconductor device of claim **12**, wherein the upper portion of the cap layer has a first bottom surface and a second bottom surface which is located outside the first bottom surface when viewed from above, and

the second bottom surface of the upper portion is located outside the second side surface of the uppermost seal component when viewed from above.

18. The semiconductor device of claim **12**, wherein a distance from an upper surface of the uppermost seal component to the substrate is substantially equal to a distance from an upper surface of the interconnect to the substrate.

19. The semiconductor device of claim **12**, wherein a thickness of the cap layer in a depth direction at a center of the cap layer is larger than a thickness of the protection film in the depth direction.

20. The semiconductor device of claim **12**, wherein a thickness of the lower portion of the cap layer, in a depth direction, is equal to or greater than a thickness of the protection film in the depth direction.

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