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**Chen et al.**

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(54) **MECHANISMS FOR FORMING  
POST-PASSIVATION INTERCONNECT  
STRUCTURE**

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See application file for complete search history.

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,906,312 A \* 5/1999 Zakel ..... *H01L* 24/11  
228/208  
6,283,359 B1 \* 9/2001 Brofman ..... B23K 35/0222  
228/180.21

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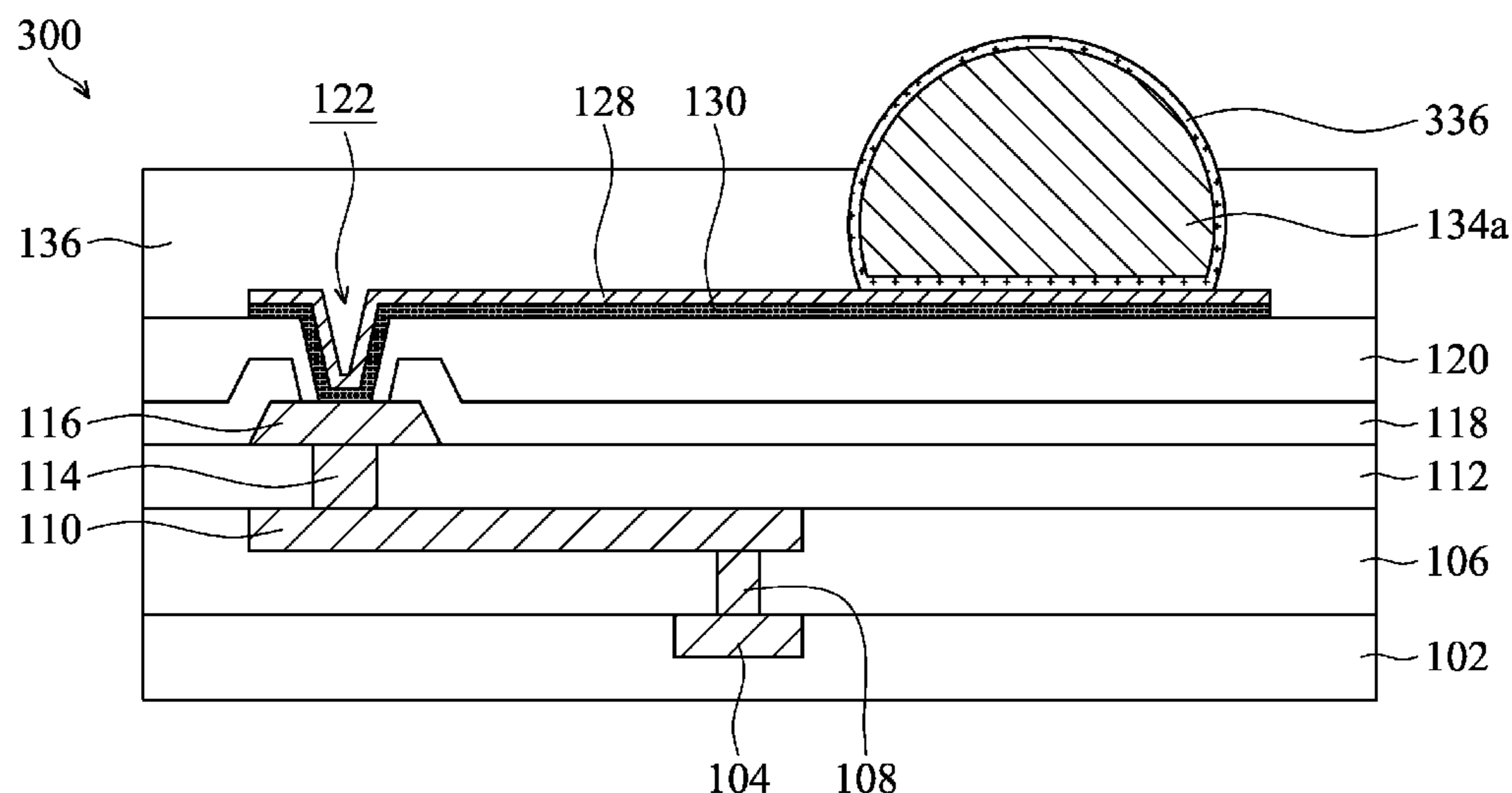
(57) **ABSTRACT**

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23/53238 (2013.01); *H01L* 24/03 (2013.01);  
*H01L* 24/05 (2013.01); *H01L* 23/3114  
(2013.01); *H01L* 23/525 (2013.01); *H01L*  
24/11 (2013.01); *H01L* 2224/0345 (2013.01);  
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Embodiments of mechanisms for forming a semiconductor device are provided. The semiconductor device includes a contact pad over a substrate. The semiconductor device also includes a passivation layer over the substrate and a first portion of the contact pad, and a second portion of the contact pad is exposed through an opening. The semiconductor device further includes a post-passivation interconnect layer over the passivation layer and coupled to the second portion of the contact pad. In addition, the semiconductor device includes a bump over the post-passivation interconnect layer and outside of the opening. The semiconductor device also includes a diffusion barrier layer physically insulating the bump from the post-passivation interconnect layer while electrically connecting the bump to the post-passivation interconnect layer.

**20 Claims, 10 Drawing Sheets**



(51)	<p><b>Int. Cl.</b>  <b>H01L 21/768</b> (2006.01)  <b>H01L 23/522</b> (2006.01)  <b>H01L 23/532</b> (2006.01)  <b>H01L 23/525</b> (2006.01)</p>	<p>2002/0020855 A1* 2/2002 Hwang ..... 257/200                  2002/0025585 A1* 2/2002 Lam et al. .... 438/1                  2003/0164552 A1* 9/2003 Tong et al. .... 257/779                  2004/0065949 A1* 4/2004 Chen ..... H01L 24/10                  257/692                  2004/0115340 A1* 6/2004 Griego ..... H01F 41/16                  174/126.2                  2005/0062169 A1* 3/2005 Dubin ..... H01L 21/288                  257/779                  2005/0087885 A1* 4/2005 Jeong ..... H01L 23/49811                  257/778                  2005/0167799 A1* 8/2005 Doan ..... H01L 21/568                  257/678                  2005/0205993 A1* 9/2005 Yamaguchi ..... H01L 23/3114                  257/738                  2006/0204650 A1* 9/2006 Hu ..... C23C 26/00                  427/96.1                  2007/0028445 A1* 2/2007 Su ..... H01L 24/11                  29/840                  2007/0045869 A1* 3/2007 Ho ..... H01L 21/563                  257/780                  2007/0075410 A1* 4/2007 Chan ..... H01L 21/563                  257/678                  2007/0252275 A1* 11/2007 Huang et al. .... 257/737                  2009/0014869 A1* 1/2009 Vrtis et al. .... 257/737                  2009/0174071 A1* 7/2009 Chao ..... H01L 24/11                  257/737                  2010/0013100 A1* 1/2010 Xiao ..... H01L 23/53238                  257/751                  2010/0096754 A1* 4/2010 Lee ..... H01L 21/568                  257/738                  2010/0155115 A1* 6/2010 Pang et al. .... 174/257                  2011/0304029 A1* 12/2011 Sogawa ..... H01L 24/03                  257/632                  2013/0075907 A1* 3/2013 Pang ..... H01L 24/11                  257/741                  2013/0147031 A1* 6/2013 Chen et al. .... 257/737                  2013/0193570 A1* 8/2013 Kuo ..... H01L 24/11                  257/737</p>
(52)	<p><b>U.S. Cl.</b>                  CPC ..... <i>H01L 2224/05124</i> (2013.01); <i>H01L 2224/05147</i> (2013.01); <i>H01L 2224/05166</i> (2013.01); <i>H01L 2224/05186</i> (2013.01); <i>H01L 2224/05569</i> (2013.01); <i>H01L 2224/05583</i> (2013.01); <i>H01L 2224/05655</i> (2013.01); <i>H01L 2224/05681</i> (2013.01); <i>H01L 2224/05686</i> (2013.01); <i>H01L 2224/11</i> (2013.01); <i>H01L 2224/11334</i> (2013.01); <i>H01L 2224/13022</i> (2013.01); <i>H01L 2224/13024</i> (2013.01); <i>H01L 2224/13111</i> (2013.01); <i>H01L 2224/13113</i> (2013.01); <i>H01L 2224/13116</i> (2013.01); <i>H01L 2224/13139</i> (2013.01); <i>H01L 2224/13147</i> (2013.01); <i>H01L 2224/13155</i> (2013.01); <i>H01L 2224/13561</i> (2013.01); <i>H01L 2224/13611</i> (2013.01); <i>H01L 2224/13613</i> (2013.01); <i>H01L 2224/13616</i> (2013.01); <i>H01L 2224/13639</i> (2013.01); <i>H01L 2224/13647</i> (2013.01); <i>H01L 2224/13655</i> (2013.01); <i>H01L 2224/13681</i> (2013.01); <i>H01L 2224/13686</i> (2013.01); <i>H01L 2924/181</i> (2013.01)</p>	
(56)	<p align="center"><b>References Cited</b></p> <p align="center">U.S. PATENT DOCUMENTS</p> <p>6,337,445 B1* 1/2002 Abbott ..... H01L 23/49816                  174/257                  7,829,453 B2* 11/2010 Jungnickel ..... H01L 24/11                  438/612                  8,058,726 B1* 11/2011 Jin et al. .... 257/738                  8,701,281 B2* 4/2014 Sidhu ..... H05K 3/3489                  174/255</p>	

\* cited by examiner

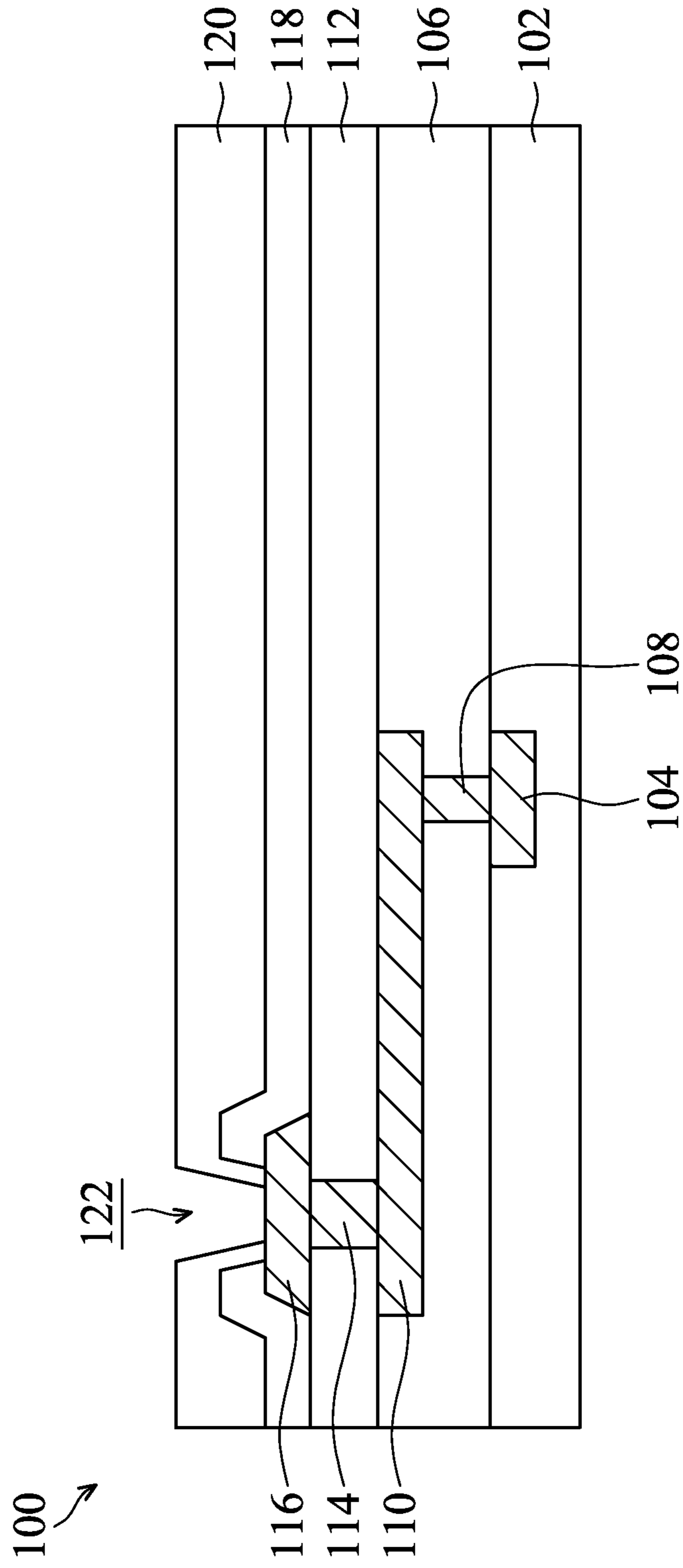


FIG. 1A

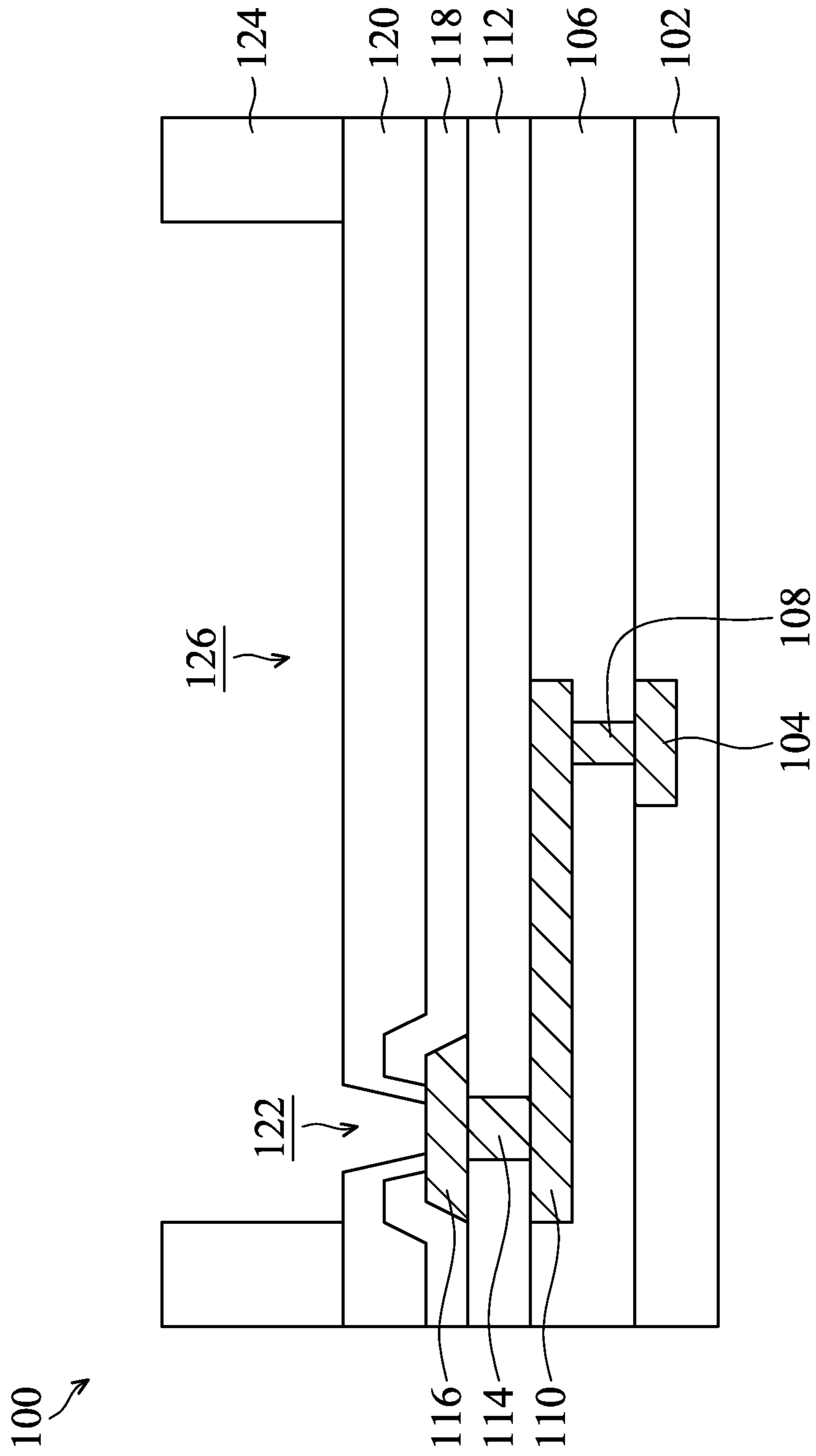


FIG. 1B

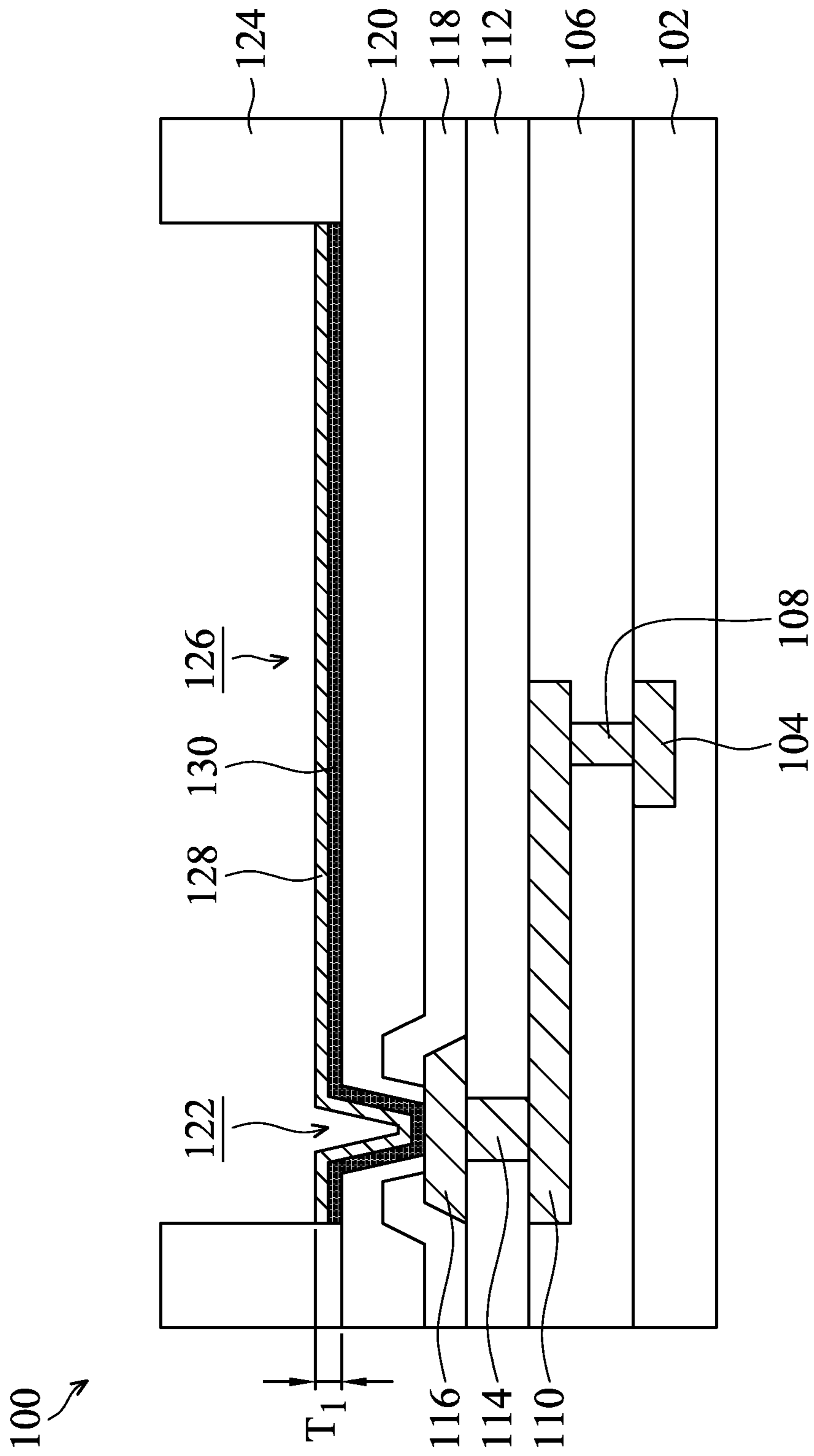


FIG. 1C

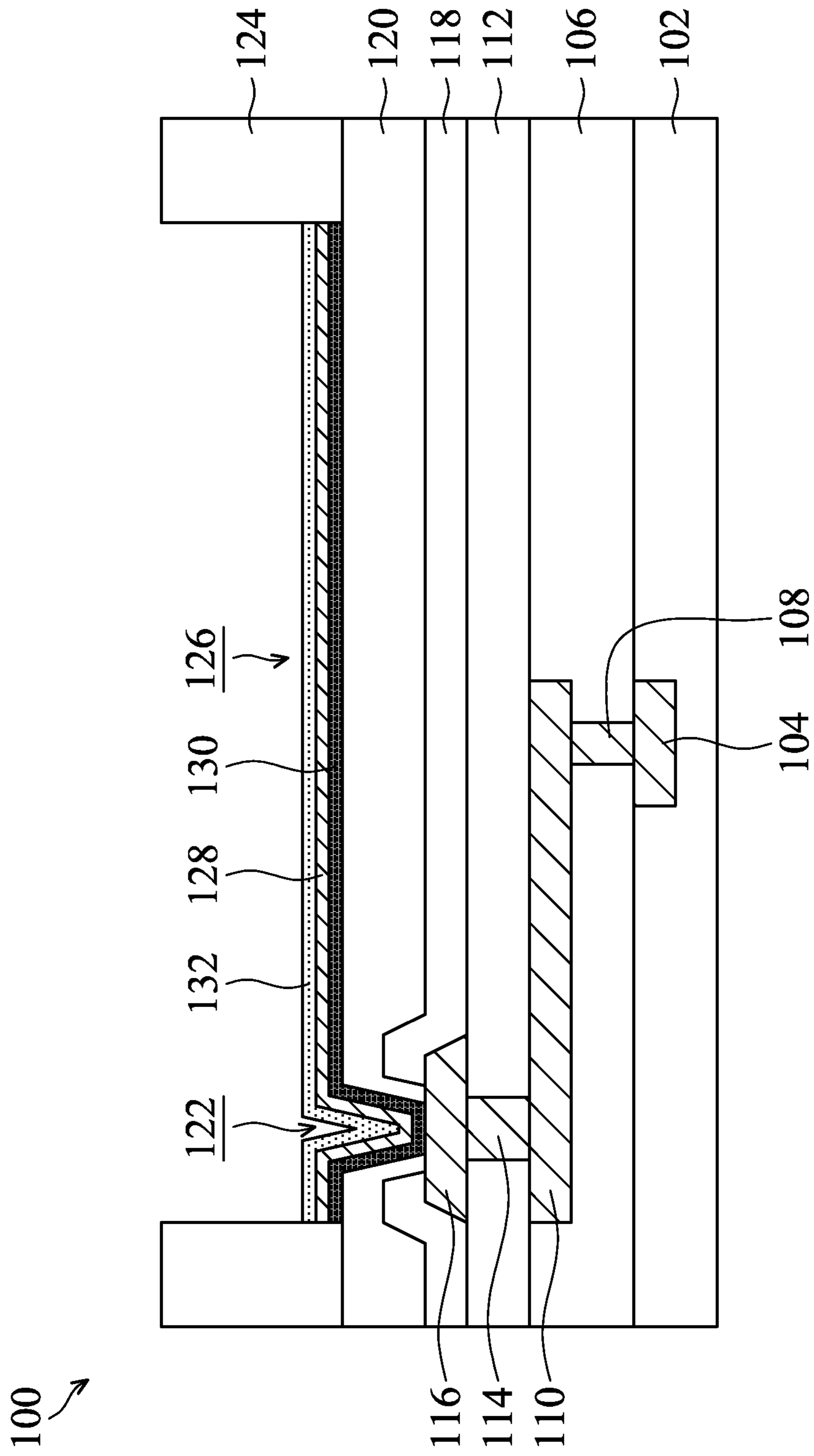


FIG. 1D

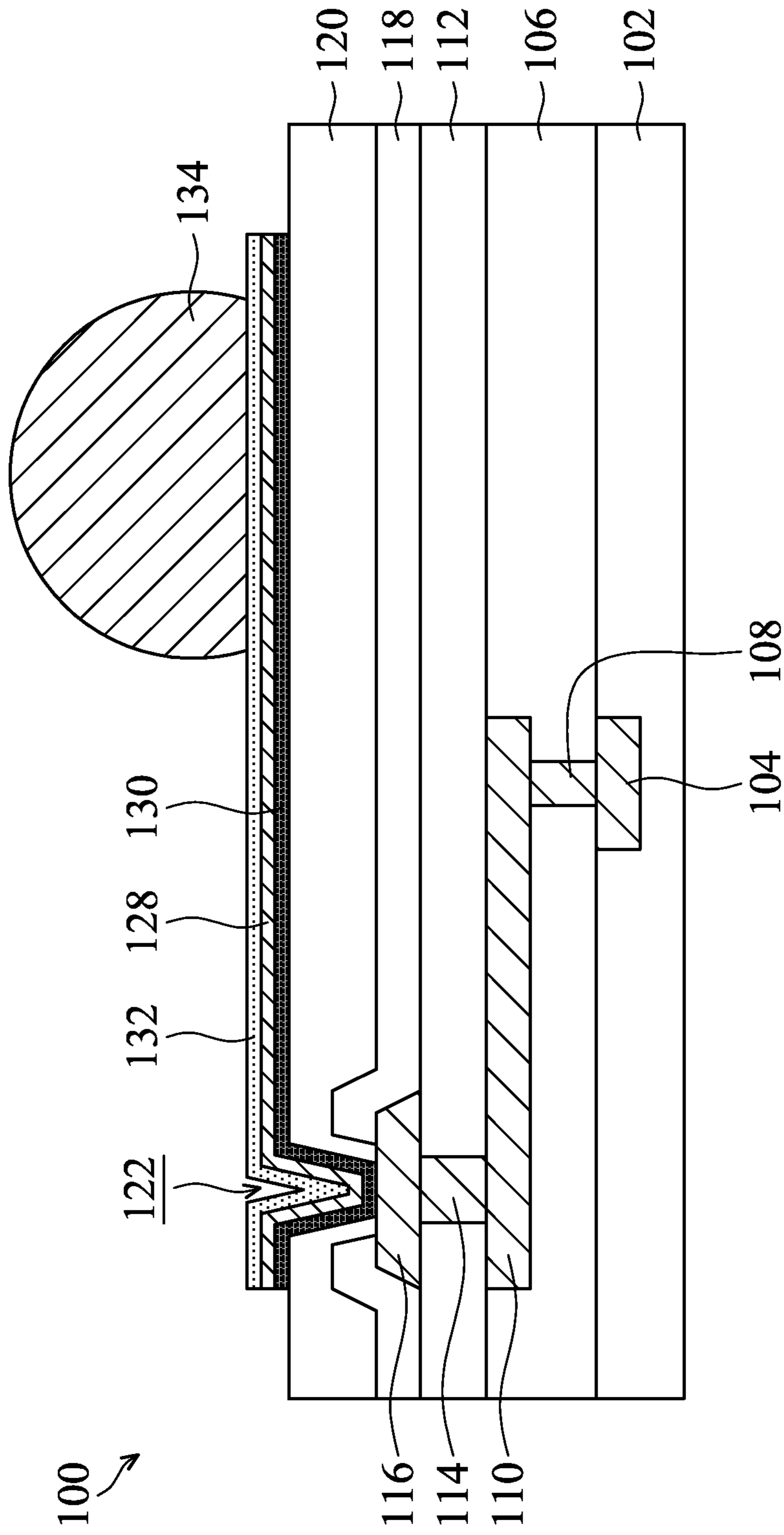


FIG. 1E

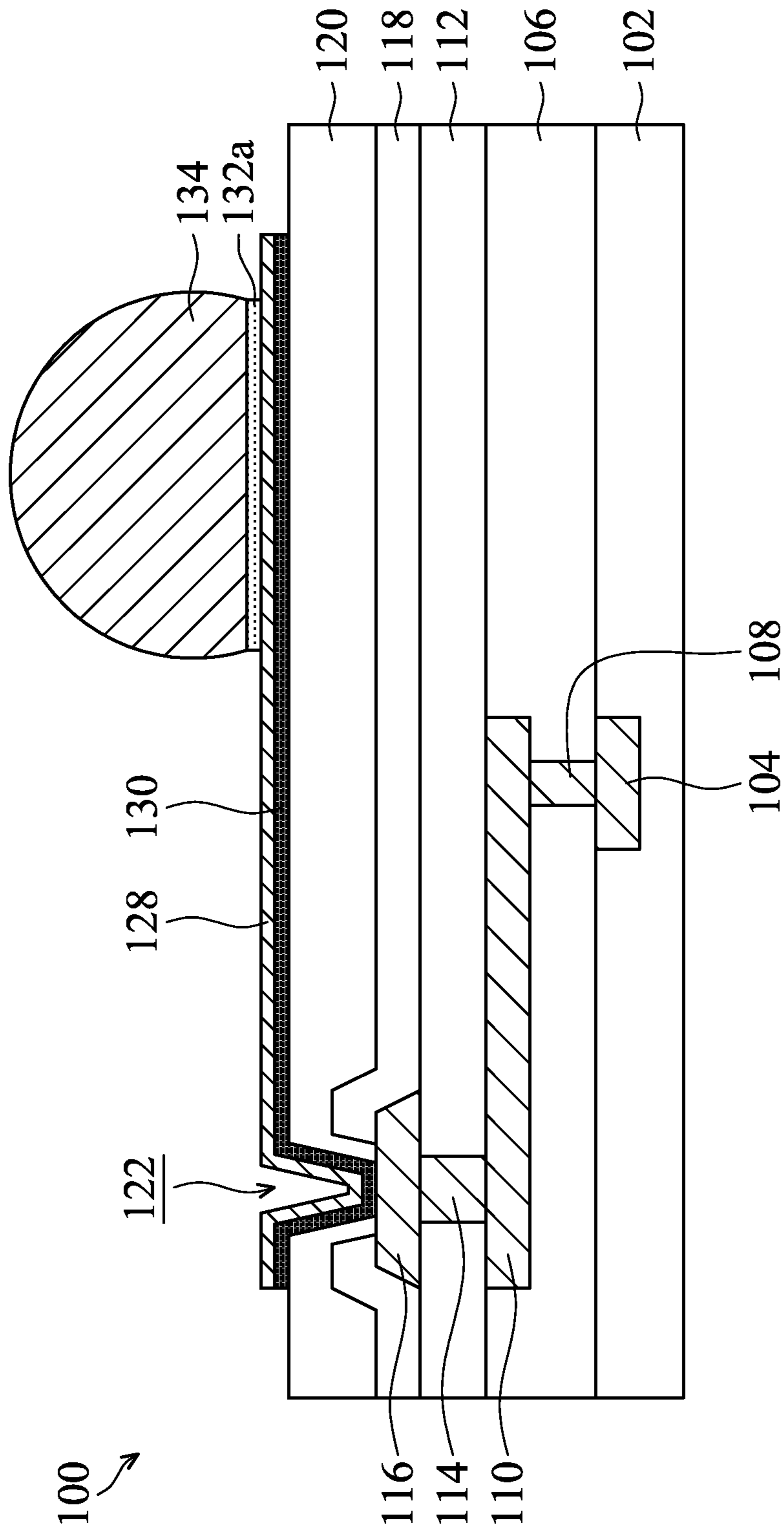


FIG. 1F



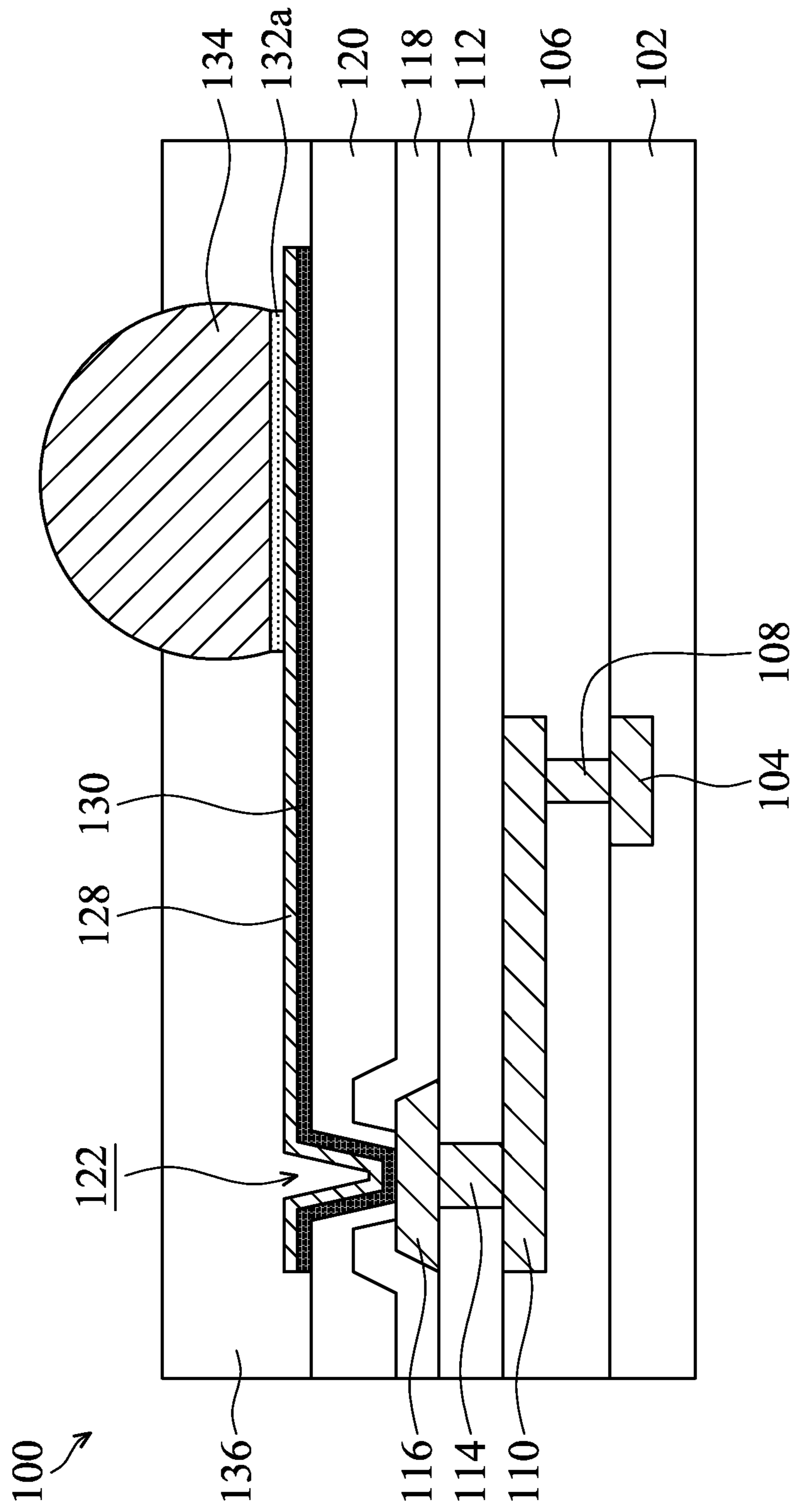


FIG. 1G

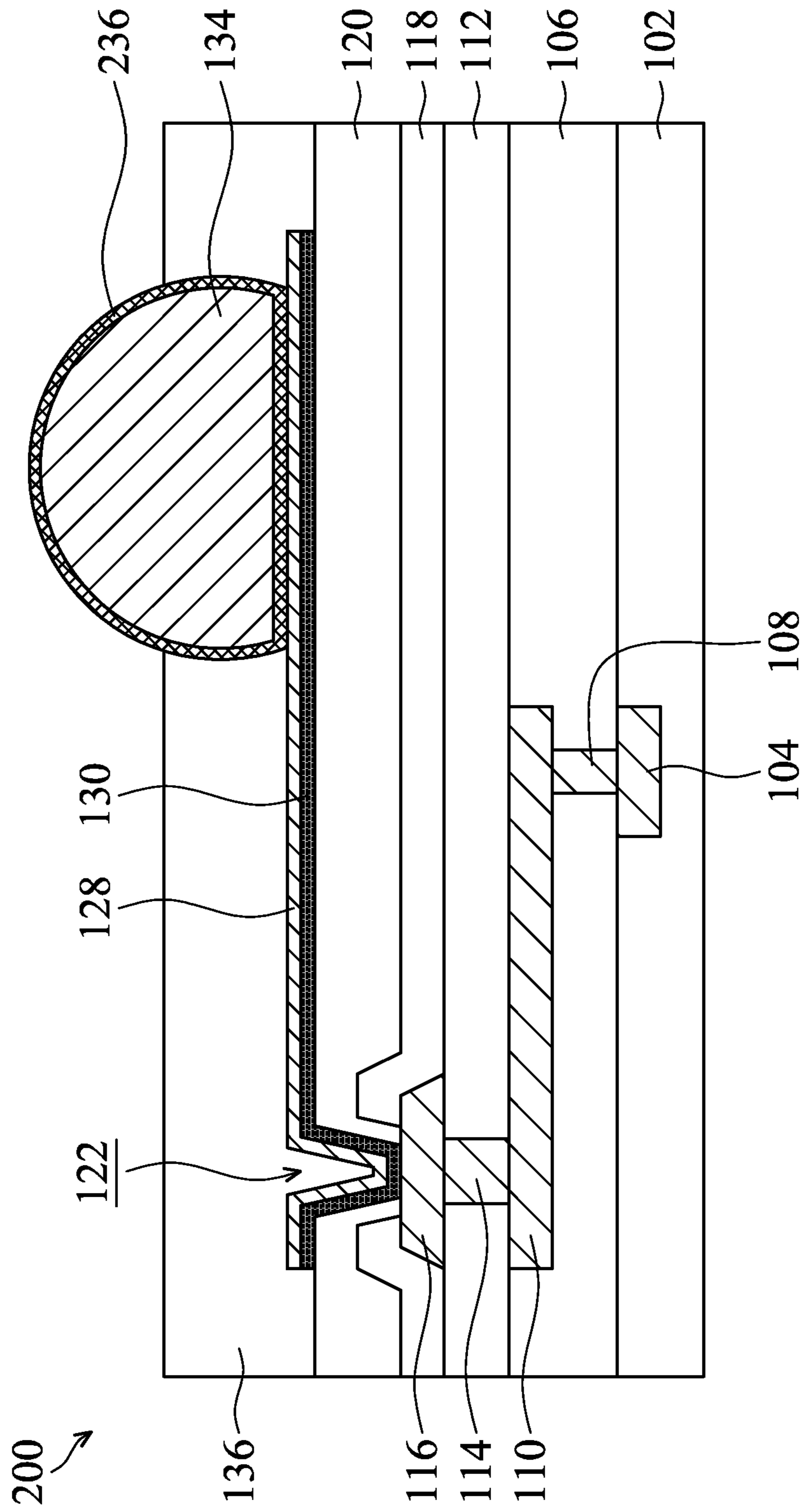


FIG. 2

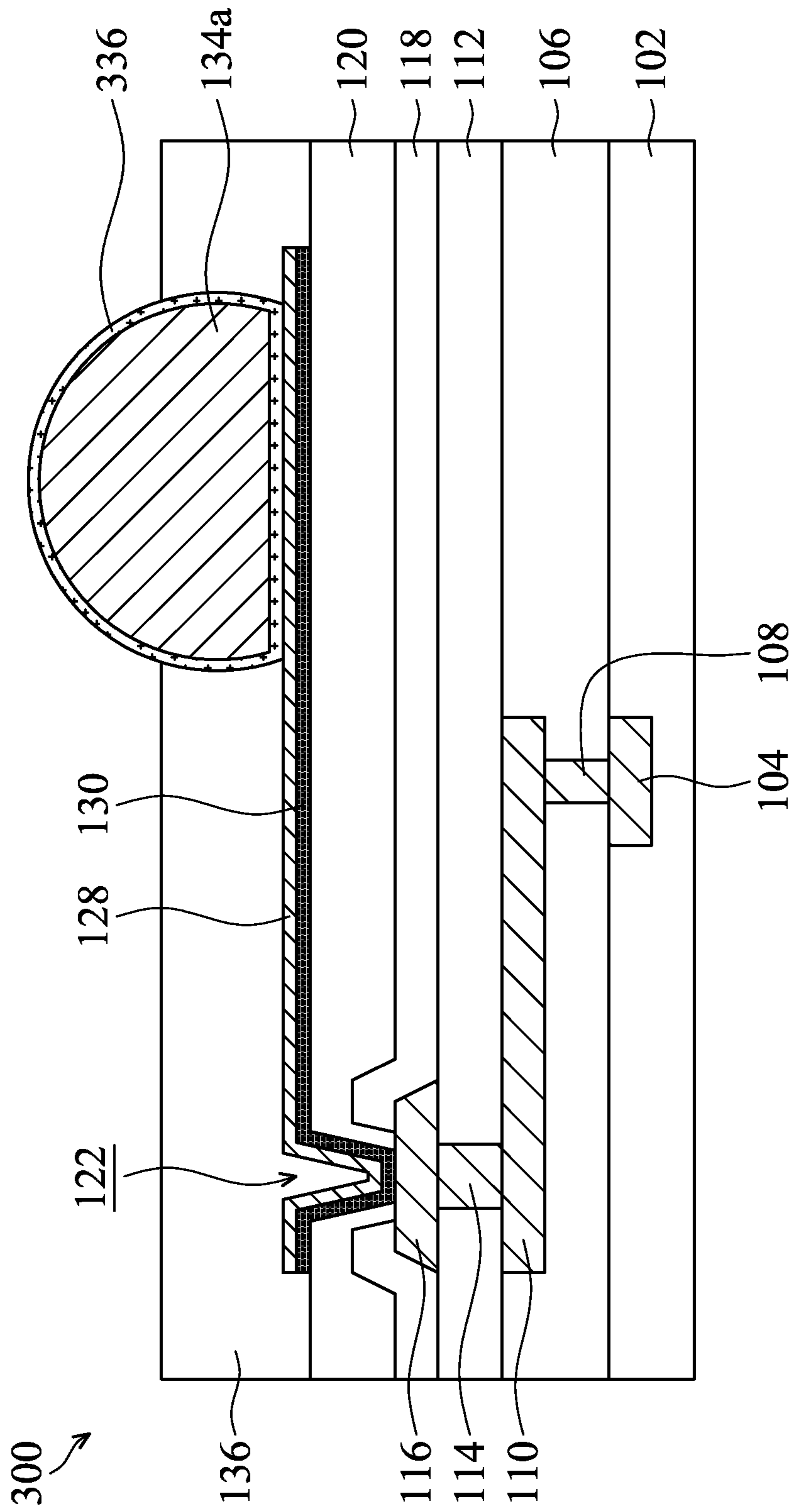


FIG. 3

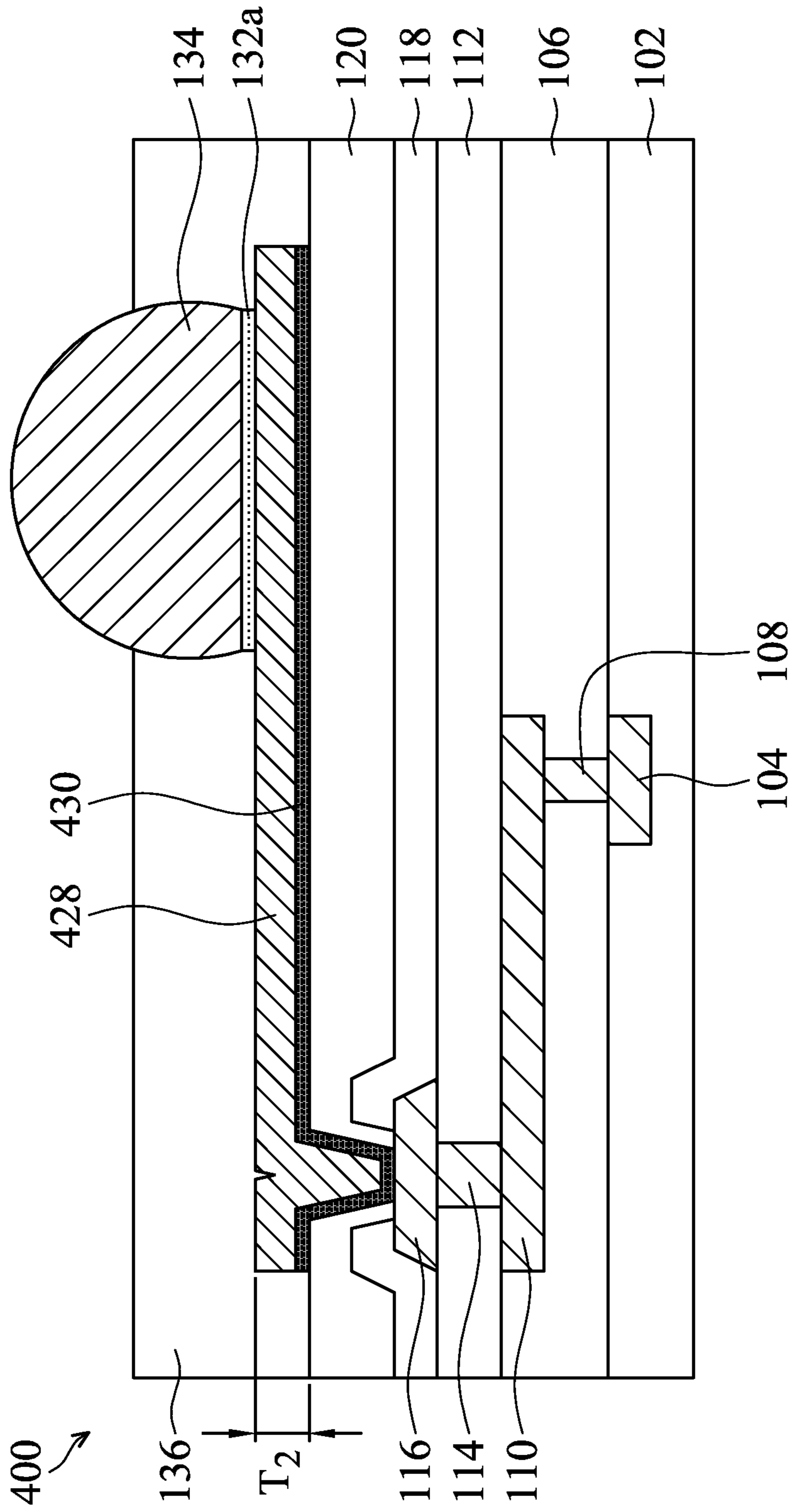


FIG. 4

## MECHANISMS FOR FORMING POST-PASSIVATION INTERCONNECT STRUCTURE

### BACKGROUND

The packaging of integrated circuit (IC) chips is one important step in the manufacturing process. The packaging of an IC chip has two main purposes: to protect delicate semiconductor chips, and to connect interior integrated circuits to exterior connections. As semiconductor devices reach higher levels of integration, especially for 3D IC technology, packaging of an IC chip accounts for a considerable portion of the cost of producing the device, and failure of the package leads to costly yield reduction.

Several packaging technologies are available. For example, a wire bonding technology uses upward-facing chips with wires connected to each pad on the chip. In flip chip technology, a flip chip microelectronic assembly includes a direct electrical connection of a downward-facing (that is “flipped”) chip onto an interposer or a substrate, using solder bumps as interconnects. The use of flip chip packaging has dramatically grown as a result of the advantages in size, performance, flexibility, reliability, and cost over other packaging methods.

### BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

FIG. 1A-1G illustrate cross-sectional views of a semiconductor device at various stages of manufacturing, in accordance with some embodiments.

FIGS. 2-4 illustrate cross-sectional views of semiconductor devices, in accordance with alternative embodiments.

### DETAILED DESCRIPTION

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Moreover, the performance of a first process before a second process in the description that follows may include embodiments in which the second process is performed immediately after the first process, and may also include embodiments in which additional processes may be performed between the first and second processes. Various features may be arbitrarily drawn in different scales for the sake of simplicity and clarity. Furthermore, the formation of a first feature over or on a second feature in the description may include embodiments in which the first and second features are formed in direct or indirect contact.

Some variations of the embodiments are described. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. It is understood that additional steps can be provided before,

during, and after the method, and some of the steps described can be replaced or eliminated for other embodiments of the method.

Flip chips may be made by placing one or more solder bumps on a chip. A post-passivation interconnect (hereinafter referred to as PPI) layer, which is formed of a conductive material, is formed under the solder bump and extending to connect to other components in the chip. It has been discovered that the conductive material of the PPI layer may diffuse to the solder bumps and react with the solder material, forming intermetallic compounds. As such, voids may be formed, and a thickness of the PPI layer is decreased. The diffusion circumstance is particularly serious at a current crowding site. For example, the current crowding site is oftentimes at or adjacent to corners of the solder bump and an interface of the solder bump and the PPI layer. The formation of the voids and the reduced thickness of the PPI layer may increase risks of bump crack and an interruption of the PPI layer. In addition, the formation of the intermetallic compound may also reduce the conductivity of the solder bump.

FIGS. 1A-1G illustrate cross-sectional views of a semiconductor device at various stages of manufacturing processes, in accordance with some embodiments. Referring to FIG. 1A, a substrate **102** is provided. The substrate **102** may be a semiconductor substrate including silicon. Alternatively, the substrate **102** may include other types of bulk semiconductor material or other materials. For example, the substrate **102** may be silicon-on-insulator (SOI), silicon carbide, III-V materials or sapphire. The substrate **102** may further include a variety of electrical circuits **104**. The electrical circuits **104** may be any type of circuitry suitable for a particular application. In certain embodiments, the electrical circuits **104** may include various n-type metal-oxide semiconductor (NMOS) and/or p-type metal-oxide semiconductor (PMOS) devices made using high-k dielectric materials including hafnium silicate, zirconium silicate, hafnium oxide, and zirconium oxide, or using multiple gate transistor designs such as fin field effect transistor (FinFET). The electrical circuits **104** may be interconnected to perform one or more functions. The functions include memory structures, processing structures, sensors, amplifiers, power distribution, input/output circuitry or the like.

An interlayer dielectric **106** is formed on the substrate **102**. The interlayer dielectric **106** may be formed of low-k dielectric materials with a k-value lower than about 3.9. For example, the low-k dielectric materials include fluorine-doped silicon oxide, carbon-doped silicon oxide, porous silicon oxide, porous carbon-doped silicon oxide, organic polymers, silicone based polymers, or a combination thereof. The interlayer dielectric **106** may be deposited by chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), metallorganic chemical vapor deposition (MOCVD), physical vapor deposition (PVD), atomic layer deposition (ALD), a spin-on-dielectric (SOD) process, the like, or a combination thereof.

A plug **108** is formed of a metal, which may be titanium, titanium nitride, tungsten, aluminum, tantalum, titanium nitride, or combinations thereof, in an interlayer dielectric **106** and is coupled to the electric circuits **104**. The plug **108** is coupled to a bottom metallization layer **110**, which is formed of copper, aluminum, tantalum, titanium, titanium nitride, tungsten, alloys thereof, or combinations thereof, and disposed in the interlayer dielectric **106**. Another interlayer dielectric **112** is over the bottom metallization layer **110** and is formed of low-k dielectric materials similar to

those discussed with respect to the interlayer dielectric 106. A top plug 114 is in the interlayer dielectric 112 and is electrically connected to the bottom metallization layer 110. The top plug 114 is formed of a metal, which may be tungsten, copper, titanium nitride, tantalum, aluminum, or an alloy thereof. A top metallization layer formed as a contact pad 116 is coupled to the top plug 114. The contact pad 116 may be formed of copper, aluminum, titanium, titanium nitride, tungsten, alloys thereof, or combinations thereof. While FIG. 1A shows the bottom metallization layer 110 and the top metallization layer (e.g., the contact pad 116), one or more interlayer dielectrics layers (not shown), and the associated plug and metallization layer (not shown) may be formed between the bottom metallization layer 110 and the top metallization layer.

One or more passivation layers, such as a passivation layer 118, are formed and patterned over the contact pad 116. In some embodiments, the passivation layer 118 is formed of non-organic materials such as un-doped silicate glass, silicon nitride, silicon oxide, silicon oxynitride, boron-doped silicon oxide, phosphorous-doped silicon oxide or the like. The passivation layer 118 is formed to cover a peripheral region of the contact pad 116. The passivation layer 118 may be a single layer or a laminated layer. In FIG. 1, a single layer of the passivation layer 118 is shown for illustrative purpose only. As such, other embodiments may include any number of passivation layers.

A polymer layer 120 is deposited and patterned over the passivation layer 118. The polymer layer 120 may cover the peripheral region of the contact pad 116. In some embodiments, a center portion of the contact pad 116 is exposed through an opening 122. The polymer layer 120 may be formed of polymer materials such as polyimide, epoxy, polybenzoxazole (PBO), or the like, although other relatively soft, often organic, dielectric materials can also be used. The polymer layer 120 may be deposited by any suitable method such as spin coating or other methods. The polymer layer 120 may have a thickness ranging from about 1  $\mu\text{m}$  to about 10  $\mu\text{m}$ .

Afterwards, referring to FIG. 1B, a photoresist 124 is formed over the polymer layer 120. The photoresist 124 is patterned to have an opening 126 exposing a portion of the polymer layer 120 adjacent to the opening 122, by using a photolithography process. The opening 126 may be positioned over the opening 122 and have a diameter greater than that of the opening 122. The contact pad 116 is exposed through the openings 122 and 126.

Referring to FIG. 1C, a post-passivation interconnect (PPI) layer (hereinafter referred as to PPI layer) 128 is deposited over the polymer layer 120 and coupled to the exposed portion of the contact pad 116. The PPI layer 128 may function as redistribution lines, power lines, inductors, capacitors or any passive components. In some embodiments, the PPI layer 128 is a redistribution layer while providing the function of preventing underlying components being attacked by moisture. The PPI layer 128 may include a conductive material, such as copper, aluminum, copper alloy, or other mobile conductive materials. The PPI layer 128 may be formed by plating, electroless plating, sputtering, chemical vapor deposition, or the like. In some embodiments, the PPI layer 128 is a copper layer or a copper alloy layer, and a seed layer 130 may be formed prior to the PPI layer 128. The seed layer 130 can be constructed as a portion of the PPI layer 128. In some embodiments, the PPI layer 128, including the seed layer 130, has a thickness  $T_1$  ranging from about 2  $\mu\text{m}$  to about 15  $\mu\text{m}$ .

Referring to FIG. 1D, a diffusion barrier layer 132 is deposited on the PPI layer 128, including partially filling the remaining portion of the opening 122. In some embodiments, the diffusion barrier layer 132 is a nickel layer. Alternatively, the diffusion barrier layer 132 is formed of electroless nickel electroless palladium (ENEP), electroless nickel electroless palladium immersion gold (ENEPIG), tantalum or tantalum nitride, or the like. The diffusion barrier layer 132 may be formed by any suitable method such as plating, electroless plating, CVD, PECVD, MOCVD, PVD, ALD or the like. In some embodiments, the diffusion barrier layer 132 has a thickness ranging from about 0.15  $\mu\text{m}$  to about 10  $\mu\text{m}$ . In some embodiments, the photoresist 124 are removed after the formation of diffusion barrier layer 132.

Referring to FIG. 1E, a bump 134 is placed over the PPI layer 128 and outside of the opening 122. That is, the bump 134 is placed over a flat portion of the PPI layer 128. The diffusion barrier layer 132 is located between a bottom of the bump 134 and the PPI layer 128. In some embodiments, the bump 134 is a solder bump. The solder bump may include a lead-free pre-solder layer, SnAg, or a solder material including alloys of tin, lead, silver, copper, nickel, bismuth, or combinations thereof. In some other embodiments, the bump 134 is a copper bump. The copper bump may not form the intermetallic compound with the conductive material of the PPI layer 128. The bump 134 may have a diameter greater than about 200  $\mu\text{m}$ . The bump 134 may be placed over the PPI layer 128 by any suitable method, such as printing or plating.

Afterwards, referring to FIG. 1F, the diffusion barrier layer 132 is patterned to form a patterned barrier layer 132a by using the bump 134 as a mask. Accordingly, the patterned diffusion barrier layer 132a has a width not greater than the bottom of the bump 134. For example, the width difference between the patterned diffusion barrier layer 132a and the bottom of the bump 134 may be in a range from 0 to about 3  $\mu\text{m}$ . The diffusion barrier layer 132 is patterned by using an etching process. In some embodiments, the diffusion barrier layer 132 (e.g., nickel layer) is ferromagnetic and can induce electromagnetic interference with underlying electronic components in the semiconductor device 100. As such, the patterned diffusion barrier layer 132a with a reduced width may reduce or avoid the electromagnetic interference. In some other embodiments, the diffusion barrier layer 132 is not patterned if there is no need to be concerned about electromagnetic interference.

Afterwards, referring to FIG. 1G, a molding compound layer 136 is applied on the PPI layer 128, where the bump 134 is partially buried in the molding compound layer 136. In some embodiments, the molding compound layer 136 is in physical contact with a lower portion of the bump 134, while an upper portion of the bump 134 is exposed and protrudes from a top surface of the molding compound layer 136. In some embodiments, the molding compound layer 136 includes various materials, for example, one or more of epoxy resins, phenolic hardeners, silica, catalysts, pigments, mold release agents, or the like. The molding compound layer 136 may be formed by applying a liquid molding compound and performing a curing process to cure and solidify the liquid molding compound. The molding compound layer 136 may be a single layer film or a composite stack.

In the semiconductor device 100, the diffusion barrier layer 132 or 132a physically insulates the bump 134 from the PPI layer 128 while electrically connecting the bump 134 to the PPI layer 128. The diffusion barrier layer 132 or

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132a provides effective diffusion resistance to the conductive material of the PPI layer 128. Therefore, the diffusion from the PPI layer 128 to the bump 134 can be reduced or prevented, and the risks of bump crack and interruption of the PPI layer 128 can be reduced.

FIG. 2 is a cross-sectional view of a semiconductor device 200, in accordance with alternative embodiments. Referring to FIG. 2, the bump 134 is placed over the PPI layer 128 and outside of the opening 122. For example, the bump 134 is placed over the flat portion of the PPI layer 128. In some embodiments, the bump 134 is wrapped by a coating layer 236. The bump 134 and the PPI layer 128 are physically insulated by the coating layer 236. In some embodiments, the coating layer 236 is a nickel layer. Alternatively, the coating layer 236 is formed of electroless nickel electroless palladium (ENEP), electroless nickel electroless palladium immersion gold (ENEPIG), tantalum or tantalum nitride, or the like. The coating layer 236 may be formed by a coating process.

The diffusion barrier layer 132 and the coating layer 236 may be only individually presented or may be simultaneously presented in the semiconductor device 200. For example, as shown in FIG. 2, the bump 134 with the coating layer 236 is directly positioned over the PPI layer 128. Alternatively, the bump 134 with the coating layer 236 is positioned over the diffusion barrier layer 132. The coating layer 236 is coated onto the bump 134 either before or after the placement of the bump 134. In some embodiments, the molding compound layer 136 is applied on the PPI layer 128 after the bump 134 is coated by the coating layer 236 and placed over the PPI layer 128. The coating layer 236 may have a thickness ranging from about 0.15  $\mu\text{m}$  to about 10  $\mu\text{m}$ . The coating layer 236 may provide the same function as the diffusion barrier layer 132 for providing diffusion resistance to the PPI layer 128. Therefore, the coating layer 236 may also be called a diffusion barrier layer.

FIG. 3 is a cross-sectional view of a semiconductor device 300, in accordance with exemplary embodiments. Referring to FIG. 3, a bump 134a wrapped by a doped layer 336 is placed over the PPI layer 128 outside of the opening 122. For example, the bump 134a is placed over the flat portion of the PPI layer 128. The bump 134a and the PPI layer 128 are physically insulated by the doped layer 336. In some embodiments, the bump 134a is formed of the same material of the bump 134 and is surrounded by a doped layer 336. The bump 134a may have a diameter greater than about 200  $\mu\text{m}$ . The doped layer 336 may include a dopant such as nickel, iron, nickel-iron alloy, cobalt or the like. The doped layer 336 may be formed by performing an ion implantation process on the bump 134. The implantation process may include providing the bump 134, and then implanting the dopant into a region of the bump 134 near an outer surface of the bump 134.

The diffusion barrier layer 132 and the doped layer 336 may be only individually presented or may be simultaneously presented in the semiconductor device 200. For example, as shown in FIG. 3, the bump 134 with the doped layer 336 is directly positioned over the PPI layer 128. Alternatively, the bump 134 with the doped layer 336 is positioned over the diffusion barrier layer 132. The implantation process of forming the doped layer 336 is performed either before or after the placement of the bump 134. In some embodiments, the molding compound layer 136 is applied on the PPI layer 128 after the bump 134a is wrapped by the doped layer 336 and placed over the PPI layer 128. The doped layer 336 may have a thickness ranging from about 0.15  $\mu\text{m}$  to about 10  $\mu\text{m}$ . The doped layer 336 may

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provide the same function as the diffusion barrier layer 132 for providing diffusion resistance to the PPI layer 128. Therefore, the doped layer 336 may also be called a diffusion barrier layer.

FIG. 4 is a cross-sectional view of a semiconductor device 400, in accordance with exemplary embodiments. The semiconductor device 400 includes a PPI layer 428 that have a thicker thickness than that of the PPI layer 128. For example, the PPI layer 428 has a thickness  $T_2$  that ranges from about 2 to 10 times that of the PPI layer 128. For example, the thickness  $T_2$  of the PPI layer 428 may be in a range from about 10  $\mu\text{m}$  to about 100  $\mu\text{m}$ . In some embodiments, the PPI layer 428 has a thickness that ranges from about  $1/100$  to about  $1/5$  of the diameter of the bump 134. The PPI layer 428, having the thicker thickness  $T_2$ , can further reduce the possibility of the interruption of the PPI layer 428 as well as at least delay the occurrence of the interruption.

Embodiments of mechanisms for forming a semiconductor device having a post-passivation interconnect structure are provided. A diffusion barrier layer is provided for physically insulating a bump from a post-passivation interconnect layer. Accordingly, the diffusion of a conductive material of the post-passivation interconnect layer can be reduced or prevented. The risks of bump crack and interruption of the post-passivation interconnect layer can be reduced.

In accordance with some embodiments, a semiconductor device is provided. The semiconductor device includes a contact pad over a substrate. The semiconductor device also includes a passivation layer over the substrate and a first portion of the contact pad, and a second portion of the contact pad is exposed through an opening. The semiconductor device further includes a post-passivation interconnect layer over the passivation layer and coupled to the second portion of the contact pad. In addition, the semiconductor device includes a bump over the post-passivation interconnect layer and outside of the opening. The semiconductor device also includes a diffusion barrier layer physically insulating the bump from the post-passivation interconnect layer while electrically connecting the bump to the post-passivation interconnect layer.

In accordance with some embodiments, a semiconductor device is provided. The semiconductor device includes a contact pad over a substrate. The semiconductor device further includes a passivation layer over the substrate and a first portion of the contact pad, and a second portion of the contact pad is exposed through an opening. The semiconductor device further includes a post-passivation interconnect layer over the post-passivation interconnect layer and coupled to the second portion of the contact pad. The post-passivation interconnect layer includes copper. In addition, the semiconductor device includes a bump over the post-passivation interconnect layer and outside of the opening. The semiconductor device also includes a diffusion barrier layer physically insulating the bump from the post-passivation interconnect layer. The diffusion barrier layer includes nickel, electroless nickel electroless palladium (ENEP), electroless nickel electroless palladium immersion gold (ENEPIG), tantalum or tantalum nitride.

In accordance with some embodiments, a method for forming a semiconductor device is provided. The method includes forming a contact pad over a substrate. The method also includes forming a passivation layer over the substrate and a first portion of the contact pad while leaving a second portion of the contact pad exposed through an opening. The method further includes forming a post-passivation interconnect layer over the passivation layer. The post-passiva-

tion interconnect layer is coupled to the second portion of the contact pad. In addition, the method includes forming a bump and a diffusion barrier layer over the post-passivation interconnect layer. The bump is outside of the opening and electrically connected to the post-passivation interconnect layer through the diffusion barrier layer.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods, and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or layer to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A semiconductor device, comprising:
  - a contact pad over a substrate;
  - a passivation layer over the substrate and a first portion of the contact pad, wherein a second portion of the contact pad is exposed through an opening;
  - a post-passivation interconnect layer over the passivation layer and coupled to the second portion of the contact pad; and
  - a bump over the post-passivation interconnect layer and outside of the opening, wherein the bump has an inner portion and a diffusion barrier region enclosing an entirety of the inner portion, the diffusion barrier region physically insulates the inner portion of the bump from the post-passivation interconnect layer while electrically connecting the inner portion of the bump to the post-passivation interconnect layer, the inner portion of the bump is made of a metal material, and the diffusion barrier region of the bump is made of the metal material doped with a dopant.
2. The semiconductor device as claimed in claim 1, wherein the dopant in the diffusion barrier region includes nickel.
3. The semiconductor device as claimed in claim 1, wherein the metal material includes a solder material or copper.
4. The semiconductor device as claimed in claim 1, wherein a portion of the diffusion barrier region is between a bottom of the inner portion of the bump and the post-passivation interconnect layer.
5. The semiconductor device as claimed in claim 4, further comprising a diffusion barrier layer directly below the diffusion barrier region of the bump and directly above the post-passivation interconnect layer.
6. The semiconductor device as claimed in claim 1, wherein the bump comprises a solder bump.
7. The semiconductor device as claimed in claim 1, wherein the bump comprises copper or copper alloys.

8. The semiconductor device as claimed in claim 1, wherein the post-passivation interconnect layer has a thickness that ranges from about  $\frac{1}{100}$  to about  $\frac{1}{5}$  of the diameter of the bump.

9. A semiconductor device, comprising:
  - a contact pad over a semiconductor substrate;
  - a passivation layer over the semiconductor substrate and a first portion of the contact pad, wherein a second portion of the contact pad is exposed through an opening;
  - a post-passivation interconnect layer over the passivation layer and coupled to the second portion of the contact pad, wherein the post-passivation interconnect layer comprises copper;
  - a bump over the post-passivation interconnect layer and outside of the opening, wherein the bump has an inner portion and a diffusion barrier region enclosing an entirety of the inner portion, the diffusion barrier region physically insulates the inner portion of the bump from the post-passivation interconnect layer, the inner portion of the bump is made of a metal material, and the diffusion barrier region of the bump is made of the metal material doped with a dopant.
10. The semiconductor device as claimed in claim 9, wherein the diffusion barrier region of the bump is in direct contact with the post-passivation interconnect layer and electrically connecting the inner portion of the bump to the post-passivation interconnect layer.
11. A method for forming a semiconductor device, comprising:
  - forming a contact pad over a substrate;
  - forming a passivation layer over the substrate and a first portion of the contact pad while leaving a second portion of the contact pad exposed through an opening;
  - forming a post-passivation interconnect layer over the passivation layer, wherein the post-passivation interconnect layer is coupled to the second portion of the contact pad; and
  - forming a bump over the post-passivation interconnect layer, wherein the bump is outside of the opening and electrically connected to the post-passivation interconnect layer, the bump has an inner portion and a diffusion barrier region enclosing an entirety of the inner portion, the diffusion barrier region physically insulates the inner portion of the bump from the post-passivation interconnect layer, the inner portion of the bump is made of a metal material, and the diffusion barrier region of the bump is made of the metal material doped with a dopant.
12. The method as claimed in claim 11, further comprising:
  - depositing a diffusion barrier layer over the passivation layer; and
  - placing the bump onto the diffusion barrier layer.
13. The method as claimed in claim 12, further comprising patterning the diffusion barrier layer by using the bump as a mask.
14. The method as claimed in claim 11, wherein the diffusion barrier region is formed by performing an implantation process on the bump to implant the dopant into a region of the bump that encloses an entirety of the inner portion of the bump.
15. The method as claimed in claim 14, further comprising forming a diffusion barrier layer on the post-passivation interconnect layer before the bump are formed over the post-passivation interconnect layer.



16. The method as claimed in claim 14, wherein the implantation process is performed to form the diffusion barrier region before the bump is placed onto the post-passivation interconnect layer.

17. The semiconductor device as claimed in claim 1, 5 further comprising a molding compound layer covering a rest of the post-passivation interconnect layer that is not covered by the bump, and the molding compound layer is spaced apart from the inner portion of the bump by the diffusion barrier region of the bump. 10

18. The semiconductor device as claimed in claim 9, further comprising a molding compound layer covering a rest of the post-passivation interconnect layer that is not covered by the bump, and the molding compound layer is spaced apart from the inner portion of the bump by the 15 diffusion barrier region of the bump.

19. The method as claimed in claim 11, further comprising forming molding compound layer covering a rest of the post-passivation interconnect layer that is not covered by the bump, wherein the molding compound layer is spaced apart 20 from the inner portion of the bump by the diffusion barrier region of the bump.

20. The semiconductor device as claimed in claim 17, wherein a bottom surface of the inner portion of the bump is between a top surface of the molding compound layer and 25 a top surface of the post-passivation interconnect layer.

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