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Lu et al.

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(54) **NON-HIERARCHICAL METAL LAYERS FOR INTEGRATED CIRCUITS**

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Related U.S. Application Data

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H01L 21/768	(2006.01)
H01L 21/311	(2006.01)
H01L 23/528	(2006.01)
H01L 23/522	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/7681*** (2013.01); ***H01L 21/31144*** (2013.01); ***H01L 21/76816*** (2013.01); ***H01L 21/76877*** (2013.01); ***H01L 23/5283*** (2013.01); *H01L 23/522* (2013.01); *H01L 23/528* (2013.01); *H01L 23/5226* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/6836; H01L 21/61732

See application file for complete search history.

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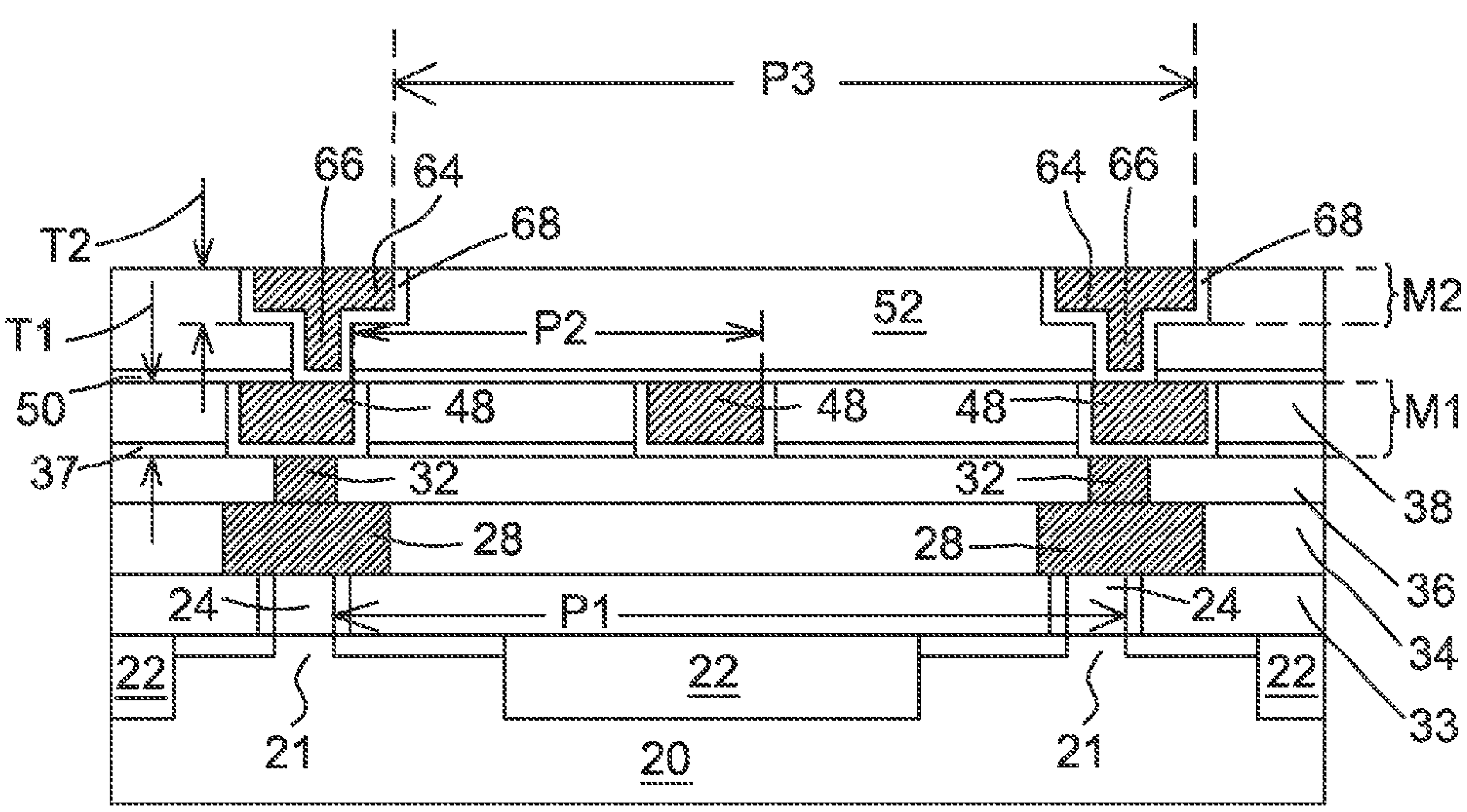
(57) **ABSTRACT**

An integrated circuit structure includes a semiconductor substrate, and a first metal layer over the semiconductor substrate. The first metal layer has a first minimum pitch. A second metal layer is over the first metal layer. The second metal layer has a second minimum pitch smaller than the first minimum pitch.

20 Claims, 10 Drawing Sheets



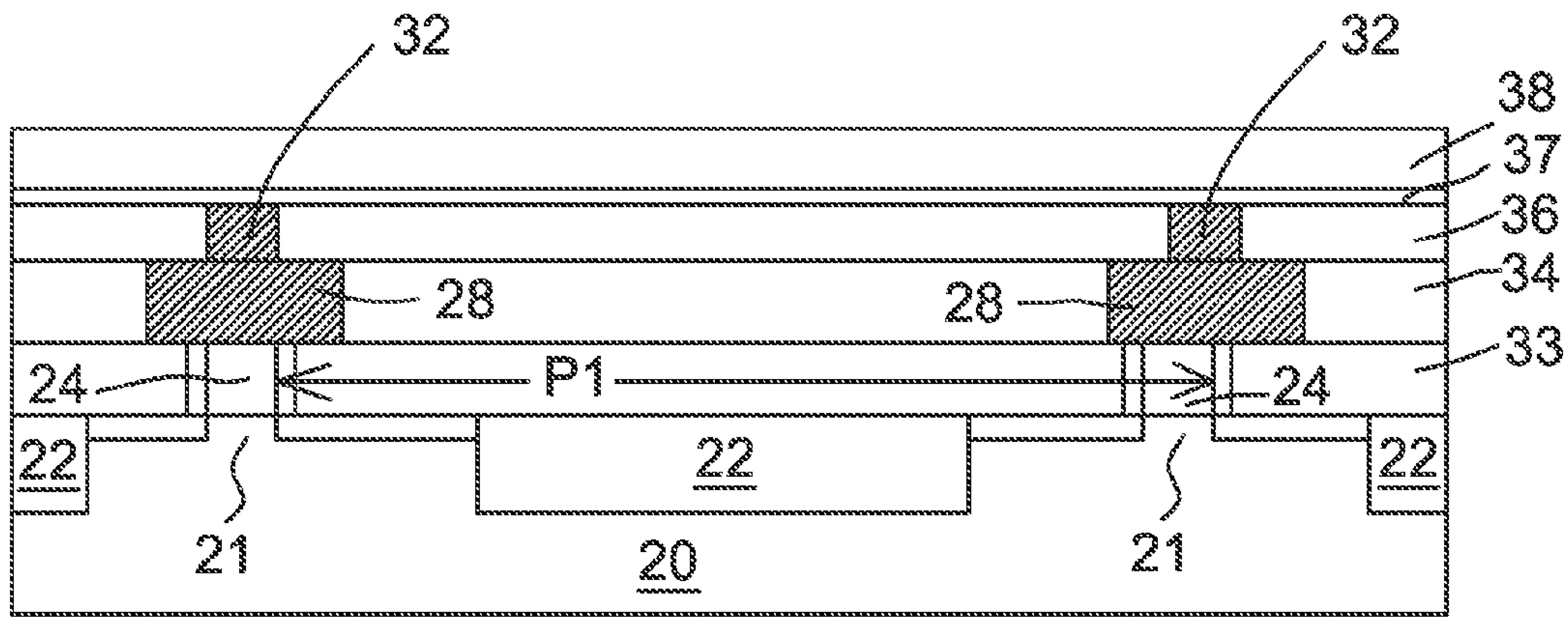

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Fig. 1

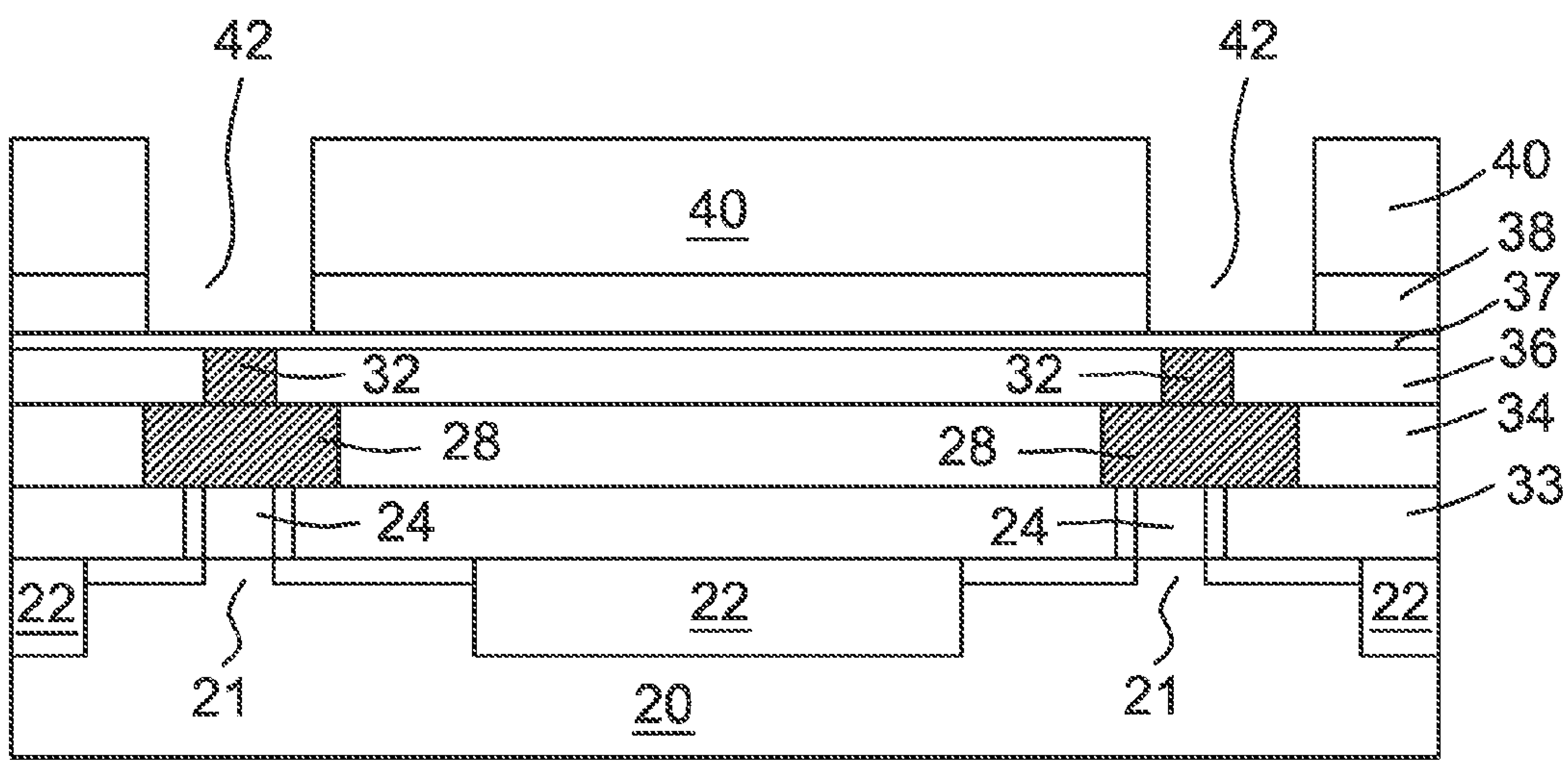
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Fig. 2

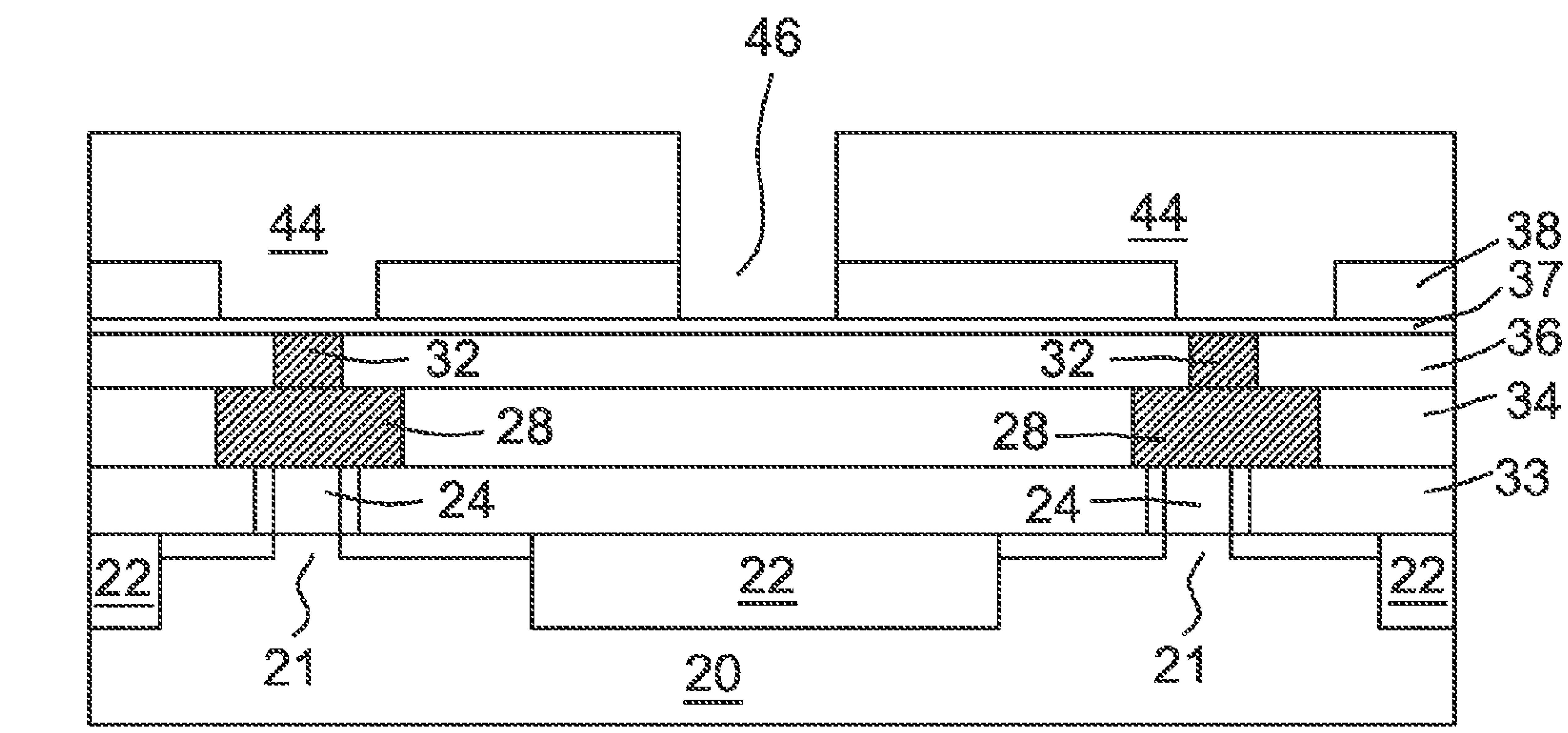
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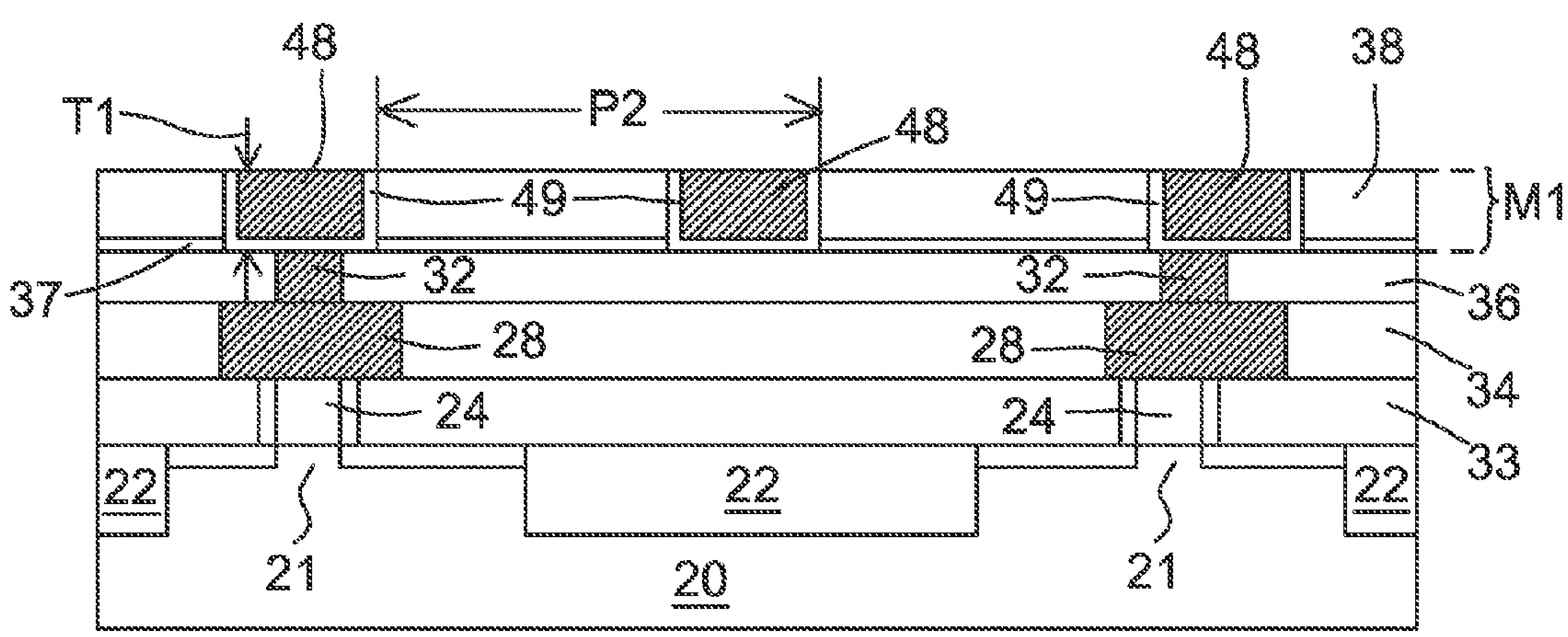
Fig. 3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38
T1
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M1
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Fig. 4

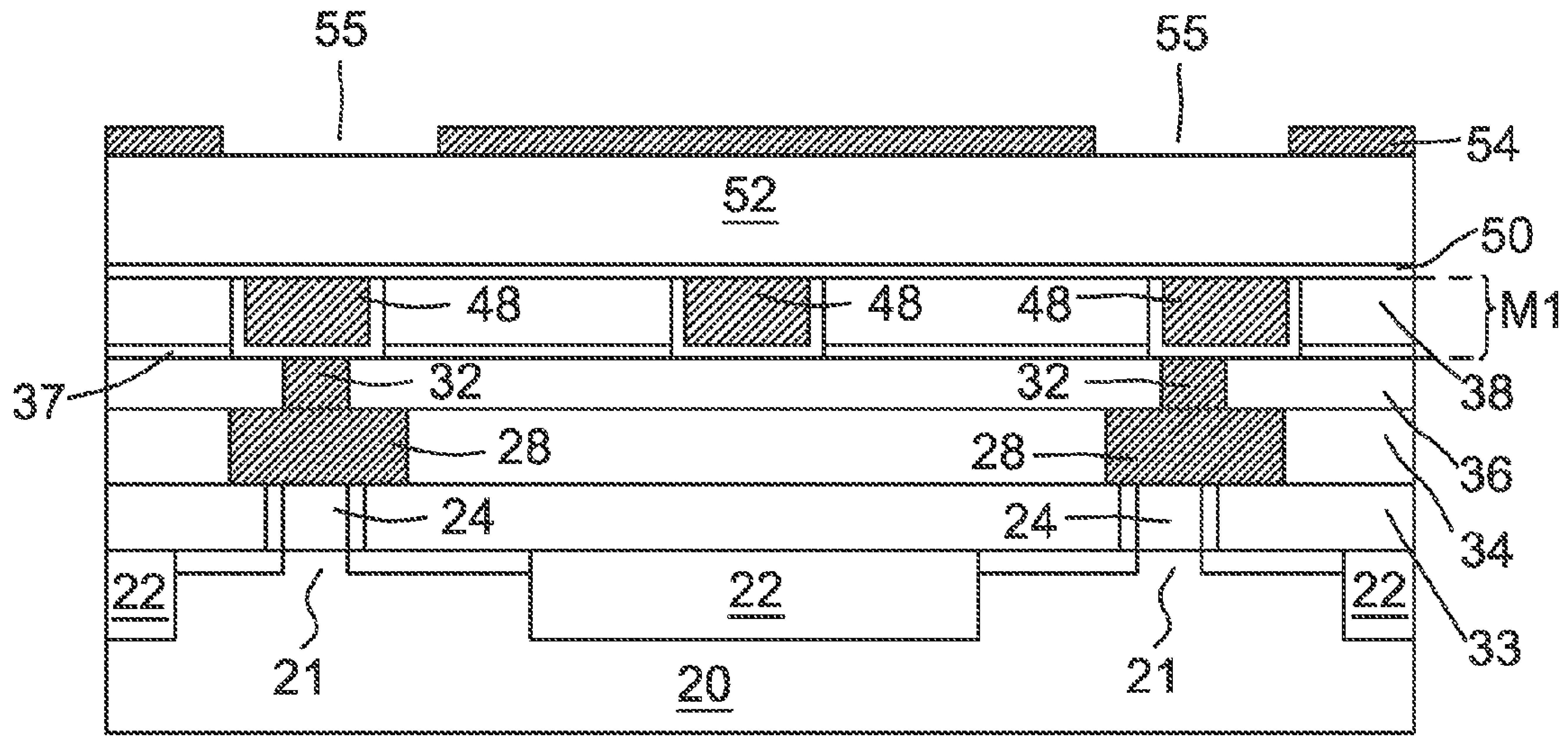
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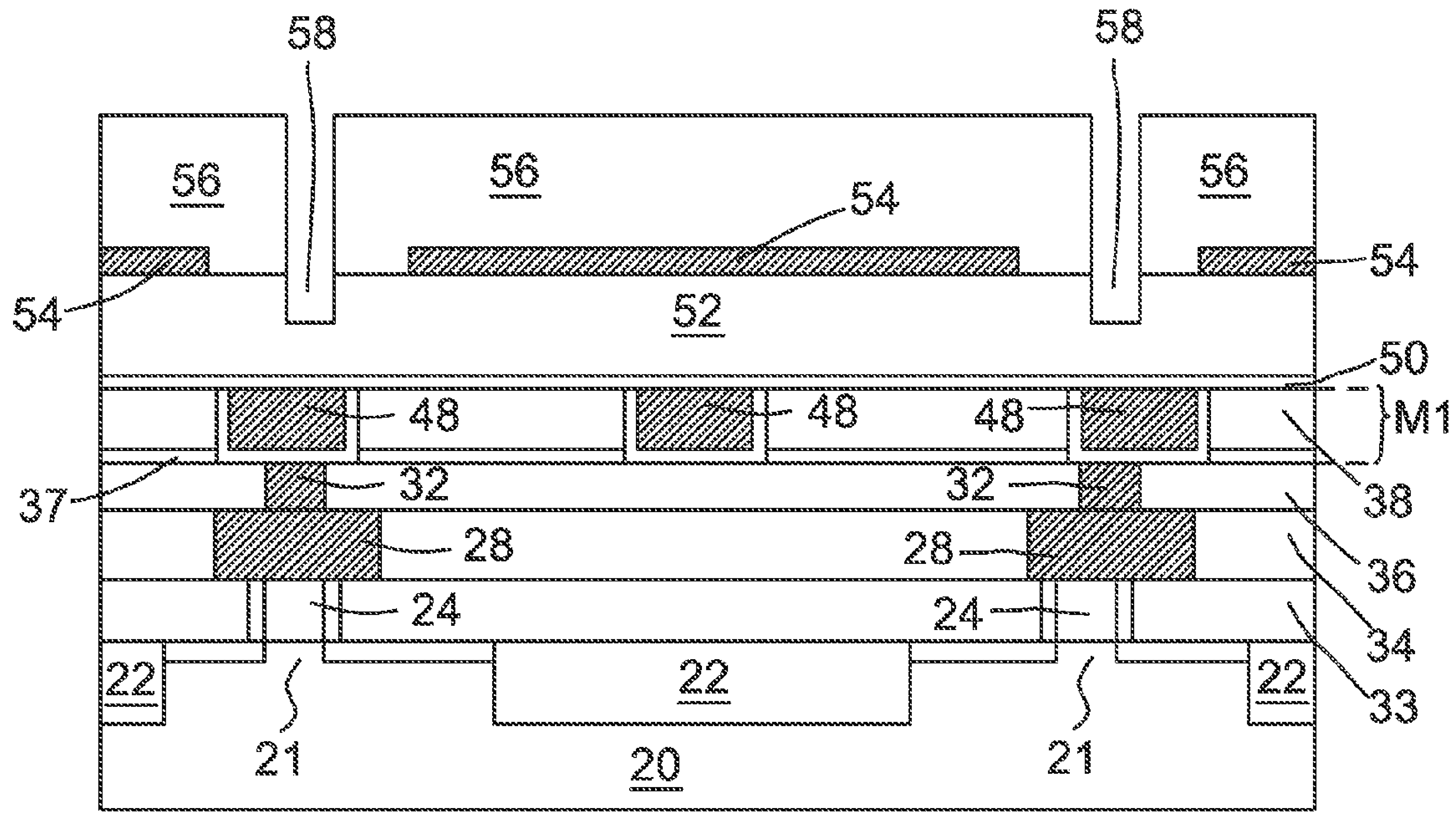
Fig. 5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M1
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Fig. 6

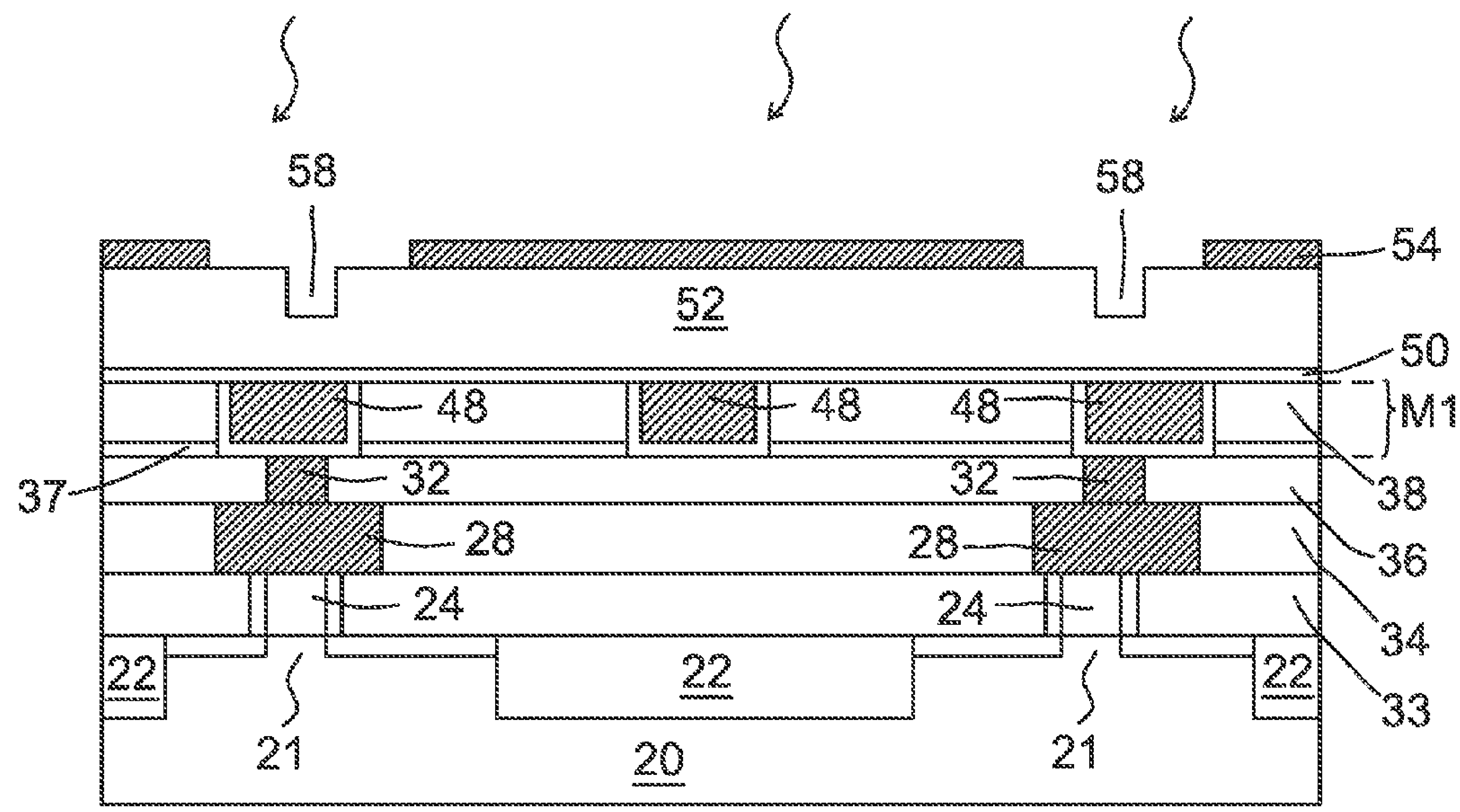
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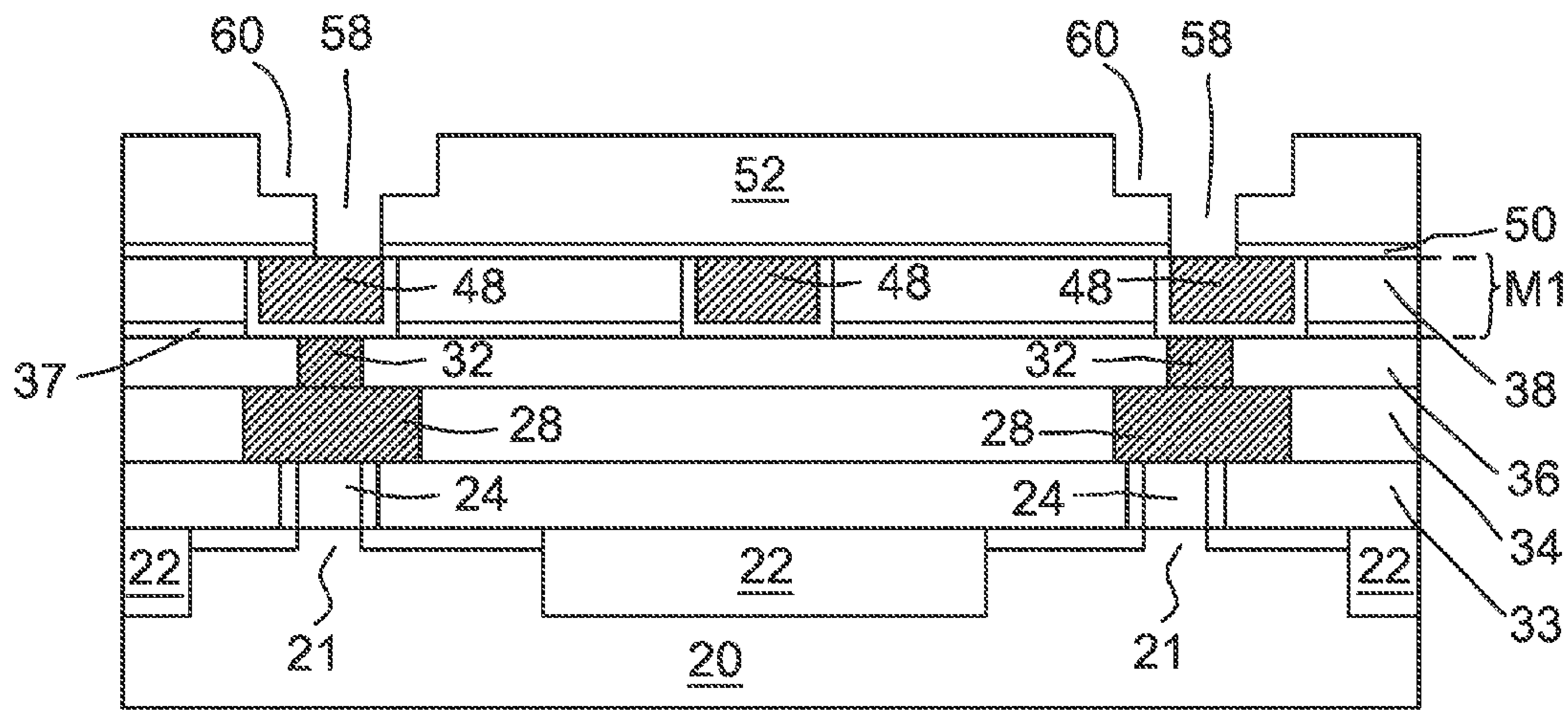
Fig. 7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M1
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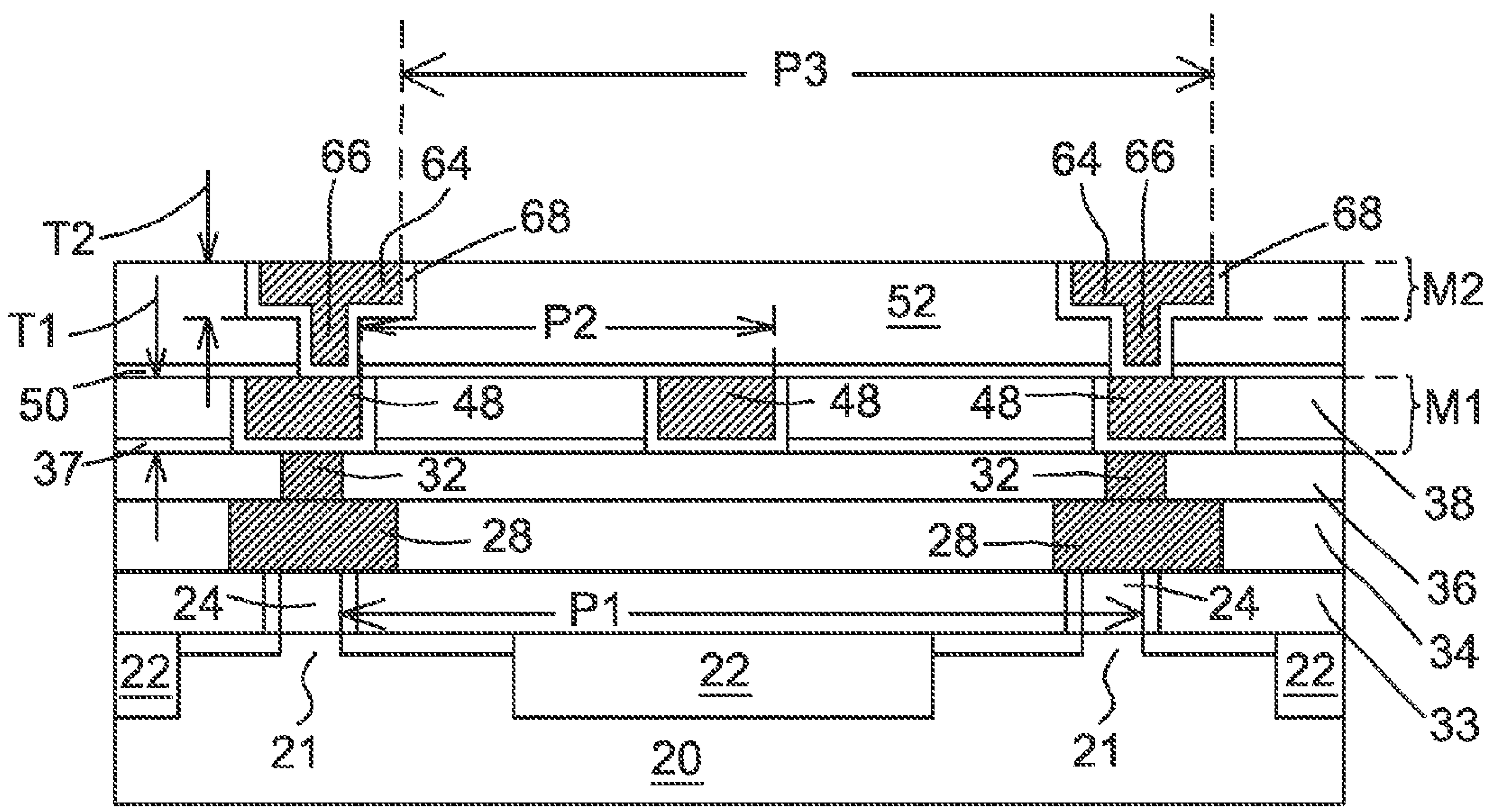
Fig. 8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T2
T1
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M2
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M1
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P1
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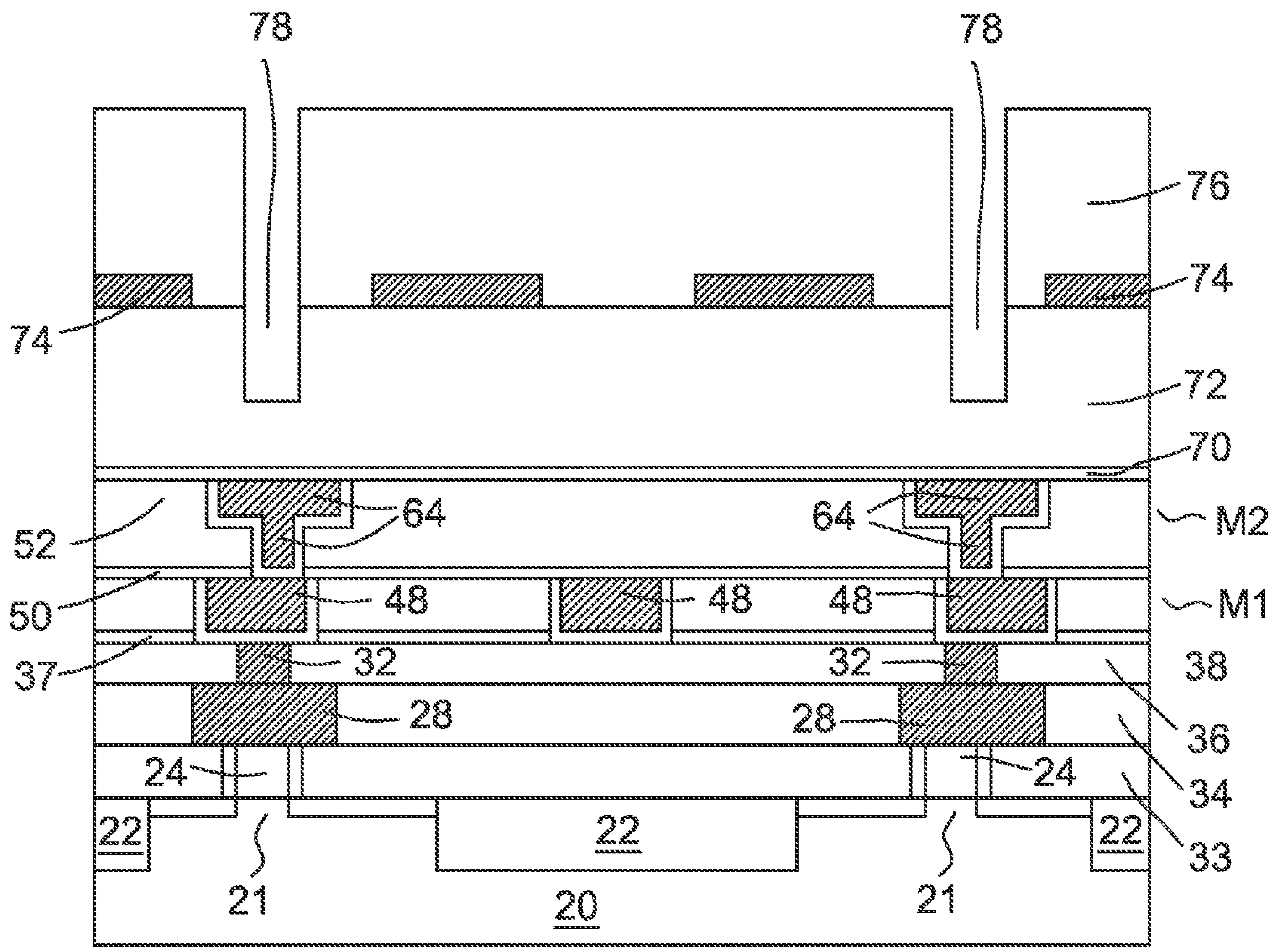
Fig. 9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M2
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M1
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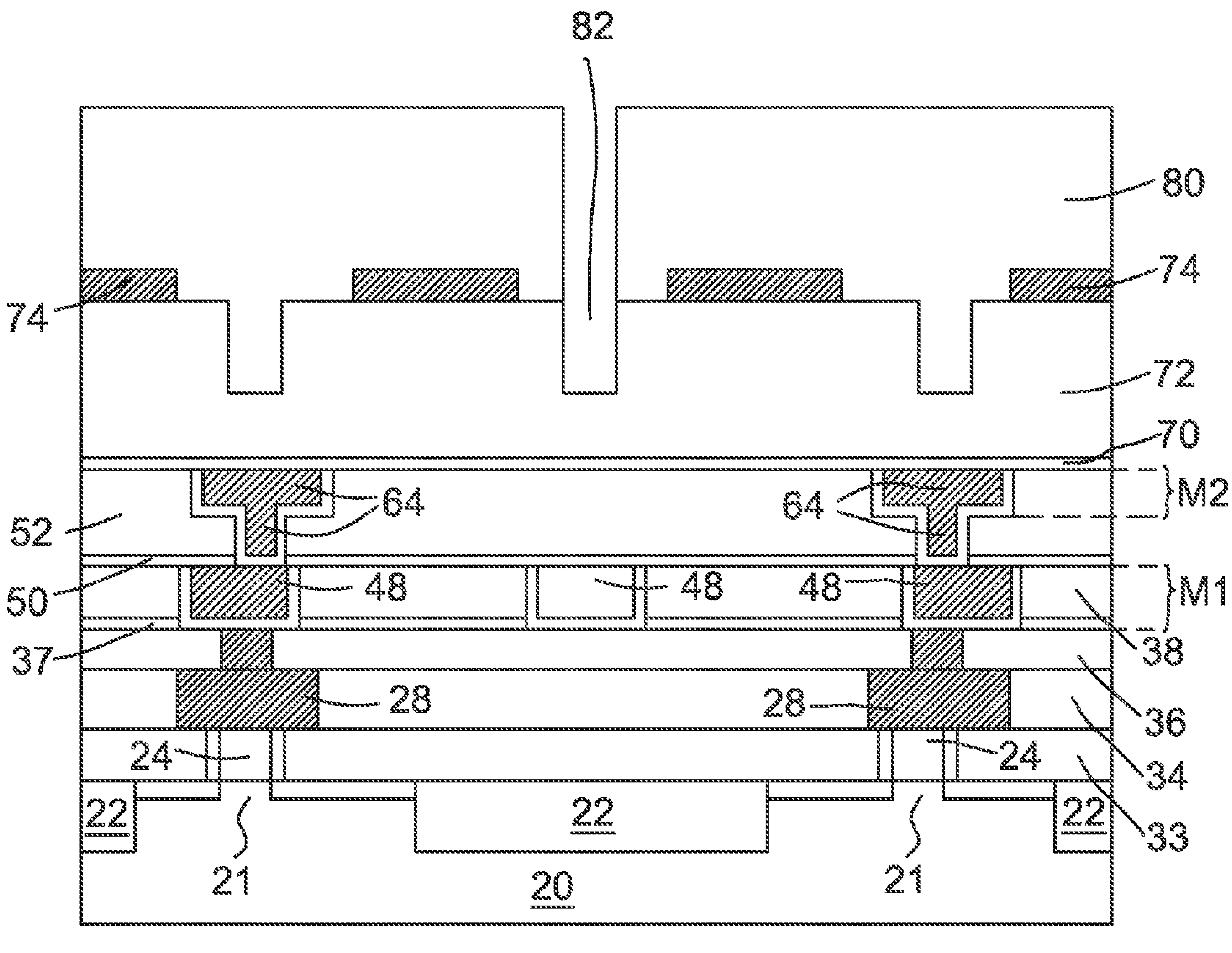
Fig. 10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80
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70
64
64
M2
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M1
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Fig. 11

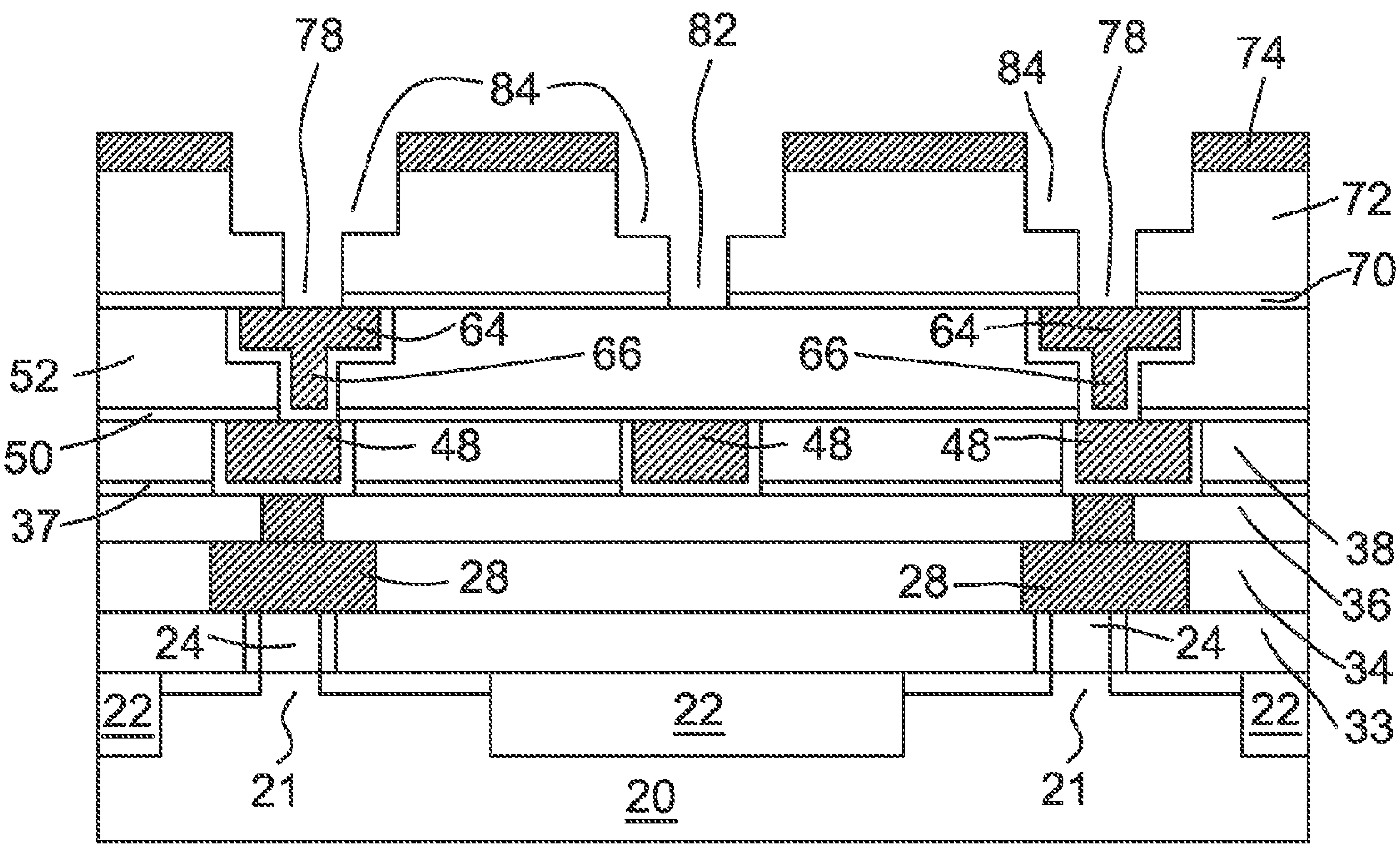
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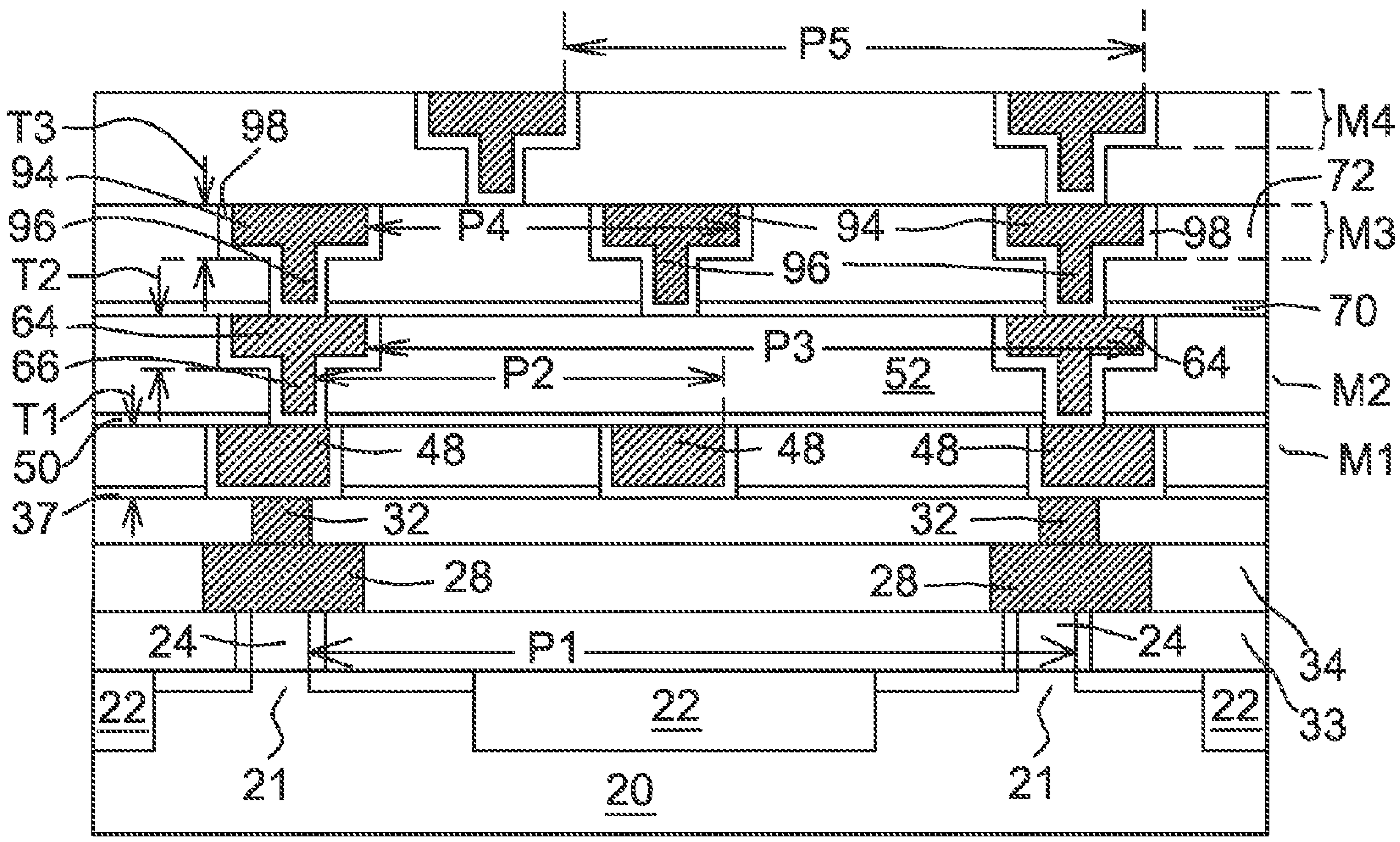
Fig. 12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T2
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22
21
20

Fig. 13

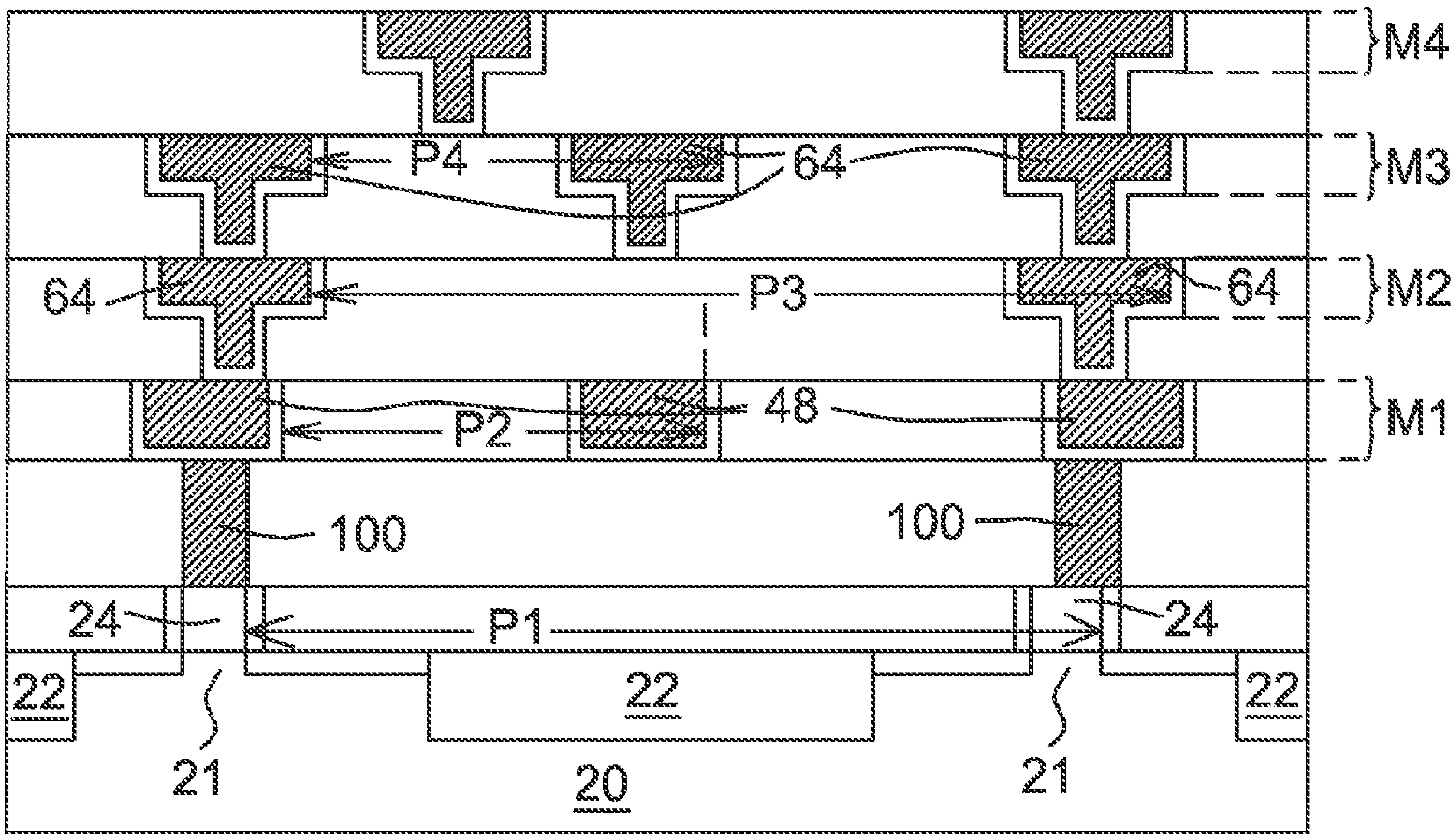

Fig. 14

NON-HIERARCHICAL METAL LAYERS FOR INTEGRATED CIRCUITS

PRIORITY CLAIM AND CROSS-REFERENCE

This application is a divisional of U.S. patent application Ser. No. 13/158,175, entitled "Non-Hierarchical Metal Layers for Integrated Circuits," filed on Jun. 10, 2011, which application is incorporated herein by reference.

BACKGROUND

Integrated circuit devices such as transistors are typically formed on the surfaces of semiconductor substrates. Metal layers are formed over the integrated circuit devices, and are used to interconnect the integrated circuit devices as functional circuits. There may be as many as ten metal layers formed over a semiconductor substrate.

Since the resistance of a metal line is related to its size, and a lower resistance leads to better performance of the respective integrated circuits, it is preferred that the metal lines are thick, wide, and short in order to have a small resistance. However, the requirement of forming thick and wide metal lines conflicts with the requirement of reducing chip area usage. Accordingly, metal layers typically adopt hierarchical structures, wherein upper metal layers have the thicknesses and widths equal to or greater than the thicknesses and widths, respectively, of lower metal layers. This is because the lower metal layers have more metal lines, and hence have to be narrow to incorporate the large amount of metal lines. The upper metal layers are relatively small in number, and can be larger in size.

When the integrated circuit manufacturing process advances to 20 nm technology or smaller, the pitch of the metal lines, particularly in the lower metal layers, are close to the wavelength of the yellow light, wherein the yellow light is used for exposing photoresists that are used for defining the patterns of metal layer. Special techniques need to be used to reduce or eliminate the problem caused by the small pitch of the metal lines. For example, two photoresists and two etching processes may be needed for defining the pattern of one metal layer. This, however, results in the increase in the manufacturing cost and the reduction in the yield.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1** through **13** are cross-sectional views of intermediate stages in the manufacturing of an interconnect structure having a non-hierarchical structure in accordance with various embodiment; and

FIG. **14** illustrates the cross-sectional view of an interconnect structure in accordance with various alternative embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of

specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

An interconnect structure of an integrated circuit and method of forming the same are provided in accordance with an embodiment. The intermediate stages of manufacturing various embodiments are illustrated. The variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

FIGS. **1** through **13** are cross-sectional views of intermediate stages in the manufacturing of an interconnect structure in accordance with an embodiment. Referring to FIG. **1**, a structure including substrate **20** and overlying devices are provided. Substrate **20** may be formed of a commonly used semiconductor material such as silicon, silicon germanium, or the like, and may be a bulk substrate or a semiconductor-on-insulator (SOI) substrate. Integrated circuit devices such as transistors **21** are formed at a surface of substrate **20**. Gate electrodes **24** are formed over substrate **20**. Gate electrodes **24** may include active gate electrodes, which form the gates of transistors **21**, and possibly dummy gate electrodes (not shown), which are electrically floating. The materials of gate electrodes **24** include metals or metal alloys, polysilicon, or the like. In an embodiment, dummy gate electrodes **24** may be formed over insulation regions such shallow trench isolation (STI) regions **22**.

The integrated circuit structure may include metal lines **28** in metal layer M**0** (referred to as M**0** hereinafter). M**0** metal lines **28** are formed over, and may contact, gate electrodes **24**. Furthermore, M**0** vias **32** are formed over and contact M**0** metal lines **28**. Gate electrodes **24**, M**0** metal lines **28**, and M**0** vias **32** are formed in inter-layer dielectrics (ILDs) **33**, **34**, and **36**, respectively. In the illustrated embodiment, M**0** vias **32** are formed using a single-damascene process. In alternative embodiments, M**0** vias **32** may be formed along with the overlying metal lines **48** (not shown in FIG. **1**, please refer to FIG. **4**) in the bottom metal layer (M**1**) using a dual-damascene process. Accordingly, the dual damascene process steps may be similar to what are shown in FIGS. **10** through **13**. Etch stop layer (ESL) **37** may optionally be formed over ILD **36**. Inter-metal Dielectric (IMD) **38** is formed over ESL **37**. In an embodiment, IMD **38** is formed using a low-k dielectric material having a low-k value, which may be smaller than about 3.0, or smaller than about 2.5.

Gate electrodes **24** have pitch P**1**, which is referred to as minimum gate electrode pitch P**1** hereinafter. It is noted that neighboring gate electrodes **24** on the same chip or wafer may have pitches equal to or greater than minimum gate electrode pitch P**1**, but cannot have pitches smaller than minimum gate electrode pitch P**1**. Similarly, the term "minimum pitch" is also used throughout the description to indicate the smallest pitch of the metal lines in other metal layers such as layers M**0** through Mtop. In an exemplary embodiment, minimum gate electrode pitch P**1** is between about 80 nm and about 100 nm, for example, although different pitches may be used.

FIGS. **2** through **4** illustrate a two-patterning-two-etching (2P2E) process for forming bottom metal layer M**1**, which comprises IMD **38**, and metal lines in IMD **38**. Referring to FIG. **2**, photoresist **40** is formed over IMD **38** using a first lithography mask (not shown), and is patterned to form openings **42**. IMD **38** is then etched using the patterned IMD **38** as a mask, so that openings **42** extend down into IMD **38**. Next, in FIG. **3**, photoresist **40** is removed, and photoresist **44** is formed and patterned, forming opening(s) **46**. The patterning of photoresist **44** is performed using a second lithography mask different from the first lithography mask, and the first and the second lithography masks belong to a same double-patterning mask set. Photoresist **44** is then removed.

FIG. **4** illustrates the formation of metal lines **48**. The formation process may include blanket forming a diffusion barrier layer, which may comprise titanium, titanium nitride, tantalum, tantalum nitride, or the like. The diffusion barrier layer is formed in openings **42** and **46** in IMD **38**, and over IMD **38**. Next, a metallic material such as a pure (or substantially pure) copper or a copper alloy is filled into openings **42** (FIG. **2**) and opening **46** (FIG. **3**). A chemical mechanical polish (CMP) is then performed to remove excess metallic material, and leaving metal lines **48** and diffusion barrier layers **49**. The formation of metal layer M**1** is thus finished.

Metal lines **48** have minimum pitch P**2**, which is referred to as minimum M**1** pitch P**2** hereinafter. Minimum M**1** pitch P**2** may be smaller than minimum gate electrode pitch P**1**. In an exemplary embodiment, minimum M**1** pitch P**2** is between about 40 nm and about 80 nm, and may be about 64 nm, for example, although different pitches may be used. Thickness T**1** of metal layer M**1** may be between about 550 Å and about 750 Å, and may be about 650 Å in an embodiment. It is observed that in FIGS. **2** through **3**, in the defining of the patterns of metal lines **48**, two photoresists **40** and **44** are used, and two respective patterning steps are performed on photoresists **40**/**44** and IMD **38**. Accordingly, the formation process of metal lines **48** (or the respective openings **42**) is referred to as a 2P2E process.

FIGS. **5** through **9** illustrate the formation of metal layer M**2** (which is the metal layer immediately over bottom metal layer M**1**) and the formation of underlying vias. Referring to FIG. **5**, ESL **50** is formed, followed by the formation of IMD **52**, which may be a low-k dielectric layer. Hard mask **54** is formed and patterned. Hard mask **54** may be formed of silicon nitride, silicon oxynitride, titanium nitride, tantalum nitride, or the like. Hard mask **54** includes openings **55** that define the patterns of metal lines in metal layer M**2**.

In an embodiment, as shown in FIG. **6**, photoresist **56** is formed and patterned to define the patterns of vias. In an embodiment, photoresist **56** is formed of a single layer. In alternative embodiments, photoresist **56** is formed of a composite layer, which may comprise a bottom layer formed of a polar material such as a polymer with hydroxyl or phenol groups, and a middle layer over the bottom layer, wherein the middle layer may be formed of an oxide-like photoresist.

Photoresist **56** is then used to etch into IMD **52** to form openings **58**. Openings **58** extend partially into IMD **52**, and the bottoms of openings **58** are at an intermediate level of IMD **52**. Next, as shown in FIG. **7**, photoresist **56** is removed. Hard mask **54** is then used to etch into IMD **52**, for example, using an anisotropic etching method. The resulting structure is shown in FIG. **8**. During the etching step, via openings **58** extend down so that ESL **50** is exposed. Furthermore, trench openings **60** are formed and stop at an intermediate level of IMD **52**. The exposed portions of ESL **50** are also etched, and the underlying metal lines **48** are exposed. Hard mask **54** is also removed.

FIG. **9** illustrates the formation of metal lines **64** and vias **66**. The formation process may include blanket forming conductive diffusion barrier layer **68**, and filling a metallic material such as substantially pure copper or a copper alloy into openings **58** and **60**. After a CMP process to remove excess metallic material, metal lines **64** and vias **66** are formed. Throughout the description, metal lines **64** and the part of IMD **52** that is at the same level as metal lines **64** in combination are referred to as metal layer M**2**.

It is observed that in the formation of metal layer M**2** and the underlying vias **66**, a single photoresist **56** (FIG. **6**) is used, and one patterning step is performed using photoresist **56** (FIG. **6**). Accordingly, the formation process of metal layer M**2** is referred to as a 1P1E process. The minimum M**2** pitch P**3** in metal layer M**2** may be between about 80 nm and about 100 nm in an exemplary embodiment. Such a minimum pitch makes the using of 1P1E process possible. Furthermore, minimum M**2** pitch P**3** may be the same (or substantially the same) as minimum gate electrode pitch P**1**. In an embodiment, metal lines **64** as in FIG. **9** are used for the connections of gate electrodes **24**, and hence metal lines **64** may be aligned to gate electrodes **24**. Therefore, even though minimum M**2** pitch P**3** is greater than minimum M**1** pitch P**2**, and is as great as minimum gate electrode pitch P**1**, there is no chip area penalty incurred. Thickness T**2** of metal layer M**2** may be between about 800 Å and about 1200 Å, and may be greater than thickness T**1**. In an exemplary embodiment, thickness T**2** is between about 120 percent T**1** and about 150 percent T**1**.

FIGS. **10** through **13** illustrate the 2P2E process for forming metal layer M**3** and the underlying vias. Referring to FIG. **10**, optional ESL **70** is formed, followed by the formation of IMD **72**, which may be a low-k dielectric layer. Hard mask **74**, which may be formed of essentially the same material as hard mask **54** in FIG. **5**, is formed and patterned. Hard mask **74** includes openings that define the patterns of the metal lines in metal layer M**3** (FIG. **13**).

Photoresist **76**, which may be formed essentially the same material as photoresist **56** (FIG. **6**) is formed and patterned to define the patterns of vias. Photoresist **76** is then used to etch into IMD **72** to form openings **78**. Openings **78** extend partially into IMD **72**, and the bottoms of openings **78** are at an intermediate level of IMD **72**. Photoresist **76** is then removed.

FIG. **11** illustrates the formation and the patterning of photoresist **80**. Photoresist **80** is patterned using a lithography mask (not shown) different from the lithograph mask (not shown) used in the step shown in FIG. **10**, wherein the lithography masks used for the steps shown in FIGS. **10** and **11** may belong to a same double-patterning mask set. Next, IMD **72** is etched to form opening(s) **82**, which may stop at a same level as openings **78** (FIG. **10**). Photoresist **80** is then removed.

Next, as shown in FIG. **12**, hard mask **74** is used to etch into IMD **72**, for example, using an anisotropic etching method. During the etching step, openings **78** and **82** extend down so that ESL **70** is exposed. Furthermore, trench openings **84** are formed and stop at an intermediate level of IMD **72**. The exposed portions of ESL **70** are etched.

FIG. **13** illustrates the formation of metal lines **94** and vias **96**. The formation process may include blanket forming conductive diffusion barrier layer **98**, and filling a metallic material such as pure (or substantially pure) copper or a copper alloy into openings **78**, **82**, and **84**. After a CMP process to remove excess metallic material, metal lines **94** and vias **96** are formed, and the formation of metal layer M**3** is finished.

It is observed that in FIGS. **10** and **11**, two photoresists **76** and **80** are used, and two respective patterning steps are performed on photoresists **76** and **80** and IMD **72**. Accordingly, the formation process of metal lines **94** and vias **96** is a 2P2E process. Throughout the description, metal lines **94** and the parts of IMD **72** at the same level as metal lines **94** in combination are referred to as metal layer M**3**.

Minimum M**3** pitch P**4** in metal layer M**3** may be between about 40 nm and about 80 nm, and may be about 64 nm in an exemplary embodiment. Minimum M**3** pitch P**4** may be smaller than Minimum M**2** pitch P**3**, with Minimum M**2** pitch P**3** being equal to about 120 percent and about 150 percent Minimum M**3** pitch P**4**. Furthermore, minimum M**3** pitch P**4** may be the same (or substantially the same) as minimum M**1** pitch P**2**. Accordingly, the interconnect structure as shown in FIG. **13** is referred to as having a non-hierarchical structure since minimum M**3** pitch P**4** is smaller than Minimum M**2** pitch P**3**. Thickness T**3** of metal layer M**3** may be between about 550 Å and about 750 Å, and may be about 650 Å in an embodiment. Thickness T**3** may also be equal to, or substantially equal to, thickness T**1** of metal layer M**1**. Furthermore, thickness T**2** may be greater than thickness T**3**, and may be equal to about 120 percent and about 150 percent thickness T**3**.

In subsequent process steps, upper metal layers M**4**, M**5** (not shown), and up to Mtop (the topmost metal layer, not shown) are formed. The formation process may include 1P1E process and 2P2E process. For metal layers M**3** to Mtop, The respective minimum pitches (including minimum M**4** pitch P**5**) may have a hierarchical structure, with the upper metal layers having minimum pitches equal to or greater than the minimum pitches of lower layers.

Metal layers M**2** and M**3** are formed using dual-damascene structures, in which the metal lines in the metal layers are forming using a same filling and a same CMP process. Accordingly, the dual-damascene metal lines and vias do not have a noticeable interface therebetween. Although metal lines in metal layer M**1** is illustrated as being formed using a single damascene process, it may also be formed along with M**0** vias **32** using a 2P2E dual-damascene process. The process steps may be similar to what are shown in FIGS. **10** through **13**.

FIG. **14** illustrates an alternative embodiment. This embodiment is essentially the same as in FIG. **13**, except contact plugs **100** (which may be formed of tungsten, for example) replace M**0** metal lines **28** and M**0** vias **32** as in FIG. **13**. Unless specified otherwise, the reference numerals in the embodiment shown in FIG. **14** represent like elements in the embodiment illustrated in FIG. **13**. The process steps of for forming metal layers M**1**, M**2**, and M**3** as in FIG. **14** are essentially the same as shown in FIGS. **1** through **13**.

In the embodiments, by forming metal layer M**2** having a greater minimum pitch and a greater thickness than the minimum pitch and the thickness, respectively, of metal layer M**3**, the metal lines in metal layer M**2** may have reduced resistance, and hence the resulting integrated circuit has improved performance. It is found that the increase in the minimum pitch and the thickness of M**2** does not incur any chip area penalty. Furthermore, the increase in the minimum pitch of metal layer M**2** makes it possible to use 1P1E process, instead of 2P2E process, for forming metal layer M**2**. Accordingly, the manufacturing cost is reduced, and manufacturing yield is improved.

In accordance with embodiments, an integrated circuit structure includes a semiconductor substrate, and a first metal layer over the semiconductor substrate. The first metal layer has a first minimum pitch. A second metal layer is over the first metal layer. The second metal layer has a second minimum pitch smaller than the first minimum pitch.

In accordance with other embodiments, an integrated circuit structure includes a semiconductor substrate, and a first metal layer over the semiconductor substrate. The first metal layer has a first thickness. A second metal layer is over the first metal layer. The second metal layer has a second thickness smaller than the first thickness.

In accordance with yet other embodiments, a method includes forming a first metal layer and forming a second metal layer. The step of forming the first metal layer includes forming a first dielectric layer over a semiconductor substrate; forming first openings in the first dielectric layer, wherein all openings in the first dielectric layer are formed using a 1P1E process; and filling a first metallic material in the first openings to form first metal lines. The step of forming the second metal layer includes forming a second dielectric layer over the first metal layer; forming second openings in the second dielectric layer, wherein two neighboring openings in the second dielectric layer are formed using a 2P2E process; and filling a second metallic material in the second openings to form second metal lines.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A method comprising:

forming a first metal layer comprising:

forming a first dielectric layer over a semiconductor substrate;

forming first openings in the first dielectric layer, wherein the first openings are formed using a one-photoresist-one-patterning (1P1E) process; and

filling a first metallic material in the first openings to form first metal lines of the first metal layer; and

forming a second metal layer over the first metal layer, wherein the forming the second metal layer comprises:

forming a second dielectric layer over the first metal layer;

forming second openings in the second dielectric layer, wherein two neighboring openings of the second openings are formed using a two-photoresist-two-patterning (2P2E) process, with the two openings ones of the second openings being at a same level; and

filling a second metallic material in the second openings to form second metal lines of the second metal layer.

2. The method of claim **1**, wherein the first metal layer has a first minimum pitch greater than a second minimum pitch of the second metal layer.

3. The method of claim **2**, wherein the first minimum pitch is measured in a first direction perpendicular to lengthwise directions of first two metal lines that are in the first metal layer and have the first minimum pitch, and the second minimum pitch is measured in a second direction perpendicular to lengthwise directions of second two metal lines that are in the second metal layer and have the second minimum pitch.

4. The method of claim **2**, wherein the first minimum pitch is substantially equal to a minimum pitch of gate electrodes, and wherein the gate electrodes are over the semiconductor substrate and under the first metal layer.

5. The method of claim **2**, wherein the first minimum pitch is between about 80 nm and about 90 nm, and the second minimum pitch is between about 40 nm and about 80 nm.

6. The method of claim **1**, wherein the first metal layer has a first thickness greater than a second thickness of the second metal layer.

7. The method of claim **1** further comprising:

before the forming the first metal layer, forming a third metal layer, wherein the forming the third metal layer comprises:

forming a third dielectric layer over the semiconductor substrate;

forming third openings in the third dielectric layer, wherein two neighboring openings in the third dielectric layer are formed using an additional 2P2E process; and

filling a third metallic material in the third openings to form third metal lines of the third metal layer.

8. The method of claim **7**, wherein the third metal layer is over gate electrodes of transistors, and wherein the gate electrodes have a minimum pitch greater than a minimum pitch of the third metal layer.

9. A method comprising:

etching a first dielectric layer over a semiconductor substrate to form first openings;

filling the first openings to form first metal lines, wherein the first metal lines have a first minimum pitch, with the first minimum pitch measured in a first direction perpendicular to lengthwise directions of two of the first metal lines that have the first minimum pitch;

etching a second dielectric layer over the first dielectric layer to form second openings;

filling the second openings to form second metal lines, wherein the second metal lines have a second minimum pitch smaller than the first minimum pitch, with the second minimum pitch measured in a second direction perpendicular to lengthwise directions of two of the second metal lines that have the second minimum pitch; and

forming metal vias electrically coupling the first metal lines to the second metal lines.

10. The method of claim **9** further comprising:

forming third metal lines under the first metal lines; and

forming gate electrodes over the semiconductor substrate and under the third metal lines, wherein some of gate electrodes form parts of transistors, and wherein the third metal lines have a third minimum pitch smaller than the first minimum pitch, and smaller than a fourth minimum pitch of the gate electrodes, with the third minimum pitch measured in a third direction perpendicular to lengthwise directions of third two of the third metal lines that have the third minimum pitch, and the fourth minimum pitch measured in a fourth direction perpendicular to lengthwise directions of two of the gate electrodes that have the fourth minimum pitch.

11. The method of claim **10**, wherein the first minimum pitch is substantially equal to the fourth minimum pitch.

12. The method of claim **9**, wherein the first metal lines are formed using a one-photoresist-one-patterning (1P1E) process.

13. The method of claim **12** and the second metal lines are formed using a two-photoresist-two-patterning (2P2E) process.

14. The method of claim **9**, wherein the first metal lines are formed using dual damascene processes.

15. A method comprising:

forming a first metal layer over gate electrodes of transistors using two-photoresist-two-patterning (2P2E) processes, wherein first metal lines in the first metal layer has a first minimum pitch;

forming a second metal layer over the first metal layer using one-photoresist-one-patterning (1P1E) processes, wherein second metal lines in the second metal layer has a second minimum pitch greater than the first minimum pitch; and

forming a third metal layer over the second metal layer using 2P2E processes, wherein third metal lines in the third metal layer has a third minimum pitch smaller than the second minimum pitch.

16. The method of claim **15**, wherein the first metal layer is formed using a single damascene process, and the second metal layer is formed using a dual damascene process.

17. The method of claim **15**, wherein the gate electrodes have a fourth minimum pitch greater than the first minimum pitch.

18. The method of claim **15**, wherein the second minimum pitch is equal to twice the first minimum pitch.

19. The method of claim **15**, wherein the first minimum pitch is measured in a first direction perpendicular to lengthwise directions of first two metal lines in the first metal layer and having the first minimum pitch, and the second minimum pitch is measured in a second direction perpendicular to lengthwise directions of second two metal lines in the second metal layer and having the second minimum pitch.

20. The method of claim **15** further comprising forming vias electrically coupling the second metal layer to the first metal layer.

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