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Kao et al.

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(54) **ELECTRO-PLATING AND APPARATUS FOR PERFORMING THE SAME**

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Related U.S. Application Data

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(51) **Int. Cl.**

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C25D 21/10	(2006.01)
C25D 17/00	(2006.01)
C25D 7/12	(2006.01)

(52) **U.S. Cl.**

CPC ***C25D 21/12*** (2013.01); ***C25D 17/001*** (2013.01); ***C25D 17/004*** (2013.01); ***C25D 17/005*** (2013.01); ***C25D 21/10*** (2013.01); *C25D 7/123* (2013.01)

(58) **Field of Classification Search**

CPC C25D 7/123; C25D 21/12; C25D 21/10; C25D 17/005

See application file for complete search history.

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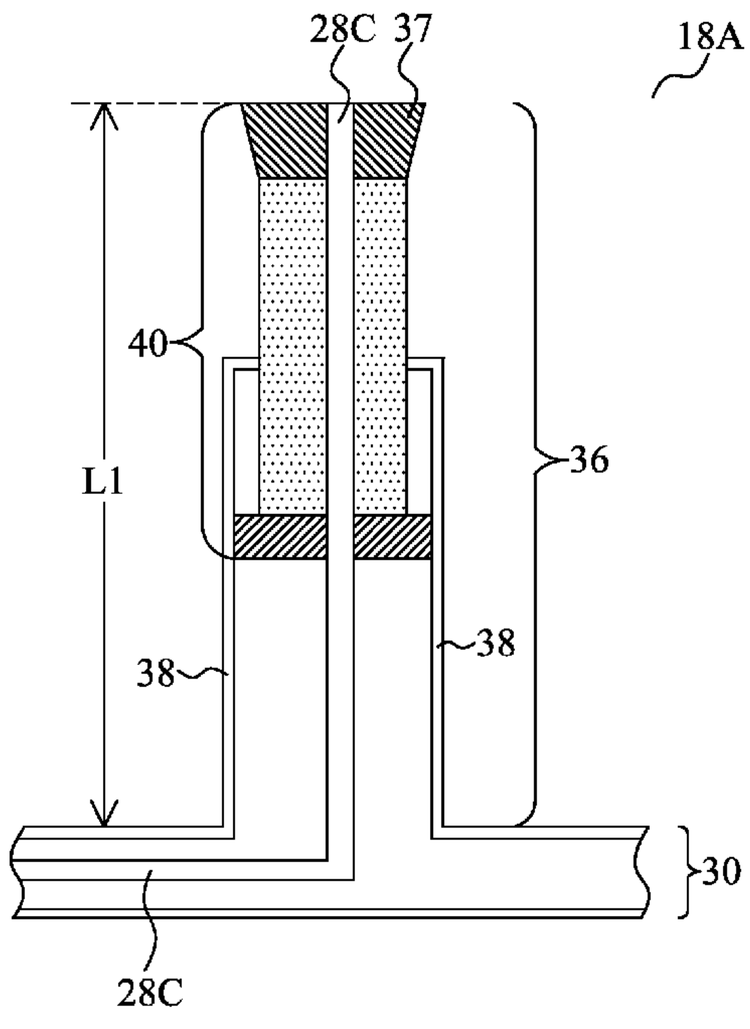
(57) **ABSTRACT**

A method of plating a metal layer on a work piece includes exposing a surface of the work piece to a plating solution, and supplying a first voltage at a negative end of a power supply source to an edge portion of the work piece. A second voltage is supplied to an inner portion of the work piece, wherein the inner portion is closer to a center of the work piece than the edge portion. A positive end of the power supply source is connected to a metal plate, wherein the metal plate and the work piece are spaced apart from each other by, and are in contact with, the plating solution.

19 Claims, 12 Drawing Sheets



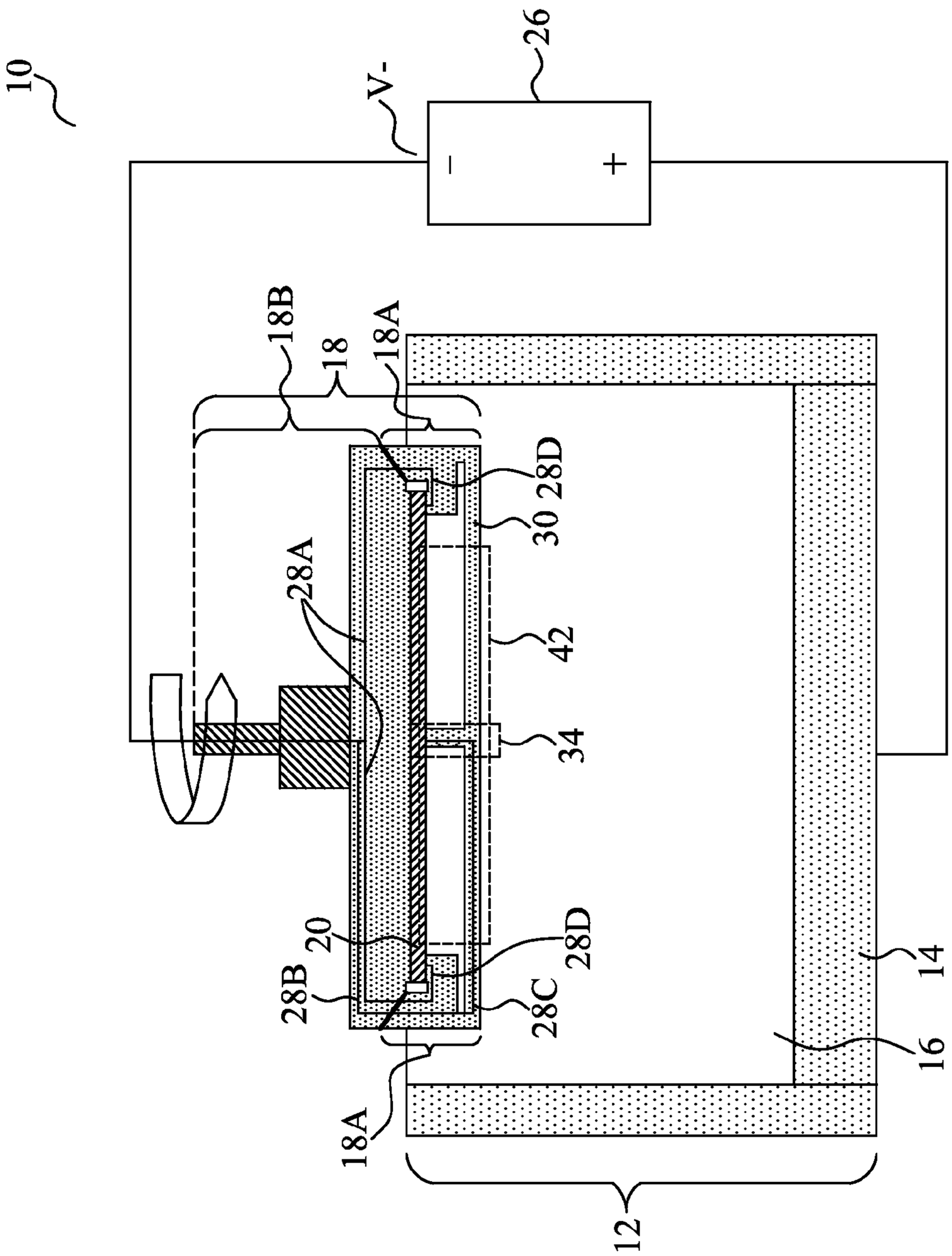


Fig. 1

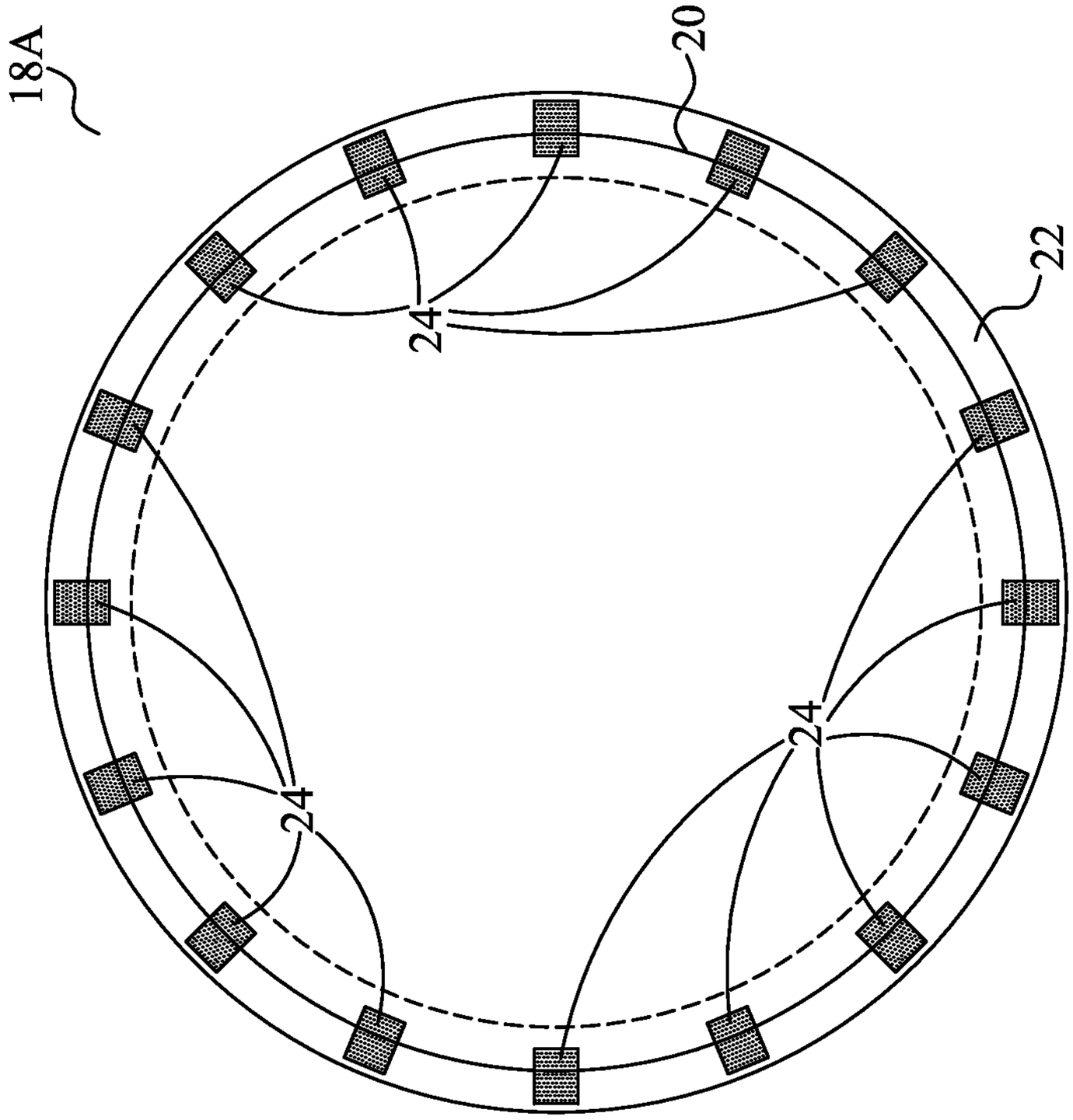


Fig. 2

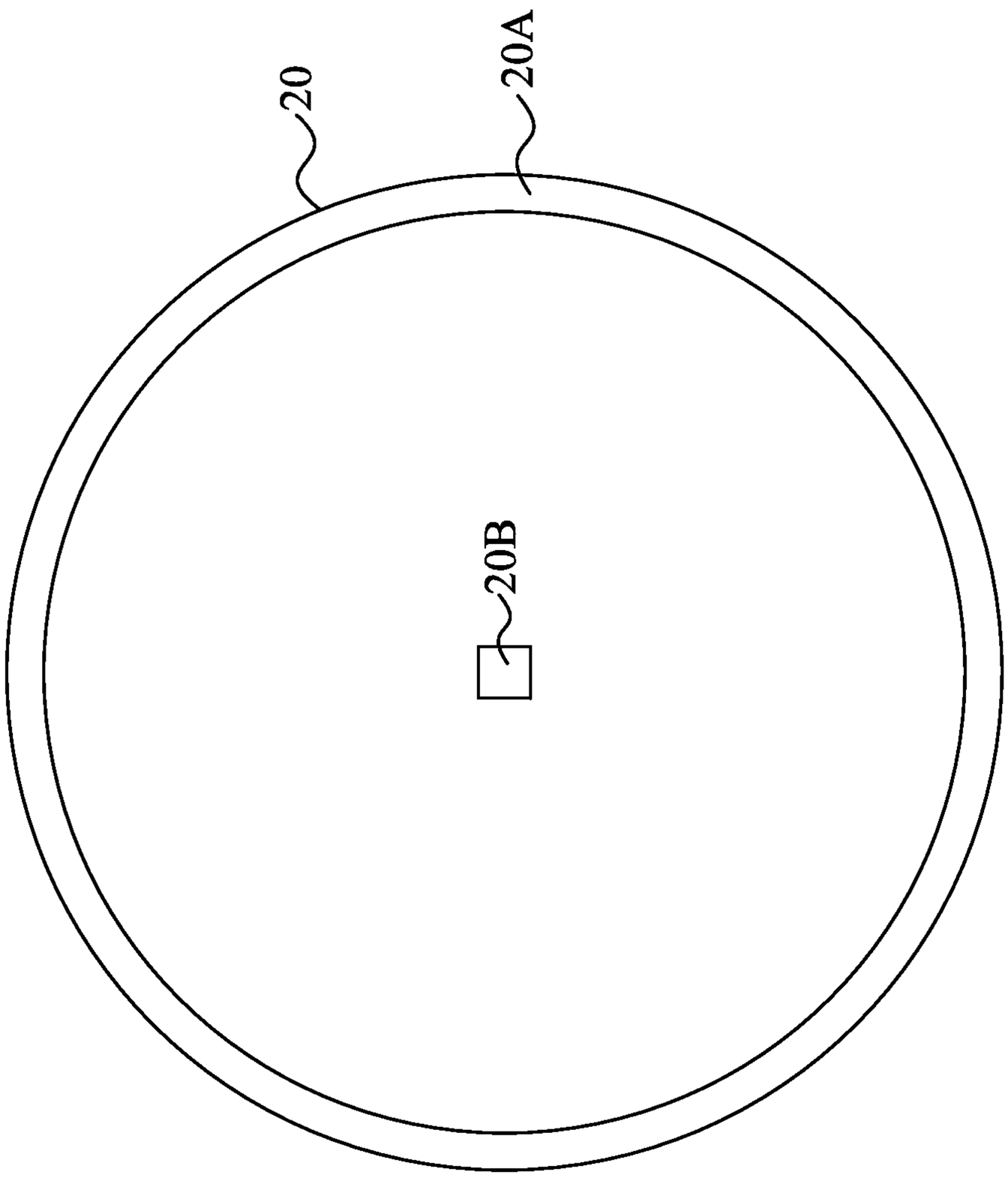


Fig. 3

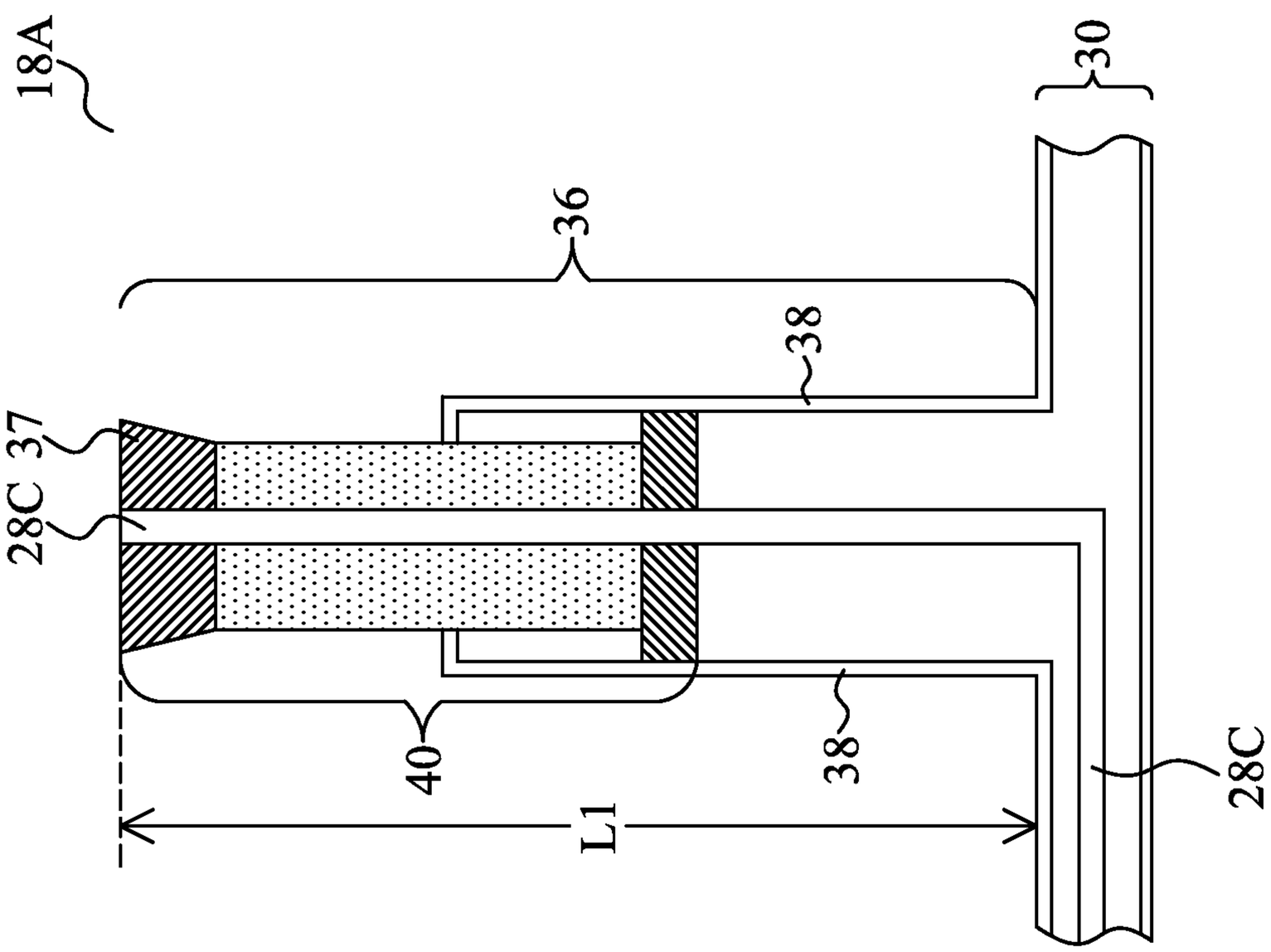


Fig. 4

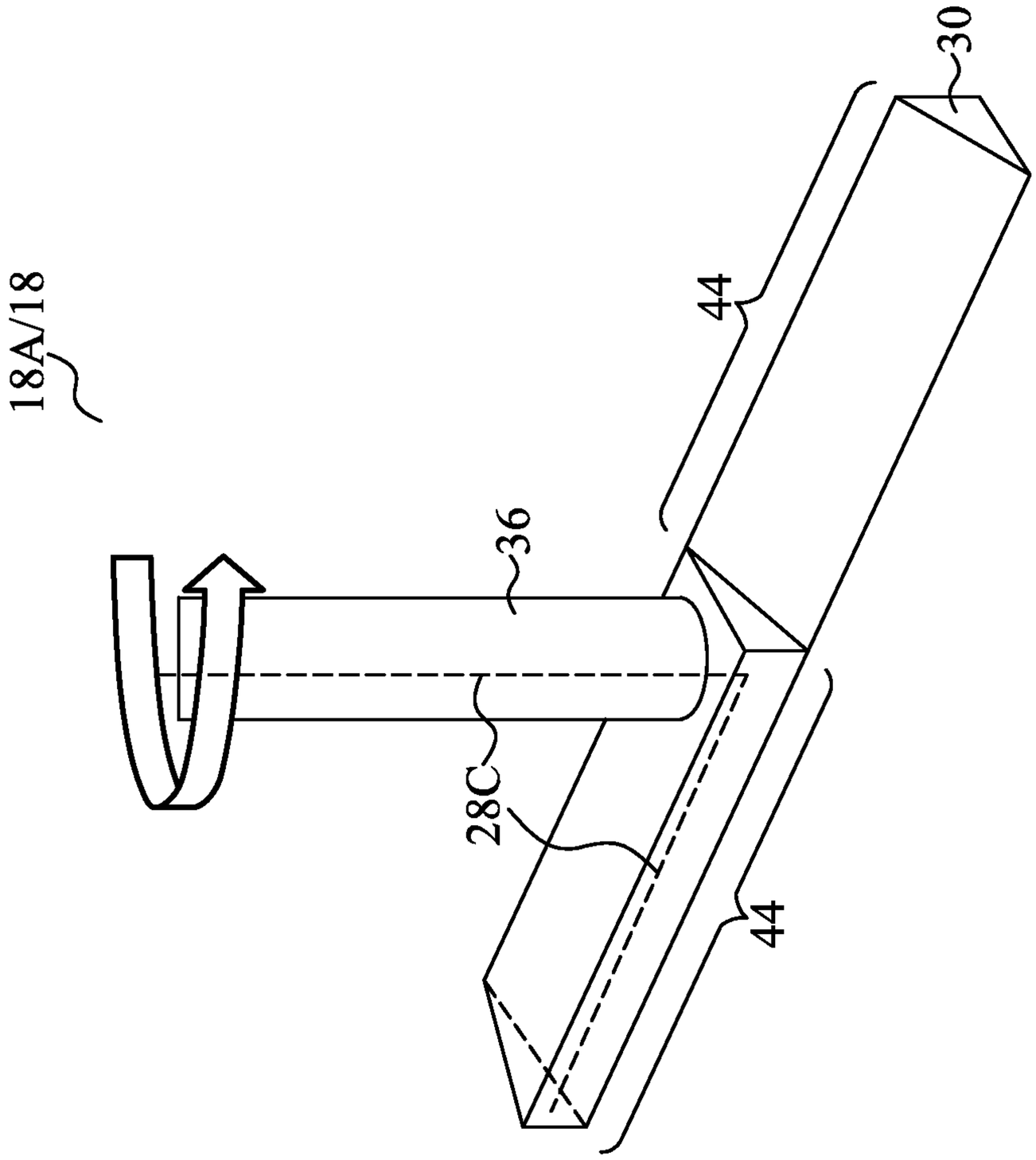


Fig. 5

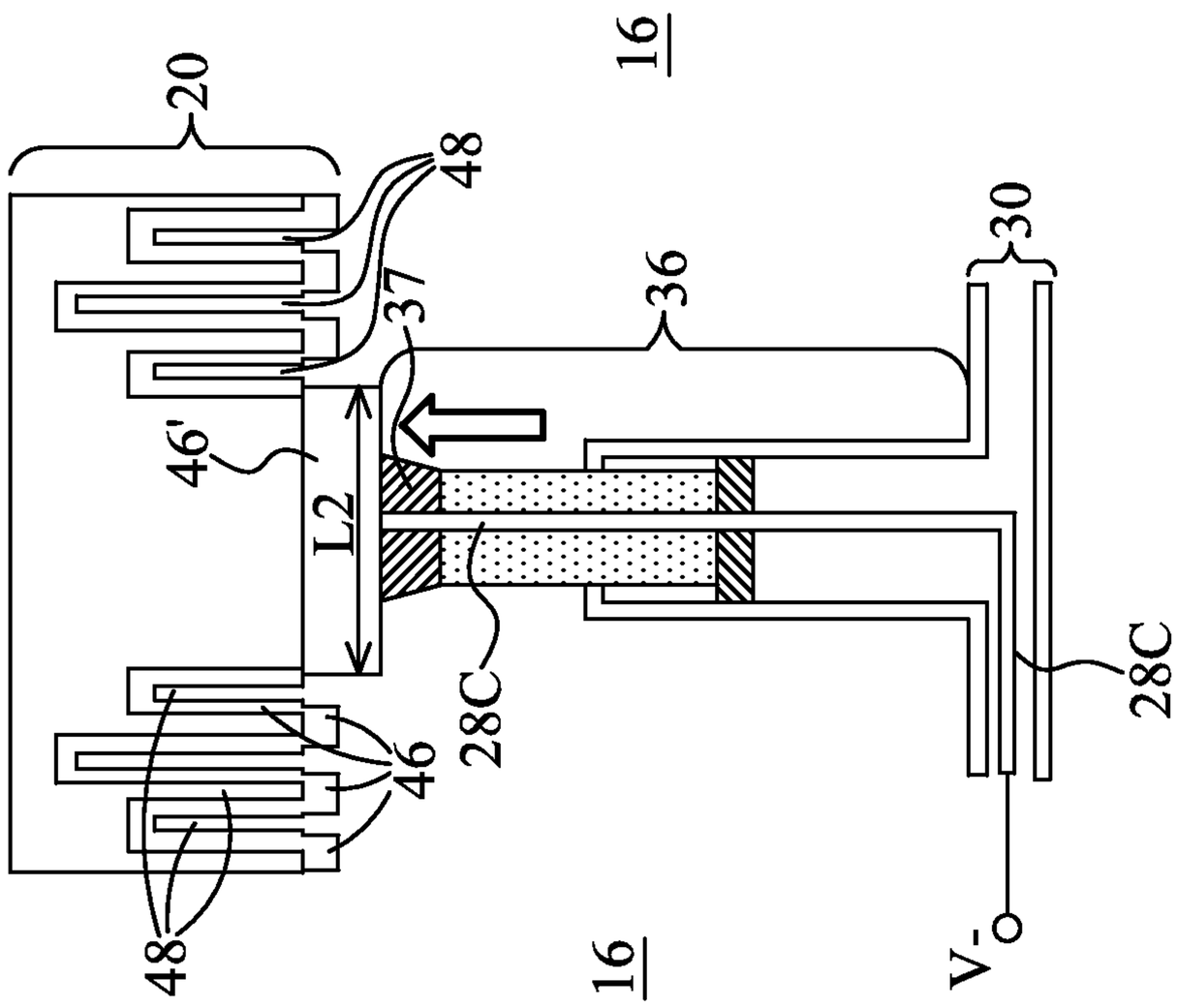


Fig. 6

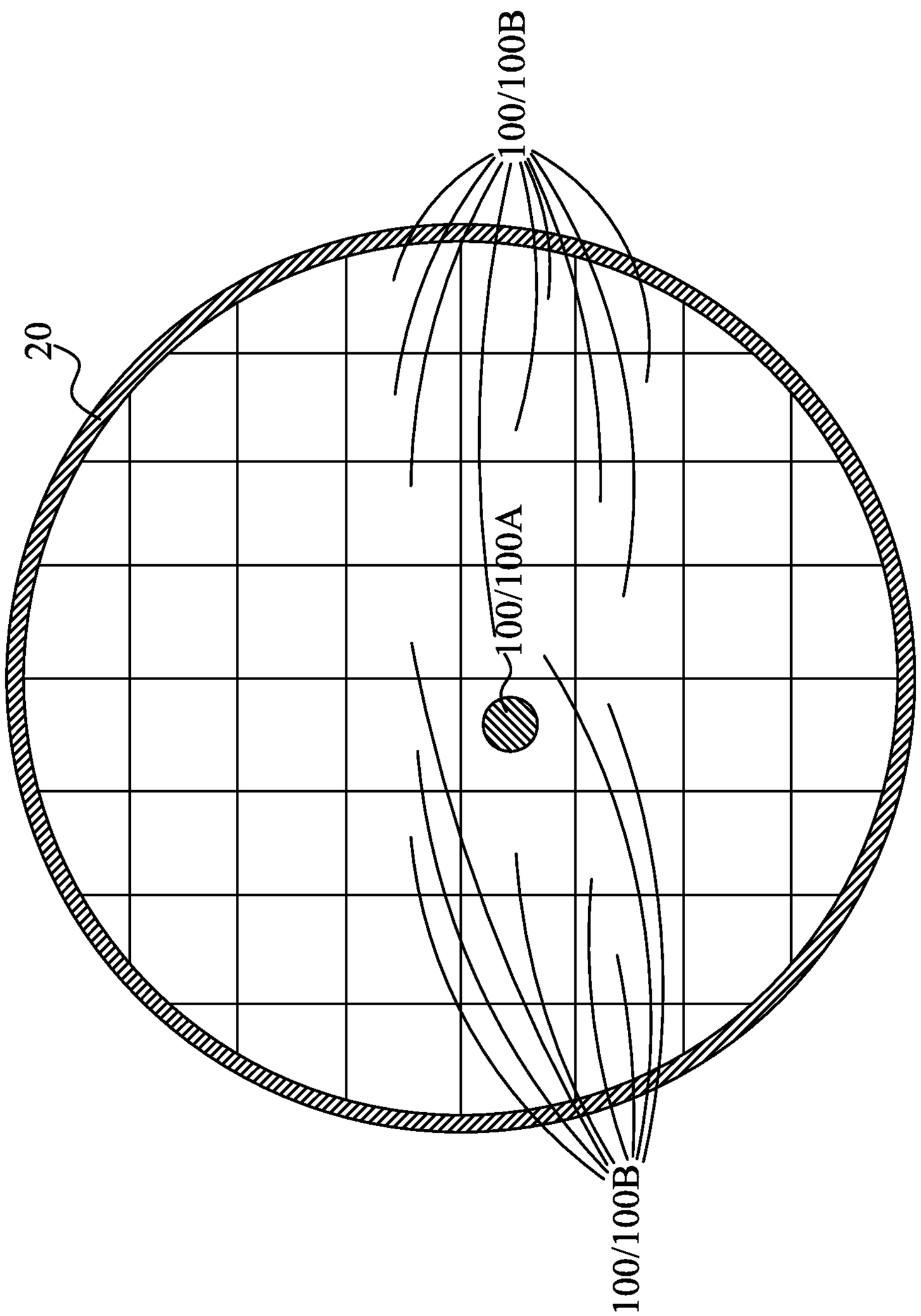


Fig. 7

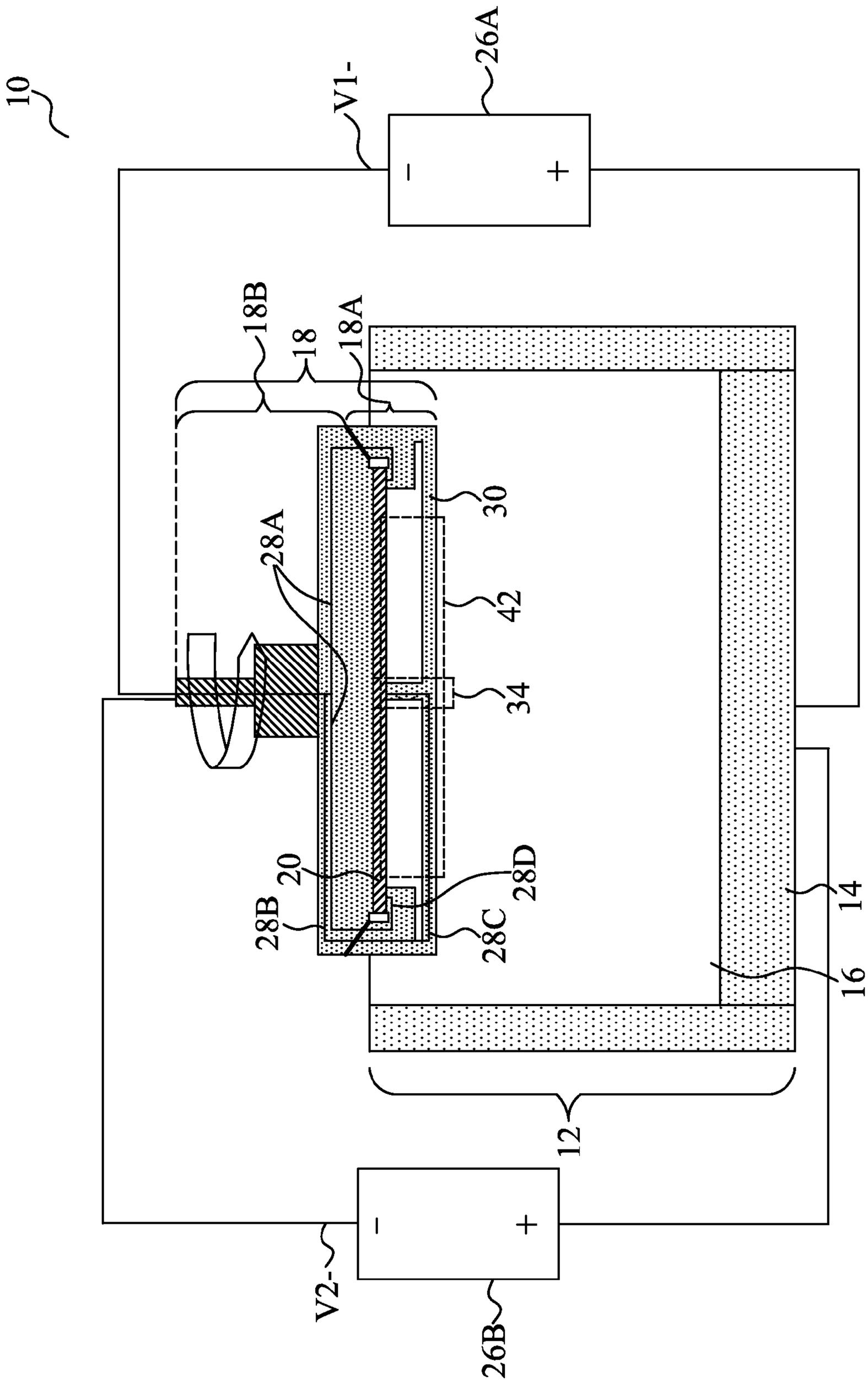


Fig. 8

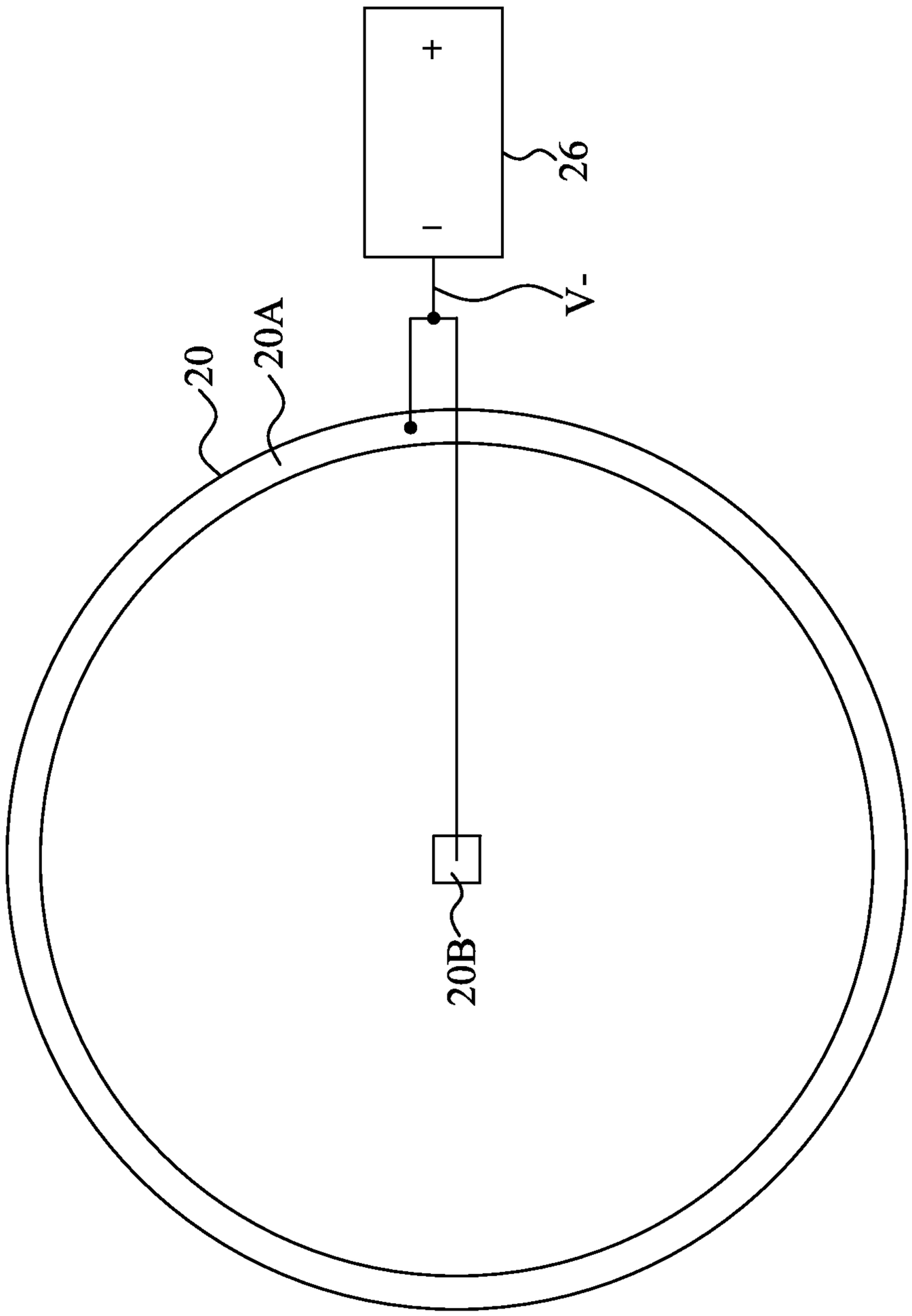


Fig. 9

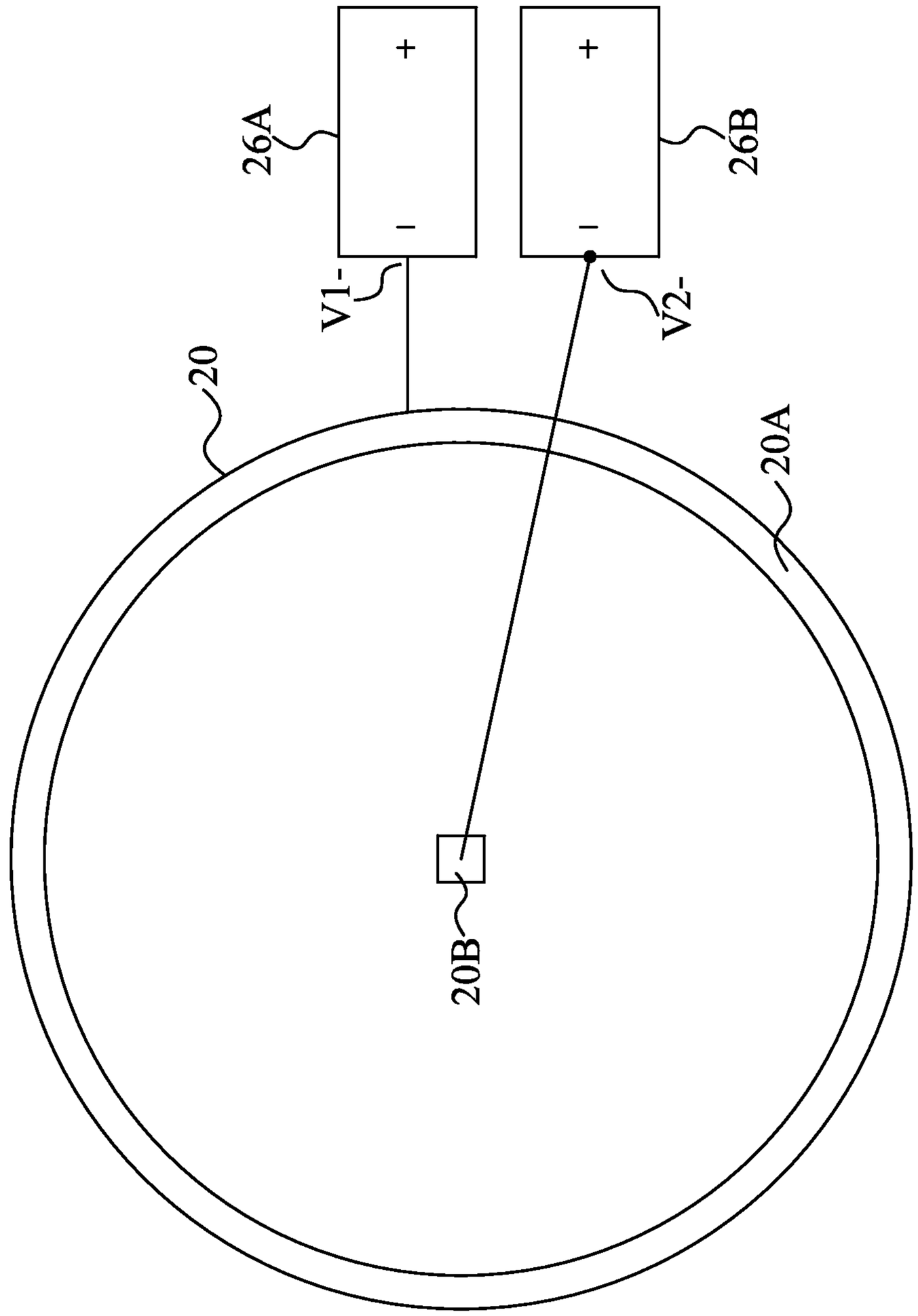


Fig. 10

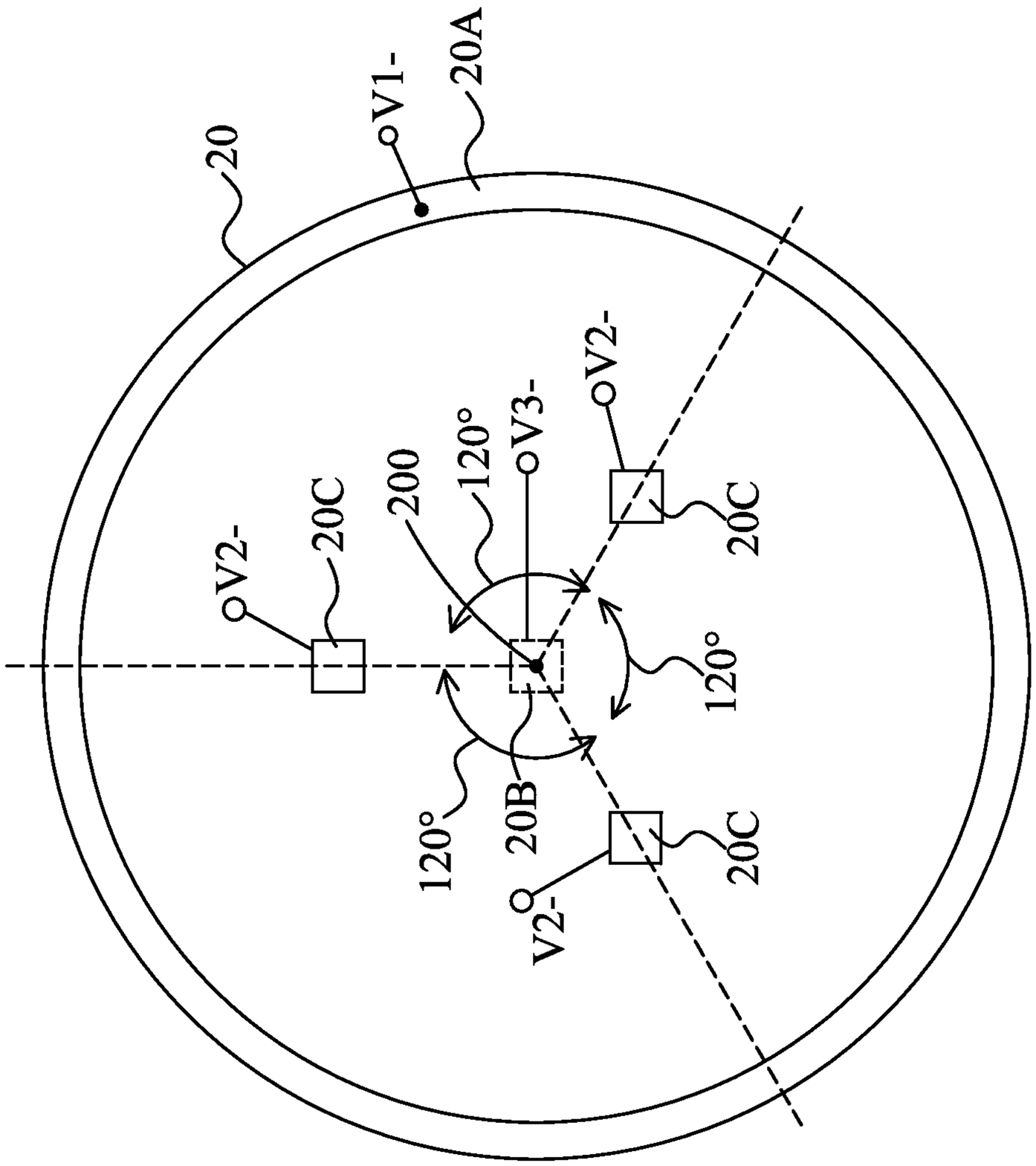


Fig. 11

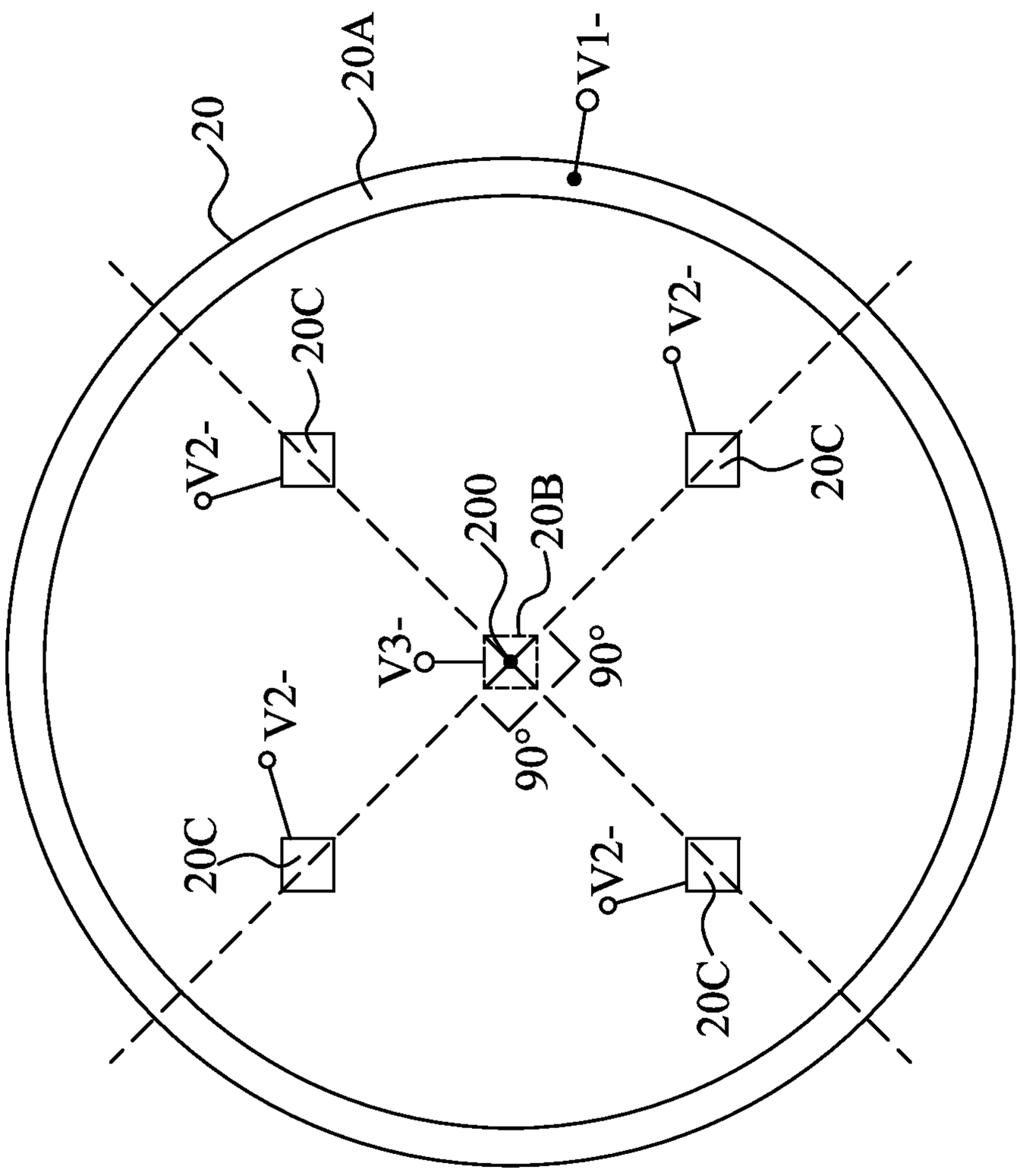


Fig. 12

ELECTRO-PLATING AND APPARATUS FOR PERFORMING THE SAME

This application claims the priority of the following provisionally filed U.S. patent application: Application Ser. No. 61/776,744, filed Mar. 11, 2013, and entitled "Electro-Plating and Apparatus for Performing the Same," which application is hereby incorporated herein by reference.

BACKGROUND

Electro-plating is a commonly used method for depositing metal and metal alloys onto semiconductor wafers. In a typical electro-plating process, the surface of a wafer is deposited with a blanket metal seed layer such as a copper seed layer. The surface of the wafer may have patterns, for example, trenches. In addition, the top surface of the wafer may also have a patterned mask layer to cover some portions of the metal seed layer, while the remaining portions of the metal seed layer are not covered. The metal is deposited on the portions of the metal seed layer that is not covered.

For performing the electro-plating, the wafer is mounted on a clamshell, which includes a plurality of electrical contacts in contact with the portions of the metal seed layer that are on the edge of the wafer. The wafer is placed into a plating solution. The metal seed layer is connected to a negative end of a DC power supply, so that the metal seed layer acts as the cathode. A metal plate, which provides the ions of the metal that is to be plated, acts as the anode, wherein the plating solution separates the anode from the cathode. When a voltage is applied between the cathode and the anode, the atoms in the metal plate are ionized and migrate into the plating solution. The ions are eventually deposited on the wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates a cross-sectional view of an apparatus for performing electro-plating in accordance with some exemplary embodiments;

FIG. **2** illustrates a top view of a wafer and electrical contacts contacting an edge portion of the wafer;

FIG. **3** illustrates a bottom view of a wafer and the portions of the wafer that are connected to electrical contacts in accordance with some embodiments;

FIG. **4** illustrates a magnified portion of a portion of a bottom piece of a wafer holder in accordance with some embodiments;

FIG. **5** illustrates a perspective view of a blade, which is a portion of the bottom piece of the wafer holder;

FIG. **6** illustrates how a portion of the metal seed layer that is in contact with an electrode;

FIG. **7** illustrates that a die of a wafer is used for the electrode to connect to the metal seed layer;

FIG. **8** illustrates a cross-sectional view of an apparatus for performing electro-plating in accordance with alternative embodiments, wherein two power supply sources are used for providing voltages to the wafer; and

FIGS. **9** through **12** illustrate various exemplary connection schemes for providing voltages to different portions of a wafer.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are illustrative, and do not limit the scope of the disclosure.

An electro-plating process and the apparatus for performing the same are provided in accordance with various exemplary embodiments. The variations and the operation of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

FIG. **1** illustrates a cross-sectional view of electro-plating apparatus **10**, which is used for plating a metal layer onto work piece **20**. Electro-plating apparatus **10** includes electro-plating solution container **12**, which holds plating solution **16**. Metal plate **14** is placed at the bottom of electro-plating solution container **12**. In some embodiments, metal plate **14** comprises the metal that is to be plated onto work piece **20**, which metal may include copper, aluminum, tungsten, nickel, and/or the like. Plating solution **16** may include sulfuric acid, hydrochloric acid, copper sulfate, and/or or the like.

Electro-plating apparatus **10** further includes work piece holder **18**, which is used to hold work piece **20**. In some embodiments, work piece **20** is a semiconductor wafer, on which integrated circuits are formed. In alternative embodiments, work piece **20** may be a dielectric wafer, an interposer wafer, a substrate strip, or another type of work piece. Throughout the description, work piece **20** is referred to as a wafer, although it may also be another type of integrated circuit component. Work piece holder **18** is accordingly referred to as a wafer holder.

Wafer holder **18** includes bottom piece **18**A, which include lip-seal **22** and electrical contact **24** as shown in FIG. **2**. FIG. **2** illustrates a top view of bottom piece **18**A and wafer **20**. Lip-seal **22** forms a full circle. A plurality of electrical contacts **24** are distributed at the edges of lip-seal **22**, and are aligned to a circle. The plurality of electrical contacts **24** may be distributed evenly along the circle. Wafer **20** is placed on lip-seal **22** and electrical contact **24**. The edge portion of wafer **20**, which edge portion forms a full ring, is in contact with a bottom surface of lip-seal **22** and electrical contacts **24**. Lip-seal **22** includes a relatively soft material such as rubber, so that when wafer **20** is pressed against lip-seal **22** by the top piece **18**B (FIG. **1**) of wafer holder **18**, wafer **20** and lip-seal **22** do not have gaps in between, and plating solution **16** (FIG. **1**) is confined below wafer **20**, as shown in FIG. **1**.

Referring back to FIG. **1**, top piece **18**B of wafer holder **18** includes electrical connection lines **28**A and **28**B embedded therein. Connection lines **28**A and **28**B are electrically coupled to the negative end (the cathode) of power supply source **26**, which may be a DC power source. Metal plate **14** is electrically coupled to the positive end (the anode) of power supply source **26**. Furthermore, bottom piece **18**A also includes electrical connection line **28**C, which is electrically connected to electrical connection line **28**B when top piece **18**B is assembled with bottom piece **18**A in order to hold wafer **20** therein. Electrical connection lines **28**A are electrically connected to electrical connection lines **28**D, which are electrically connected to electrical contacts **24** in FIG. **2**. Hence, voltage V− at the negative end of power supply source **26** is supplied to the bottom edge of wafer **20**.

In some embodiments, blade **30** is built as a part of bottom piece **18**A, and is mounted under wafer **20**. Blade **30** may be formed as an integrated component of bottom piece **18**A. Electrical connection line **28**C may be embedded in blade **30**. Through blade **30**, electrical connection line **28**C is connected to a center portion of wafer **20**, and hence voltage V− at the negative end of power supply source **26** is provided to the center portion of wafer **20**. During the plating, seed layer **46** (FIG. **6**) may be formed at the bottom surface of wafer **20**, and hence voltage V− of power supply source **26** is supplied to seed layer **46**.

As shown in FIG. **1**, during the plating of wafer **20**, wafer holder **18** is rotated. Wafer **20**, which has been fixed to wafer holder **18**, is also rotated along with wafer holder **18**. The atoms in metal plate **14** are ionized (and become ions) and migrate into electro-plating solution **16**. The metal ions are deposited on seed layer **46** (FIG. **6**) of wafer **20**. With the rotation of wafer holder **18**, the deposition is more uniform.

FIG. **3** illustrates a bottom view of wafer **20** and portions of wafer **20** that are connected to electrical contacts. Wafer **20** has bottom edge portion **20**A, which faces down (as in FIG. **1**) and are in contact with electrical contacts **24** in FIG. **2**. Furthermore, wafer **20** has bottom center region **20**B, which faces down (as in FIG. **1**) and are electrically connected to electrical connection line **28**C in FIG. **1**. Accordingly, the voltage V− at the negative end of power supply source **26** (FIG. **1**) is connected to both the edge portion **20**A and center portion **20**B. During the plating process, the deposition rates on different portions of wafer **20** are affected by the voltages on the respective portions of wafer **20**. If voltage V− is connected to wafer **20** only at the edge portions **20**A of wafer **20**, since metal seed layer **46** (FIG. **6**) has a resistance between edge portion **20**A and other portions of wafer **20**, there are voltage drops between edge portion **20**A and other portions. The voltages at portions **20**A and other portions (such as portion **20**B) are hence different from each other, resulting in different deposition rates on wafer **20**. In the embodiments of the present disclosure, with voltage V− also provided to center portion **20**B in addition to edge portion **20**A, the voltage across the entire wafer **20** is more uniform than if voltage V− is provided only to edge portion **20**A, and the deposition rates across wafer **20** are more uniform.

FIG. **4** illustrates a magnified portion of bottom piece **18**A of wafer holder **18** in FIG. **1**, wherein the magnified portion is portion **34** in FIG. **1**. As shown in FIG. **4**, bottom piece **18**A includes blade **30**, and retractable electrode **36** fixed onto blade **30**. Retractable electrode **36** includes outer shell **38**, which is fixed onto blade **30**, and cylinder **40**, which is movable in outer shell **38**. When cylinder **40** moves up and down in outer shell **38**, the length L**1** of retractable electrode **36** changes, so that connection line **28**C, which is also an electrical contact (electrode), is in contact with (the seed layer of) wafer **20** (FIG. **1**). The movement of cylinder **40** may be enabled through air pressure, a motor (not shown), or the like.

Retractable electrode **36** also includes seal ring **37** penetrated through by electrical contact **28**C. The top end of electrical contact **28**C and seal ring **37** are substantially co-planar, so that both electrical contact **28**C and seal ring **37** may be in physical contact with the surface of wafer **20** at the same time. Seal ring **37** may be formed of a flexible material such as rubber in some embodiments.

FIG. **5** illustrates a perspective view of blade **30**, wherein the illustrated structure is a magnified view of portion **42** in FIG. **1**. In some embodiments, blade **30** includes wings **44**, wherein the shape of wings **44** are specifically designed. When wafer holder **18** rotates, blade **30** (which is an integrated part of the bottom piece **18**A of wafer holder **18**) rotates accordingly. Blade **30** hence stirs plating solution **16** (FIG. **1**), so that the concentrations of the ingredients in electro-plating solution **16** (FIG. **1**) are more uniform. Hence, blade **30** has the function of the fluid field control.

FIG. **6** illustrates how electrical connection line **28**C is connected to seed layer **46** of wafer **20**. In accordance with some embodiments, seed layer **46**, which may a metal seed layer comprising copper, aluminum, nickel, tungsten, or the like, is deposited on wafer **20** through, for example, Physical Vapor Deposition (PVD). The surface of wafer **20** may be, or may not be, planar, depending on the respective plating process and the features to be formed by the plating process. For example, FIG. **6** illustrates that wafer **20** include trenches **48**, and seed layer **46** extends into trenches **48**. Seed layer **46** is deposited as a blanket layer covering the entire bottom surface of wafer **20**. As a result, when voltage V− of power supply source **26** (FIG. **1**) is applied to the edge portion and the center portion of seed layer **46**, the entire seed layer **46** is biased by voltage V−. The voltages on different portions of seed layer **46**, however, may be different from each other due to the resistance of seed layer **46**. This results in the non-uniformity of the deposition rates. For example, if voltage V− is applied only to the edge portions of seed layer **46**, then the plating rate at the edge portions is higher than the portions encircled by the edge portions. With the increasing down-scaling of integrated circuits, the thickness of seed layer **46** becomes increasingly smaller, and the resistance of seed layer **46** becomes increasingly greater. Hence, voltage V−, when applied to the center portion **20**B and edge portion **20**A (FIG. **3**) of wafer **20** simultaneously, the voltage difference on different portions of seed layer **46** may be reduced.

Referring again to FIG. **6**, in some embodiments, in order for electrical contact **28**C to be in good contact with seed layer **46**, and for seal ring **37** to seal plating solution **16** from reaching electrical contact **28**C, seed layer **46** is designed to have a planar surface at least as large as seal ring **37**, or slightly larger. In some embodiments, seed layer pad **46'** has lateral dimension L**2** greater than about 10 mm. It is appreciated that a typical wafer may not have such a large metal pad. In accordance with some embodiments, a chip in wafer **20** may be dedicated to the formation of seed layer pad **46'**. For example, FIG. **7** illustrates an exemplary top view of wafer **20**, which includes a plurality of chips **100** (including chip **100**A and chips **100**B). Chip **100**A is dedicated to the formation of large metal pad seed layer pad **46'** (FIG. **6**), and hence the pattern of seed layer **46** in chip **100**A is different from the pattern of seed layer **46** in chips **100**B. Alternatively stated, chips **100**B are identical to each other, and have structures different from that of chip **100**A. In some embodiments, an entirety of or a major portion of chip **100**A is used for forming a large seed layer pad **46'**, which has the size substantially the same as the size of chip **100**A.

Referring back to FIG. **6**, before a plating process is started, retractable electrode **36** is pushed toward wafer **20**, so that electrical contact **28**C is in physical and electrical contact with seed layer pad **46'**. Seal ring **37** seals electrical contact **28**C, so that plating solution **16** is not in contact with electrical contact **28**C, and no metal will be plated on electrical contact **28**C. Through the contact scheme in FIG. **6**, a good contact may be established to supply voltage V− to seed layer **46**.

FIG. **8** illustrates electro-plating apparatus **10** and the plating process in accordance with alternative embodiments. Unless specified otherwise, the materials and formation

methods of the components in these embodiments are essentially the same as the like components, which are denoted by like reference numerals in the embodiments shown in FIGS. **1** through **7**. The details regarding the formation process and the materials of the components shown in these embodiments may thus be found in the discussion of the embodiment shown in FIGS. **1** through **7**. The embodiments in FIG. **8** are similar to the embodiments in FIG. **1**, except that the edge portion and the center portion of wafer **20** are connected to different voltage supply sources **26**A and **26**B, which provide voltages V**1**− and V**2**−, respectively. Voltage supply sources **26**A and **26**B may have different voltages. For example, voltage V**1**− may be in the range of about 1V to about 10V, and voltage V**2**− may be in the range of about 5V to about 10V. By making voltages V**1**− and V**2**− to be adjustable separately, the plating thickness profile on wafer **20** may be adjusted. Voltage V**1**− may be greater than, substantially equal to, or lower than, voltage V**2**− in some embodiments.

FIGS. **9** through **12** illustrate schemes for applying voltages in accordance with various embodiments. In FIG. **9**, edge portion **20**A of wafer **20** and center portion **20**B of wafer **20** are applied with the same voltage. These embodiments may be achieved using electro-plating apparatus **10** shown in FIG. **1**. In FIG. **10**, edge portion **20**A and center portion **20**B are applied with different voltages V**1**− and V**2**−, respectively, wherein voltages V**1**− and V**2**− are provided by voltage supply sources **26**A and **26**B, respectively. These embodiments may be achieved using electro-plating apparatus **10** shown in FIG. **8**.

FIG. **11** illustrates the voltage application scheme in accordance with yet another embodiment, wherein wafer portions **20**C may be applied with a voltage separately. The voltage applying scheme may be similar to what is shown in FIG. **6**, for example. In these embodiments, wafer portions **20**C are between center **200** of wafer **20** and edge portion **20**A. Wafer portions **20**C may be distributed with a rotational symmetric pattern, for example, with the lines connecting wafer portions **20**C to the center **200** of wafer **20** forming 120-degree angles. Furthermore, wafer portions **20**C may have substantially equal distances from center **200** of wafer **20**. In accordance with some embodiments, no additional voltage is applied to wafer center portion **20**B. In alternative embodiments, an additional voltage V**3**− is applied to wafer center portion **20**B. Voltages V**1**−, V**2**−, and V**3**−, which are provided to portions, **20**A, **20**B, and **20**C, respectively, may be the same as each other, or may be different from each other.

FIG. **12** illustrates the voltage application scheme in accordance with yet alternative embodiments. These embodiments are similar to the embodiments in FIG. **11**, except there are four wafer portions **20**C applied with voltages V**3**. In these embodiments, wafer portions **20**C may be symmetric, for example, with the lines connecting wafer portions **20**C to center **200** of wafer **20** forming 90-degree angles. Furthermore, wafer portions **20**C may have substantially equal distances from center **200** of wafer **20**. In accordance with some embodiments, no additional voltage is applied to wafer center portion **20**B. In alternative embodiments, an additional voltage V**3**− is applied to wafer center **20**B. Voltages V**1**−, V**2**−, and V**3**− may be the same as each other, or may be different from each other.

In the embodiments of the present disclosure, voltages are applied to different portions of the work piece during the plating process. Hence, the uniformity of the thicknesses of the plated metal layer is improved. In addition, a blade may be added for the fluid field control, so that the uniformity of the plating process is further improved. The capability of applying different voltages onto different portions of the work pieces results in the desirable ability for adjusting the profile of the plated metal layer.

In accordance with some embodiments, a method of plating a metal layer on a work piece includes exposing a surface of the work piece to a plating solution, and supplying a first voltage at a negative end of a power supply source to an edge portion of the work piece. A second voltage is supplied to an inner portion of the work piece, wherein the inner portion is closer to a center of the work piece than the edge portion. A positive end of the power supply source is connected to a metal plate, wherein the metal plate and the work piece are spaced apart from each other by, and are in contact with, the plating solution.

In accordance with other embodiments, a method of plating a metal layer on a wafer through electro-plating includes exposing a surface of the wafer to a plating solution, and supplying a first voltage to an edge portion of the wafer. The first voltage is connected through a plurality of electrical contacts that are in contact with the edge portion of the wafer. The plurality of electrical contacts is aligned to a ring adjacent to an edge of the wafer. A second voltage is supplied to a center portion of the wafer. During the plating, the wafer acts as a cathode, and a metal plate acts as an anode, with a metal in the metal plate being plated to the wafer.

In accordance with yet other embodiments, an apparatus is configured to perform electro-plating on a wafer. The apparatus includes a first electrical contact configured to contact an edge portion of the wafer, and a power supply source electrically connected to the first electrical contact. The power supply source is configured to supply a voltage to the edge portion of the wafer. A second electrical contact is configured to contact an inner portion of the wafer, wherein the inner portion of the wafer is encircled by the edge portion of the wafer.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A method comprising:

plating a metal layer on a work piece, wherein the plating comprises:

exposing a surface of the work piece to a plating solution;

supplying a first voltage at a negative end of a first power supply source to an edge portion of the work piece;

contacting an electrical connection line of a retractable electrode with the work piece, wherein the retractable electrode comprises:

a cylinder comprising a seal ring and the electrical connection line encircled by the seal ring; and

an outer shell having a portion of the cylinder therein, wherein a length of the cylinder out of the outer shell is adjusted to contact the electrical connection line with the work piece;

supplying a second voltage to a first inner portion of the work piece through the electrical connection line, wherein the first inner portion is closer to a center of the work piece than the edge portion; and

connecting a positive end of the first power supply source to a metal plate, wherein the metal plate and the work piece are spaced apart from each other by, and are in contact with, the plating solution.

2. The method of claim **1**, wherein the first inner portion of the work piece is a center portion of the work piece.

3. The method of claim **1**, wherein the first inner portion of the work piece is comprised in a first chip of the work piece, wherein the first chip of the work piece has a surface profile different from surface profiles of a plurality of chips in the work piece, and wherein the first chip comprises a planar contact pad, with the first voltage applied on the planar contact pad through an electrical contact.

4. The method of claim **3**, wherein when the electrical contact is in physical contact with the planar contact pad, the planar contact pad is sealed by the seal ring, and wherein the seal ring is in contact with the planar contact pad.

5. The method of claim **1**, wherein the first voltage is substantially equal to the second voltage.

6. The method of claim **5**, wherein the second voltage is supplied by the first power supply source.

7. The method of claim **1**, wherein the first voltage is different from the second voltage, and wherein the second voltage is supplied by a second power supply source different from the first power supply source.

8. The method of claim **1** further comprising, when the plating is performed:

rotating the work piece; and

stirring the plating solution using a blade that is rotated together with the work piece.

9. A method comprising:

plating a metal layer on a wafer through electro-plating, wherein the electro-plating comprises:

exposing a surface of the wafer to a plating solution;

supplying a first voltage to an edge portion of the wafer, wherein the first voltage is connected through a plurality of electrical contacts that are in contact with the edge portion of the wafer, and wherein the plurality of electrical contacts is aligned to a ring adjacent to an edge of the wafer;

supplying a second voltage to a center portion of the wafer, wherein during the plating, the wafer acts as a cathode, and a metal plate acts as an anode, with a metal in the metal plate being plated to the wafer; and

stirring the plating solution using a blade that is rotated together with the wafer, wherein the blade comprises a vertical surface substantially perpendicular to a direction of rotation, and a major slant surface neither perpendicular to nor parallel to the vertical surface.

10. The method of claim **9** further comprising supplying the second voltage to the wafer through an electrical connection line embedded in the blade.

11. The method of claim **9** further comprising connecting a third voltage to a portion of the wafer, wherein the portion of the wafer is between the center portion of the wafer and the edge portion of the wafer.

12. The method of claim **9**, wherein the center portion of the wafer is comprised in a center chip of the wafer, wherein the center chip of the wafer has a surface profile different from surface profiles of a plurality of chips in the wafer, and wherein the center chip comprises a planar contact pad, with the first voltage applied on the planar contact pad.

13. The method of claim **9**, wherein the blade has a triangular shape in a cross-sectional view of the blade.

14. A method comprising:

contacting a plurality of edge portions of a front surface of a wafer to a plurality of electrical contacts;

contacting a center portion of the front surface of the wafer to an additional electrical contact by adjusting a length of a cylinder protruding out of an outer shell of a retractable electrode, wherein the additional electrical contact is a part of the cylinder; and

plating a metal layer on the front surface of the wafer, wherein during the plating, first voltages are applied on the plurality of electrical contacts and the additional electrical contact, and a second voltage higher than the first voltages is applied on a metal plate, wherein the metal plate and the wafer are spaced apart from each other by, and are in contact with, a plating solution.

15. The method of claim **14**, wherein the center portion has equal distances to the plurality of electrical contacts.

16. The method of claim **14**, wherein the plurality of electrical contacts and the additional electrical contact are supplied with different voltages.

17. The method of claim **14** comprising, when the plating is performed:

stirring the plating solution using a blade that is rotated together with the wafer, wherein the blade comprises a vertical surface substantially perpendicular to a direction of rotation, and a major slant surface neither perpendicular to nor parallel to the vertical surface.

18. The method of claim **14**, wherein the additional electric contact is a part of the retractable electrode, and the retractable electrode comprises a seal ring encircling the additional electrical contact, wherein the seal ring comprises a flexible material, and a surface of the additional electrical contact is co-planar with a surface of the seal ring.

19. The method of claim **18**, wherein the retractable electrode is fixed onto the wafer when the wafer is rotated.

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