US009484746B2

(12) **United States Patent**
Tang et al.

(10) **Patent No.: US 9,484,746 B2**
(45) **Date of Patent: Nov. 1, 2016**

(54) **POWER CONVERTER CIRCUIT WITH AC OUTPUT**

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(73) Assignee: **Infineon Technologies Austria AG**, Villach (AT)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 989 days.

(21) Appl. No.: **13/352,202**

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(51) **Int. Cl.**

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H02J 3/38	(2006.01)
H02M 7/5387	(2007.01)
H02M 1/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H02J 3/383*** (2013.01); ***H02M 7/53871*** (2013.01); *H02M 2001/0074* (2013.01); *H02M 2001/0077* (2013.01); *Y02E 10/563* (2013.01); *Y10T 307/707* (2015.04)

(58) **Field of Classification Search**

CPC H02J 3/383; H02M 7/53871; H02M 2001/0074; H02M 2001/0077; Y10T 307/707; Y02E 10/563

USPC 307/82

See application file for complete search history.

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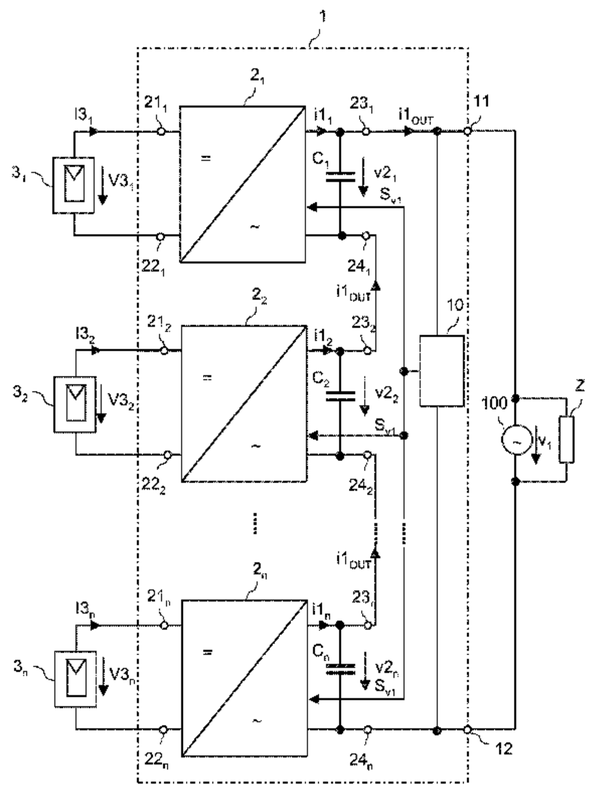
Primary Examiner — Daniel Cavallari

(74) *Attorney, Agent, or Firm* — Slater Matsil, LLP

(57) **ABSTRACT**

A power converter circuit includes output terminals configured to receive an external AC voltage. At least one series circuit has at least two converter units. Each converter unit includes input terminals configured to be coupled to a DC power source. Output terminals provide an AC output current. The at least one series circuit is connected between the output terminals of the power converter circuit. A voltage measurement circuit is connected between the output terminals of the power converter circuit and configured to provide at least one measurement signal that includes information related to phase and frequency of the external AC voltage. At least one of the converter units is configured to receive the at least one measurement signal and is configured to regulate the generation of the AC output current dependent on the at least one measurement signal.

27 Claims, 15 Drawing Sheets



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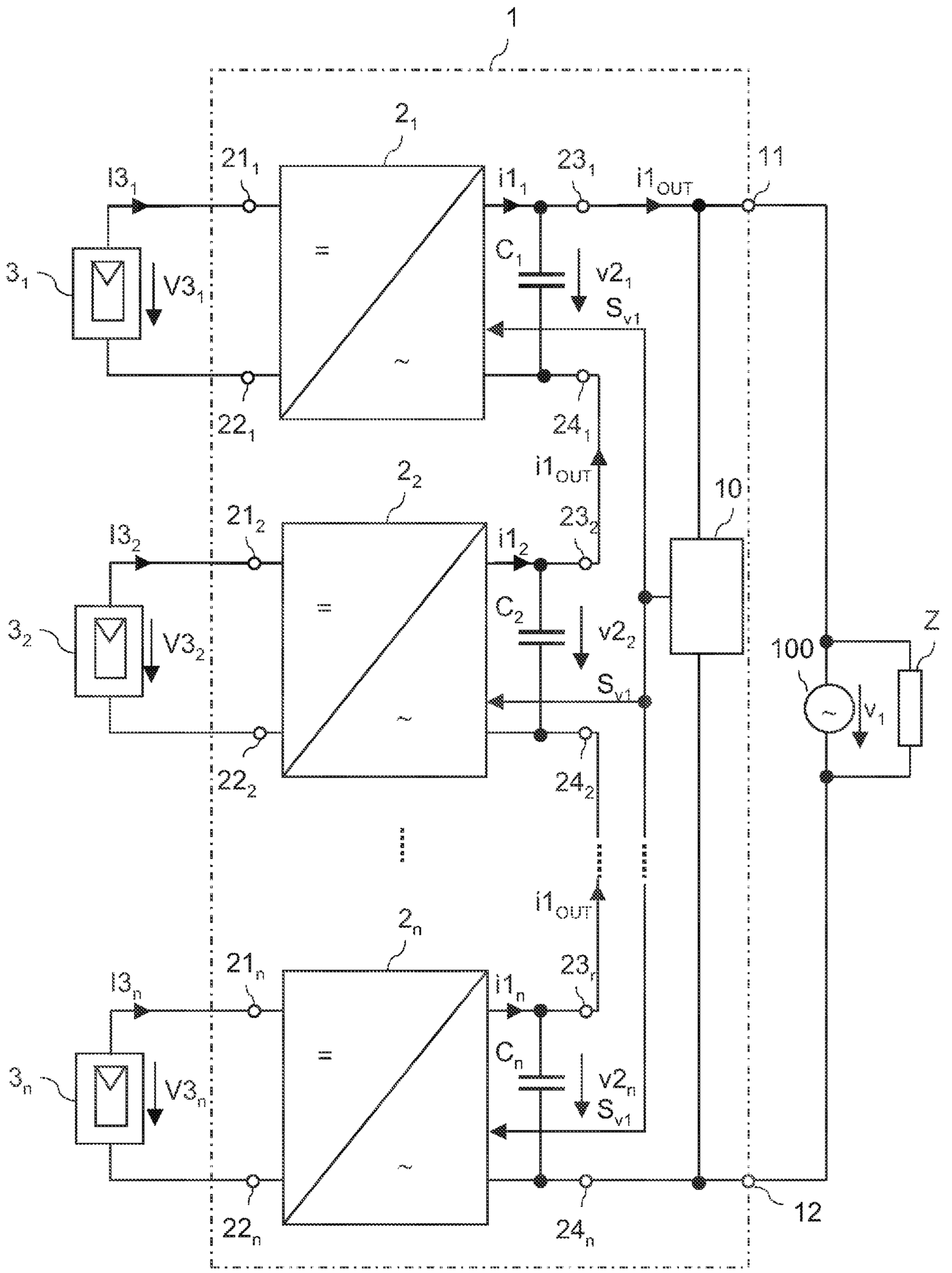
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i1₁
23₁
i1OUT
11
3₁
V3₁
C₁
v2₁
Sv1
22₁
24₁
i1OUT
2₂
21₂
i3₂
i1₂
23₂
10
3₂
V3₂
C₂
v2₂
Sv1
100
Z
V1
22₂
24₂
i1OUT
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Cn
v2n
Sv1
22n
24n
12

FIG 1

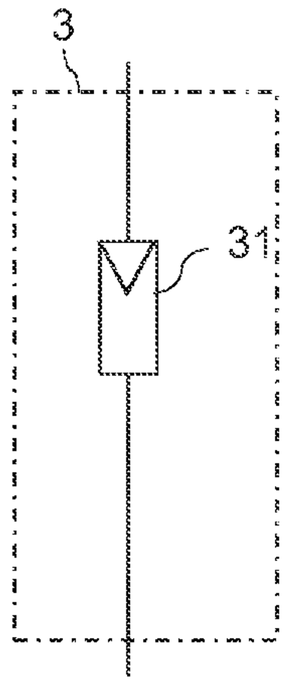


FIG 2A

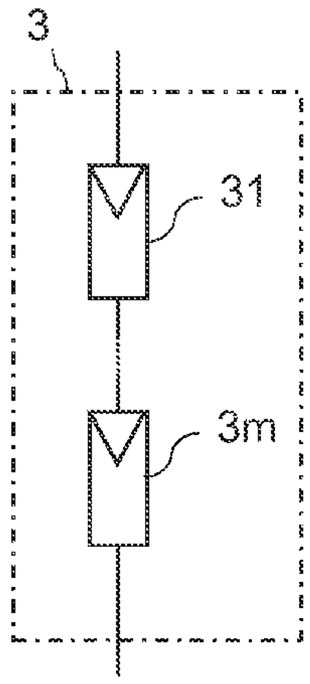


FIG 2B

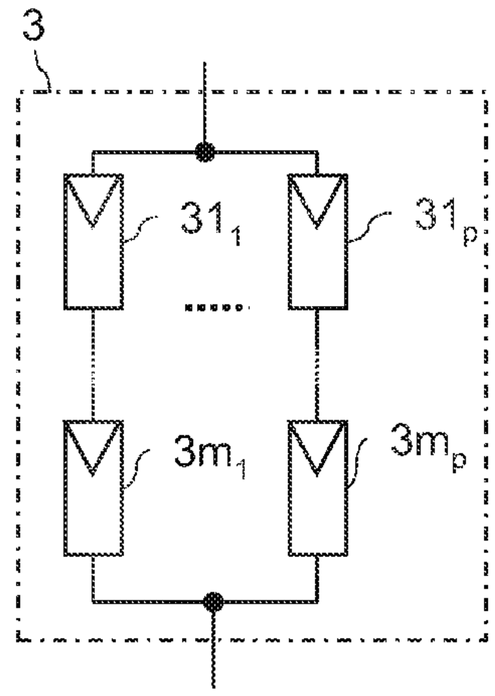


FIG 2C

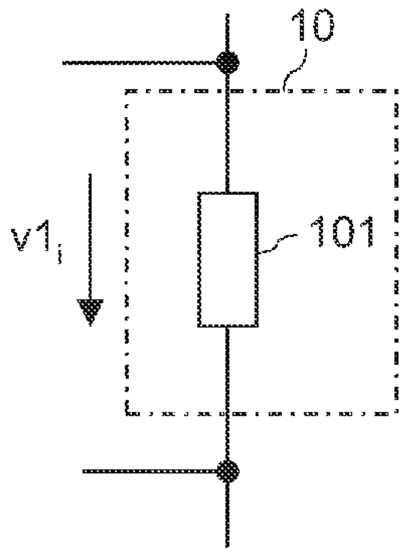


FIG 4A

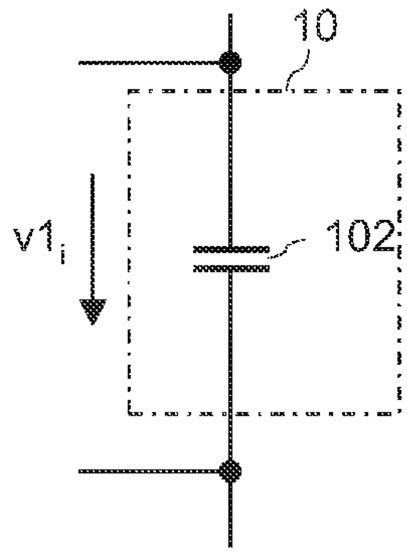


FIG 4B

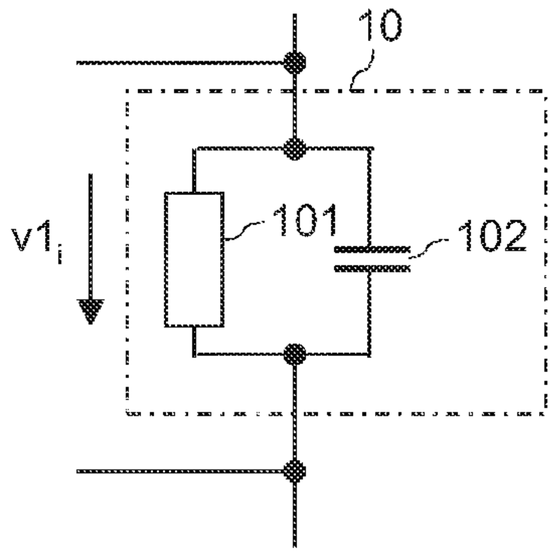


FIG 4C

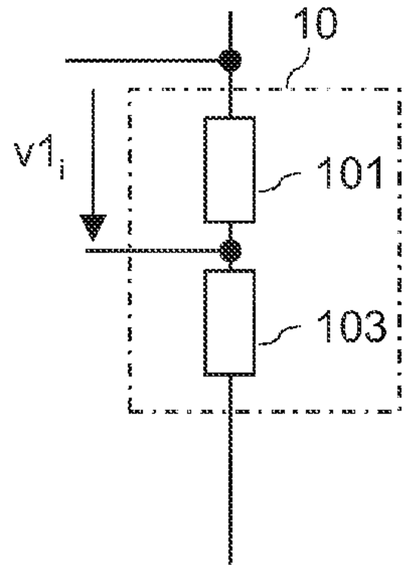
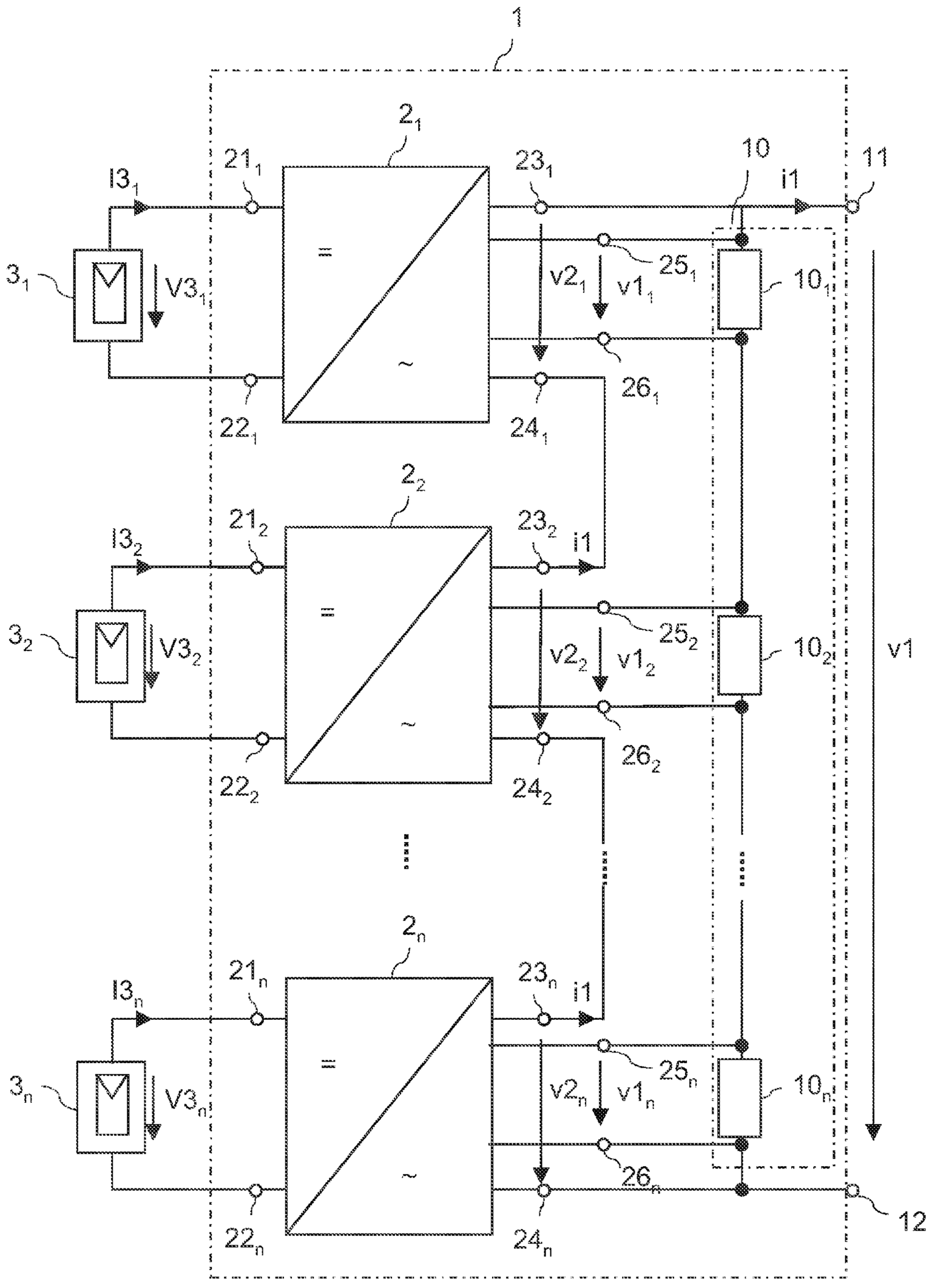


FIG 4D


1
2₁
21₁
23₁
10
i1
11
I3₁
3₁
V3₁
=
~
v2₁
v1₁
25₁
10₁
26₁
22₁
24₁
2₂
21₂
23₂
I3₂
i1
3₂
V3₂
25₂
v2₂
v1₂
10₂
v1
26₂
22₂
24₂
2ₙ
21ₙ
23ₙ
I3ₙ
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10ₙ
26ₙ
22ₙ
24ₙ
12

FIG 3

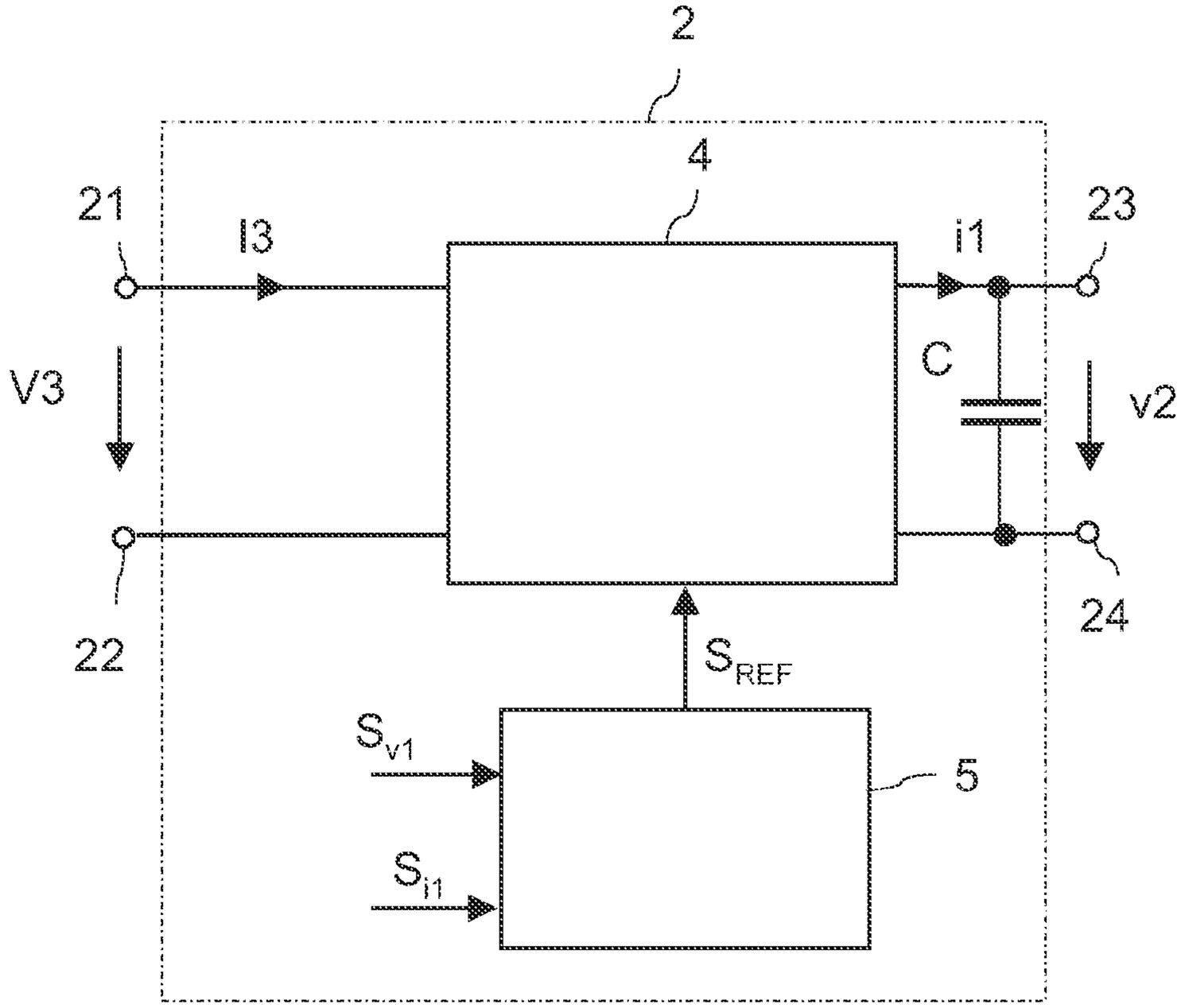


FIG 5

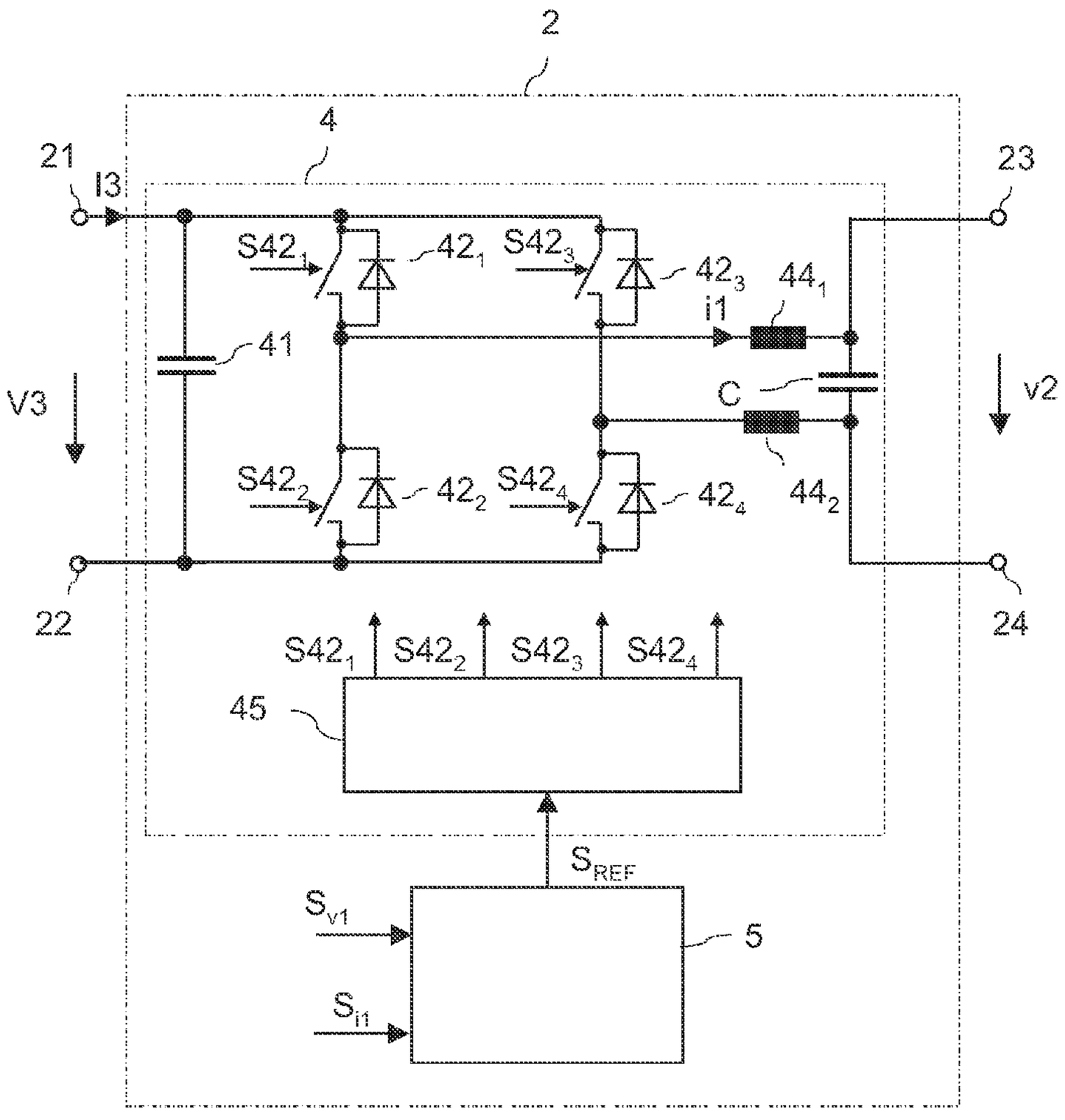


FIG 6

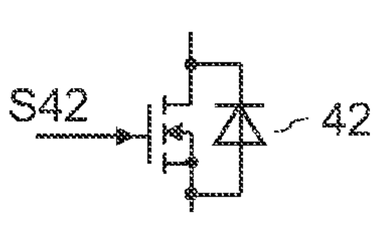


FIG 7A

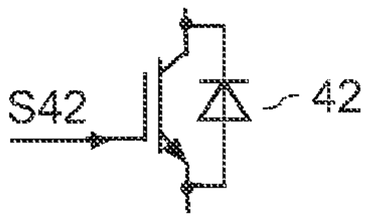


FIG 7B

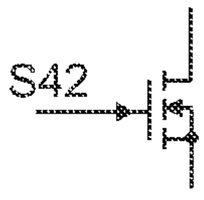


FIG 7C

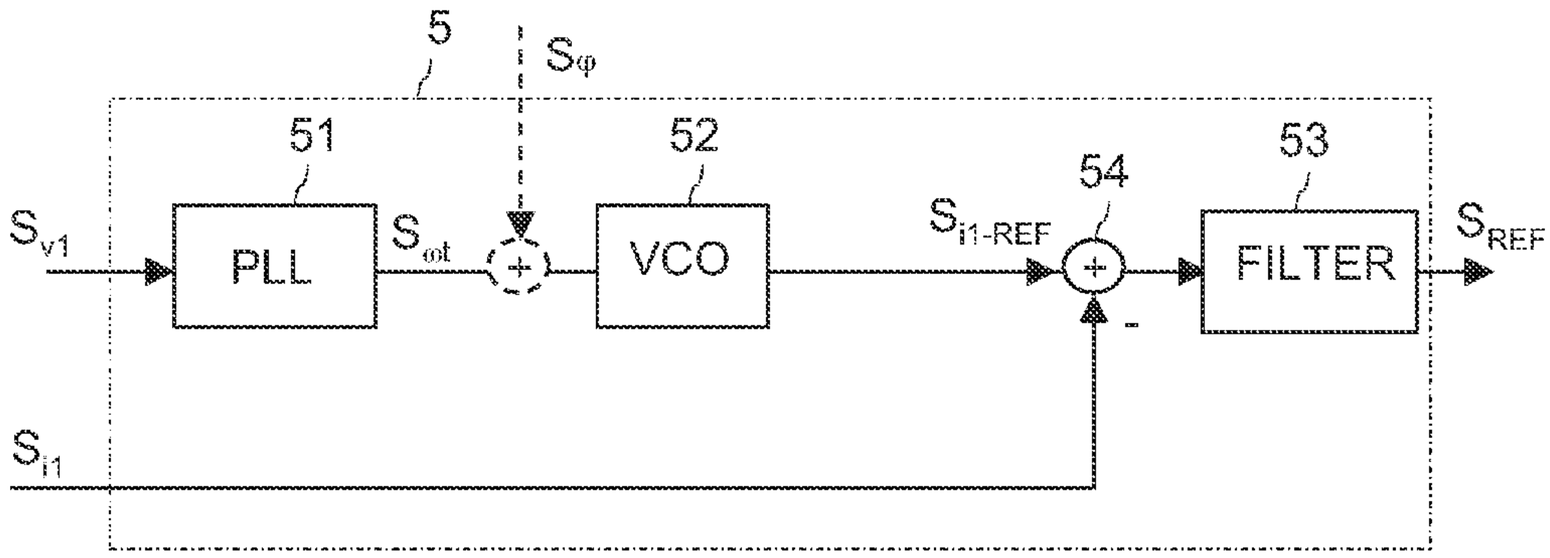


FIG 8

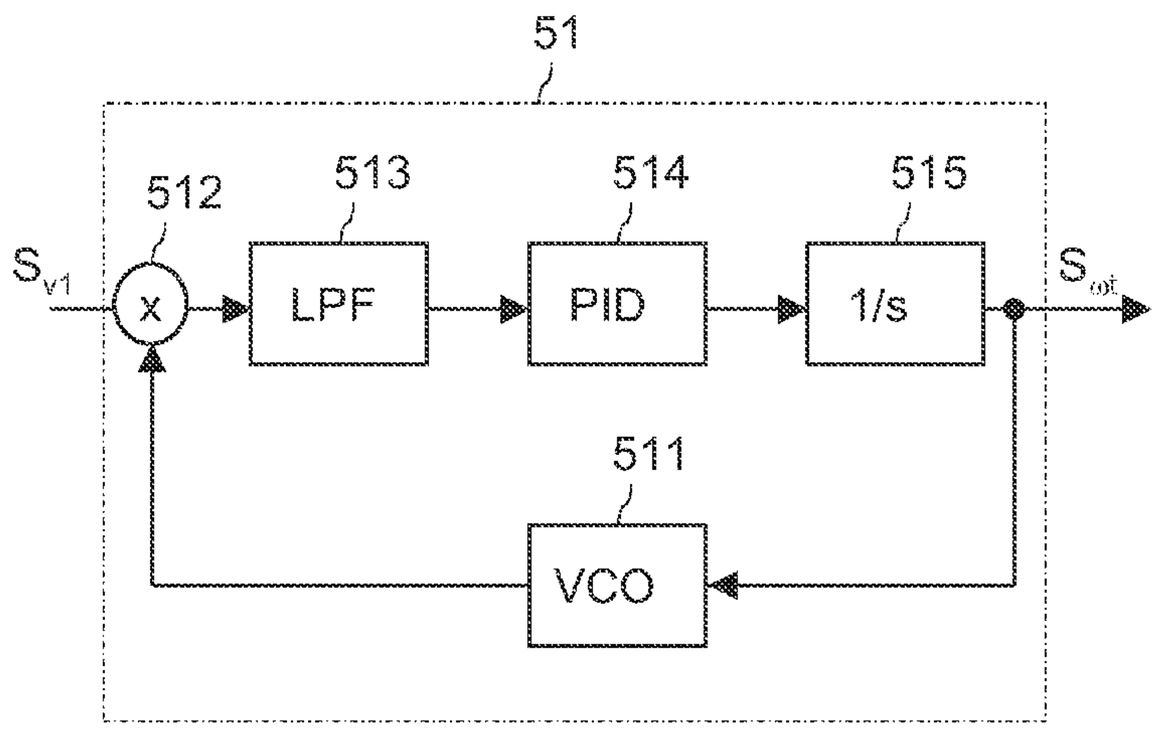
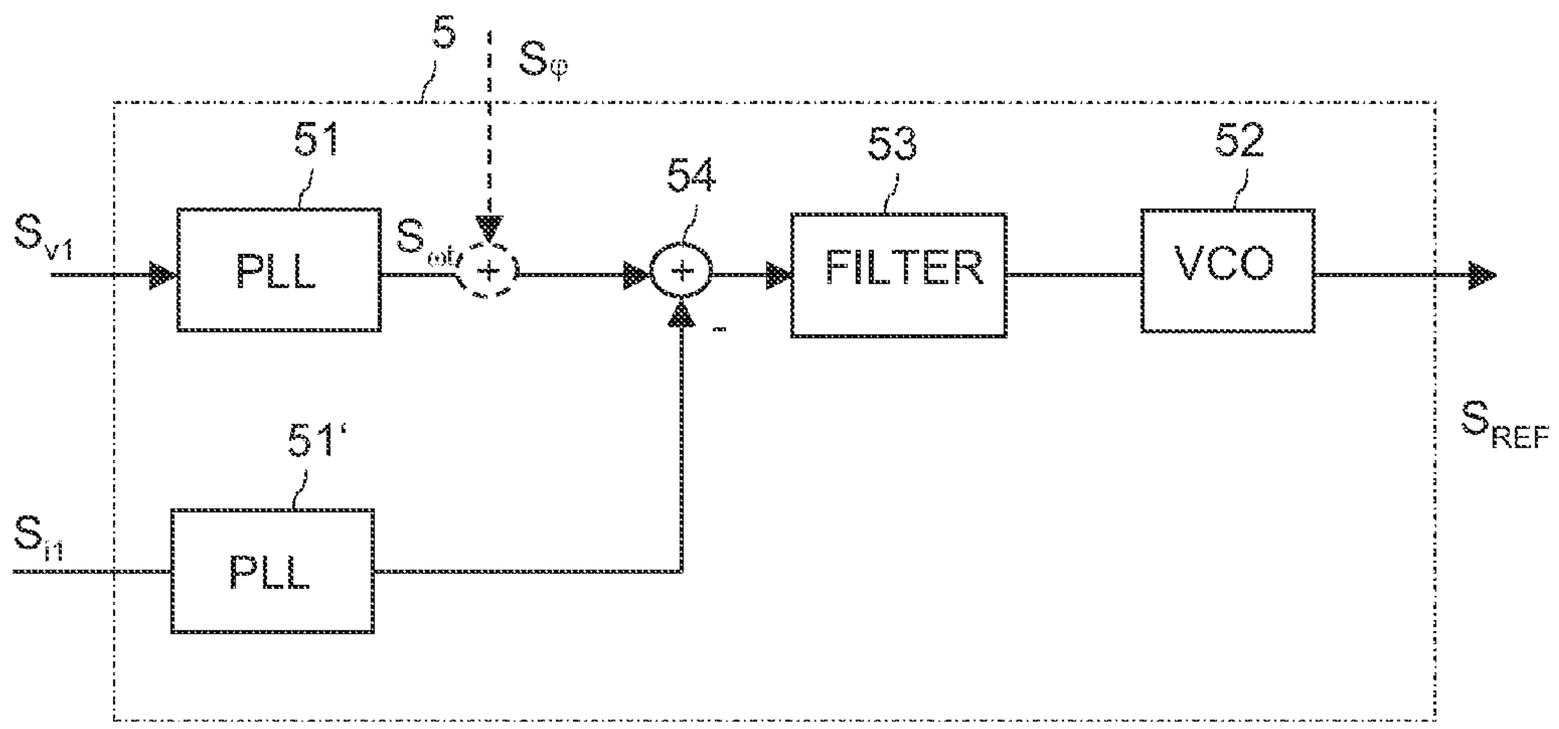


FIG 9



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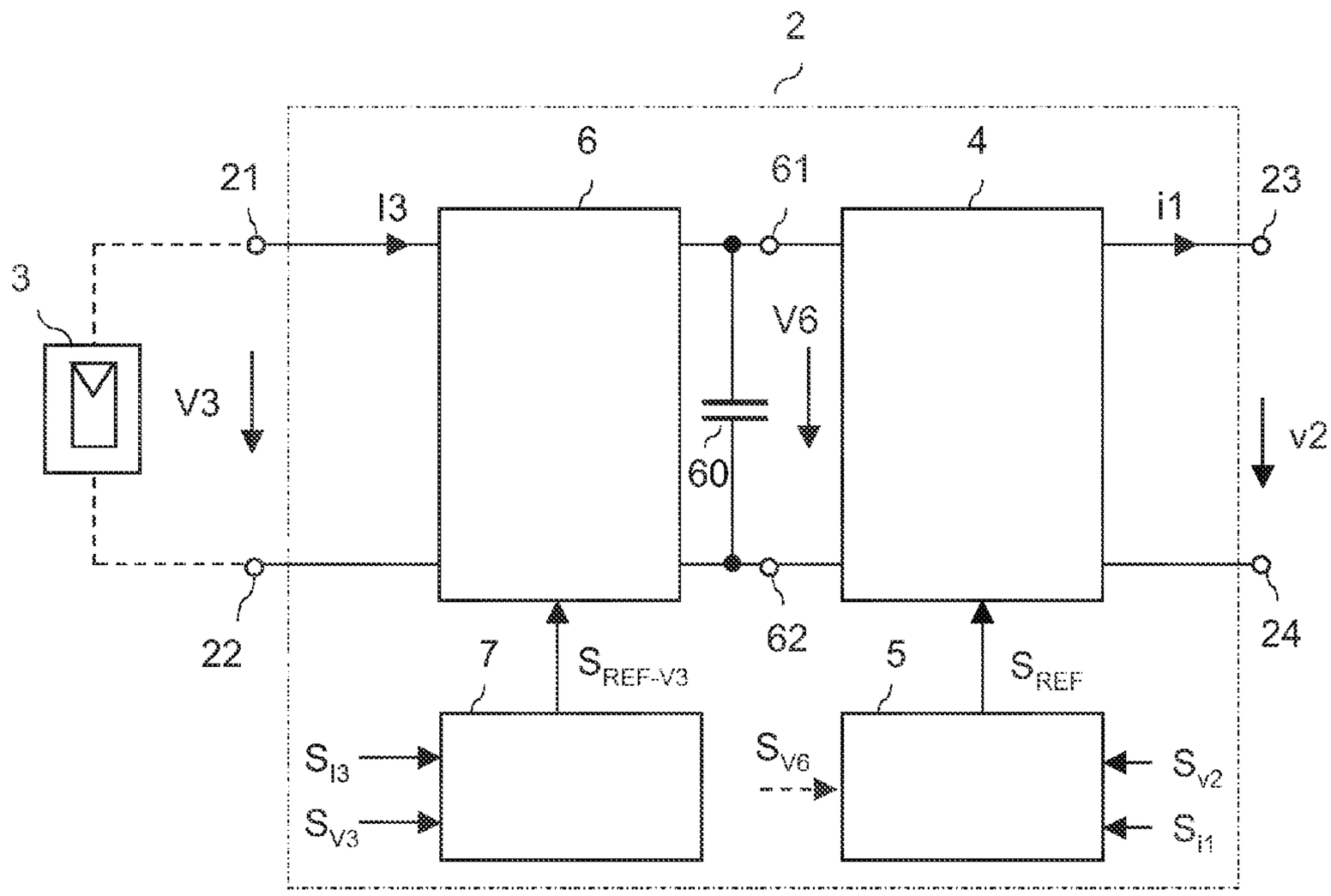
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6
4
21
I3
61
i1
23
3
V6
V3
60
v2
22
62
24
7
S_{REF-V3}
5
S_{REF}
S_{I3}
S_{V6}
S_{V2}
S_{V3}
S_{I1}

FIG 11

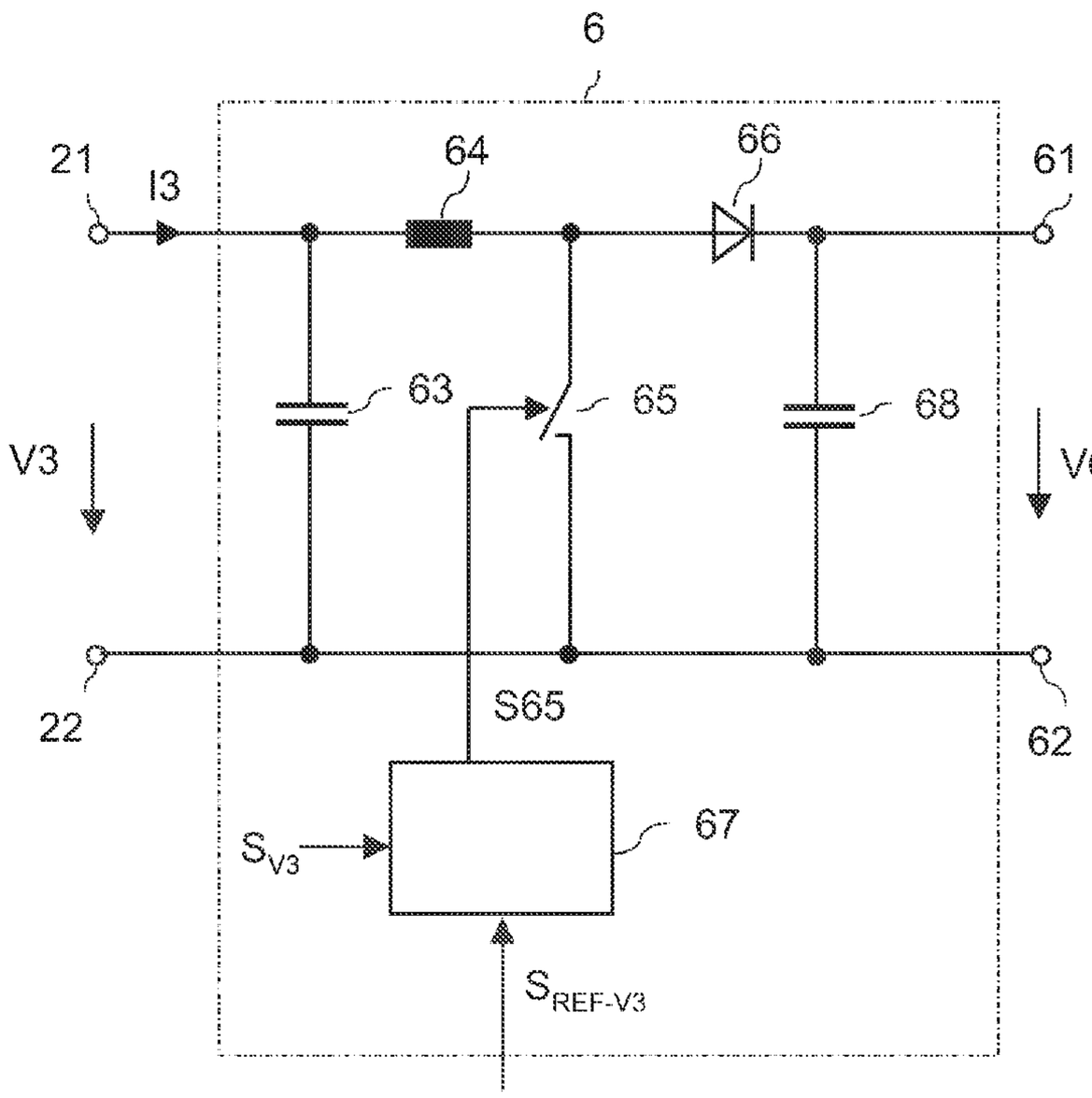
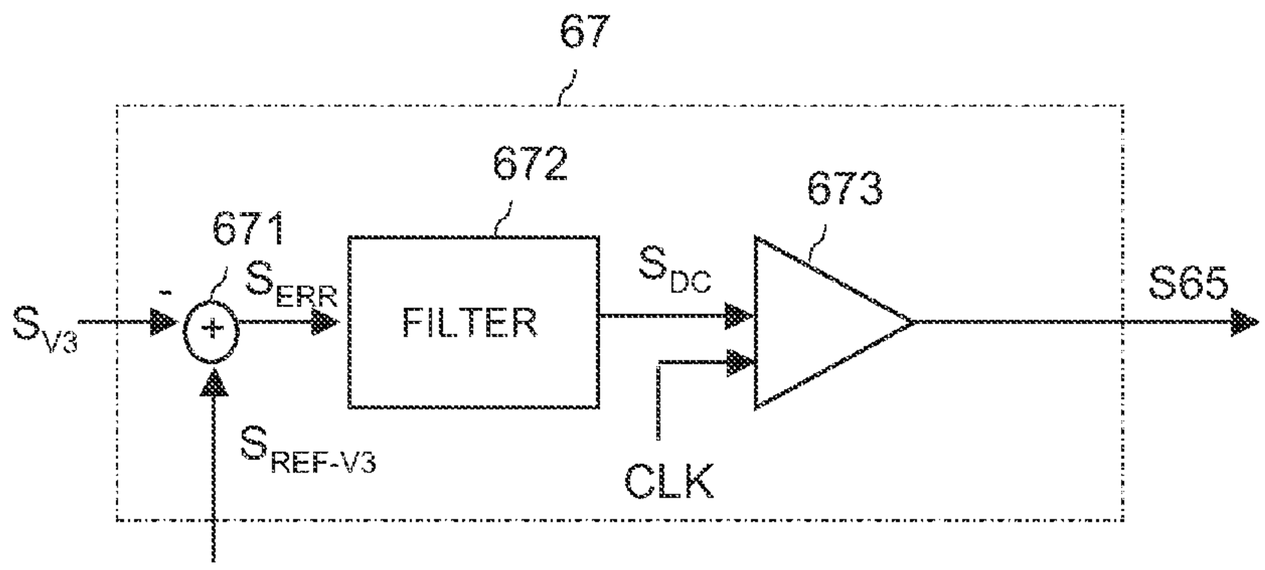

6
21
I3
64
66
61
63
65
68
V3
V6
22
S65
62
67
S_{V3}
S_{REF-V3}

FIG 12


67
672
673
671
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S_{DC}
S_{V3}
FILTER
S65
S_{REF-V3}
CLK

FIG 13

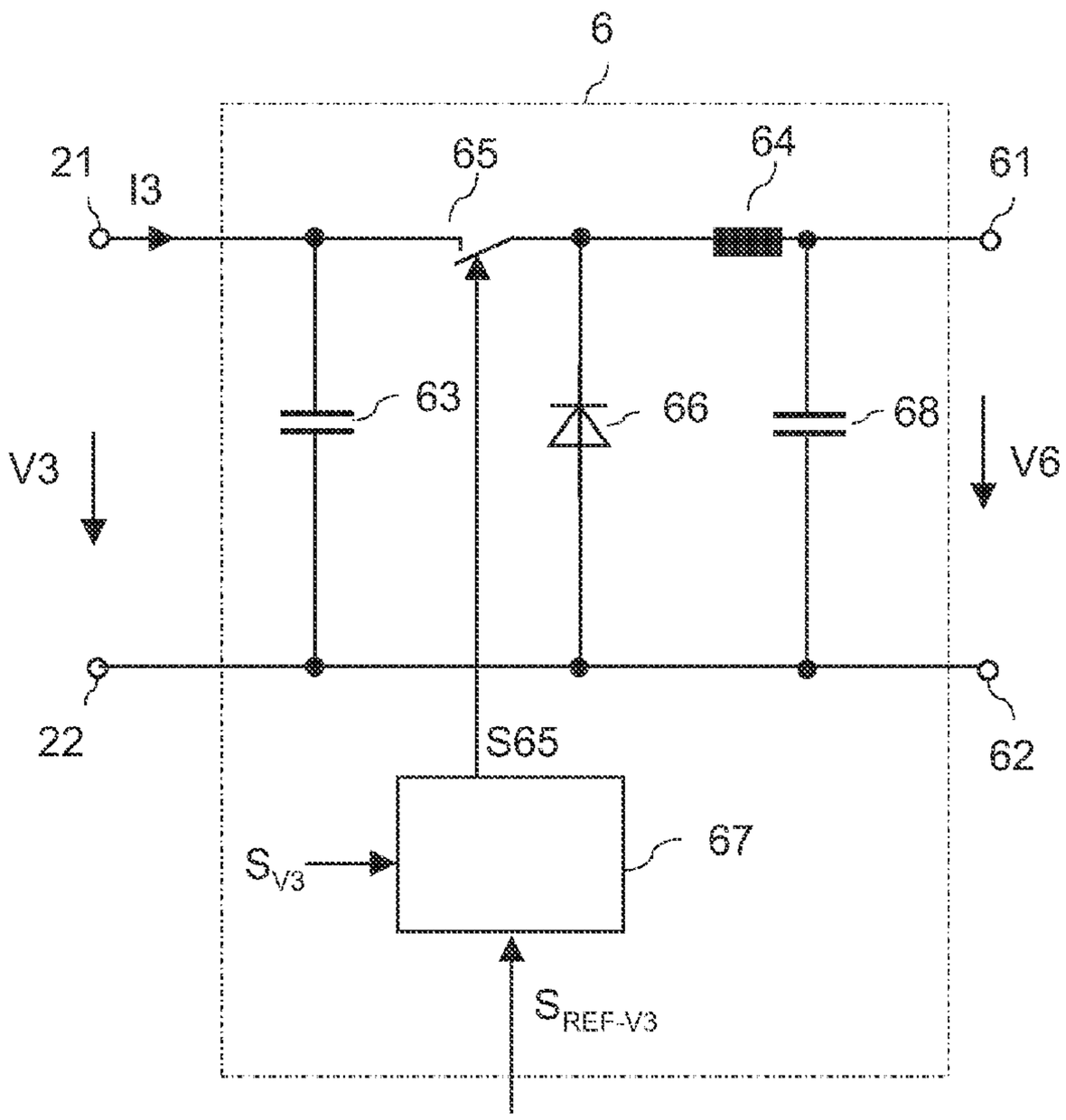

6
21
I3
65
64
61
63
66
68
V3
V6
22
S65
62
67
S_{V3}
S_{REF-V3}

FIG 14

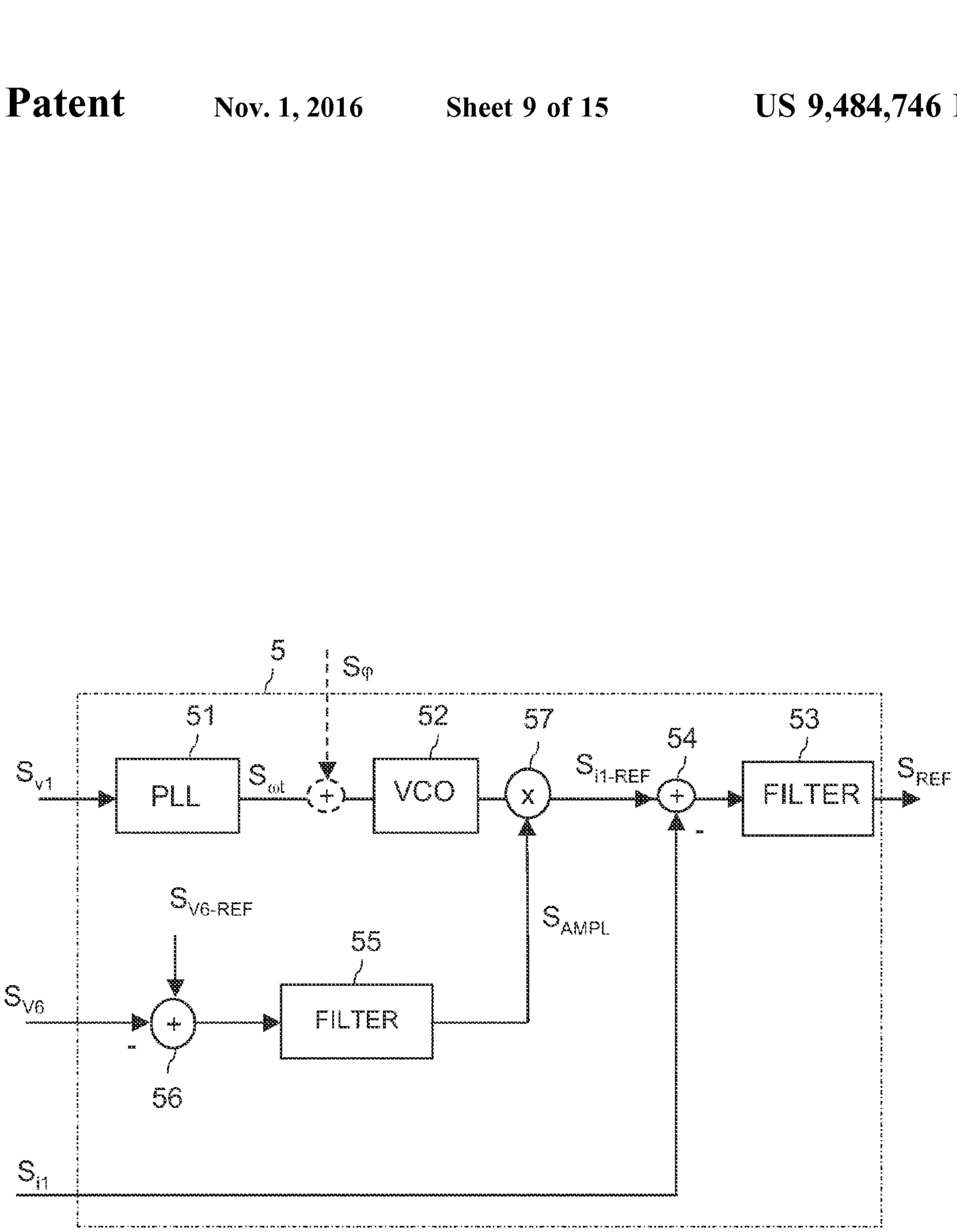
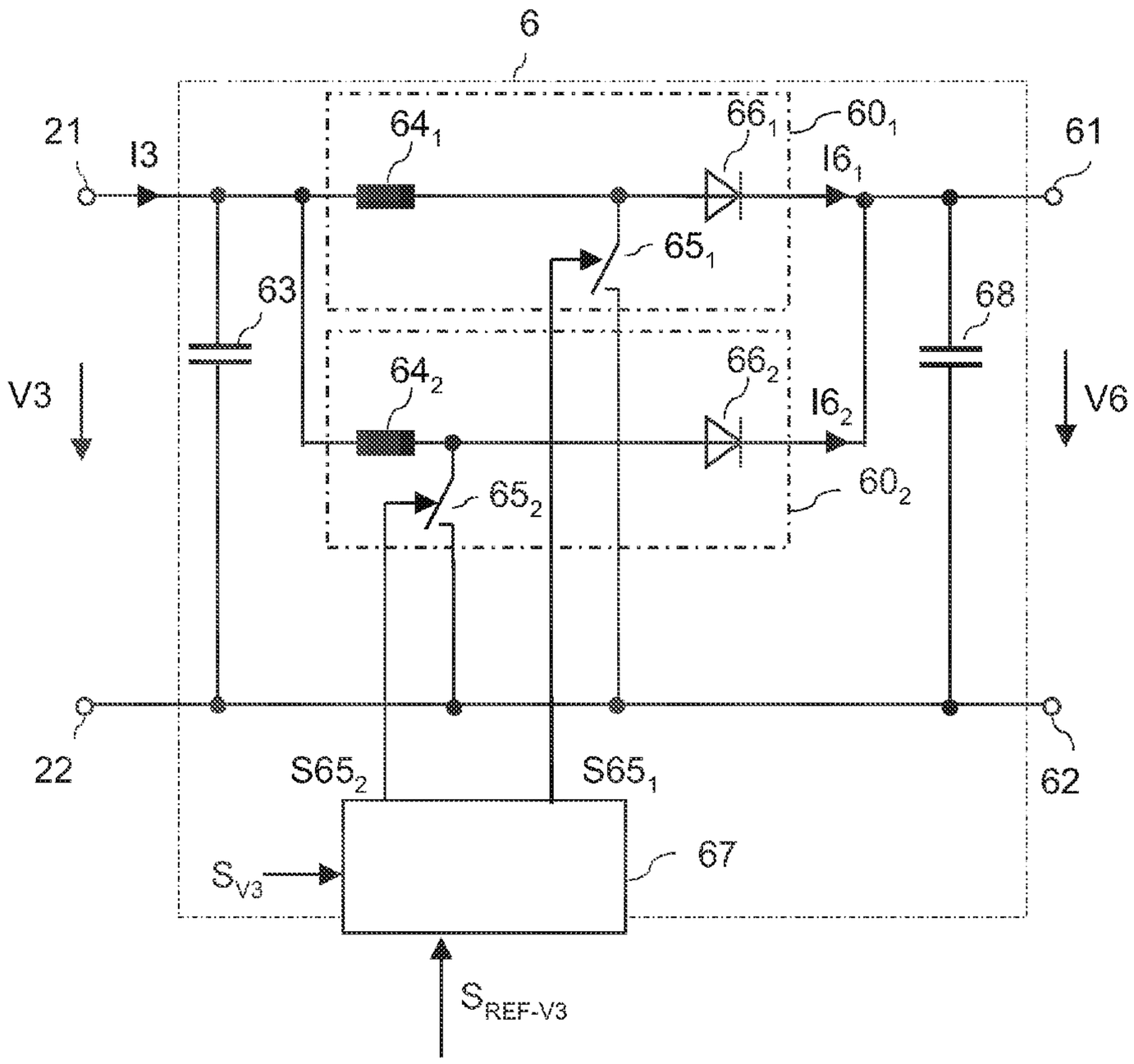

5
S_φ
51
52
57
54
53
S_{v1}
PLL
$S_{\omega t}$
VCO
$S_{i1\text{-}REF}$
FILTER
S_{REF}
$S_{V6\text{-}REF}$
S_{AMPL}
55
S_{V6}
FILTER
56
S_{i1}

FIG 15


6
21
I3
64₁
66₁
60₁
I6₁
61
65₁
63
68
V3
64₂
66₂
I6₂
V6
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60₂
22
S65₂
S65₁
62
67
S_V3
S_REF-V3

FIG 16

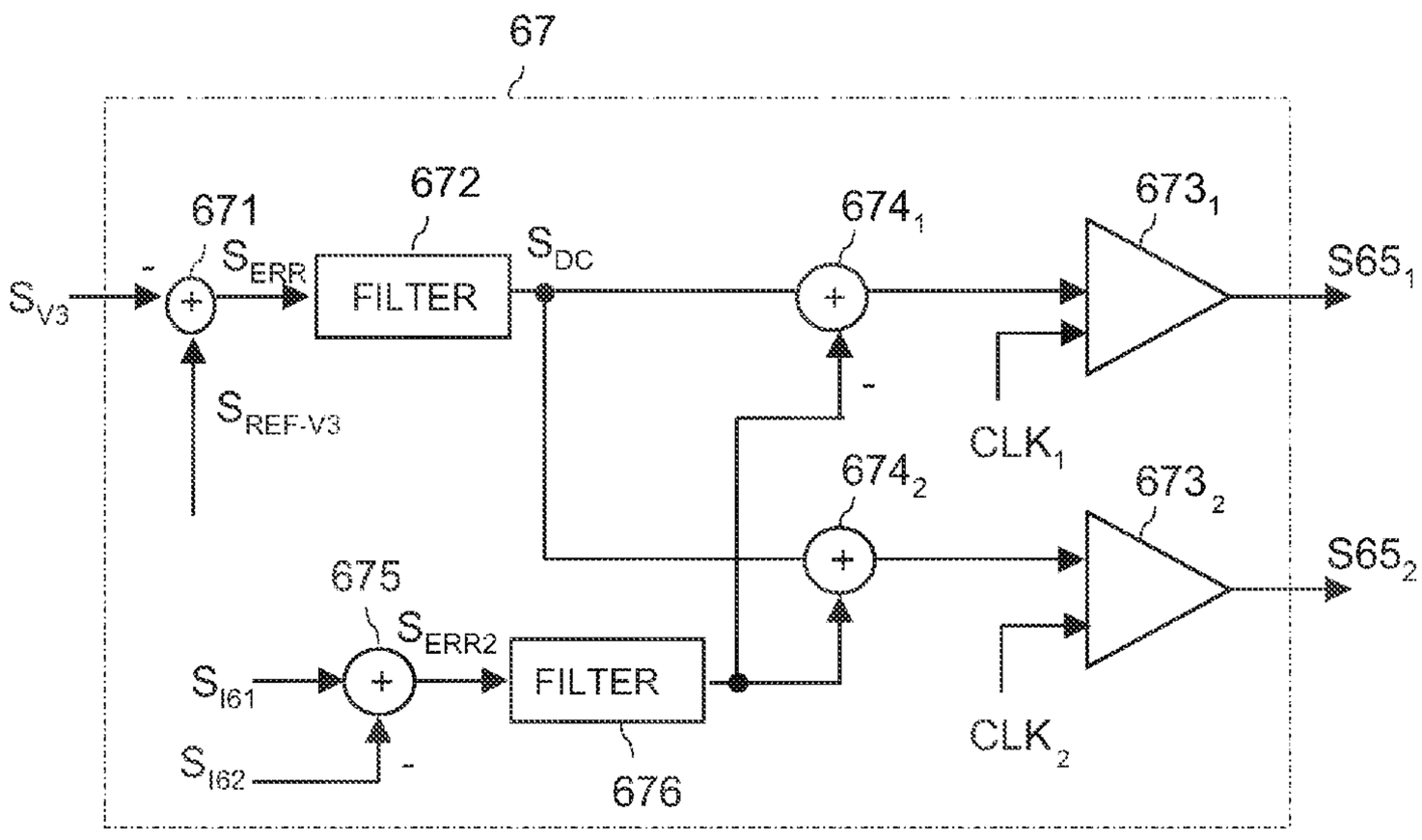

67
671
672
S_V3
S_ERR
FILTER
S_DC
674₁
673₁
S65₁
S_REF-V3
CLK₁
674₂
673₂
675
S_ERR2
S65₂
S_I61
FILTER
S_I62
CLK₂
676

FIG 17

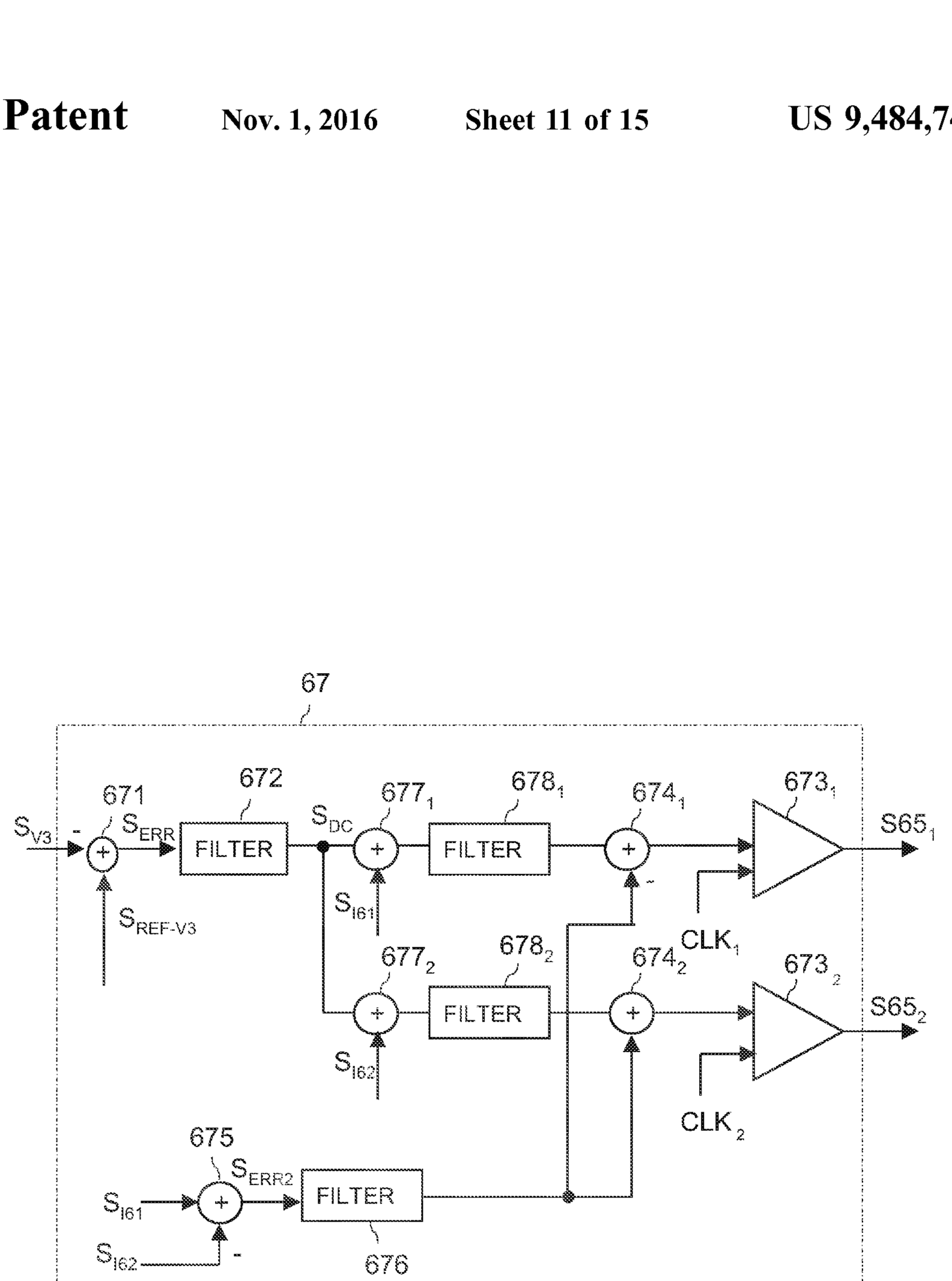
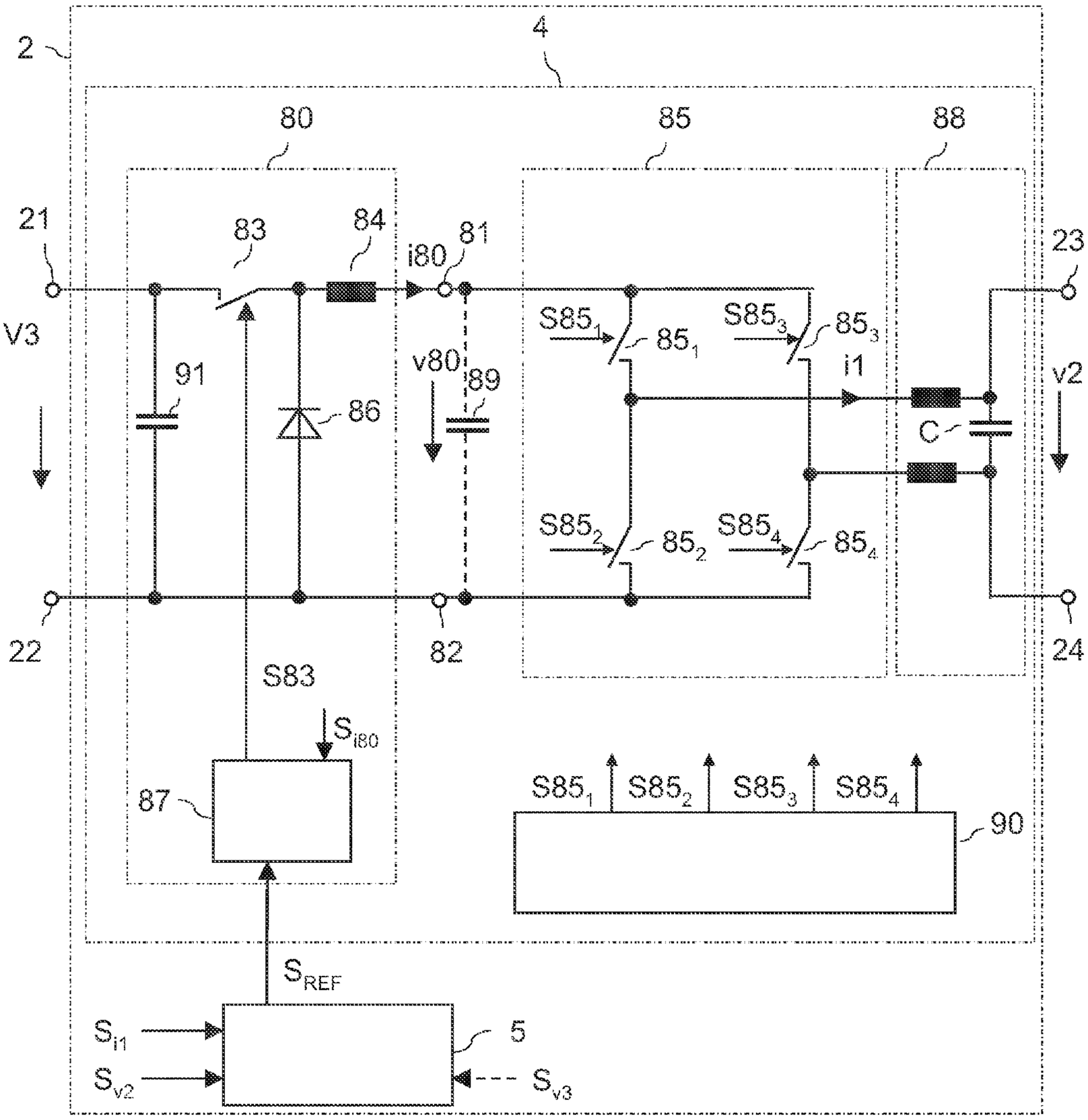

67
671
672
677 1
678 1
674 1
673 1
S65 1
S V3
S ERR
FILTER
S DC
FILTER
S REF-V3
S I61
677 2
678 2
674 2
673 2
S65 2
CLK 1
FILTER
S I62
CLK 2
675
S ERR2
S I61
FILTER
S I62
676

FIG 18


2
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83
84
i80
81
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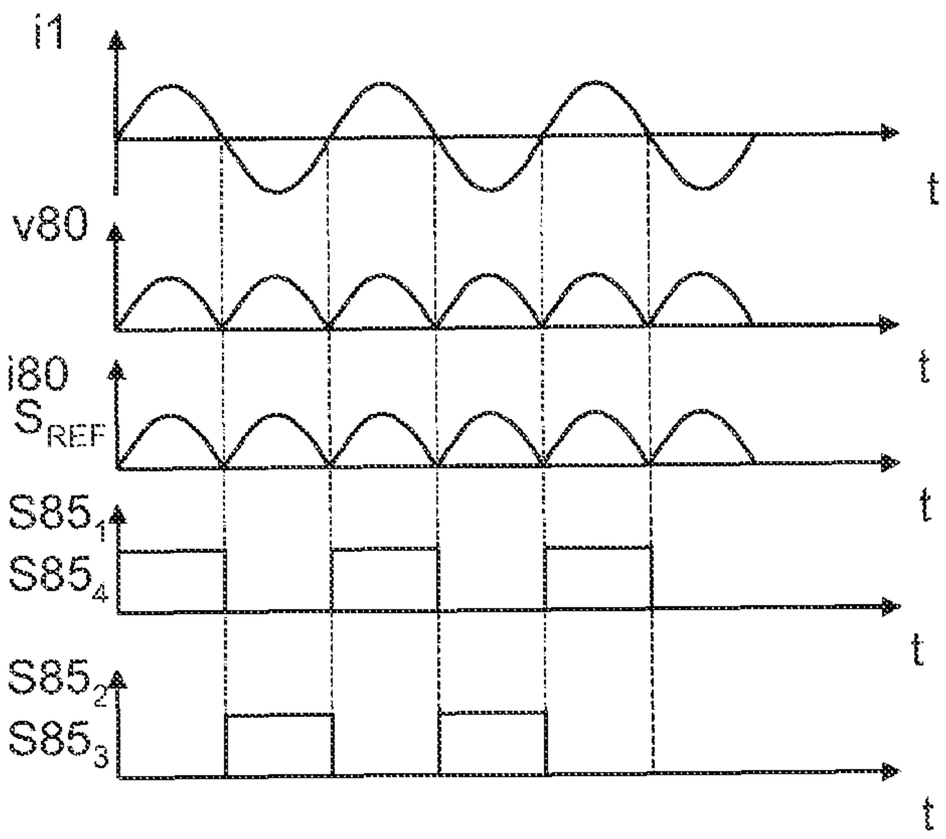
V3
S85$_1$
85$_1$
S85$_3$
85$_3$
i1
v80
89
91
86
C
v2
S85$_2$
85$_2$
S85$_4$
85$_4$
22
82
24
S83
S$_{i80}$
87
S85$_1$
S85$_2$
S85$_3$
S85$_4$
90
S$_{REF}$
S$_{i1}$
S$_{v2}$
5
S$_{v3}$

FIG 19


i1
t
v80
t
i80
S_{REF}
t
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$S85_4$
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$S85_2$
$S85_3$
t

FIG 20

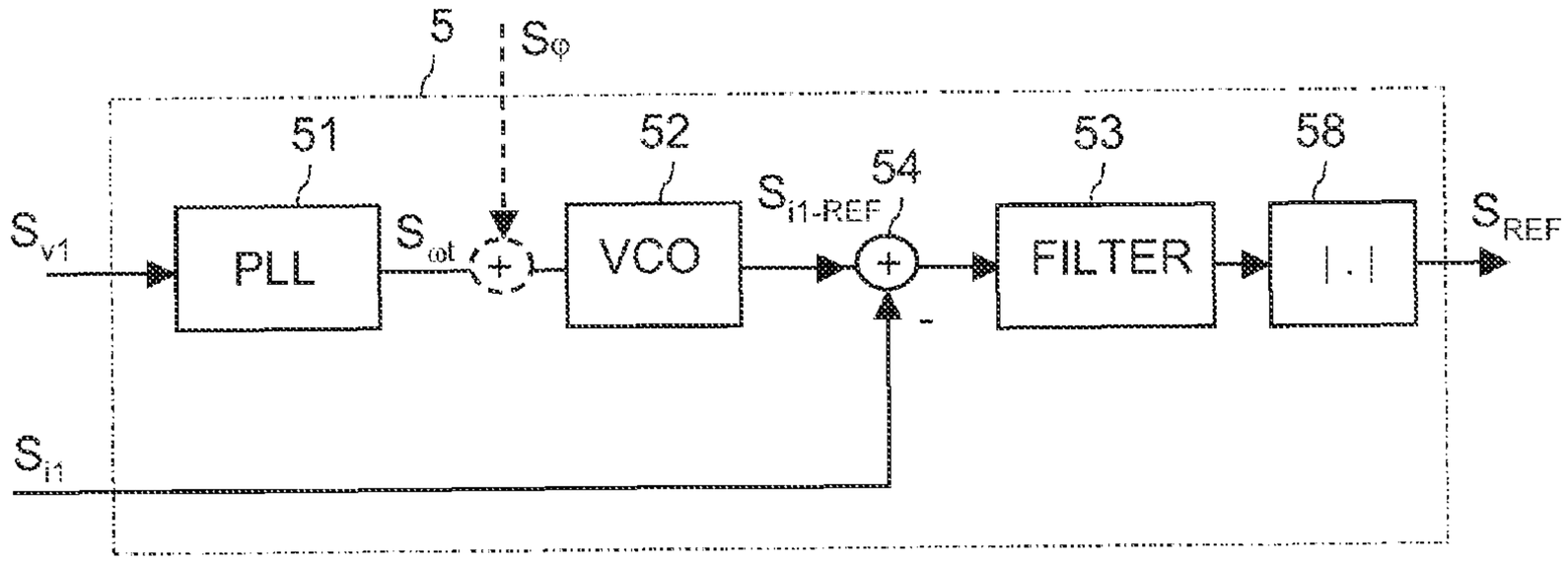
5
S_φ
51
52
54
53
58
S_{v1}
PLL
$S_{\omega t}$
VCO
$S_{i1\text{-}REF}$
FILTER
| . |
S_{REF}
S_{i1}
-

FIG 21

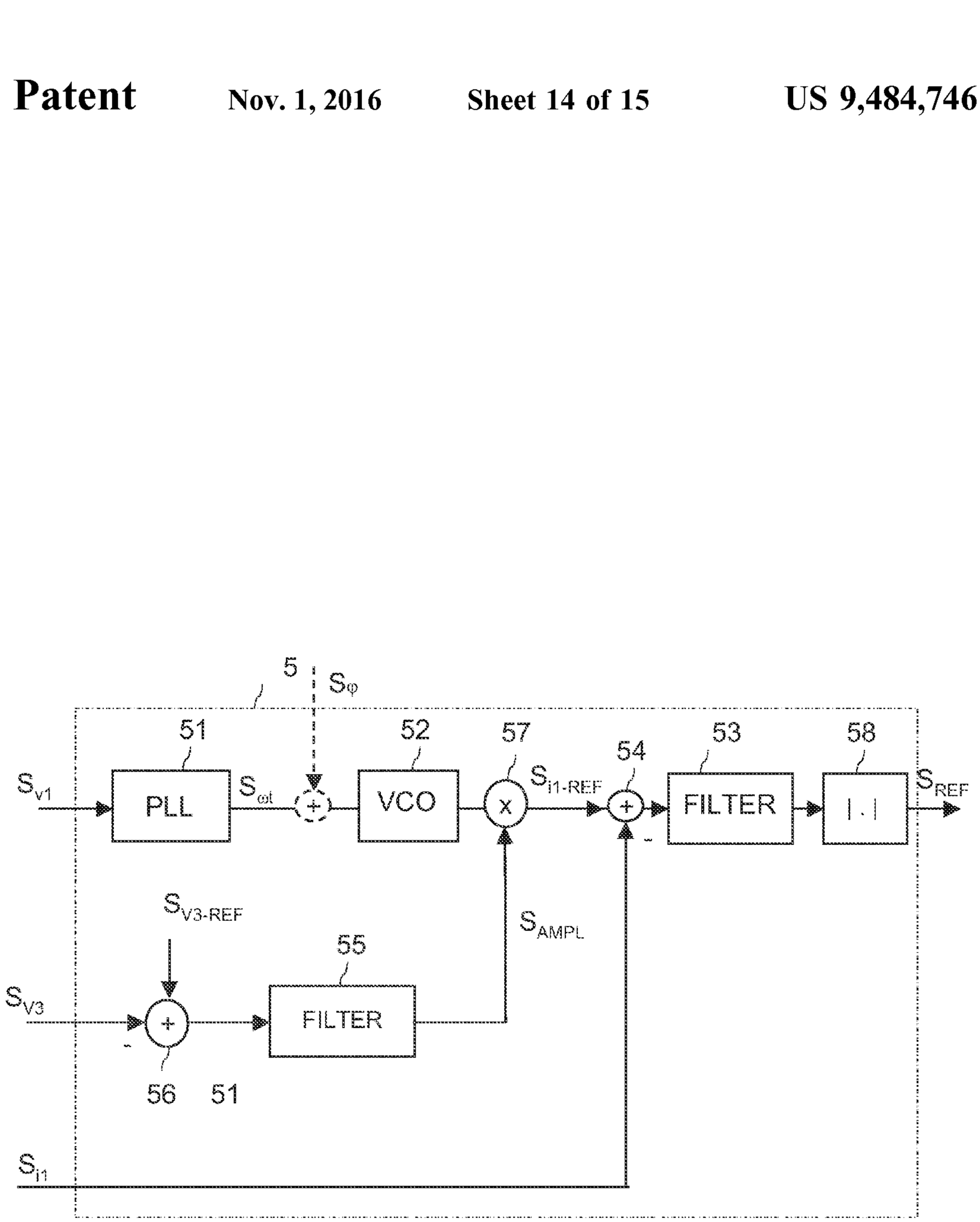
5
S_φ
51
52
57
54
53
58
S_{v1}
PLL
$S_{\omega t}$
VCO
$S_{i1\text{-}REF}$
FILTER
S_{REF}
$S_{V3\text{-}REF}$
S_{AMPL}
55
S_{V3}
FILTER
56
51
S_{i1}

FIG 22

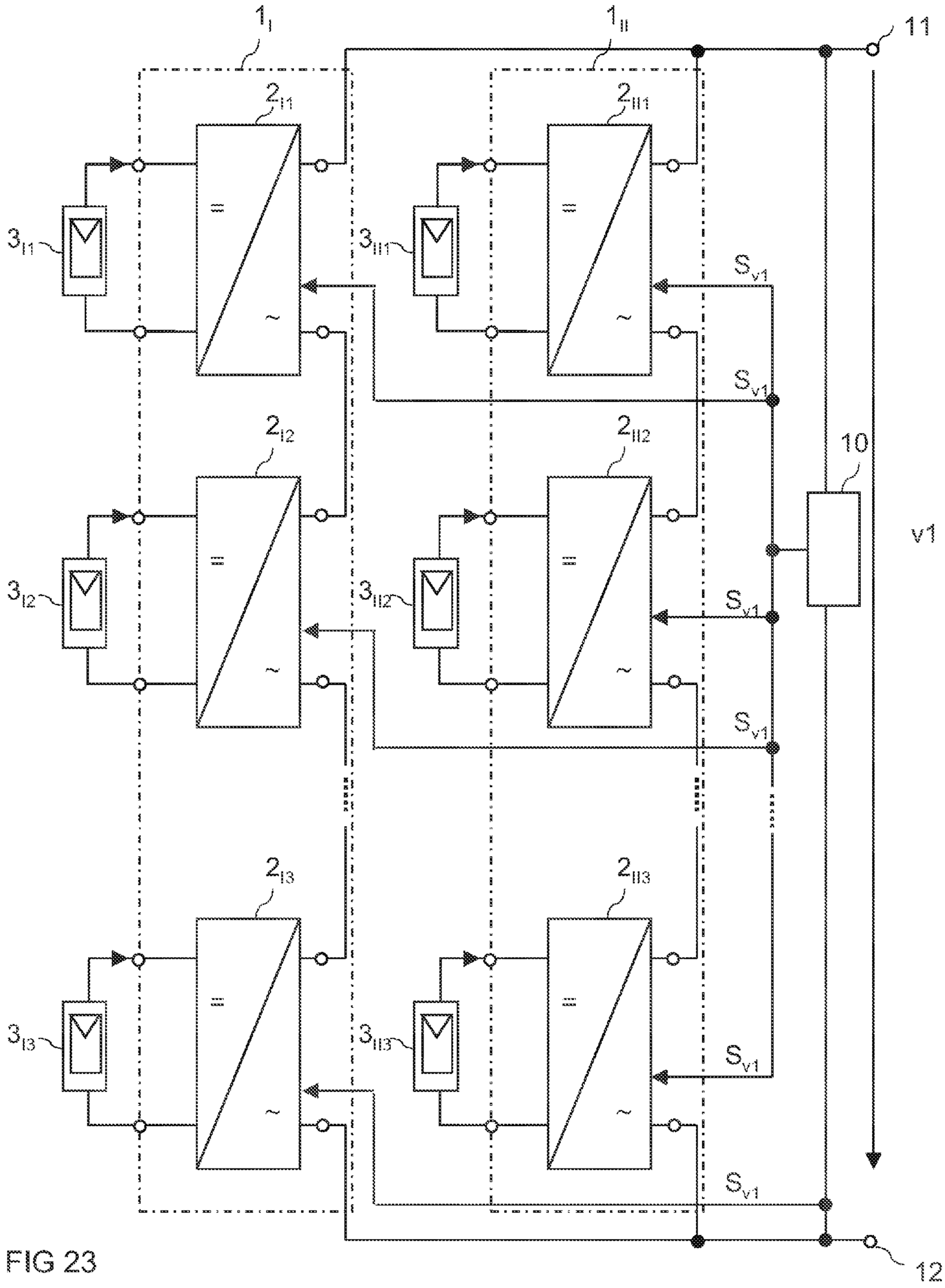
1I
1II
11
2I1
2II1
3I1
3II1
Sv1
2I2
2II2
3I2
3II2
10
v1
2I3
2II3
3I3
3II3
12

FIG 23

POWER CONVERTER CIRCUIT WITH AC OUTPUT

TECHNICAL FIELD

Embodiments of the present invention relate to a power converter circuit, a power supply system with a power converter circuit, and a method for operating a power converter circuit.

BACKGROUND

With an increasing interest in sustainable energy production there is a focus on using photovoltaic modules for producing electric power. Photovoltaic (PV) modules include a plurality of photovoltaic (PV) cells, that are also known as solar cells. Since the output voltage of one cell is relatively low, a PV module usually includes a string with a plurality of series connected solar cells, such as between 50 to 100 cells connected in series, or even several such strings connected in parallel.

A PV module provides a DC supply voltage, while power grids, such as national power grids, have an AC supply voltage. In order to supply the energy provided by a PV module to the power grid it is, therefore, necessary to convert the DC voltage of the PV module into an AC voltage that is consistent with the AC supply voltage of the power grid.

A first approach for converting the PV module DC voltage into a power grid AC voltage includes connecting several PV modules in series so as to obtain a DC voltage that is higher than the peak voltage of the power grid AC voltage, and converting the DC voltage into the AC voltage using a DC/AC converter. The amplitude of the DC voltage is typically between 200V and 1000V. High DC voltages, however, are critical in terms of the occurrence of electric arcs.

According to a second approach, a plurality of DC/AC converters are provided, where each of these converters is connected to a PV module. The individual converters have their AC voltage outputs connected in parallel and each of these converters generates an AC voltage that is consistent with the power grid AC supply voltage from the DC voltage provided by the string of solar cells. The DC voltage provided by one PV module usually has an amplitude in the range of between 20V and 100V, depending on the number of cells that are connected in series within one module and depending on the technology used to implement the solar cells, while the peak voltage of the power grid AC voltage is about 155V or 325V, depending on the country. However, due to the large difference between input and output voltages these converters have a disadvantage in terms of efficiency.

According to a further approach, several DC/AC converters are connected in series, where each of these converters receives a DC supply voltage from a PV module. In this system a central control unit is employed to synchronize the individual DC/AC converters in a multi-level switching pattern. This system requires constant synchronized control of all individual units.

There is, therefore, need for a power converter circuit that is capable of efficiently transforming relatively low DC supply voltages into a AC supply voltage that is consistent with a power grid voltage.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a power converter circuit. The power converter circuit includes output terminals configured to receive an external voltage, and at least one series circuit with at least two converter units. Each converter unit includes input terminals configured to be coupled to a DC power source, and output terminals for providing an AC output current. The at least one series circuit is connected between the output terminals of the power converter circuit. The power converter circuit further includes a voltage measurement circuit connected between the output terminals of the power converter circuit and configured to provide at least one measurement signal including an information on the phase and frequency of the external AC voltage. At least one of the converter units is configured to receive the at least one measurement signal and is configured to regulate a generation of the AC output current dependent on the at least one measurement signal such that a phase difference between the AC output current and the external AC voltage assumes a given set value.

A second aspect of the invention relates to a power supply system. The power supply system includes output terminals configured to receive an external voltage, and at least one series circuit with at least two converter units. The at least two converter units each include input terminals configured to be coupled to a DC power source, and output terminals for providing an AC output current. The at least one series circuit is connected between the output terminals of the power converter circuit. The power supply system further includes at least two voltage sources, each DC voltage source coupled to the input terminals of one converter unit, and a voltage measurement circuit connected between the output terminals of the power converter circuit and configured to provide at least one measurement signal including an information on the phase and frequency of the external AC voltage. At least one of the converter units is configured to receive the at least one measurement signal, and is configured to regulate a generation of the AC output current dependent on the at least one measurement signal such that a phase difference between the AC output current and the AC output voltage assumes a given set value.

A third aspect of the invention relates to a power converter unit. The power converter unit includes input terminals configured to be coupled to a DC power source, output terminals for providing an AC output current, and a measurement input configured to receive a measurement signal including a frequency and phase information. The converter unit is configured to regulate a generation of the AC output current such that a phase difference between a phase of the AC output current and the phase as represented by the phase information assumes a given set value.

A fourth aspect of the invention relates to a method for operating a power converter circuit including output terminals configured to receive an external voltage, and at least one series circuit with at least two converter units each including input terminals configured to be coupled to a DC power source, and output terminals for providing an AC output current, the at least one series circuit connected between the output terminals of the power converter circuit. The power converter circuit further includes a voltage measurement circuit connected between the output terminals of the power converter circuit and configured to provide at least one measurement signal including an information on the phase and frequency of the external AC voltage. The method includes regulating a generation of the AC output current such that a phase difference between a phase of the AC output current and a phase as represented by the phase information assumes a given set value.

BRIEF DESCRIPTION OF THE DRAWINGS

Examples will now be explained with reference to the drawings. The drawings serve to illustrate the basic prin-

ciple, so that only aspects necessary for understanding the basic principle are illustrated. The drawings are not to scale. In the drawings the same reference characters denote like signals and circuit components.

FIG. **1** schematically illustrates a power converter circuit including a plurality of DC/AC converter units connected in series and a voltage measurement circuit;

FIG. **2**, which includes FIGS. **2**A-**2**C, illustrates different embodiments of photovoltaic arrays, each including at least one solar cell;

FIG. **3** schematically illustrates a power converter circuit including a plurality of DC/AC converter units connected in series and a voltage measurement circuit including a plurality of measurement units connected in series;

FIG. **4**, which includes FIGS. **4**A-**4**D, illustrates different embodiments of measurement units;

FIG. **5** shows a block diagram illustrating a first embodiment of one DC/AC converter unit, including a DC/AC converter and a control circuit;

FIG. **6** illustrates an embodiment of the DC/AC converter of FIG. **5** in detail;

FIG. **7**, which includes FIGS. **7**A to **7**C, illustrates different embodiments of switches that may be used in the DC/AC converter of FIG. **6**;

FIG. **8** illustrates a first embodiment of the control circuit of one DC/AC converter unit;

FIG. **9** illustrates a first branch of the control circuit of FIG. **8** in detail;

FIG. **10** illustrates a second embodiment of the control circuit of one DC/AC converter unit;

FIG. **11** shows a block diagram illustrating a second embodiment of one converter unit, including a DC/DC converter, a maximum power point tracker, a DC/AC converter, and a control circuit;

FIG. **12** illustrates an embodiment of the DC/DC converter implemented as a boost converter;

FIG. **13** schematically illustrates a control circuit of the DC/DC converter of FIG. **12**;

FIG. **14** illustrates an embodiment of the DC/DC converter implemented as a buck converter;

FIG. **15** illustrates a further embodiment of the control circuit of one DC/AC converter;

FIG. **16** illustrates an embodiment of the DC/DC converter implemented with two interleaved boost converter stages;

FIG. **17** illustrates a first embodiment of a control circuit for the DC/DC converter of FIG. **16**;

FIG. **18** illustrates a second embodiment of a control circuit for the DC/DC converter of FIG. **16**;

FIG. **19** shows a block diagram illustrating a further embodiment of one DC/AC converter unit including a buck converter and an unfolding bridge;

FIG. **20** shows timing diagrams illustrating the operating principle of the DC/AC converter unit of FIG. **19**;

FIG. **21** illustrates a first embodiment of a controller implemented in the DC/AC converter unit of FIG. **19**;

FIG. **22** illustrates a second embodiment of a controller implemented in the DC/AC converter unit of FIG. **19**; and

FIG. **23** illustrates an embodiment of a power converter circuit having a plurality of converter units organized in two series circuits being connected in parallel.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings, which form a part thereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the figures being described. Because components of embodiments can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims. It is to be understood that the features of the various exemplary embodiments described herein may be combined with each other, unless specifically noted otherwise.

In the following, embodiments of the present invention will be explained in a specific context, namely in the context of converting electrical power or electrical voltages provided by a plurality of photovoltaic arrays into an AC voltage, specifically an AC power grid supply voltage. However, this is only an example. Embodiments of the invention may be employed in a wide range of applications in which a conversion of DC voltages into an AC voltage is required. Any type of DC power source may be used instead of a photovoltaic array, such as a fuel cell. It is even possible, to employ DC power source of different types, such as photovoltaic arrays and fuel cells, in one application.

FIG. **1** illustrates a first embodiment of a power converter circuit (power inverter circuit) **4** for converting a plurality of n (at least two) DC input voltages $V3_1$, $V3_2$, $V3_n$ into one AC output voltage v**1**. It should be noted in this connection that throughout the drawings DC voltages and DC currents will be denoted using capital letters "V" and "I", while AC voltages and AC currents will be denoted using lowercase letters "v" and "i." The power converter circuit includes a plurality of n (at least two) converter units 2_1, 2_2, 2_n, with $n \geq 2$. Each of these converter units includes input terminals 21_1, 22_1; 21_2, 22_2; and 21_n, 22_n that are configured to be coupled to a DC power source 3_1, 3_2, 3_n. In FIG. **1**, besides the power converter circuit **1** with the converter units 2_1, 2_2, 2_n DC power sources 3_1, 3_2, 3_n are also illustrated. These DC power sources 3_1, 3_2, 3_n together with the power converter circuit **1** form an AC power supply system or an AC current supply system. The DC power sources 3_1, 3_2, 3_n are implemented as photovoltaic (PV) modules in the embodiment illustrated in FIG. **1**. However employing PV modules as DC power sources is only an example. Any other type of DC power source, such as a power source including fuel cells, may be used as well. It is even possible to employ different types of DC power sources in one power supply system.

Each of the converter units 2_1, 2_2, 2_n further includes output terminals 23_1, 24_1; 23_2, 24_2; and 23_n, 24_n. The converter units 2_1, 2_2, 2_n are connected in series (in cascade) between output terminals **11**, **12** of the power converter circuit **1**. For this, a first converter unit 2_1 has a first output terminal 23_1 coupled to a first output terminal **11** of the power converter circuit **1** and a last converter unit 2_n in the cascade has a second output terminal 24_n coupled to a second output terminal **12** of the power converter circuit **1**. Further, each of the first output terminals (other than output terminal 23_1) are connected to one second output terminal (other than output terminal 24_n) of another converter unit.

The output terminals **11**, **12** of the power converter circuit **1** are configured to receive a voltage v**1**. For example, the output terminals **11**, **12** are configured to be connected to a

power grid, so that the external voltage v**1** corresponds to a grid voltage or, more specifically, corresponds to one phase of the power grid. In FIG. **1**, the power grid is represented by a voltage source **100** and a load Z connected in parallel with the power source **100**. The voltage source **100** of the power grid represents a plurality of AC voltage sources in the power grid, and load Z represents a plurality of loads connected to the power sources in the power grid. The power grid defines the AC voltage v**1** between the output terminal. Since this voltage v**1** is defined by an external source, such as the power grid, this voltage will be referred to as external AC voltage v**1** in the following.

Each of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ provides an AC output voltage v$\mathbf{2}_1$, v$\mathbf{2}_2$, v$\mathbf{2}_n$ between its output terminals $\mathbf{23}_1$, $\mathbf{24}_1$, $\mathbf{23}_2$, $\mathbf{24}_2$, $\mathbf{23}_n$, $\mathbf{24}_n$. By having the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ connected in series, the sum of the individual AC output voltages v$\mathbf{2}_1$, v$\mathbf{2}_2$, v$\mathbf{2}_n$ of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ corresponds to the external voltage v**1** when the power converter circuit **1** is in the steady state, that is,

$$v1 = \sum_{i=1}^{n} v2_i. \tag{1}$$

Each power converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ further includes an output capacitance C_1, C_2, C_n connected between the individual output terminals $\mathbf{23}_1$, $\mathbf{24}_1$, $\mathbf{23}_2$, $\mathbf{24}_2$, $\mathbf{23}_n$, $\mathbf{24}_n$ and provides an output current i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$. The output current of one converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ is the current received at a circuit node common to the output capacitance C_1, C_2, C_n and one of the output terminals. For example, in the first converter unit $\mathbf{2}_1$, the output current of the converter unit $\mathbf{2}_1$ is the current flowing into the circuit node at which the output capacitor C_1 is connected to the first output terminal $\mathbf{23}_1$. The current flowing from the first output terminal $\mathbf{23}_1$ of the first converter unit $\mathbf{2}_1$ will be referred to as converter circuit output current i$\mathbf{1}_{OUT}$. This current corresponds to the current flowing between the individual converter units $\mathbf{2}_1$-$\mathbf{2}_n$. The output capacitances C_1, C_2, C_n are part of the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ and can be implemented in many different ways as will be explained with reference to several examples herein below.

In the steady state, the AC output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$ or, more precisely, the RMS values of the AC output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$, correspond to the power converter circuit output current i$\mathbf{1}_{OUT}$ or the RMS value of the output current i$\mathbf{1}_{OUT}$, respectively, so that there is very little to no RMS current into the output capacitors C_1-C_n. However, there can be situations in which the output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$ of the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ change and in which the output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$ are mutually different until the system has settled at new (equal) output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$. This is explained in further detail below.

The power converter circuit **1** further includes a voltage measurement circuit **10** connected between the output terminals **11**, **12** of the power converter circuit **1**. The voltage measurement circuit **10** is configured to provide at least one measurement signal S_{v1} that includes an information on the phase and the frequency of the external AC voltage v**1**.

The individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ are each configured to receive one measurement signal S_{v1}. In the embodiment illustrated in FIG. **1**, the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ receive the same measurement signal S_{v1}. However, this is only an example. It is also possible to generate one measurement signal for each of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$. An embodiment is explained with reference to FIG. **3** herein below. The at least one measurement signal S_{v1} can be transmitted to the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ in different ways. Referring to FIG. **1**, a signal transmission bus can be provided through which the at least one measurement signal S_{vN} is transmitted to the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$. According to a further embodiment (not illustrated in FIG. **1**), there is a dedicated transmission path between the voltage measurement circuit and each of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$. The signal transmission bus or the signal transmission paths can be implemented like conventional signal transmission buses or like conventional signal transmission paths. The signal bus or the signal paths may include level shifter or other means to transmit the at least one measurement signal from the measurement circuit **10** to the individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ that (due to being connected in cascade) have different reference potentials or different voltage domains.

The individual converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ each include at least one internal control loop which will be explained in further detail herein below. The control loop of each converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ is configured to have each converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ generate the corresponding output current i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$ such that there is a given phase difference between the phase as represented by the at least one measurement signal S_{v1}, and which corresponds to the phase of the external AC voltage v**1**, and the phase of its AC output current i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$. According to one embodiment, the individual output currents i$\mathbf{1}_1$, i$\mathbf{1}_2$, i$\mathbf{1}_n$ are generated to be in phase with the external AC voltage v**1**, so that the phase difference is zero. According to another embodiment, the phase difference is not zero. When setting the difference to a value other than zero, reactive power is fed into the power grid. This may help to stabilize the external AC voltage, which is, e.g., a power grid.

In FIG. **1**, same features of the DC voltage sources $\mathbf{3}_1$, $\mathbf{3}_2$, $\mathbf{3}_n$ have the same reference characters, where the reference characters of the individual DC voltage sources $\mathbf{3}_1$, $\mathbf{3}_2$, $\mathbf{3}_n$ can be distinguished from each other by subscript indices "1", "2", "n". Equivalently, same features of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ have the same reference characters that can be distinguished by subscript indices, "1" for the first converter unit $\mathbf{2}_1$, "2" for the second converter unit $\mathbf{2}_2$ and "n" for the n-th converter unit $\mathbf{2}_n$. In the following, when explanations equivalently apply to each of the DC power sources $\mathbf{3}_1$, $\mathbf{3}_2$, $\mathbf{3}_n$ or to each of the converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$, reference characters will be used without indices. In the following, reference character **2**, for example, represents an arbitrary one of the converter units, reference character **23** represents a first output terminal of an arbitrary one of the converter units, reference character i**1** denotes the output current of an arbitrary converter unit **2**, reference character denotes the output capacitance C of an arbitrary converter unit **2**, and so on.

The power converter of FIG. **1** includes n=3 converter units **2**. However, having n=3 converter units is only an example. Any number of n converter units **2**, wherein n>1, can be connected in series to form the power converter circuit **1**.

Besides the internal control loops of the converter units **2** the power converter circuit **1** does not require an outer control loop connected to the individual converter units **2** and/or additional communication paths between the individual converter units **2**, when the power converter circuit **1** is in the steady state. When the power converter circuit **1** is in the steady state the system can be defined by equation (1) and one further equation for each of the converter units **2**:

$$v2_{RMS} \cdot i1_{RMS} = V3 \cdot I3 \tag{2},$$

where $v2_{RMS}$ denotes the RMS (route mean square) value of the output voltage v**2** of one converter units **2**, $i1_{RMS}$ denotes the RMS value of the output current i**1** of one converter unit, V**3** denotes the input voltage and I**3** denotes the input current of the converter unit **2**. It should be noted that (very low) losses may occur in each converter unit **2**. For the sake of simplicity, these losses are not considered in equation (2). In the steady state, the RMS values of the individual output currents $i1_{RMS}$ are equal and correspond to the RMS value of the power converter circuit output current $i1_{OUT\text{-}RMS}$, that is:

$$i1_{RMS}=i1_{OUT\text{-}RMS} \tag{3}$$

Since equations (2) and (3) are valid for each of the individual converter units, there are n equations, each of these equations describing the relationship between the input power and the average output power of each of the converter units **2**, where the input power Pin is given as:

$$Pin=V3\cdot I3 \tag{4},$$

and the output power Pout is given as:

$$Pout=v2_{RMS}\cdot i1_{RMS} \tag{5}.$$

The input power Pin of each of the individual converter units **2** and the input voltage V**3** and the input current I**3**, respectively, are external parameters given by the individual DC power sources **3**. The external AC voltage v**1** between the output terminals **11**, **12** is defined by the power grid.

Thus, there are n+1 variables in the power converter circuit **1**, namely the n output voltages v**2** of the individual converter units **2** and the (equal) output currents i**1**. However, referring to equations (1) and (2) the system is defined by n+1 equations, so that each of the n+1 variables is determined when the system is in its steady state. Besides having each of the converters **2** generate its AC output current i**1** such that there is a given phase difference (such as zero) between the AC output current i**1** and the external AC voltage no additional control or regulation mechanism is required. When the output currents i**1** of the individual converter units **2** are in phase with the external AC voltage v**1** the real output power of each converter unit equals the apparent output power, so that the reactive output power is zero. The individual converter units **2** control their output currents i**1** dependent on the phase information as represented by the at least one measurement signal S_{v1} and control their output current such that the input power received at the input terminals **21**, **22** equals the output power at the output terminals **23**, **24**.

The DC power sources **3** implemented as PV arrays are only schematically illustrated in FIG. **1**. These PV arrays each include at least one solar cell. Some exemplary embodiments of PV arrays including at least one solar cell are illustrated in FIGS. **2**A to **2**C. FIG. **2**A illustrates a first embodiment. In this embodiment, the PV array **3** includes only one solar cell **31**. Referring to a further embodiment illustrated in FIG. **2**B, one PV array **3** includes a string of m solar cells **31**, **3***m* wherein m>1, connected in series. According to yet another embodiment illustrated in FIG. **2**C, p strings of solar cells are connected in parallel, wherein p>1. Each of the strings includes m solar cells $\mathbf{31}_1$, $\mathbf{3}m_1$, $\mathbf{31}_p$, $\mathbf{3}m_p$. However, the embodiments illustrated in FIGS. **2**A to **2**C are only exemplary. Many other solar cell arrangements may be used as well as a DC source **3**.

FIG. **3** illustrates an embodiment of a power converter circuit that includes a voltage measurement circuit **10** with a plurality of measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$. The individual measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ are connected in series between the output terminals **11**, **12**. For simplicity of the illustration, the output capacitances (C_1-C_n in FIG. **1**) are not illustrated in FIG. **3**. The plurality of measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ forms a voltage divider, wherein a voltage drop $v\mathbf{1}_1$, $v\mathbf{1}_2$, $v\mathbf{1}_n$ across each of the measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ is a function of the external AC voltage v**1** and includes an information on the frequency and the phase of the external AC voltage v**1**. In this embodiment, each converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ has a measurement input with two input terminals $\mathbf{25}_1$, $\mathbf{26}_1$, $\mathbf{25}_2$, $\mathbf{26}_2$, $\mathbf{25}_n$, $\mathbf{26}_n$, and each converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ has the measurement input terminals coupled to one measurement unit **101**, **102**, **10***n*, so as to receive one measurement voltage $v\mathbf{1}_1$, $v\mathbf{1}_2$, $v\mathbf{1}_n$ as the measurement signal.

In the embodiment illustrated in FIG. **3**, the number of measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ corresponds to the number of converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$, so that each measurement unit $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ is associated with one converter unit $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$. However, this is only an example. According to a further embodiment (not illustrated) the measurement voltage provided by one measurement unit is received by two or more converter units.

The individual measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ can be implemented in many different ways. Some examples are explained with reference to FIGS. **4**A to **4**D below. In these FIGS. **4**A to **4**D, reference character $\mathbf{10}_i$ denotes an arbitrary one of the measurement units $\mathbf{10}_1$, $\mathbf{10}_2$, $\mathbf{10}_n$ illustrated in FIG. **3**.

Referring to FIG. **4**A, one measurement unit $\mathbf{10}_i$ may include a resistor $\mathbf{10}_1$ connected between the terminals of the measurement unit $\mathbf{10}_i$ that serve to connect the individual measurement units ($\mathbf{10}_1$-$\mathbf{10}_n$ in FIG. **3**) in series and that serve to couple the individual measurement units to the converter units ($\mathbf{2}_1$-$\mathbf{2}_n$ in FIG. **3**). According to one embodiment, the resistances of the resistors $\mathbf{10}_1$ in the individual measurement units $\mathbf{10}_i$ are equal or at least approximately equal. In this case, the absolute values of the measurement voltages $v\mathbf{1}_i$ provided by the individual measurement units $\mathbf{10}_i$ are equal. In a measurement circuit **10** that includes measurement units $\mathbf{10}_i$ implemented with a resistor $\mathbf{10}_1$, the individual measurement voltages $v\mathbf{1}_i$ are proportional to the output voltage v**1**.

In a measurement circuit **10** with measurement units $\mathbf{10}_i$ including resistors, the individual measurement units $\mathbf{10}_i$ form a resistive voltage divider. Referring to a further embodiment illustrated in FIG. **4**B, the individual measurement units $\mathbf{10}_i$ each include a capacitor **102** instead of a resistor. In this case, the individual measurement units $\mathbf{10}_i$ form a capacitive voltage divider between the output terminals **11**, **12**.

Referring to FIG. **4**C, that illustrates a further embodiment, each measurement unit $\mathbf{10}_i$ can be implemented with a parallel circuit including a resistor **101** and a capacitor **102**.

Referring to FIG. **4**D, that illustrates yet another embodiment of one measurement unit $\mathbf{10}_i$, each measurement unit or at least some of the measurement units can be implemented with a voltage divider having a first voltage divider **101** and a second voltage divider element **103**. These voltage divider elements are implemented as resistors in the embodiment according to FIG. **4**D. However, these voltage divider elements **101**, **103** could also be implemented as capacitors or as combinations with at least one resistor and at least one capacitor. In this embodiment, the measurement voltage $v\mathbf{1}_i$ is not the voltage across the measurement unit $\mathbf{10}_i$, but is the voltage across the first voltage divider element **101**, so that the measurement voltage $v\mathbf{1}_i$ is a fraction of the voltage across the measurement unit $\mathbf{10}_i$.

FIG. **5** illustrates a first embodiment of a converter unit **2** for converting the DC input voltage provided by one DC source (not shown in FIG. **3**) into an AC output voltage v**2**. The converter unit **2** includes a DC/AC converter **4** connected between the input terminals **21**, **22** and the output terminals **23**, **24**. The DC/AC converter **4** receives the DC voltage V**3** provided by the DC power source as an input voltage and the DC supply current I**3** of the DC power source as an input current. The DC/AC converter **4** further receives a reference signal S_{REF}, which may be an alternating signal having a frequency and a phase. The DC/AC converter **4** is configured to generate the AC output current i**1** dependent on the reference signal S_{REF} such that a frequency and a phase of the output current i**1** correspond to a frequency and a phase, respectively, of the measurement signal S_{v1}. The DC/AC converter **4** can be implemented like a conventional DC/AC converter that is configured to generate an output current in phase with an alternating reference signal. Such DC/AC converters are commonly known.

It should be noted that each of the DC/AC converter units $\mathbf{2}_1$, $\mathbf{2}_2$, $\mathbf{2}_n$ controls its output current i**1** to have a phase and frequency that is dependent on the at least one measurement signal S_{v1}.

The reference signal S_{REF} is generated by a control circuit **5** dependent on the measurement signal S_{v1} and an output current signal S_{i1}. The measurement signal S_{v1} is either the measurement signal S_{v1} explained with reference to FIG. **1**, one of the measurement voltages $\mathbf{v1}_i$ explained with reference to FIG. **3**, or a scaled version or a fraction thereof. The output current signal S_{i1} represents the output current i**1**, i.e., the output current signal S_{i1} is dependent on the output current i**1**. According to one embodiment, the output current signal S_{i1} is a scaled version of the output current i**1**. The output current signal S_{i1} can be generated in a conventional manner from the output current i**1** using a current measurement circuit (not illustrated). The output current signal S_{i1} is generated for each of the converter units ($\mathbf{2}_1$-$\mathbf{2}_n$) individually by detecting the respective output current of each converter unit. Referring to FIG. **5**, the output current i**1** of the illustrated converter unit **2** is the current received at the circuit node common to the first output terminal **23** and the output capacitance C.

The control circuit **5**, which will also be referred to as controller in the following, generates the reference signal S_{REF} dependent on the measurement signal S_{v1} and the output current signal S_{i1} such that the output current, when generated in correspondence with the reference signal S_{REF}, is in phase with the external AC voltage v**1** or has a given phase shift relative to the external AC voltage v**1**. It should be noted that, since the external AC voltage v**1** the output current i**1** are alternating signals, the measurement signal S_{v1} and the output current signal S_{i1} are also alternating signals. In the converter unit **2**, the DC/AC converter **4** and the controller **5** are part of a control loop that controls the output current i**1** to be in phase with the external AC voltage v**1** or to have a given phase shift relative thereto.

Although a conventional DC/AC converter may be used in the converter unit **2** as the DC/AC converter **4** connected between the input terminals **21**, **22** and the output terminals **23**, **24**, one example of a DC/AC converter **4** will be explained in detail with reference to FIG. **6**, in order to ease understanding of embodiments of the invention.

The DC/AC converter **4** illustrated in FIG. **6** is a full-bridge (H**4**) converter with two half-bridge circuits each connected between the input terminals **21**, **22**. Each of these half-bridge circuits includes two switches each having a load path and a control terminal. The load paths of the two switches of one half-bridge circuit are connected in series between the input terminals **21**, **22**, where a first switch $\mathbf{42}_1$ and a second switch $\mathbf{42}_2$ form the first half-bridge, and a third switch $\mathbf{42}_3$ and a fourth switch $\mathbf{42}_4$ form the second half-bridge. Each of the half-bridges includes an output, where an output of the first half-bridge is formed by a circuit node common to the load paths of the first and second switch $\mathbf{42}_1$, $\mathbf{42}_2$. An output of the second half-bridge is formed by a circuit node common to the load paths of the third and fourth switches $\mathbf{42}_3$, $\mathbf{42}_4$. The output of the first half-bridge is coupled to the first output terminal **23** of the converter unit **2** via a first inductive element $\mathbf{44}_1$, such as a choke. The output terminal of the second half-bridge is coupled to the second output terminal **24** of the converter unit **2** via a second inductive element $\mathbf{44}_2$, such as a choke. According to a further embodiment (not illustrated) only one of the first and second inductive elements **44**, $\mathbf{44}_2$ is employed. The converter **4** further includes an input capacitance **41**, such as a capacitance, connected between the input terminals **21**, **22**, and the output capacitance C connected between the output terminals **23**, **24**.

Each of the switches $\mathbf{42}_1$, $\mathbf{42}_2$, $\mathbf{42}_3$, $\mathbf{42}_4$ receives a control signal S$\mathbf{42}_1$, S$\mathbf{42}_2$, S$\mathbf{42}_3$, S$\mathbf{42}_4$ at its control terminal. These control signals S$\mathbf{42}_1$-S$\mathbf{42}_4$ are provided by a drive circuit **45** dependent on the reference signals S_{REF} received from the controller **5**. The drive signal S$\mathbf{42}_1$-S$\mathbf{42}_4$ are pulse-width modulated (PWM) drive signals configured to switch the corresponding switch $\mathbf{42}_1$-$\mathbf{42}_4$ on and off. It should be noted that a switching frequency of the PWM signals S$\mathbf{42}_1$-S$\mathbf{42}_4$ is significantly higher than a frequency of the alternating reference signal S_{REF}. The reference signal SREF may be a sinusoidal signal with a frequency of 50 Hz or 60 Hz, depending on the country in which the power grid is implemented, while the switching frequency of the individual switches $\mathbf{42}_1$-$\mathbf{42}_4$ may be in the range of several kHz up to several 10 kHz, or even up to several 100 kHz. The drive circuit **45** is configured to individually adjust the duty cycle of each of the drive signals S$\mathbf{42}_1$-S$\mathbf{42}_4$ between 0 and 1 in order to have the waveform of the output current i**1** follow the waveform of the reference signal S_{REF}. When the duty cycle of one drive signal is 0, the corresponding switch is permanently switched off, and when the duty cycle of one drive signal is 1, the corresponding switch is permanently switched on. The duty cycle of a drive signal is the relationship between the time period for which the drive signal switches the corresponding switch and the duration of one switching cycle. The duration of one switching cycle is the reciprocal of the switching frequency.

Referring to what has been explained before, the output current i**1** is an AC current with a positive half-cycle in which the output current is positive, and with a negative half-cycle in which the output current i**1** is negative. The time behavior of the output current i**1** is dependent on the reference signal S_{REF} which also has positive and negative half-cycles.

Two possible operating principles of the converter **4** will briefly be explained. First, it is assumed that a positive half-cycle of the output current i**1** is to be generated. According to a first operating principle, which is known as bipolar switching or 2-level switching, the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ are switched on and off synchronously, while the second and third switches $\mathbf{42}_2$, $\mathbf{42}_3$ are permanently switched off. During an on-phase of the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ an output current i**1** is forced through the choke(s) $\mathbf{44}_1$, $\mathbf{44}_2$ that is dependent on the voltage difference between the input voltage V**3** across the input capacitance **41** and the output voltage v**2**, where the output voltage v**2** is

defined by the power grid voltage v_N. The switches $\mathbf{42}_1$-$\mathbf{42}_4$ each include a freewheeling element, such as a diode, that is also illustrated in FIG. **4**. The freewheeling elements of the second and third switches $\mathbf{42}_2$, $\mathbf{42}_3$ take the current flowing through the choke(s) $\mathbf{44}_1$, $\mathbf{44}_2$ when the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ are switched off. In this method, the amplitude of the output current i**1** can be adjusted through the duty cycle of the synchronous switching operation of the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$. When the switching frequency of the switches $\mathbf{42}_1$, $\mathbf{42}_4$ is much higher than the desired frequency of the output current, amplitude, frequency and phase of the AC output current i**1** can be adjusted dependent on the reference signal S_{REF} through the duty cycle of the synchronous switching operation of the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$. During the negative half-cycle the second and third switches $\mathbf{42}_2$, $\mathbf{42}_3$ are switched on and off synchronously, while the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ are permanently off, so that the body diodes of these first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ are conducting. Alternatively, the switches $\mathbf{42}_1$, $\mathbf{42}_4$ are switched (with short dead times) when their body diodes are forward biased, so as to be operated as synchronous rectifiers.

According to a second operating principle, which is known as phase chopping or 3-level switching, the first switch $\mathbf{42}_1$ is permanently switched on during the positive half cycle of the output voltage v**2**, the second and third switches $\mathbf{42}_2$, $\mathbf{42}_3$ are permanently off, and the fourth switch $\mathbf{42}_4$ is switched on and off in a clocked fashion. During an on-phase of the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ an output current i**1** is forced through the choke(s) $\mathbf{44}_1$, $\mathbf{44}_2$ that is dependent on voltage difference between the input voltage V**3** across the input capacitance **41** and the output voltage v**2**, where the output voltage v**2** is defined by the power grid voltage vN. During an off-phase of the fourth switch $\mathbf{42}_4$ a freewheeling path is offered by the freewheeling element of switch $\mathbf{42}_3$ and the switched-on first switch $\mathbf{42}_1$ thus enabling a zero volt state across the output chokes. In this method, the amplitude of the output current i**1** can be adjusted through the duty cycle of the switching operation of the first and fourth switch $\mathbf{42}_1$, $\mathbf{42}_4$. During the negative half-cycle the first and fourth switches $\mathbf{42}_1$, $\mathbf{42}_4$ are permanently switched off, the second switch $\mathbf{42}_2$ is permanently switched on, and the third switch $\mathbf{42}_3$ is switched on and off in a clocked fashion.

In order to control an instantaneous amplitude of the output current i**1** during the positive half-cycle, the drive circuit **45** varies the duty cycle of the at least one switch that is switched on and off in a clocked fashion. The duty cycle of the at least one clocked switch and the duty cycle of its drive signal, respectively, is increased in order to increase the amplitude of the output current i**1** and is decreased in order to decrease the amplitude of the output current i**1**. This duty cycle is dependent on the instantaneous amplitude of the reference signal S_{REF}.

The switches $\mathbf{42}_1$-$\mathbf{42}_4$ may be implemented as conventional electronic switches. Referring to FIG. **7**A, which illustrates a first embodiment for implementing the switches, the switches may be implemented as MOSFETs, specifically as n-type MOSFETs. Electronic switch **42** in FIG. **7**A represents an arbitrary one of the switches $\mathbf{42}_1$-$\mathbf{42}_4$. A MOSFET, such as the n-type MOSFET illustrated in FIG. **7**A has an integrated diode that is also illustrated in FIG. **7**A. This diode is known as body diode and may act as a freewheeling element. A drain-source path, which is a path between a drain terminal and a source terminal, forms a load path of a MOSFET, and a gate terminal forms a control terminal.

Referring to FIG. **7**B, the switches $\mathbf{42}_1$-$\mathbf{42}_4$ could also be implemented as IGBTs, where additionally a diode may be connected between a collector and an emitter terminal of the IGBT. This diode acts as a freewheeling element. In an IGBT, the load path runs between the emitter and the collector terminal, and the gate terminal forms a control terminal.

According to a further embodiment, two of the four switches, such as the first and third transistors $\mathbf{42}_1$, $\mathbf{42}_3$ are implemented as SCR Thyristors, while the other two switches are implemented as MOSFET.

According to yet another embodiment, illustrated in FIG. **7**C, the switches $\mathbf{42}_1$-$\mathbf{42}_4$ can be implemented as GaN-HEMTs (Gallium-Nitride High Electron Mobility Transistors). Unlike a conventional (silicon or silicon carbide) MOSFET a GaN-HEMT does not include an integrated body diode. In a GaN-HEMT, a current conduction in a reverse direction (corresponding to the forward direction of a body diode in a conventional MOSFET) can be obtained through a substrate biased turn-on. When implementing the switches in GaN technology, all switches of one converter unit can be implemented on a common semiconductor substrate.

FIG. **8** schematically illustrates an embodiment of the controller **5** that generates the reference signal S_{REF} dependent on the measurement signal S_{v1} and the output current signal S_{i1}. FIG. **8** shows a block diagram of the controller **5** in order to illustrate its operating principle. It should be noted that the block diagram illustrated in FIG. **8** merely serves to illustrate the functionality of the controller **5** rather than its implementation. The individual function blocks, that will be explained in further detail below, may be implemented using a conventional technology that is suitable to implement a controller. Specifically, the function blocks of the controller **5** may be implemented as analog circuits, digital circuits, or may be implemented using hardware and software, such as a microcontroller on which a specific software is running in order to implement the functionality of the controller **5**.

Referring to FIG. **8**, the controller **5** includes a phase locked loop (PLL) **51** that provides a frequency and phase signal $S_{\omega t}$ representing the frequency and the phase of the measurement signal S_{v1}. The PLL **51** receives the measurement signal S_{v1}. The frequency and phase signal provided by the PLL **51** is received by a signal generator **52**, such as a VCO, that generates a sinusoidal signal $S_{i1\text{-}REF}$ being in phase with the measurement signal Sv**1** and forming a reference signal for the output current i**1** of the converter unit **2**.

Referring to FIG. **8**, the controller further receives the output current signal S_{i1} and calculates an error signal by subtracting the output current signal S_{i1} from the output current reference signal $S_{i1\text{-}REF}$. The subtraction operation is performed by a subtractor receiving the output current measurement signal $S_{i1\text{-}REF}$ and the output current signal S_{i1} at input terminals and providing the error signal at an output terminal. The error signal, which is also a sinusoidal signal is filtered in a filter **53** connected downstream the subtractor **54**. The reference signal S_{REF} is a filtered version of the error signal available at the output of the filter **53**. The filter is, e.g., a proportional (P) filter.

Optionally, a phase signal S_Φ is added to the output signal of the PLL **51** before generating the sinusoidal reference signal $S_{i1\text{-}REF}$. In this embodiment the reference signal $S_{i1\text{-}REF}$ and, therefore, the output current i**1**, has a phase relative to the measurement signal S_{v1}, with the phase shift being defined by the phase signal S_Φ.

FIG. **9** illustrates an embodiment of the PLL **51** of FIG. **6**. This PLL includes a VCO **511** that receives the frequency and phase signal $S_{\omega t}$ and generates an oscillating signal with a frequency and phase dependent on the frequency and phase signal $S_{\omega t}$. This oscillating signal is multiplied with the measurement signal S_{v1} using a multiplier. An output signal of the multiplier is filtered using a low-pass filter **513** and PID filter **514** connected downstream the low-pass filter. Instead of a PID-filter a PI-filter may be used as well. The output signal of the filter **514** is multiplied with 1/s in the frequency domain, where the result of this multiplication is the frequency and phase signal $S_{\omega t}$.

FIG. **10** illustrates a further embodiment of the controller **5**. In this embodiment, a second PLL **51'** receives the output current signal S_{i1} and calculates a further frequency and phase signal representing frequency and phase of the output current signal S_{i1}. The further frequency and phase signal is subtracted from the frequency and phase signal $S_{\omega t}$ representing frequency and phase of the measurement signal S_{v1} (and, optionally, the phase shift S_{ϕ}) using a subtractor **54**, so as to provide an error signal. The error signal is filtered using a filter **53** and a signal generator **52**, such as a VCO, receives the error signal and generates a sinusoidal reference signal with frequency and phase defined by the filtered error signal. In this embodiment, the filter **53** can be implemented as a P-filter or as a PI-filter.

FIG. **11** illustrates a further embodiment of one converter unit **2**. This converter unit besides the DC/AC converter **4** and the controller **5** includes a DC/DC converter **6** connected between the input terminals **21**, **22**, and the DC/AC converter **4**. The DC/AC converter **4** may be implemented as explained with reference to FIGS. **6** to **10** with the difference that the DC/AC converter **4** of FIG. **11** receives a DC input voltage V**6** from the DC/DC converter **6** instead of the input voltage V**3** of the converter unit **2**. A capacitor **60** connected between the terminals **61**, **62** may represent an output capacitor of the DC/DC converter **6** or an input capacitor **41** of the DC/AC converter **4**, or both. This capacitor **60** can be referred to as DC link capacitor.

The DC/DC converter **6** is configured to adjust the input voltage V**3** or the input current I**3** to a voltage or current value, respectively, that is dependent on a reference signal $S_{REF\text{-}V3}$ received by the DC/DC converter **6**. For explanation purposes it is assumed that the DC/DC converter **6** adjusts the input voltage V**3** dependent on the reference signal $S_{REF\text{-}V3}$. Adjusting the input voltage V**3** of the converter unit **2** may help to operate the DC power source **3** connected to the input terminals **21**, **22**, in an optimum operating point. This will be explained in the following.

A solar cell and, therefore, a PV module including several solar cells, acts like a power generator providing a DC output voltage and a DC output current when it is exposed to sunlight. For a given light power received by the PV array there is a range of output currents and a range of corresponding output voltages at which the PV array can be operated. However, there is only one output current and one corresponding output voltage at which the electric power provided by the PV array has its maximum. The output current and the output voltage at which the output power assumes its maximum define the maximum power point (MPP). The MPP varies dependent on the light power received by the array and dependent on the temperature.

Referring to FIG. **11**, the converter unit **2** further includes a maximum power point tracker (MPPT) **7** that is configured to provide the reference signal $S_{REF\text{-}V3}$ such that DC/DC converter **6** adjusts the input voltage such that the DC power source **3** is operated in its MPP. The MPPT **7** receives an input current signal S_{I3} that represents the input current I**3** provided by the DC power source **3** (illustrated in dashed lines in FIG. **9**), and an input voltage signal S_{V3} that represents the input voltage V**3** provided by the DC power source **3**. From the input current signal S_{I3} and the input voltage signal S_{V3} the MPPT **7** calculates the instantaneous input power provided by the DC source **3**. The input voltage signal S_{V3} can be obtained from the input voltage V**3** in a conventional manner by, for example, using a voltage measurement circuit. Equivalently, the input current signal S_{I3} can be obtained from the input current I**3** in a conventional manner using, for example, a current measurement circuit. Those voltage measurement circuits and current measurement circuits are commonly known and are not illustrated in FIG. **11**.

The basic operating principle of the MPPT **7** in order to find the MPP is to vary the reference signal $S_{REF\text{-}V3}$ within a given signal range and to determine the input power provided by the DC power source **3** for each of the input voltages V**3** defined by the different reference signals $S_{REF\text{-}V3}$. The MPPT **7** is further configured to detect the input voltage V**3** for which the maximum input power has been obtained, and to finally set the reference signal $S_{REF\text{-}V3}$ to that value for which the maximum input power has been detected.

Since the solar energy received by the PV array **3** may vary, the MPPT **7** is further configured to check whether the DC power source **3** is still operated in its maximum power point either regularly or when there is an indication that the maximum power point might have changed. An indication that the maximum power point might have changed is, for example, when the input current I**3** represented by the input current signal S_{I3} changes without the reference signal $S_{REF\text{-}V3}$ having changed. The regular check or the event-driven check of the MPPT **7** whether the DC power source **3** is still operated in its maximum power point, may include the same algorithm that has been explained before for detecting the maximum power point for the first time. Conventional algorithms for detecting the maximum power point that can be implemented in the MPPT **7** include, for example, a "hill climbing algorithm" or a "perturb-and-observe algorithm".

The DC/DC converter **6** can be implemented like a conventional DC/DC converter. A first embodiment of a DC/DC converter **6** that can be used in the converter unit **2** is illustrated in FIG. **12**. The DC/DC converter **6** illustrated in FIG. **12** is implemented as a boost converter. This type of converter includes a series circuit with an inductive storage element **64**, such as a choke, and a switch **65** between the input terminals of the DC/DC converter **6**, where the input terminals of the DC/DC converter **6** correspond to the input terminals **21**, **22** of the converter unit **2**. Further, a rectifier element **66**, such as a diode, is connected between a circuit node common to the inductive storage element **64** and the switch **65** and a first output terminal **61** of the DC/DC converter **6**. A second output terminal **62** of the DC/DC converter **6** is connected to the second input terminal **22**. An output voltage V**6** of the DC/DC converter is available between the output terminals **61**, **62**. Referring to FIG. **12**, the DC/DC converter **6** may further include a first capacitive storage element **63**, such as a capacitor, between the input terminals **21**, **22**, and a second capacitive storage element **68**, such as a capacitor, between the output terminals **61**, **62**. The second capacitive storage element **68** acts as an energy storage that is necessary when generating the AC output current i**1** from the DC voltage V**6** available at the output of the DC/DC converter **6**.

The switch **65** can be implemented as a conventional electronic switch, such as a MOSFET or an IGBT. Further, the rectifying element **66** could be implemented as a synchronous rectifier, which is a rectifier implemented using an electronic switch, such as a MOSFET or an IGBT. According to a further embodiment, the switch **65** is implemented as GaN-HEMT.

The DC/DC converter **6** further includes a control circuit (controller) **67** for generating a drive signal S**65** for the switch **65**. This drive signal S**65** is a pulse-width modulated (PWM) drive signal. The PWM controller **67** is configured to adjust the duty cycle of this drive signal S**65** such that the input voltage V**3** corresponds to the desired input voltage as represented by the reference signal $S_{REF\text{-}V3}$. For this, the control circuit **67** receives the reference signal $S_{REF\text{-}V3}$ and the input voltage signal S_{V3} that represents the input voltage V**3**.

A first embodiment of the PWM control circuit **67** is illustrated in FIG. **13**. Like in FIG. **8** (which illustrates an embodiment of the controller **5**) in FIG. **11** functional blocks of the controller **67** are illustrated. These functional blocks can be implemented as analog circuits, as digital circuits or can be implemented using hardware and software. Referring to FIG. **13**, the control circuit **67** calculates an error signal S_{ERR} from the input voltage signal S_{V3} and the reference signal $S_{REF\text{-}V3}$. The error signal S_{ERR} is calculated by either subtracting the input voltage signal S_{V3} from the reference signal $S_{REF\text{-}V3}$ (as illustrated) or by subtracting the reference signal $S_{REF\text{-}V3}$ from the input voltage signal S_{V3}. The error signal S_{ERR} is provided by a subtraction element **671** that receives the input voltage signal S_{V3} and the reference signal $S_{REF\text{-}V3}$.

The error signal S_{ERR} is received by a filter **672** that generates a duty cycle signal S_{DC} from the error signal S_{ERR}. The duty cycle signal S_{DC} represents the duty cycle of the drive signal S**65** provided by the control circuit **67**. The filter **672** can be a conventional filter for generating a duty cycle signal S_{DC} from an error signal S_{ERR} in a PWM controller of a DC/DC converter, such as a P-filter, a PI-filter, or a PID-filter.

A PWM driver **673** receives the duty cycle signal S_{DC} and a clock signal CLK and generates the drive signal S**65** as a PWM signal having a switching frequency as defined by the clock signal CLK and a duty cycle as defined by the duty cycle signal S_{DC}. This driver **673** can be a conventional PWM driver that is configured to generate a PWM drive signal based on a clock signal and a duty cycle information. Such drivers are commonly known, so that no further information are required in this regard.

The basic control principle of the controller **67** of FIG. **12** will briefly be explained. Assume that the input voltage V**3** has been adjusted to a given value represented by the reference signal $S_{REF\text{-}V3}$ and that the reference signal $S_{REF\text{-}V3}$ changes, so that the input voltage V**3** has to be readjusted. For explanation purposes it is assumed that the input voltage V**3** is to be increased as defined by the reference signal $S_{REF\text{-}V3}$. In this case the control circuit **67** reduces the duty cycle of the drive signal S**65**. Reducing the duty cycle of the drive signal S**65** results in a decreasing (average) input current I**3**, where decreasing the input current I**3**, at a given power provided by the DC power source **3** results in an increasing input voltage V**3**. Equivalently, the duty cycle is increased when the input voltage V**3** is to be decreased. An increase in the duty cycle results in an increase of the input current I**3**.

The boost converter according to FIG. **12** does not only provide a load to the DC power source **3** in order to operate the DC power source **3** in its maximum power point. This boost converter also generates an output voltage V**6** received by the DC/AC converter **4** (see FIG. **11**) that is higher than the input voltage V**3**. Further, the boost converter is implemented such that the output voltage V**6** is higher than a peak voltage of the output voltage v**2** of the DC/AC converter, but lower than a voltage blocking capability of the switches (see $\mathbf{42}_1$-$\mathbf{42}_4$ in FIG. **6**) implemented in the DC/AC converter.

Referring to FIG. **14**, the DC/DC converter **6** may also be implemented as a buck converter. This buck converter includes a series circuit with an inductive storage element **64**, such as a choke, and a switch **65** between the first input terminal **21** and the first output terminal **61**. A freewheeling element **66**, such as a diode, is connected between the second output terminal **62** and a circuit node common to the inductive storage element **64** and the switch **65**. A capacitive storage element **63**, such as a capacitor, is connected between the input terminals **21**, **22**.

Like in the boost converter of FIG. **12**, the switch **65** in the buck converter of FIG. **14** can be implemented as a conventional electronic switch, such as a MOSFET or an IGBT, or could be implemented as a GaN-HEMT. Further, the freewheeling element **66** could be implemented as a synchronous rectifier.

Like in the boost converter according to FIG. **12**, the switch **65** in the buck converter according to FIG. **14** is driven by a PWM drive signal S**65** provided by a control circuit **67**. The control circuit **67** may be implemented as illustrated in FIG. **13**. The operating principle of the control circuit **67** in the buck converter of FIG. **14** is the same as in the boost converter of FIG. **12**, i.e., the duty cycle of the drive signal S**65** is increased when the input voltage V**3** is to be decreased, and the duty cycle is decreased, when the input voltage V**3** is to be increased.

It should be noted that implementing the DC/DC converter **6** as a boost converter (see FIG. **12**) or as a buck converter (see FIG. **14**) is only an example. The DC/DC converter **6** could also be implemented as a buck-boost converter, a boost-buck-converter, a flyback converter, and so on. Whether a boost converter or a buck converter is used as a DC/DC converter for tracking the maximum power point of the DC power source **3** and for providing the input voltage V**6** to the DC/AC converter **4**, influences the number of converter units **2** to be connected in series in order for the sum of the output voltages v**2** of the converter units **2** to correspond to the external AC voltage v**1**. This will be explained by the way of an example in the following.

Assume that there is an external AC voltage v**1** with $240V_{RMS}$ is desired. The peak voltage (maximum amplitude) of this voltage v**1** is 338V (240V·sqrt(2), where sqrt is the square root). Further assume that the DC power sources **3** are PV arrays each providing an output voltage between 24V and 28V when exposed to sunlight. The DC/AC converter **4** has a buck characteristic, which means that the peak value of the output voltage v**2** (see FIG. **4**) is less than the received DC input voltage V**3** or V**6**, respectively. Thus, when buck converters are employed as DC/DC converters **6** in the converter units **2** or when no DC/DC converters are used, at least 15 converter units **2** with PV panels connected thereto need to be connected in series. This is based on the assumption that each PV array generates a minimum voltage of V**3**=24V and that a peak voltage of the external AC voltage v**1** is 338V. The number of 15 is obtained by simply dividing 338V through 24V (338V/24V=14.08) and rounding the result to the next highest integer.

When, however, a boost converter is used as the DC/DC converter **6** that, for example, generates an output voltage

V**6**=60V from the input voltage V**3** (which is between 24V and 28V) the number of converter units **2** to be connected in series may be reduced to about 6.

In the DC/AC converter **4** illustrated in FIG. **11**, the output voltage V**6** of the DC/DC converter **6** may vary dependent on the input power received at the input terminals **21**, **22** from the DC power source **3** and dependent on the output current i**1** or, more exactly, dependent on the average of the output current i**1**. According to a further embodiment illustrated in FIG. **15**, the control circuit **5** is further configured to control the input voltage of the DC/AC converter **4** and the output voltage of the DC/DC converter **6**, respectively. For this, the control circuit **5** receives an input voltage signal S_{V6} that represents the input voltage V**6**. The control circuit **5** is configured to adjust the input voltage V**6** by varying the duty cycle of those switches in the DC/AC converter **4** that are driven in a clocked fashion. The input voltage can be increased by generally decreasing the duty cycle and can be decreased by generally increasing the duty cycle. For this, the control circuit **5** includes a further control loop, where this control loop is slower than the control loop that causes the output current i**1** to follow the reference signal S_{REF}. This control loop is, for example configured to cause variations of the duty cycle at a frequency of between 1 Hz and 10 Hz.

The control circuit **5** of FIG. **15** is based on the control circuit illustrated in FIG. **8** and additionally includes a further control loop that serves to adjust the amplitude of the output current reference signal $S_{i1\text{-}REF}$ dependent on the input voltage signal S_{V6}. Instead of the control loop illustrated in FIG. **8**, the control circuit according to FIG. **15** could also be implemented based on the control circuit of FIG. **10**. Referring to FIG. **15**, the control loop includes a further subtraction element **56**, a filter **55**, and a multiplier **57**. The subtraction element **56** receives the input voltage signal S_{V6} and a reference signal $S_{V6\text{-}REF}$ that represents a set value of the input voltage V**6**. The subtraction element **56** generates a further error signal based on a difference between the input voltage signal S_{V6} and the reference signal $S_{V6\text{-}REF}$. The filter **55** receives the further error signal and generates an amplitude signal S_{AMPL} representing an amplitude of the reference signal S_{REF} from the further error signal. The filter may have a P-characteristic, an I-characteristic, a PI-characteristic, or a PID-characteristic. The amplitude signal S_{AMPL} and the output signal of the VCO **52** are received by the multiplier **57** that provides the output current reference signal $S_{i1\text{-}REF}$. The output current reference signal $S_{i1\text{-}REF}$ has an amplitude that is dependent on the input voltage V**6** and that serves to control the input voltage V**6** of the DC/AC converter (**4** in FIG. **11**), and a frequency and phase of the output current i**1**. The frequency and the phase of the reference signal S_{REF} are dependent on the at least one measurement signal S_{v1} and the output current signal S_{i1} and serve to adjust frequency and phase of the output current i**1** such that there is a given phase difference between the output current and the output voltage.

The input voltage reference signal $S_{V6\text{-}REF}$ may have a fixed value that is, selected such that the input voltage V**6** is sufficiently below the voltage blocking capability of switches employed in the DC/AC converter. However, it is also possible to vary the input voltage reference signal $S_{V6\text{-}REF}$ dependent on the output current, specifically on the RMS value of the output current i**1**. According to one embodiment, the input voltage reference signal $S_{V6\text{-}REF}$ decreases when the output current i**1** increases, and the input voltage reference signal $S_{V6\text{-}REF}$ increases when the output current decreases. According to one embodiment, the input voltage reference signal $S_{V6\text{-}REF}$ has a first signal value when the output current i**1** is below a given threshold value, and has a lower second signal value when the output current i**1** is above a given threshold value.

The control circuit illustrated in FIG. **15** could also be implemented in a converter as illustrated in FIG. **6** in which the DC/DC converter is omitted. In this case, the input voltage to be controlled is the output voltage V**3** of the PV module, so that the voltage signal S_{V6} in FIG. **15** is replaced by the voltage signal S_{V3} representing the output voltage of the DC source **3**, and the input voltage reference signal $S_{V6\text{-}REF}$ is replaced by the reference signal $S_{V3\text{-}REF}$ defining a desired output voltage of the DC power source **3**. The input voltage reference signal $S_{V3\text{-}REF}$ may in this case be provided by an MPPT in order to operate the DC power source (PV module) **3** in its MPP.

FIG. **16** illustrates a further embodiment of a DC/DC converter **6** that can be implemented in a DC/AC converter unit **2** of FIG. **11**. The DC/DC converter of FIG. **16** is implemented as a boost converter with two converter stages $\mathbf{60}_1$, $\mathbf{60}_2$. The two converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ are connected in parallel between the input terminals **21**, **22** and the output terminals **61**, **62**. Each of the converter units $\mathbf{60}_1$, $\mathbf{60}_2$ is implemented like the boost converter of FIG. **12** and includes a series circuit with an inductive storage element $\mathbf{64}_1$, $\mathbf{64}_2$, such as a choke, and a switch $\mathbf{65}_1$, $\mathbf{65}_2$ between the input terminals of the DC/DC converter **6**, where the input terminals of the DC/DC converter **6** correspond to the input terminals **21**, **22** of the converter unit **2**. Further, each converter stage includes a rectifier element $\mathbf{66}_1$, $\mathbf{66}_2$ such as a diode, connected between a circuit node common to the corresponding inductive storage element $\mathbf{64}_1$, $\mathbf{64}_2$ and the corresponding switch $\mathbf{65}_1$, $\mathbf{65}_2$ and the first output terminal **61** of the DC/DC converter **6**. The second output terminal **62** of the DC/DC converter **6** is connected to the second input terminal **22**.

The two converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ share the first capacitive storage element **63** between the input terminals **21**, **22**, and share the second capacitive storage element **68** between the output terminals **61**, **62**. The output voltage V**6** of the DC/DC converter **6** is available across the second capacitive storage element **68**.

Referring to FIG. **16**, the control circuit (controller) **67** of the DC/DC converter **6** generates two PWM drive signals $S\mathbf{65}_1$, $S\mathbf{65}_2$, namely a first drive signal $S\mathbf{65}_1$ for the switch $\mathbf{65}_1$ of the first converter stage $\mathbf{60}_1$, and a second drive signal $S\mathbf{65}_2$ for the switch $\mathbf{65}_2$ of the second converter stage $\mathbf{60}_2$. According to one embodiment, the first and second boost converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ are operated interleaved, which means that there is a time offset between the switching cycles of the first switch $\mathbf{65}_1$ and the switching cycles of the second switch $\mathbf{65}_2$. Providing two converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ and operating these converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ in an interleaved mode helps to reduce voltage ripples of the input voltage V**3** and the output voltage V**6** of the DC/DC converter **6**. Of course, more than two boost converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ can be connected in parallel.

Referring to FIG. **16**, each boost converter stage $\mathbf{60}_1$, $\mathbf{60}_2$ provides an output current $\mathbf{I6}_1$, $\mathbf{I6}_2$. These output currents $\mathbf{I6}_1$, $\mathbf{I6}_2$ add and form the overall output current I**6** of the DC/DC converter. FIG. **17** illustrates a first embodiment of the controller **67** configured to generate PWM drive signals $S\mathbf{65}_1$, $S\mathbf{65}_2$ for each converter stage $\mathbf{60}_1$, $\mathbf{60}_2$, and further configured to generate the PWM drive signals $S\mathbf{65}_1$, $S\mathbf{65}_2$ such that the output currents $\mathbf{I6}_1$, $\mathbf{I6}_2$ of the converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ are balanced.

Referring to FIG. **17** the control circuit **67** is based on the control circuit **67** of FIG. **13** and includes the subtraction element **671** receiving the input voltage signal S_{V3} and the input voltage reference signal $S_{REF\text{-}V3}$ and the filter **672** for providing the duty cycle signal S_{DC}. The controller **67** of FIG. **17** further includes a first PWM driver $\mathbf{673}_1$ receiving a first duty cycle signal S_{DC1} that is dependent on the duty cycle signal S_{DC} provided by the filter **672** and receiving a first clock signal CLK_1, and a second PWM driver $\mathbf{673}_2$ receiving a second duty-cycle signal S_{DC2} that is dependent on the duty cycle signal S_{DC} provided by the filter **672** and receiving a second clock signal CLK_2. According to one embodiment, the first and second clock signals CLK_1, CLK_2 have the same frequency. However, there is a phase shift between the first and second clock signal CLK_1, CLK_2, so that there is a phase shift between the first PWM drive signal $S\mathbf{65}_1$ provided by the first PWM driver $\mathbf{673}_1$ and the second PWM drive signal $S\mathbf{65}_2$ provided by the second PWM driver $\mathbf{673}_2$.

If the first and second converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ would perfectly match so that there would be no risk of unbalanced output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$, the duty cycle signal S_{DC} could be used as the first duty cycle signal S_{DC1} and as the second duty cycle signal S_{DC2}. However, due to an inevitable mismatch of the components in the converter stages $\mathbf{60}_1$, $\mathbf{60}_2$ the output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$ can be unbalanced when the first and second drive signal $S\mathbf{65}_1$, $S\mathbf{65}_2$ would be generated with exactly the same duty cycle.

In order to compensate for such unbalances of the first and second output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$, the controller **67** of FIG. **17** includes an additional control loop, that can be referred to as current balancing loop or power balancing loop. This control loop receives a first output current signal S_{I61} representing the first output current $I\mathbf{6}_1$ of the first converter stage $\mathbf{60}_1$, and a second output current signal S_{I62} representing the output current $I\mathbf{6}_2$ of the second converter stage $\mathbf{60}_2$. These output current signals S_{I61}, S_{I62} can be generated using conventional current measurement units. The output current signals S_{I61}, S_{I62} are received by a subtraction unit **675** that generates a further error signal S_{ERR2}. The further error signal S_{ERR2} is representative of a difference between the first and second output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$. Further error signal S_{ERR2} is received by a filter **676** that generates a filtered error signal. The filter **676** may have a P-characteristic, a I-characteristic, or a PI-characteristic.

A further subtraction unit $\mathbf{674}_1$ subtracts the filtered error signal from the duty cycle signal S_{DC} to generate the first duty cycle signal S_{DC1}, and an adder $\mathbf{674}_2$ adds the filtered error signal to the duty cycle signal S_{DC} to generate the second duty cycle signal S_{DC2}.

The operating principle of the controller **67** of FIG. **17** is as follows. When the first and second output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$ are identical, the further error signal S_{ERR2} is zero. In this case, the first duty cycle signal S_{DC1} corresponds to the second duty cycle signal S_{DC2}. When, for example, the first output current $I\mathbf{6}_1$ is larger than the second output current $I\mathbf{6}_2$, the further error S_{ERR2} and the filtered error signal have a positive value. In this case, the duty cycle signal S_{DC1} (obtained by subtracting the filtered error signal from the duty cycle signal S_{DC}) becomes smaller than the second duty cycle signal S_{DC2} (obtained by adding the filtered error signal to the duty cycle signal S_{DC}). Thus, the duty cycle of the first drive signal $S\mathbf{65}_1$ becomes smaller than the duty cycle of the second drive signal $S\mathbf{65}_2$ in order to reduce the first output current $I\mathbf{6}_1$ and to increase the second output current $I\mathbf{6}_2$, so as to balance these output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$.

FIG. **18** illustrates a further embodiment of the control circuit **67** that is configured to balance the output currents $I\mathbf{6}_1$, $I\mathbf{6}_2$. The control circuit **67** of FIG. **18** is based on the control circuit **67** of FIG. **17**. In the control circuit **67** of FIG. **18**, the subtraction unit $\mathbf{674}_1$ that generates the first duty cycle signal S_{DC1} does not receive the duty cycle signal S_{DC} but receives a filtered version of a difference between the duty cycle signal S_{DC} and the first output current signal S_{I61}. A subtraction unit $\mathbf{677}_1$ calculates the difference and a filter $\mathbf{678}_1$, filters the difference. The filter may have a P-characteristic, an I-characteristic or PI-characteristic. Equivalently, the adder $\mathbf{674}_2$ that provides the second duty cycle signal S_{DC2} does not receive the duty cycle signal S_{DC} but receives a filtered difference between the duty cycle signal S_{DC} and the second input current signal S_{I62}. A subtraction unit $\mathbf{677}_2$ calculates the difference between the duty cycle signal S_{DC} and the second output current signal S_{I62}, and a filter $\mathbf{678}_2$ filters the difference. The output signals of the filter $\mathbf{678}_1$, $\mathbf{678}_2$ are received by the subtraction unit $\mathbf{674}_1$ and the adder $\mathbf{674}_2$, respectively.

While in the embodiment illustrated in FIG. **17** a single control loop is employed to regulate the input voltage V**3**, a dual control loop structure is employed in the embodiment according to FIG. **18**.

FIG. **19** illustrates a further embodiment of a converter unit **2** with a DC/AC converter **4**. The converter unit **2** may further include a DC/DC converter **6** (see FIG. **9**) connected between the input terminals **21**, **22** and the DC/AC converter **4**. However, such DC/DC converter is not illustrated in FIG. **13**. Dependent on whether or not the converter unit **2** includes a DC/DC converter, the DC/AC converter **4** receives the input voltage V**3** of the converter unit **2** or the output voltage of the DC/AC converter **4** (not illustrated in FIG. **19**) as an input voltage. Just for explanation purposes it is assumed that the DC/AC converter **4** receives the input voltage V**3**.

The DC/AC converter **4** of FIG. **19** includes a buck converter **80** that receives the input voltage V**3** as an input voltage. The buck converter **80** is configured to generate an output current i**80** which is a rectified version of the output current i**1** of the DC/AC converter **4**. Assume, for example that a desired waveform of the output current i**1** is a sinusoidal waveform. In this case, the output current i**80** provided by the converter **80** has the waveform of a rectified sinusoidal curve or the waveform of the absolute value of a sinusoidal curve, respectively. This is schematically illustrated in FIG. **20**, in which exemplary timing diagrams of a sinusoidal output current i**1** and the corresponding output current i**80** of the converter **80** are illustrated.

The output current i**1** of the DC/AC converter **4** is produced from the output current i**80** of the buck converter **80** using a bridge circuit **85** with two half-bridges, where each of these half-bridges is connected between output terminals **81**, **82** of the buck converter **80**. This bridge circuit **85** can be referred to as unfolding bridge. A first half-bridge includes a first and a second switch $\mathbf{85}_1$, $\mathbf{85}_2$ connected in series between the output terminals **81**, **82**, and a second half-bridge includes a third switch $\mathbf{85}_3$ and a fourth switch $\mathbf{85}_4$ connected in series between the output terminals **81**, **82**. An output terminal of the first half-bridge, which is a circuit node common to the first and second switches $\mathbf{85}_1$, $\mathbf{85}_2$ is coupled to the first output terminal **23**. An output terminal of the second half-bridge, which is a circuit node common to the third and fourth switch $\mathbf{85}_3$, $\mathbf{85}_4$ is coupled to the second output terminal **24** of the converter unit **2**. Optionally, an EMI filter **88** with two inductances, such as chokes, is coupled between the output terminals of the half-bridges and

the output terminals **23**, **24** of the converter unit **2**. The output capacitance C of the converter unit **2** that is connected between the output terminals can be part of the EMI filter **88**.

Referring to FIG. **19**, the output current i**80** of the buck converter **80** has a frequency which is twice the frequency of the output current i**1**. A switching frequency of the switches $\mathbf{85}_1$-$\mathbf{85}_4$ of the bridge circuit **85** corresponds to the frequency of the output current i**1**. During a positive half-cycle of the output current i**1** the first and fourth switch $\mathbf{85}_1$, $\mathbf{85}_4$ are switched on, and during a negative half-cycle of the output voltage v**2** the second and third switches $\mathbf{85}_2$, $\mathbf{85}_3$ are switched on. The switches of the bridge circuit **85** are driven by drive signals S$\mathbf{85}_1$-S$\mathbf{85}_4$ generated by a drive circuit **90**. Timing diagrams of these drive signals S$\mathbf{85}_1$-$\mathbf{585}_4$ are also illustrated in FIG. **20**. In FIG. **20**, a high signal level of these timing diagrams represents an on-level of the corresponding drive signal S$\mathbf{85}_1$-S$\mathbf{85}_4$. An on-level of the drive signal is a signal level at which the corresponding switch is switched on. The drive signals S$\mathbf{85}_1$-S$\mathbf{85}_4$ may, for example, be generated dependent on the output voltage v**80** of the buck converter **80**, where, according to one embodiment, drive circuit **90** changes the switching state of the switches each time the output voltage v**80** has decreased to 0. "Changing the switching state" means either switching the first and the fourth switches $\mathbf{85}_1$, $\mathbf{85}_4$ on and the other two switches off, or means switching the second and the third switch $\mathbf{85}_2$, $\mathbf{85}_3$ on and the other two switches off.

The buck converter **80** may have a conventional buck converter topology and may include a switch **83** connected in series with an inductive storage element **84**, where the series circuit is connected between the first input terminal **21** of the converter unit **2** or the first output terminal **61** of a DC/DC converter (not shown), and the first output terminal **81** of the buck converter **80**, respectively. A rectifier element **86** is connected between the second output terminal **82** (corresponding to the second input terminal **22**) of the buck converter and a circuit node common to the switch **83** and the inductive storage element **84**. The switch **83** can be implemented as a conventional electronic switch, such as a MOSFET or an IGBT, or as a GaN-HEMT. The rectifier element **86** can be implemented as a diode or as a synchronous rectifier. Further, a capacitive storage element **91**, such as a capacitor, is connected between the input terminals of the buck converter **80**, and an optional smoothing capacitor **89** is connected between the output terminals **81**, **82**.

The switch **83** of the buck converter **80** is driven by a PWM drive signal S**83** generated by a control circuit or controller **87**. The controller **87** of the buck converter **80** receives the reference signal S_{REF} from the controller **5** of the converter unit **2**. The controller **87** of the buck converter **80** is configured to generate its output current i**80** in correspondence with the reference signal S_{REF}. This reference signal S_{REF} according to FIG. **19**, unlike the reference signal S_{REF} of FIG. **11**, does not have the waveform of the output current i**1**, but has the waveform of the rectified output current i**1**. This reference signal S_{REF} is also generated from the measurement signal S_{v1} and the output current signal S_{i1}.

The controller **5** for generating the reference signal S_{REF} according to FIG. **19** may correspond to the controllers illustrated in FIGS. **8** and **15** with the difference that the oscillating signal provided at the output of the filter **53** is rectified. An embodiment of the controller **5** according to FIG. **19** is illustrated in FIG. **21**. This controller **5** corresponds to the controller according to FIG. **8** with the difference that the output signal of the filter **53** is received by a rectifier **58** that generates a rectified version of the oscillating output signal of the filter **53**. Mathematically this is equivalent to forming the absolute value of the oscillating output signal of the filter **53**. The reference signal S_{REF} is available at the output of the rectifier **58**.

FIG. **22** illustrates a further embodiment of a controller **5** that can implemented in the DC/AC converter **4** of FIG. **19**. The controller **5** of FIG. **22** is based on the controller **5** of FIG. **15** with the difference that the amplitude signal S_{AMPL} is generated from the input voltage signal S_{V3} that represents the input voltage V**3** provided by the DC power source **3**, and from the input voltage reference signal $S_{V3\text{-}REF}$. The input voltage reference signal $S_{V3\text{-}REF}$ can be generated by an MPPT, such as an MPPT **7** explained with reference to FIG. **11**.

The control loops illustrated in FIGS. **15**, **21** and **22** could, of course, be amended to be based on the control loop structure of FIG. **10** instead of FIG. **8**.

Referring to FIG. **19**, the controller **87** of the buck converters **80** can be implemented like a conventional controller for providing a PWM drive signal in a buck converter. The controller **87** receives the reference signal S_{REF} and an output current signal S_{i80}, where the output current signal S_{i80} represents the output current vi**80** of the buck converter **80**. The controller **87** is configured to vary the duty cycle of the drive signal S**83** such that the output current i**80** of the buck converter **80** is in correspondence with the reference signal S_{REF}. The functionality of this controller **87** corresponds to the functionality of the controller **67** illustrated in FIG. **13**. In the embodiment illustrated in FIG. **19** the controller receives the output current signal S_{i1} representing the output current i**1** and the measurement signal S_{v1} for generating the reference signal S_{REF}. However, this is only an example. It would also be possible to generate the reference signal S_{REF} based on signals representing the output voltage v**80** and the output current i**80** of the buck converter **80**. In this case, the reference signal is generated such that output current i**80** and the output voltage v**80** of the buck converter **80** have a given phase difference.

The operating principle of a power converter circuit **1** including DC/AC converters as illustrated in FIG. **19** will now be explained with reference to FIGS. **1** and **19**. The explanation will be based on the assumption that the voltage of the power grid **100** is a sinusoidal voltage so that an output current i**1** with a sinusoidal waveform is desired. Further, it is assumed that the input powers of the individual DC/AC converters is zero, while the power grid voltage v_N is applied to the input terminals **11**, **12** and the bridge circuits **85** in the individual converter units are in operation. In this case, the smoothing capacitors **89** of the buck converters are connected in series between the output terminals **11**, **12**. When the individual capacitors **89** have the same size, the voltage across each of these capacitors **89** is 1/n times the power grid voltage v_N.

Assume now that the DC/AC converters receives an input power from the PV modules **3** connected thereto. The DC/AC converters then adjust their common output current i**1** to be in phase with the external voltage v**1** (the power grid voltage). The amplitude of the output current i**1** is, in particular, controlled through the input voltage V**3**, where the current is increased when the voltage V**3** increases, and the current is decreased when the voltage V**3** decreases.

When the output current i**1** provided by one DC/AC converter decreases, a current that corresponds to a difference between the output current i**1** and the common current $\mathbf{i1}_{OUT}$ is provided by the output capacitor C which causes the voltage v**2** across the output capacitor C to decrease until the input power provided to the DC/AC converter corresponds

to its output power. A decrease of the voltage v**2** across the output capacitor **89** of one DC/AC converter **4** or one converter unit **2** causes an increase of the voltages across the output capacitors of the other converter units. This process proceeds until the converter unit **2** has settled in stable operation point at a lower output current i**1**. If the other converter units **2** at first continue to run at the same duty cycle, the increase of the voltages across their output capacitors leads to a reduction of their output currents i**1** (and hence to a reduction of the common output current) in order to keep their output powers equal their input powers. When the output current i**1** provided by one DC/AC converter increases so as to be higher than the common current $i\mathbf{1}_{OUT}$, the corresponding output capacitor C is charged which results in an increase of the voltage across the output capacitor C of the one converter and a decrease of the voltage across the output capacitors of the other converters.

It became obvious from the explanation provided before that besides the control loops in the individual converter units **2** no additional control loop is required in order to control the output voltages of the individual converter units **2**. The power converter circuit **1** with the converter units **2** is "self organizing." Referring to FIG. **1**, assume that, for example, in the steady state the input power provided by the first DC power source $\mathbf{3}_1$ to the first converter unit $\mathbf{2}_1$ would drop, for example, because the corresponding PV array is shaded. The output voltage $v\mathbf{2}_1$ of the corresponding converter unit **2** would then drop, while the output voltages of the other converter units $\mathbf{2}_2$, $\mathbf{2}_n$ would increase in order to meet the condition defined by equation (1). Further, the common output current $i\mathbf{1}_{OUT}$ would decrease. The transient process is as follows. When the input power received by the first converter unit $\mathbf{2}_1$ decreases, the common output current $i\mathbf{1}_{OUT}$ at first remains unchanged, while the output current $i\mathbf{1}_1$ of the first converter unit $\mathbf{2}_1$ decreases. The decrease of the output current $i\mathbf{1}_1$ and the unchanged common output current $i\mathbf{1}_{OUT1}$ causes a discharging of the output capacitor C_1 of the first converter unit $\mathbf{2}_1$ so that the output voltage $v\mathbf{2}_1$ decreases. A decrease of the output voltage of the first converter unit, however, causes an increase of the output voltages of the other converters, which now decrease their output currents in order to keep their output powers equal their input powers. The transition processes finishes when a "new" common output current $i\mathbf{1}_{OUT}$ has settled in to which the individual output currents i**1** correspond. This is a self-organizing and self-stabilizing process that does not require and additional control loop besides the control loops in the individual converter units **2** disclosed before.

FIG. **23** illustrates a further embodiment of a power converter circuit **1**. In this power converter circuit two series circuits $\mathbf{1}_I$, $\mathbf{1}_{II}$ each including one group with a plurality of converter units $\mathbf{2}_{I1}$-$\mathbf{2}_{In}$, and $\mathbf{2}_{II1}$-$\mathbf{2}_{IIn}$ connected in series are connected in parallel between the output terminals **11**, **12**. Each of the series circuits $\mathbf{1}_I$, $\mathbf{1}_{II}$ can be implemented in accordance with the series circuit **1** of converter units $\mathbf{2}_1$-$\mathbf{2}_n$ explained before. The converter units of the two groups (the two series circuits) are coupled to the same measurement circuit **10** that can be implemented in accordance with one of the embodiments explained before. Of course, more than two series circuits each with a plurality of converter units can be connected in parallel.

Although various exemplary embodiments of the invention have been disclosed, it will be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the spirit and scope of the invention. It will be obvious to those reasonably skilled in the art that other components performing the same functions may be suitably substituted. It should be mentioned that features explained with reference to a specific figure may be combined with features of other figures, even in those cases in which this has not explicitly been mentioned. Further, the methods of the invention may be achieved in either all software implementations, using the appropriate processor instructions, or in hybrid implementations that utilize a combination of hardware logic and software logic to achieve the same results. Such modifications to the inventive concept are intended to be covered by the appended claims.

Spatially relative terms such as "under," "below," "lower," "over," "upper," and the like, are used for ease of description to explain the positioning of one element relative to a second element. These terms are intended to encompass different orientations of the device in addition to different orientations than those depicted in the figures. Further, terms such as "first," "second," and the like, are also used to describe various elements, regions, sections, etc. and are also not intended to be limiting. Like terms refer to like elements throughout the description.

As used herein, the terms "having," "containing," "including," "comprising," and the like are open ended terms that indicate the presence of stated elements or features, but do not preclude additional elements or features. The articles "a," "an," and "the" are intended to include the plural as well as the singular, unless the context clearly indicates otherwise.

With the above range of variations and applications in mind, it should be understood that the present invention is not limited by the foregoing description, nor is it limited by the accompanying drawings. Instead, the present invention is limited only by the following claims and their legal equivalents.

It is to be understood that the features of the various embodiments described herein may be combined with each other, unless specifically noted otherwise.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A power converter circuit, comprising:

output terminals configured to receive an external AC voltage;

at least one series circuit with at least two DC/AC converter circuits, each DC/AC converter circuit comprising input terminals configured to be coupled to a DC power source, and output terminals for providing an AC output current, the at least one series circuit connected between the output terminals of the power converter circuit; and

a voltage divider circuit connected between the output terminals of the power converter circuit and configured to provide at least one measurement signal that includes a phase and frequency based on the external AC voltage;

wherein at least one of the DC/AC converter circuits is configured to receive the at least one measurement signal and is configured to regulate generation of the AC output current dependent on the at least one mea-

surement signal such that a phase difference between the AC output current and the external AC voltage assumes a set value.

2. The power converter circuit of claim **1**,

wherein the voltage divider circuit comprises a plurality of passive circuit components connected in series between the output terminals of the power converter circuit, and

wherein each passive circuit component is configured to provide one measurement signal having a phase and frequency based on the phase and frequency of the external AC voltage, and wherein each measurement signal is received by one DC/AC converter circuit.

3. The power converter circuit of claim **2**, wherein the measurement signal provided by one passive circuit component comprises a voltage across the passive circuit component or a fraction thereof.

4. The power converter circuit of claim **2**, wherein each passive circuit component includes a resistor or a capacitor.

5. The power converter circuit of claim **1** wherein the set value is zero.

6. The power converter circuit of claim **1**, wherein the at least one DC/AC converter circuit comprises:

a DC/AC converter coupled between the input terminals and the output terminals of the DC/AC converter circuit and configured to generate the AC output current with a frequency and phase that is dependent on a first reference signal; and

a control circuit configured to generate the first reference signal dependent on the at least one measurement signal and the AC output current of the DC/AC converter circuit.

7. The power converter circuit of claim **6**, wherein the DC/AC converter comprises at least one switch that comprises a GaN-HEMT.

8. The power converter circuit of claim **7**, wherein the control circuit comprises:

a phase-locked loop configured to generate a frequency dependent on the at least one measurement signal;

a phase detector configured to detect a phase difference between the phase represented by the at least one measurement signal and a phase of the AC output current and to provide a first phase difference based on the detected phase difference; and

an oscillator configured to generate the first reference signal dependent on the generated frequency and the first phase difference.

9. The power converter circuit of claim **7**,

wherein the DC/AC converter is configured to receive an input voltage, and

wherein the control circuit is configured to generate the first reference signal dependent on the input voltage.

10. The power converter circuit of claim **7**, wherein

the DC/AC converter is coupled to a second reference signal terminal; and

the at least one DC/AC converter circuit further comprises a DC/DC converter coupled between the input terminals of the at least one DC/AC converter circuit and the DC/AC converter, the DC/DC converter configured to adjust an input voltage between the input terminals or an input current at the input terminals dependent on a second reference signal.

11. The power converter circuit of claim **10**, wherein the DC/DC converter comprises at least one switch comprising a GaN-HEMT.

12. The power converter circuit of claim **10**, further comprising a reference signal source implemented as a maximum power point tracker, the reference signal source having an input coupled to the at least one DC/AC converter circuit and an output coupled to the second reference signal terminal.

13. The power converter circuit of claim **10**, wherein the DC/DC converter is a boost converter.

14. The power converter circuit of claim **10**, wherein the DC/DC converter is a buck converter.

15. The power converter circuit of claim **1**, wherein the at least one series circuit comprises:

at least two series circuits connected in parallel, each series circuit with at least two DC/AC converter circuit s connected between the output terminals,

wherein the DC/AC converter circuit s of the at least two series circuits are coupled to the voltage divider circuit.

16. The power converter circuit of claim **6**, wherein the control circuit comprises:

a phase-locked loop having an input coupled to the at least one measurement signal;

a VCO having a control input coupled to an output of the phase-locked loop;

a subtractor having a first input coupled to an output of the phase-locked loop and an input coupled to a current measurement signal proportional to the AC output current; and

a filter coupled to an output of the subtractor.

17. A power supply system, comprising:

output terminals configured to receive an external AC voltage;

at least one series circuit with at least two DC/AC converter circuit s, each DC/AC converter circuit comprising input terminals configured to be coupled to a DC power source and output terminals for providing an AC output current, the at least one series circuit connected between the output terminals of the power supply system;

at least two DC voltage sources, each DC voltage source coupled to the input terminals of one DC/AC converter circuit; converter unit; and

a voltage divider circuit connected between the output terminals of the power supply system and configured to provide at least one measurement signal including an information on a phase and frequency of the external AC voltage;

wherein at least one of the DC/AC converter circuit s is configured to receive the at least one measurement signal, and is configured to regulate a generation of the AC output current dependent on the least one measurement signal such that a phase difference between the AC output current and the external AC voltage assumes a set value.

18. The power supply system of claim **17**, wherein each DC voltage source comprises a photovoltaic array with at least one solar cell.

19. The power supply system of claim **17**, wherein each DC voltage source comprises a fuel cell.

20. The power supply system of claim **17** wherein the set value is zero.

21. The power supply system of claim **17**, wherein the at least one DC/AC converter circuit comprises:

a DC/AC converter coupled between the input and the output terminals of the DC/AC converter circuit and configured to generate the AC output current with a frequency and phase that is dependent on a first reference signal; and

a control circuit configured to generate the first reference signal dependent on the at least one measurement signal and the AC output current of the DC/AC converter circuit.

22. The power supply system of claim **21**, wherein the control circuit comprises:

a phase-locked loop having an input coupled to the at least one measurement signal;

a VCO having a control input coupled to an output of the phase-locked loop;

a subtractor having a first input coupled to an output of the phase-locked loop and an input coupled to a current measurement signal proportional to the AC output current; and

a filter coupled to an output of the subtractor.

23. A DC/AC converter circuit, comprising:

input terminals configured to be coupled to a DC power source;

output terminals for providing an AC output current; and

a measurement input terminals for receiving a measurement signal comprising a frequency and a phase;

a DC/AC converter coupled between the input terminals and the output terminals and configured to generate the AC output current with a frequency and phase that is dependent on a first reference signal;

a control circuit configured to generate the first reference signal dependent on the measurement signal and the AC output current of the DC/AC converter circuit, wherein the control circuit comprises

a phase-locked loop having an input coupled to measurement signal,

a VCO having a control input coupled to an output of the phase-locked loop,

a subtractor having a first input coupled to an output of the phase-locked loop and an input coupled to a current measurement signal proportional to the AC output current, and

a filter coupled to an output of the subtractor, wherein the DC/AC converter circuit is configured to regulate a phase difference between a phase of the AC output current and the phase of the measurement signal to a first set value.

24. The DC/AC converter circuit of claim **23**, wherein the first set value is zero.

25. A method for operating a power converter circuit, the power converter circuit comprising:

output terminals configured to receive an external voltage, and

at least one series circuit with at least two DC/AC converter circuit s each comprising input terminals configured to be coupled to a DC power source, the at least one series circuit connected between output terminals of the power converter circuit;

a voltage divider circuit connected between the output terminals of the power converter circuit, the method comprising:

providing an AC output current at the output terminals,

generating, by the voltage divider circuit, at least one measurement signal having a phase and frequency based on an external AC voltage, and

regulating a generation of the AC output current, regulating comprising using a control loop to regulate a phase difference between a phase of the AC output current and a phase of the at least one measurement signal to a set value.

26. The method of claim **25** wherein the set value is zero.

27. The method of claim **25**, wherein:

the at least one DC/AC converter circuit further comprises

a DC/AC converter coupled between the input terminals and the output terminals of the power converter circuit, and

a control circuit coupled to the DC/AC converter;

the method further comprises generating, by the control circuit, a first reference signal dependent on the at least one measurement signal and the AC output current; and

the providing the AC output current at the output terminals comprises generating, by the DC/AC converter, the AC output current with the frequency and phase that is dependent on the first reference signal.

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