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Wang et al.

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(54) **STRESS BUFFER STRUCTURES IN A MOUNTING STRUCTURE OF A SEMICONDUCTOR DEVICE**

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This patent is subject to a terminal disclaimer.

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H01L 23/31 (2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 23/3192*** (2013.01); ***H01L 21/76804*** (2013.01); ***H01L 21/76885*** (2013.01); ***H01L 23/293*** (2013.01); ***H01L 23/31*** (2013.01); ***H01L 23/3171*** (2013.01); ***H01L 24/03*** (2013.01); ***H01L 24/05*** (2013.01); ***H01L 24/13*** (2013.01); *H01L 24/11* (2013.01); *H01L 2224/0215* (2013.01); *H01L 2224/02125* (2013.01); *H01L 2224/0345* (2013.01); *H01L 2224/0346* (2013.01); *H01L 2224/03452* (2013.01);

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CPC H01L 21/76804; H01L 21/76885; H01L 23/293; H01L 23/31; H01L 23/3171; H01L 23/3192; H01L 24/03; H01L 24/05; H01L 24/13; H01L 2224/02125; H01L 2224/0215; H01L 2224/0345; H01L 2224/03452; H01L 2224/0346; H01L 2224/0401; H01L 2224/05

USPC 257/737–738, 774, 779–780

See application file for complete search history.

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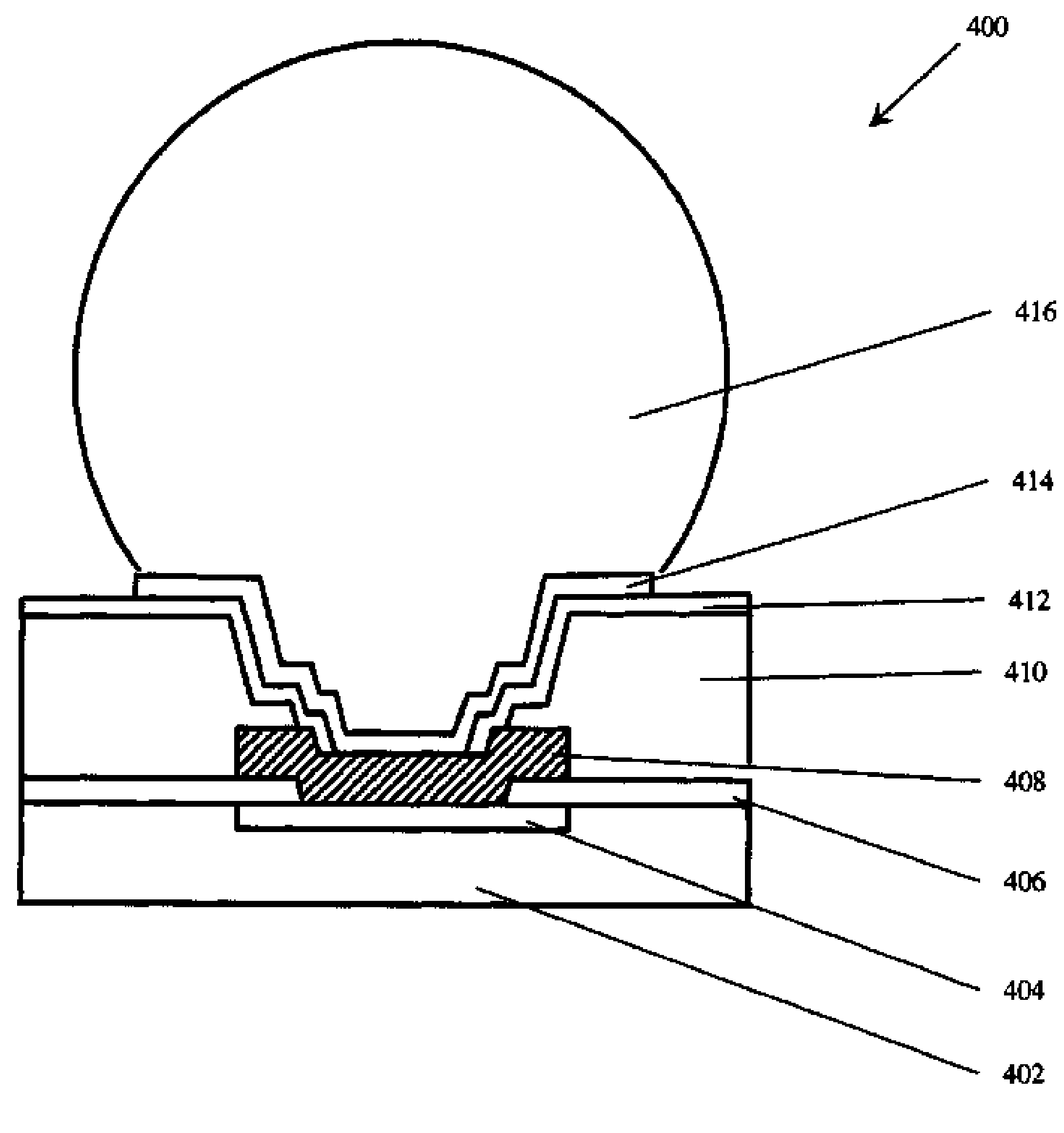
(74) *Attorney, Agent, or Firm* — Hauptman Ham, LLP

(57) **ABSTRACT**

A semiconductor device includes a bonding pad on a substrate. The semiconductor device further includes a passivation layer covering a peripheral portion of the bonding pad while exposing a middle portion of the bonding pad. Additionally, the semiconductor device includes a stress buffer layer over the passivation layer where the stress buffer layer exposes a portion of the bonding pad, and where a wall of the stress buffer layer extends, in steps, upwardly from the exposed portion of the bonding pad. Furthermore, the semiconductor device includes an under-bump metallurgy (UBM) layer over the stress buffer layer, where the UBM layer contacts a portion of the bonding pad.

12 Claims, 14 Drawing Sheets



(51) **Int. Cl.**

H01L 21/768	(2006.01)
H01L 23/29	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC *H01L2224/0401* (2013.01); *H01L 2224/05022* (2013.01); *H01L 2224/05124* (2013.01); *H01L 2224/05147* (2013.01); *H01L 2224/05558* (2013.01); *H01L 2224/05572* (2013.01); *H01L 2224/05639* (2013.01); *H01L 2224/05644* (2013.01); *H01L 2224/05647* (2013.01); *H01L 2224/05655* (2013.01); *H01L 2224/05664* (2013.01); *H01L 2224/05666* (2013.01); *H01L 2224/05669* (2013.01); *H01L 2224/05671* (2013.01); *H01L 2224/05684* (2013.01); *H01L 2224/10156* (2013.01); *H01L 2224/131* (2013.01); *H01L 2224/81815* (2013.01); *H01L 2924/0002* (2013.01); *H01L 2924/00014* (2013.01); *H01L 2924/351* (2013.01)

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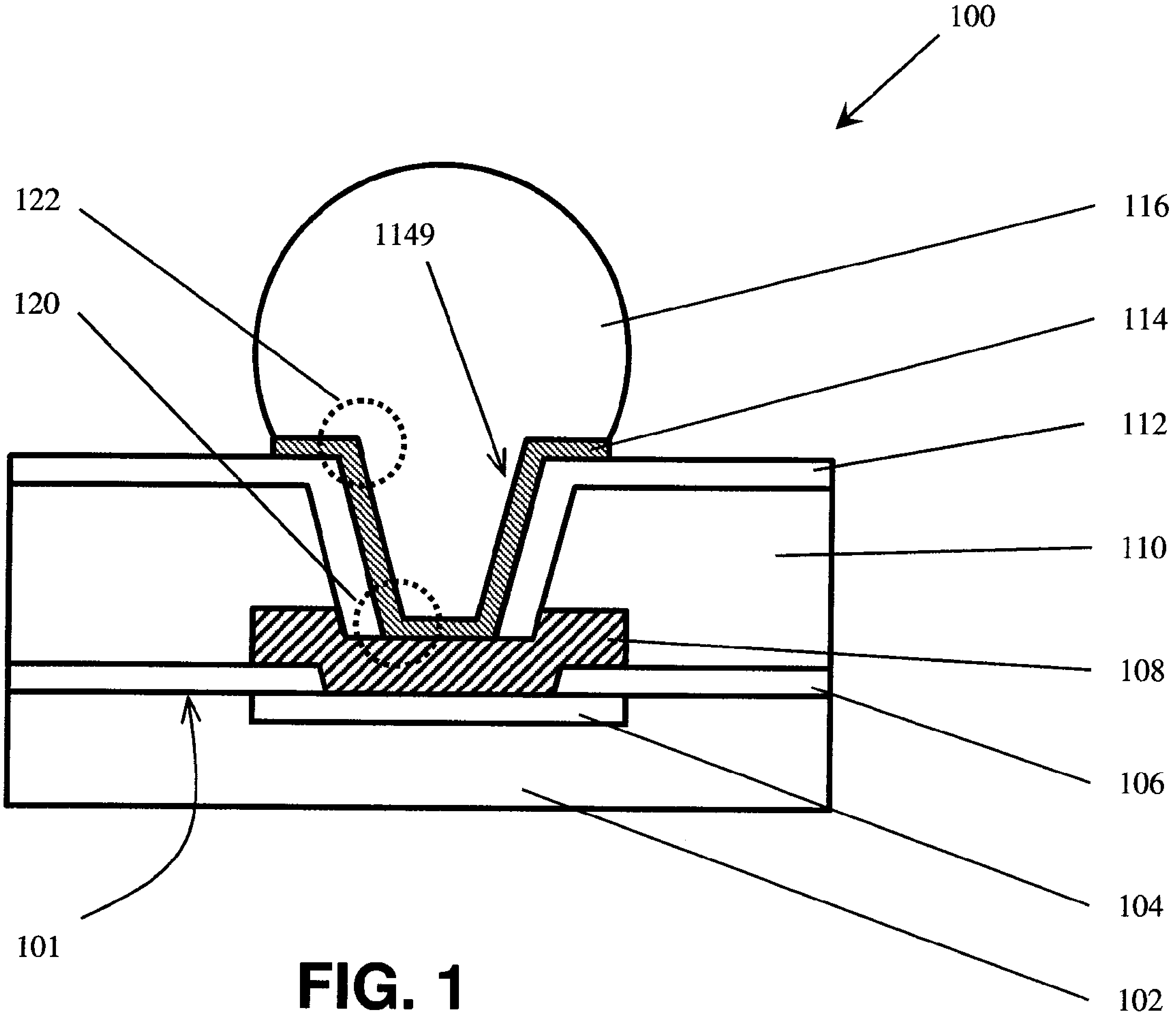

FIG. 1

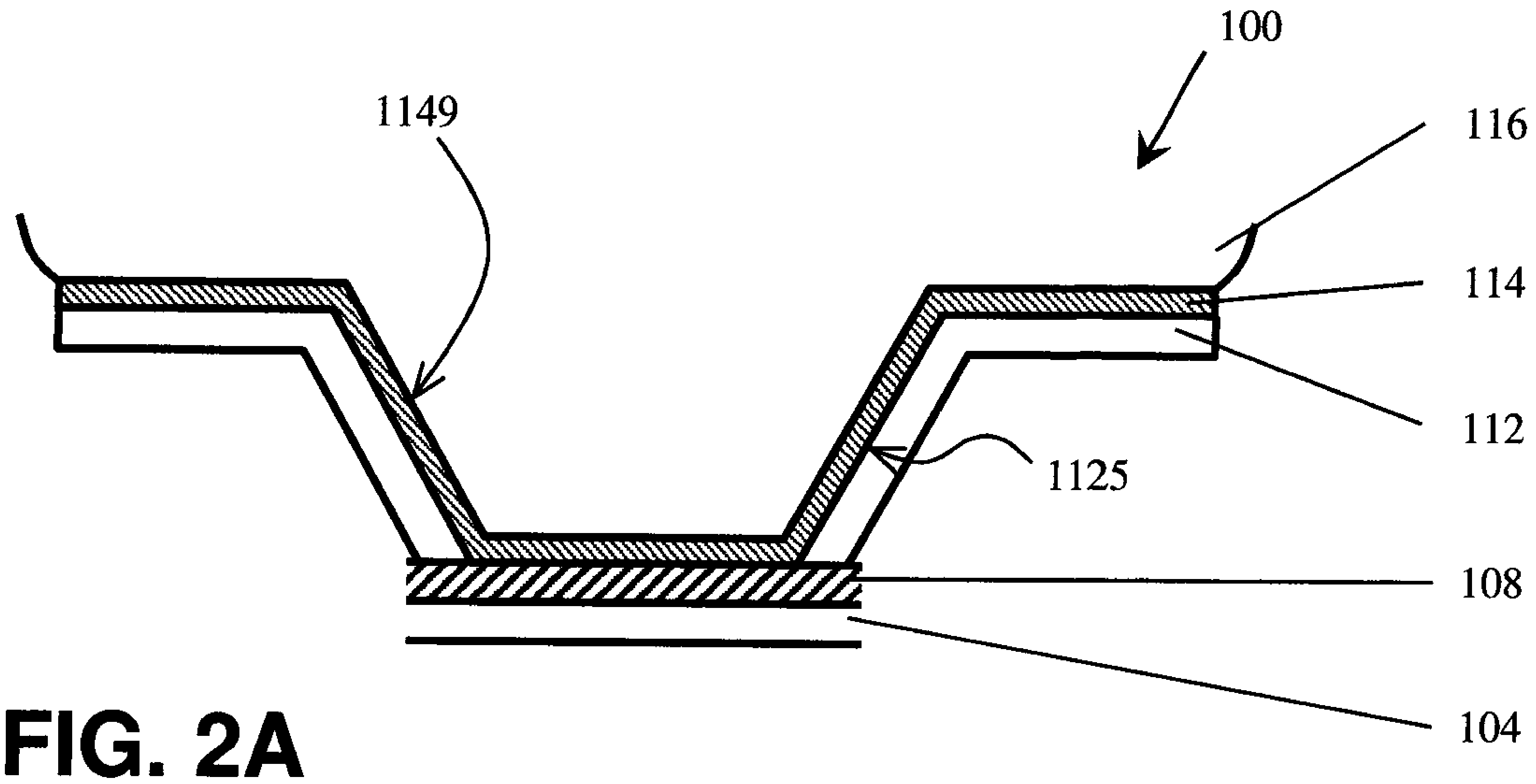

FIG. 2A

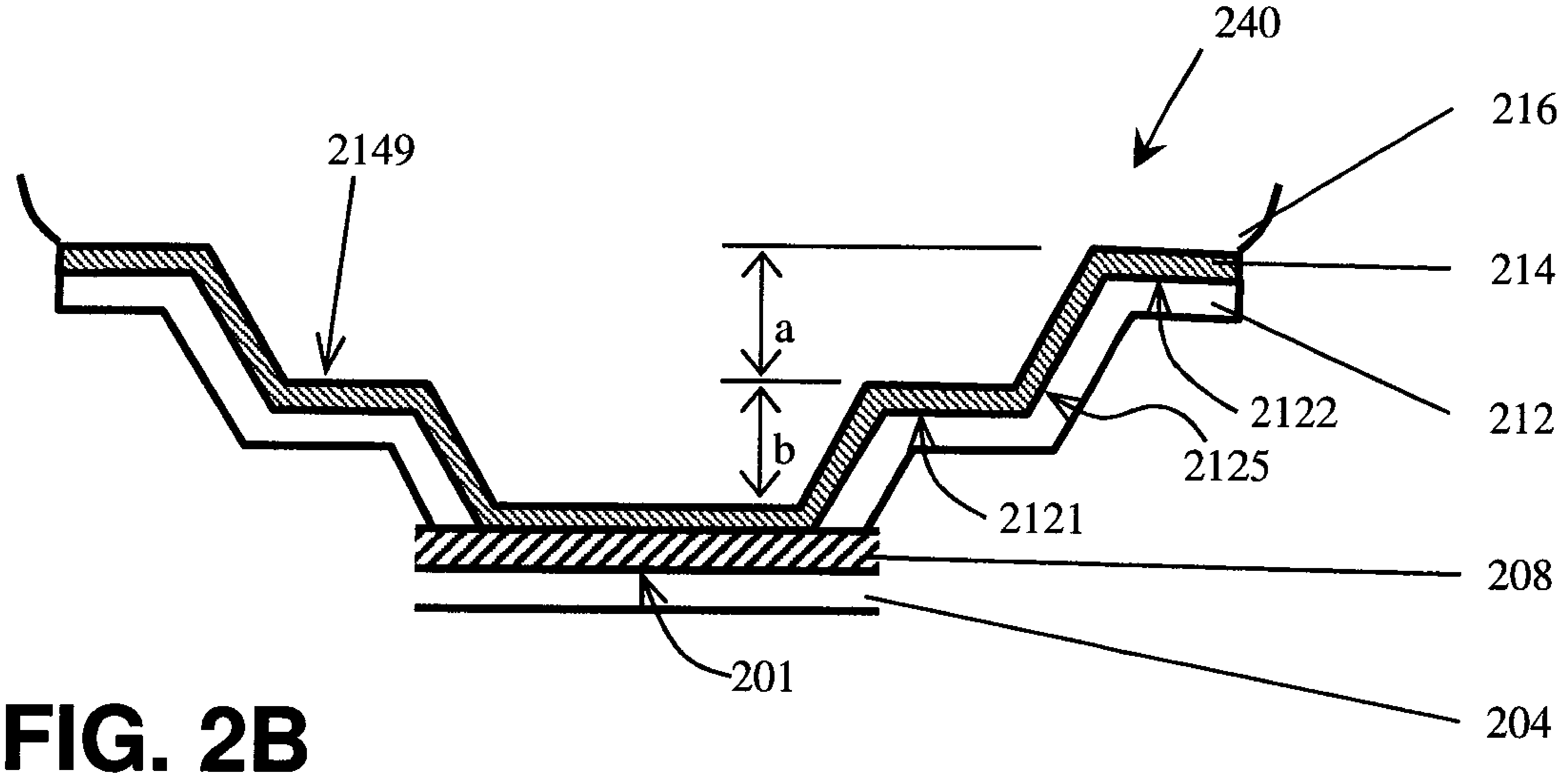

FIG. 2B

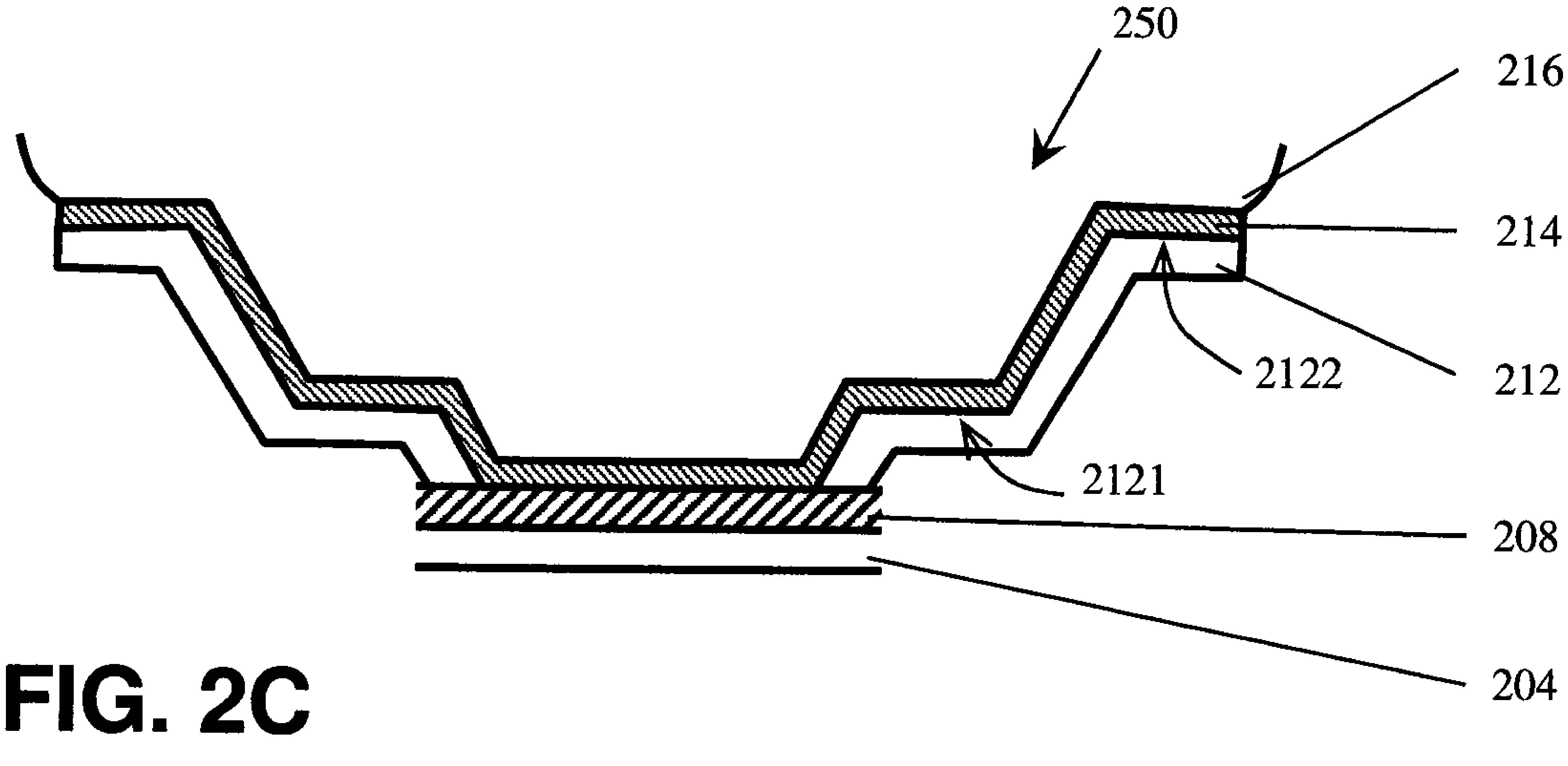

FIG. 2C

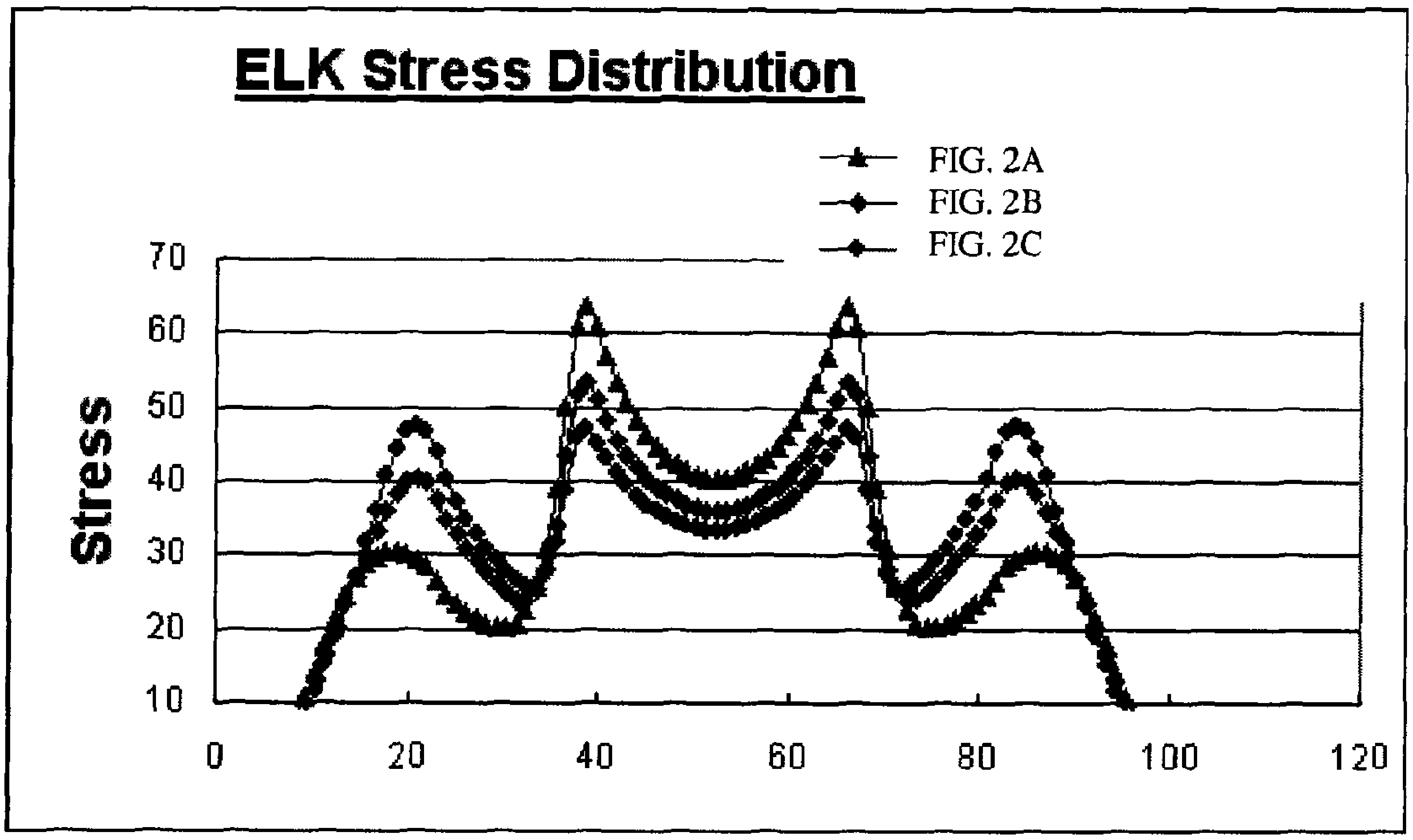
ELK Stress Distribution
FIG. 2A
FIG. 2B
FIG. 2C
Stress
70
60
50
40
30
20
10
0
20
40
60
80
100
120

FIG. 3A

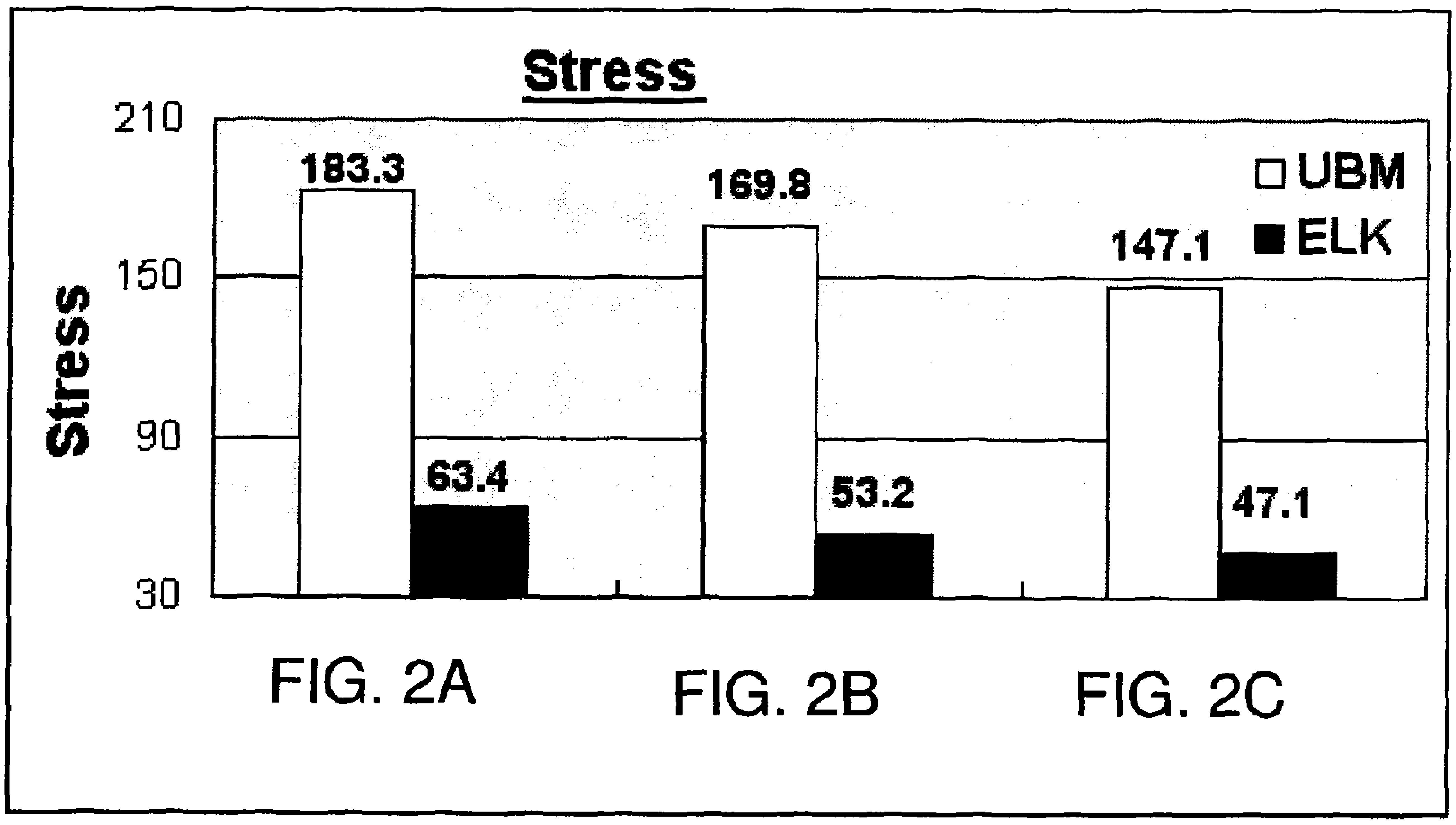
Stress
210
150
90
30
Stress
183.3
63.4
169.8
53.2
147.1
47.1
□ UBM
■ ELK
FIG. 2A
FIG. 2B
FIG. 2C

FIG. 3B

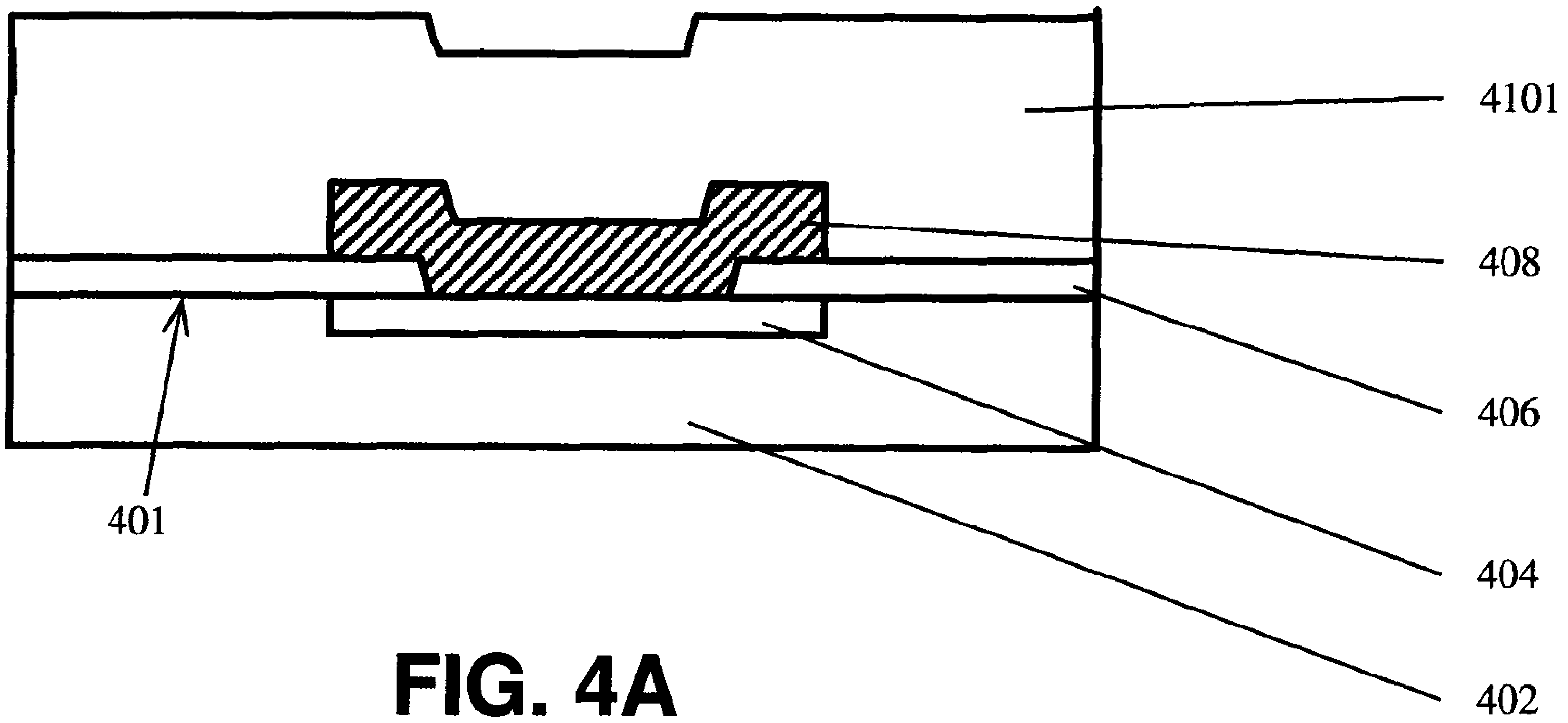

FIG. 4A

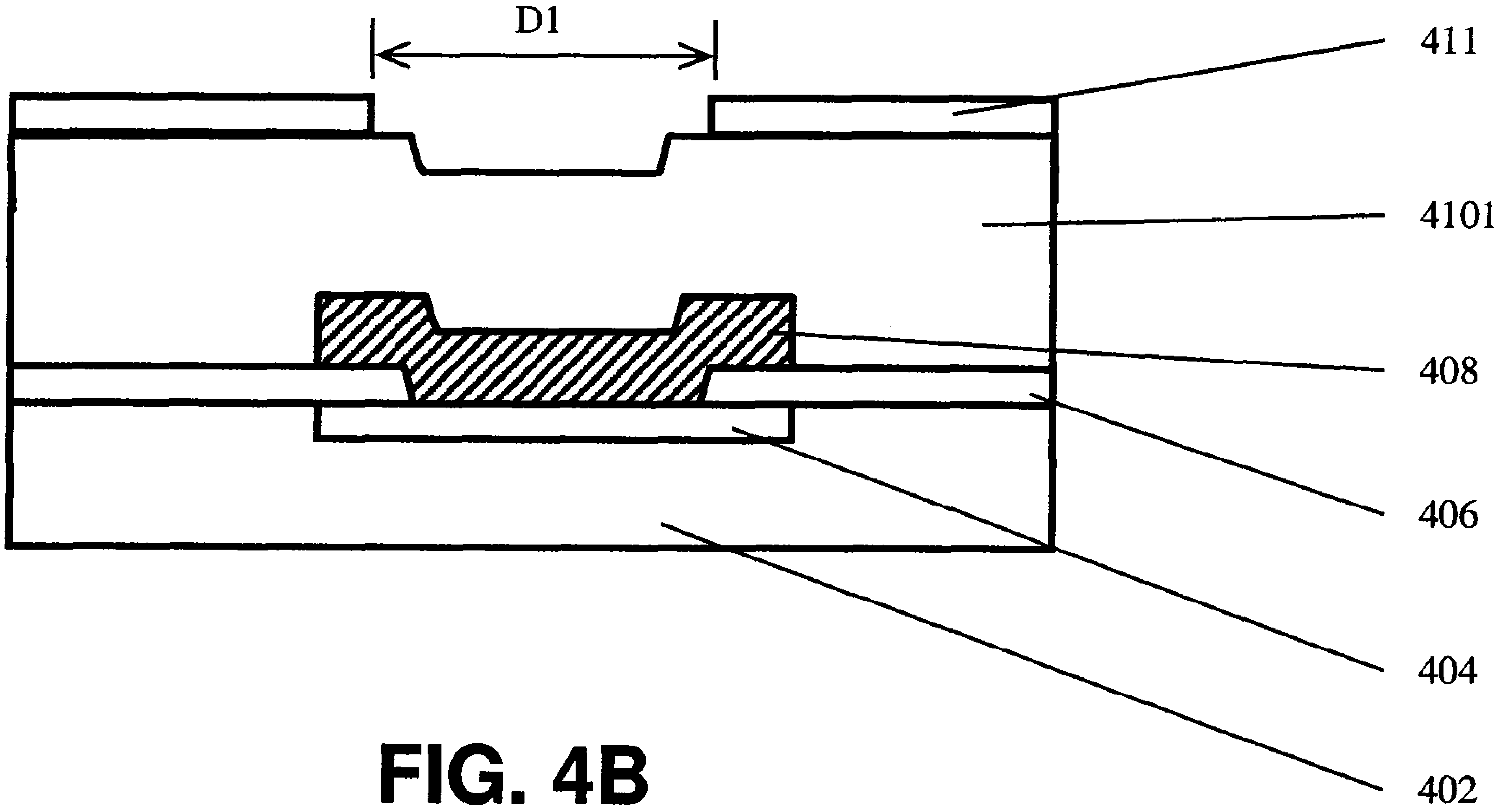

FIG. 4B

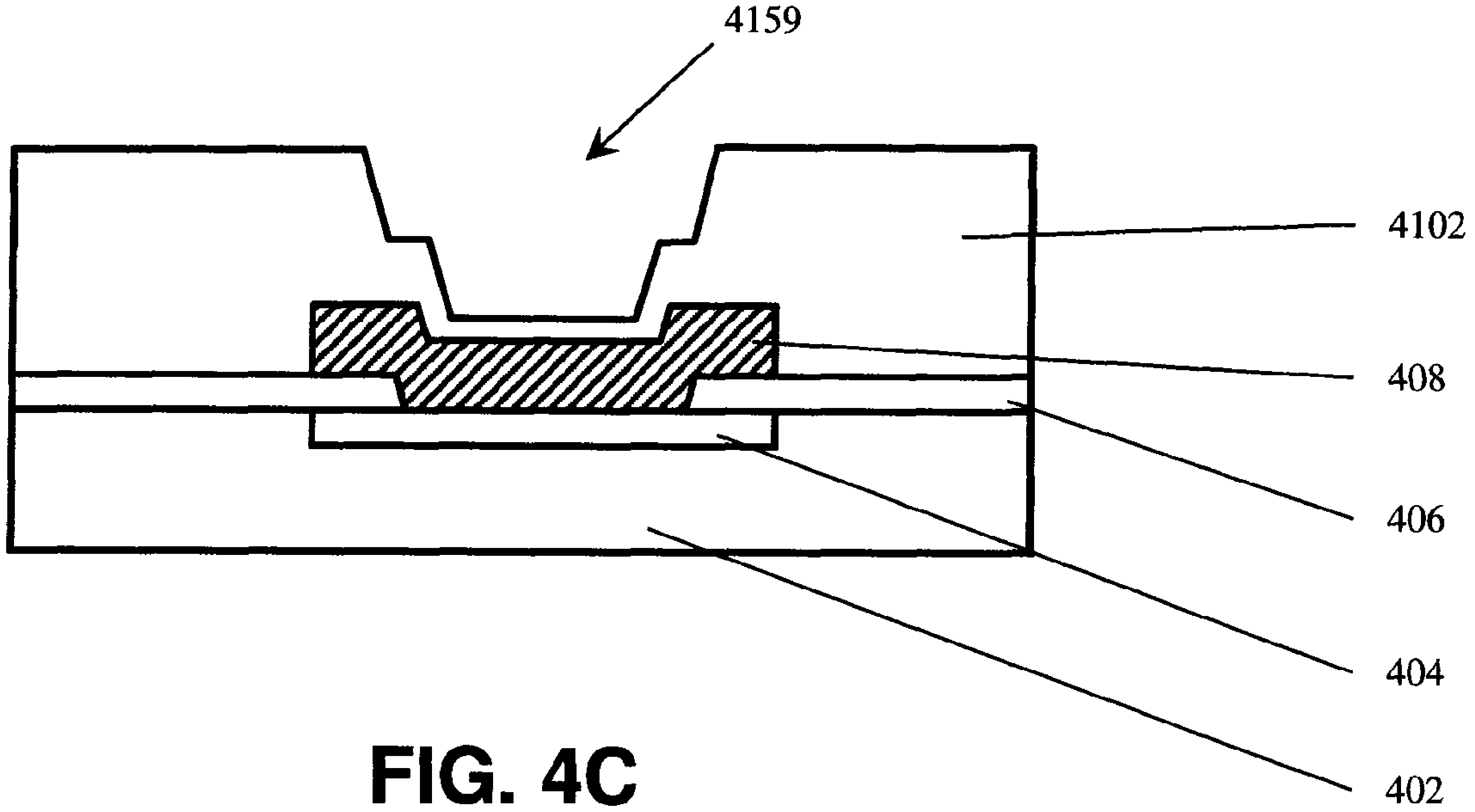

FIG. 4C

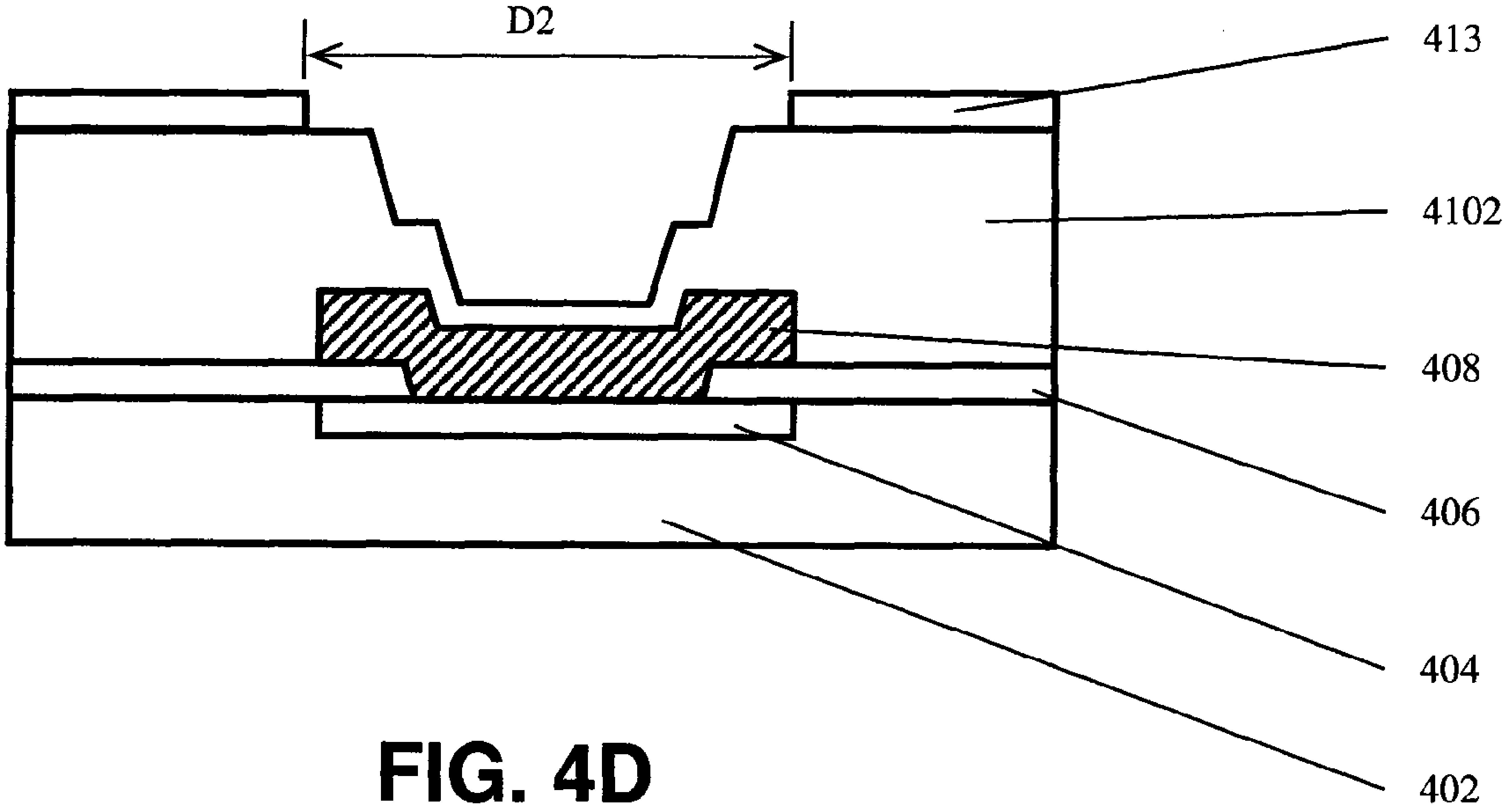

FIG. 4D

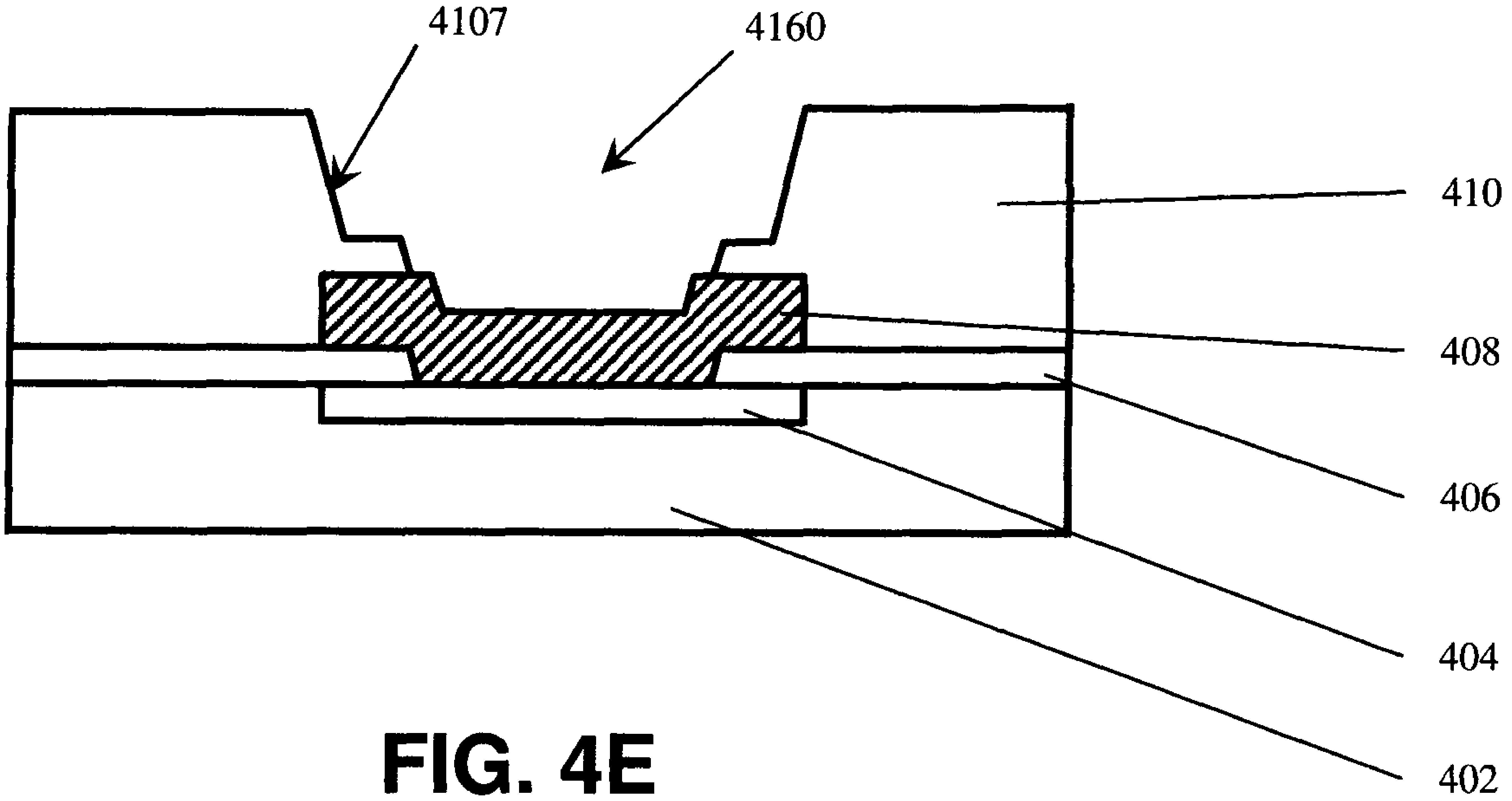
4107
4160
410
408
406
404
402

FIG. 4E

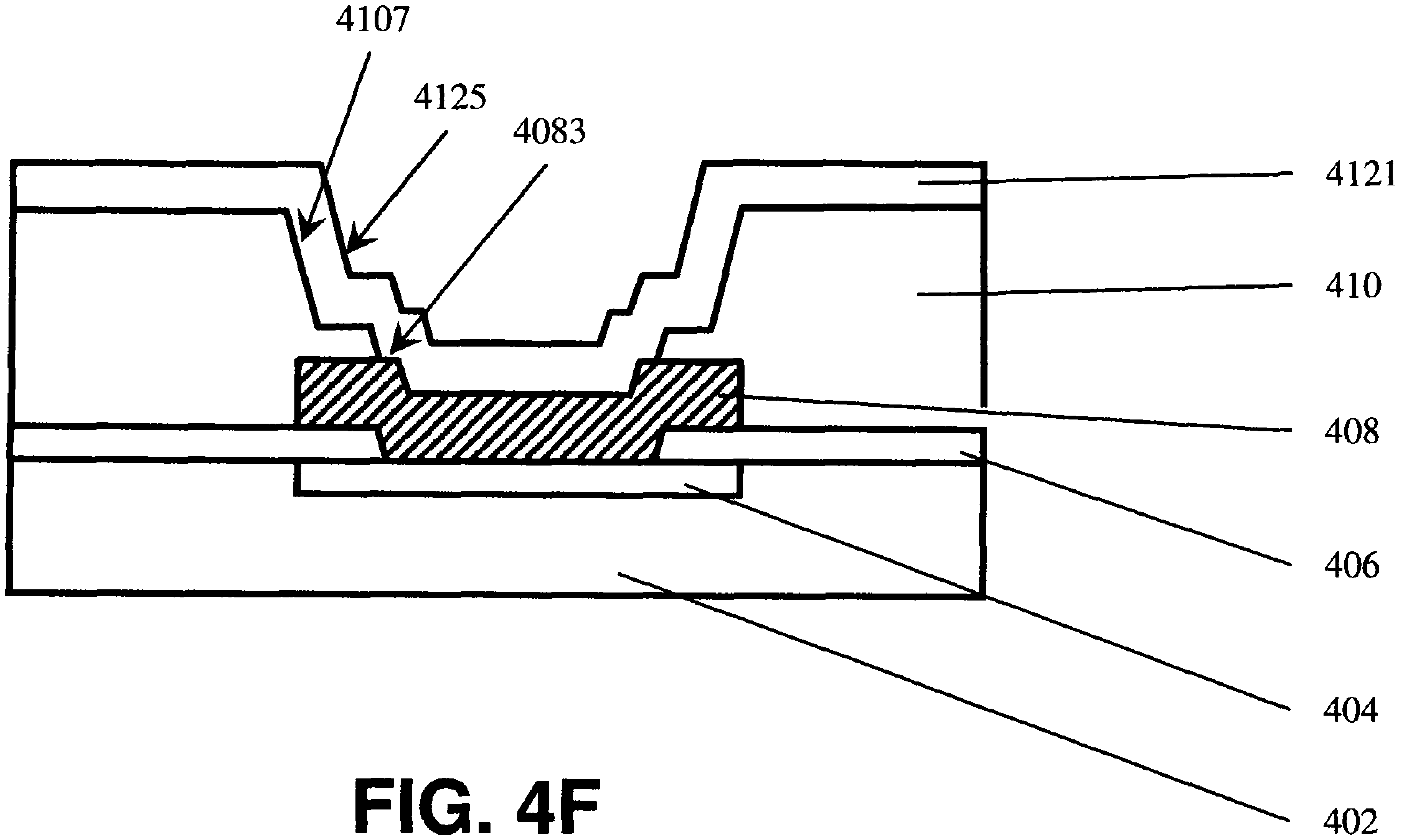
4107
4125
4083
4121
410
408
406
404
402

FIG. 4F

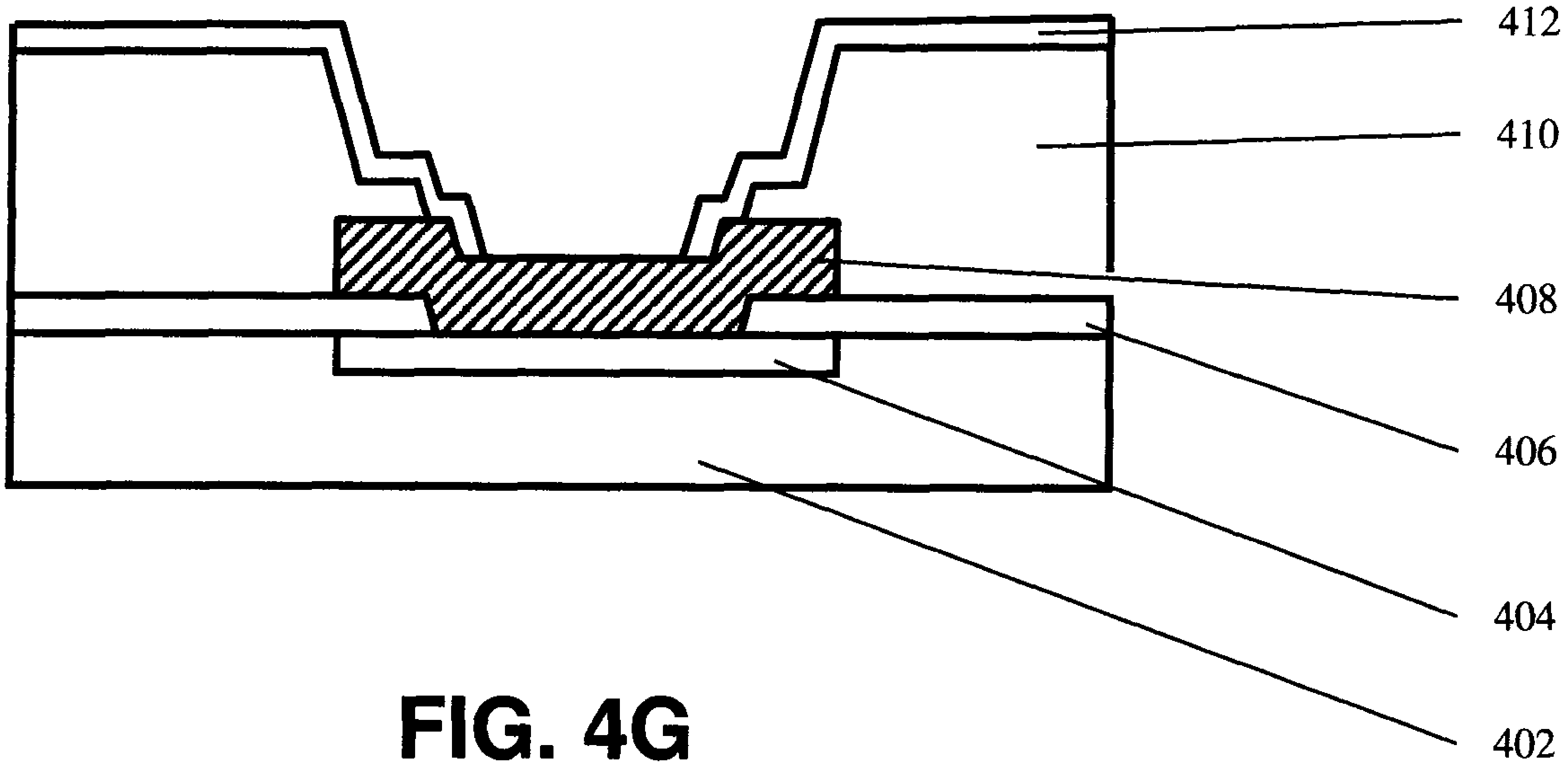

FIG. 4G

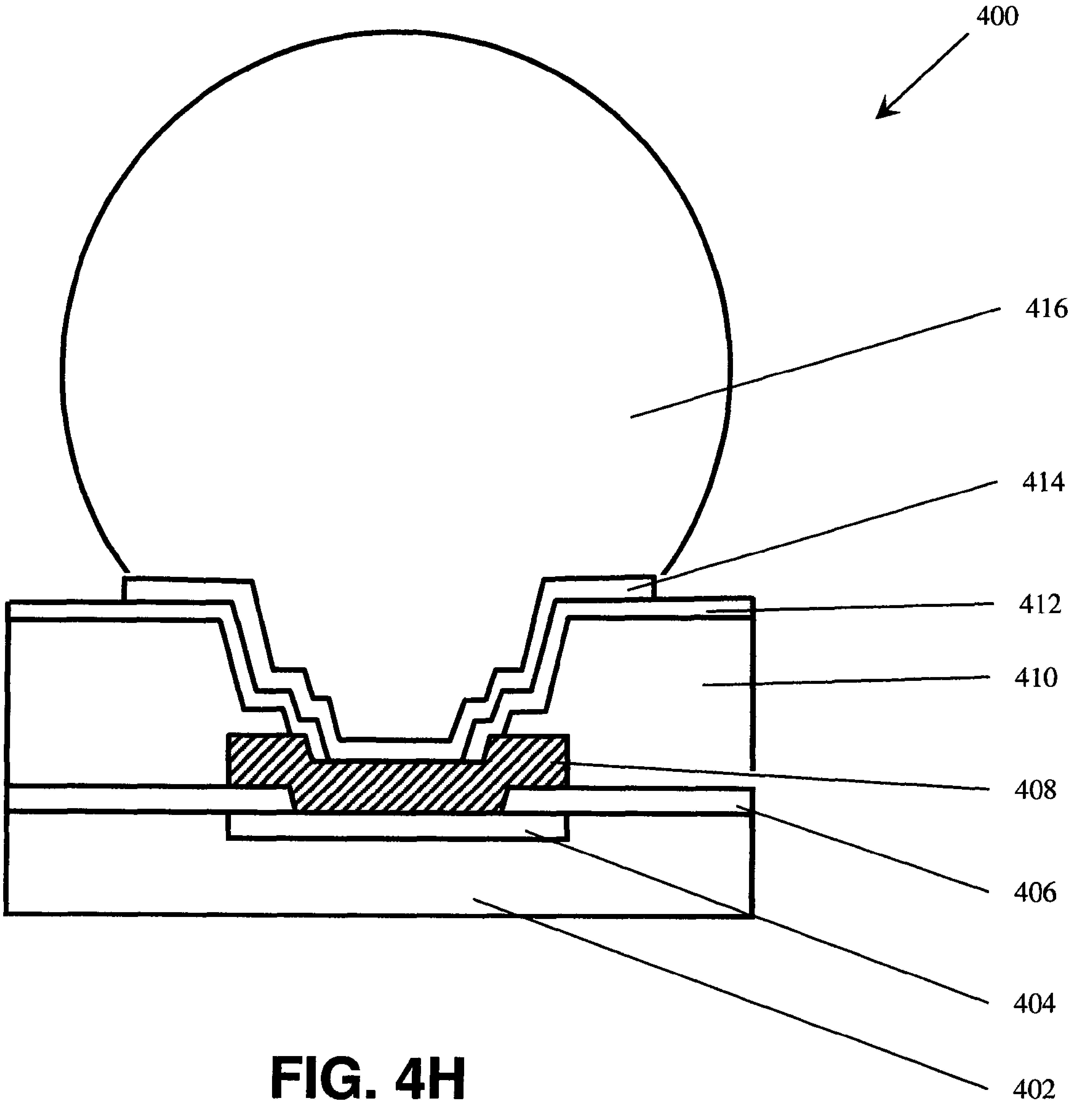

FIG. 4H

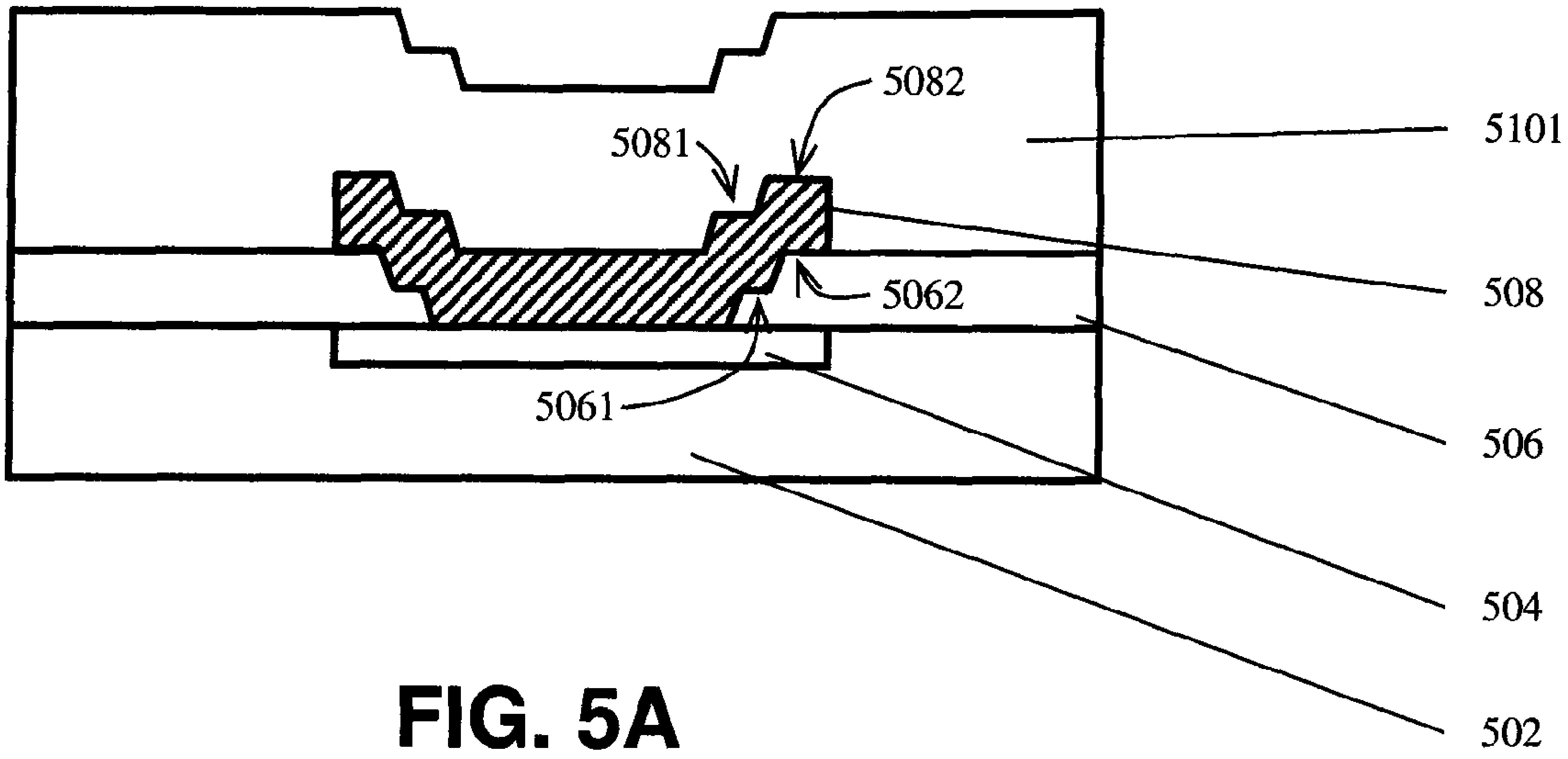
5082
5081
5101
508
5062
506
5061
504
502

FIG. 5A

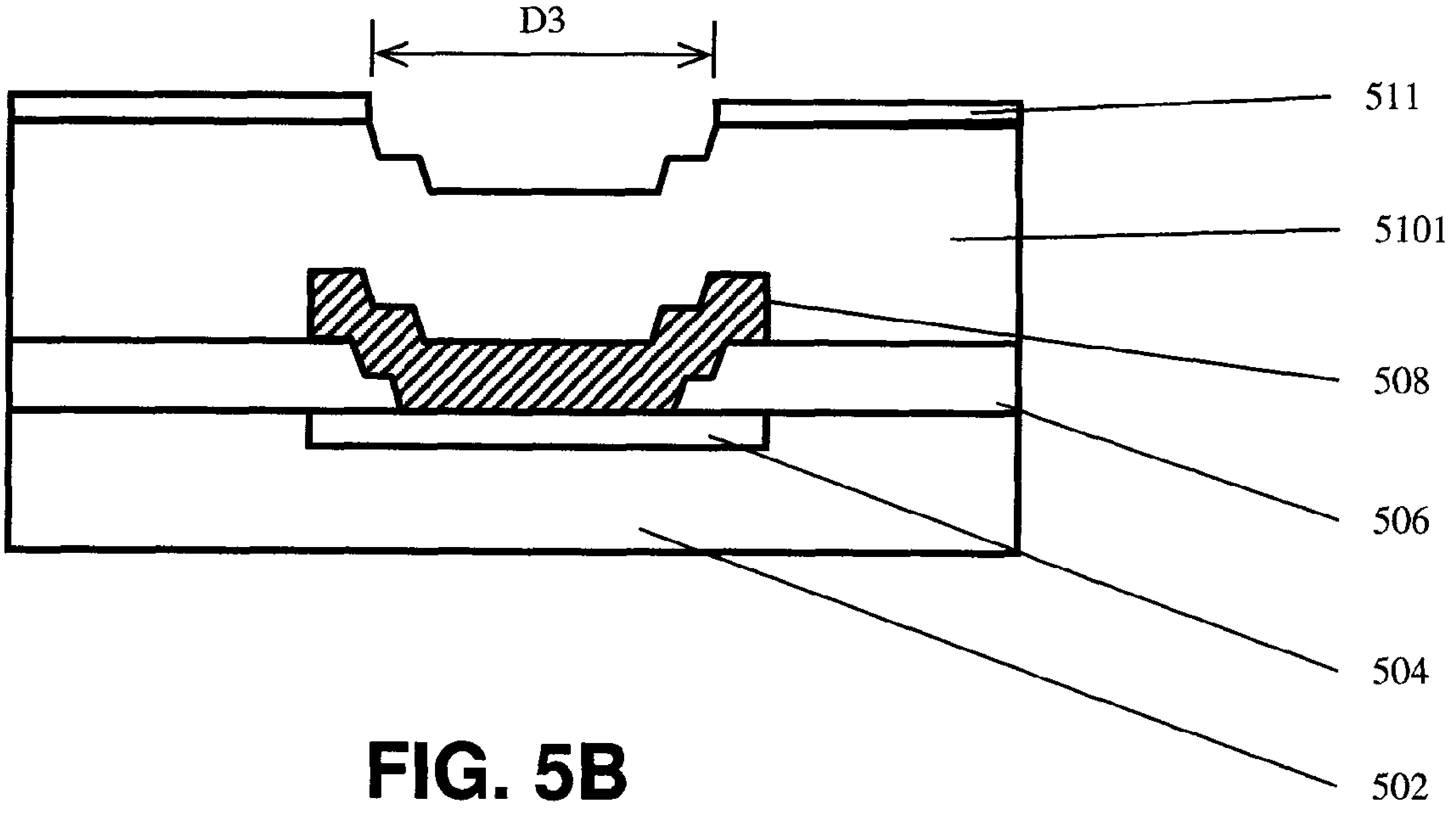
D3
511
5101
508
506
504
502

FIG. 5B

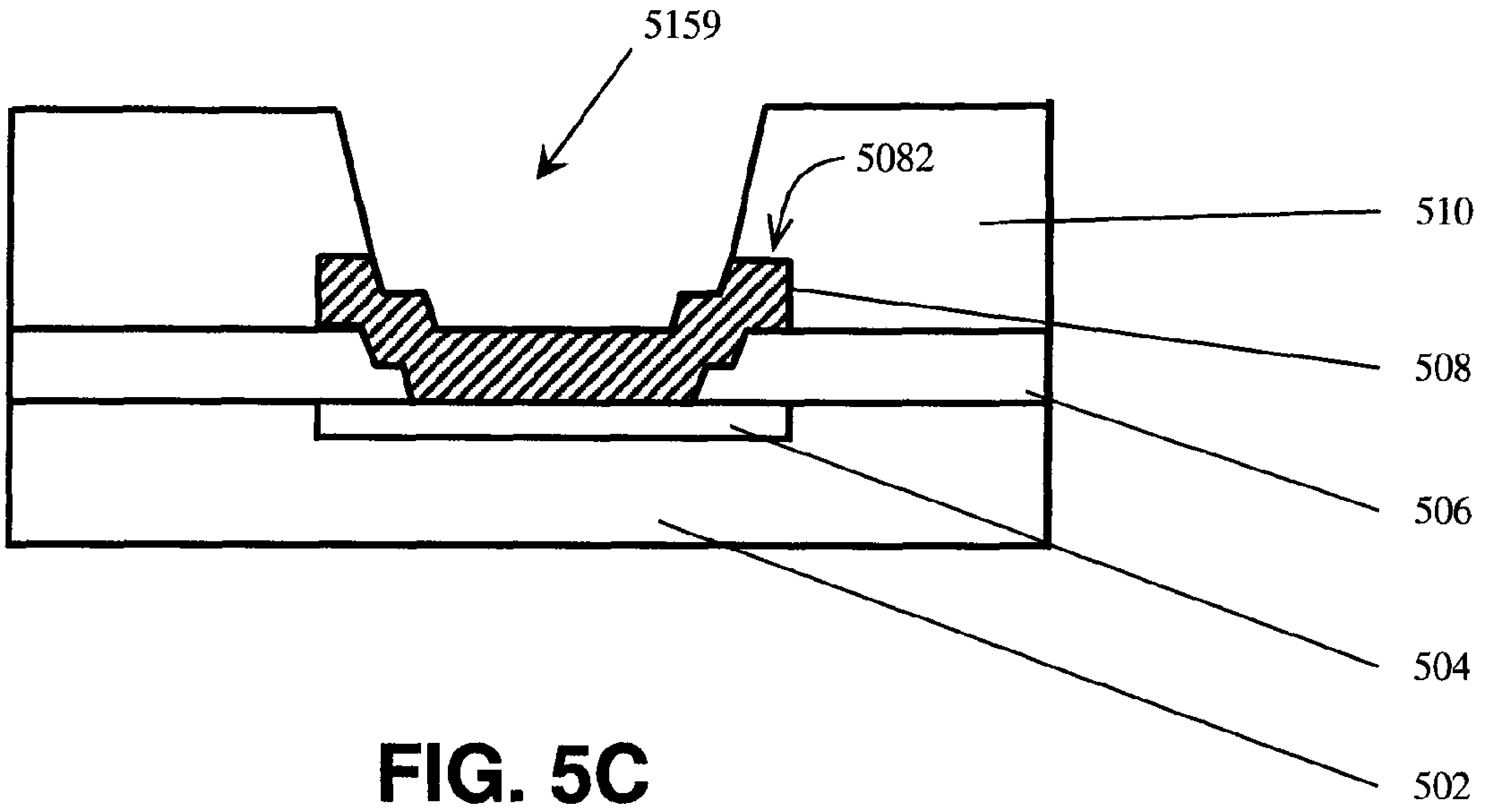
5159
5082
510
508
506
504
502

FIG. 5C

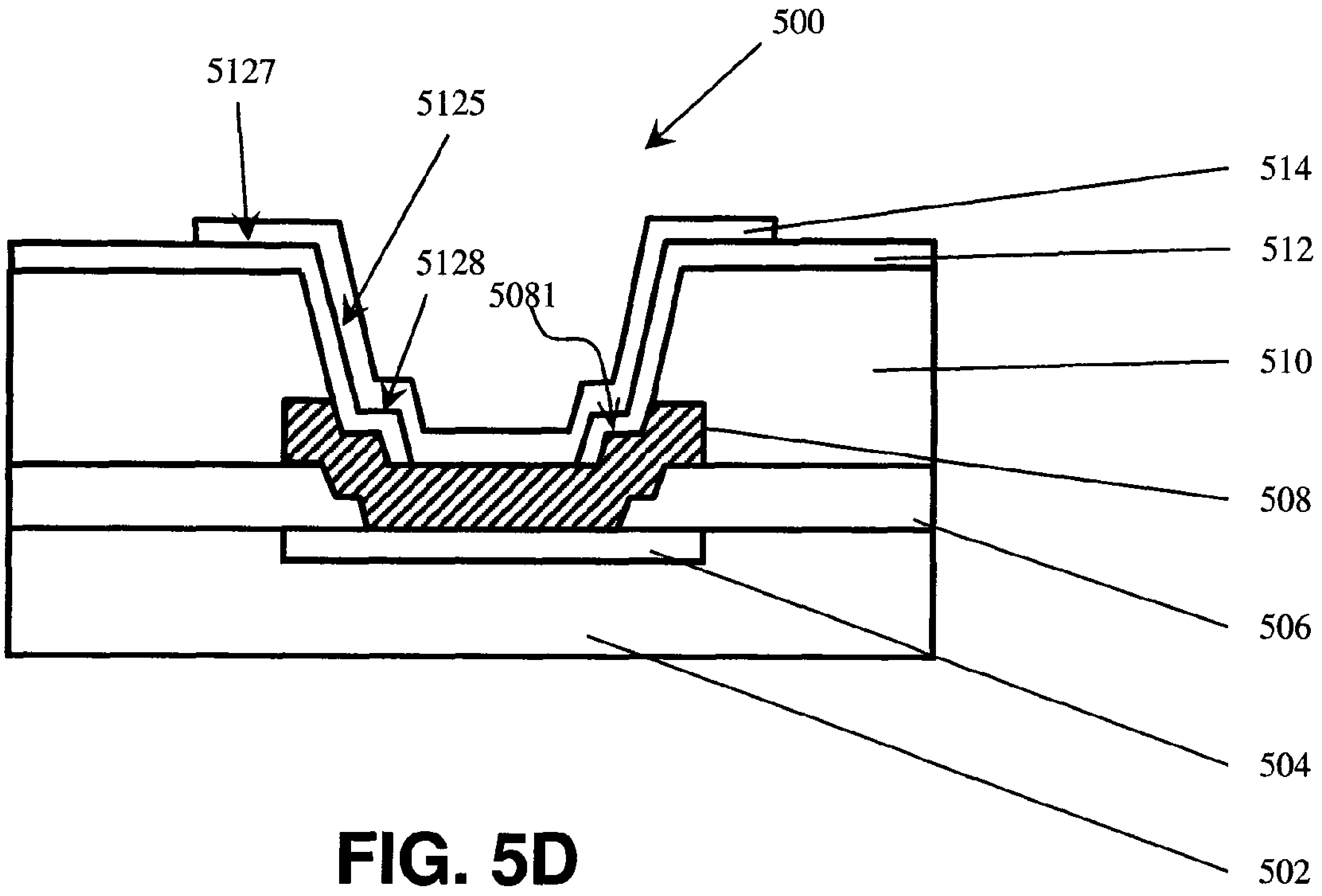
500
5127
5125
514
512
5128
5081
510
508
506
504
502

FIG. 5D

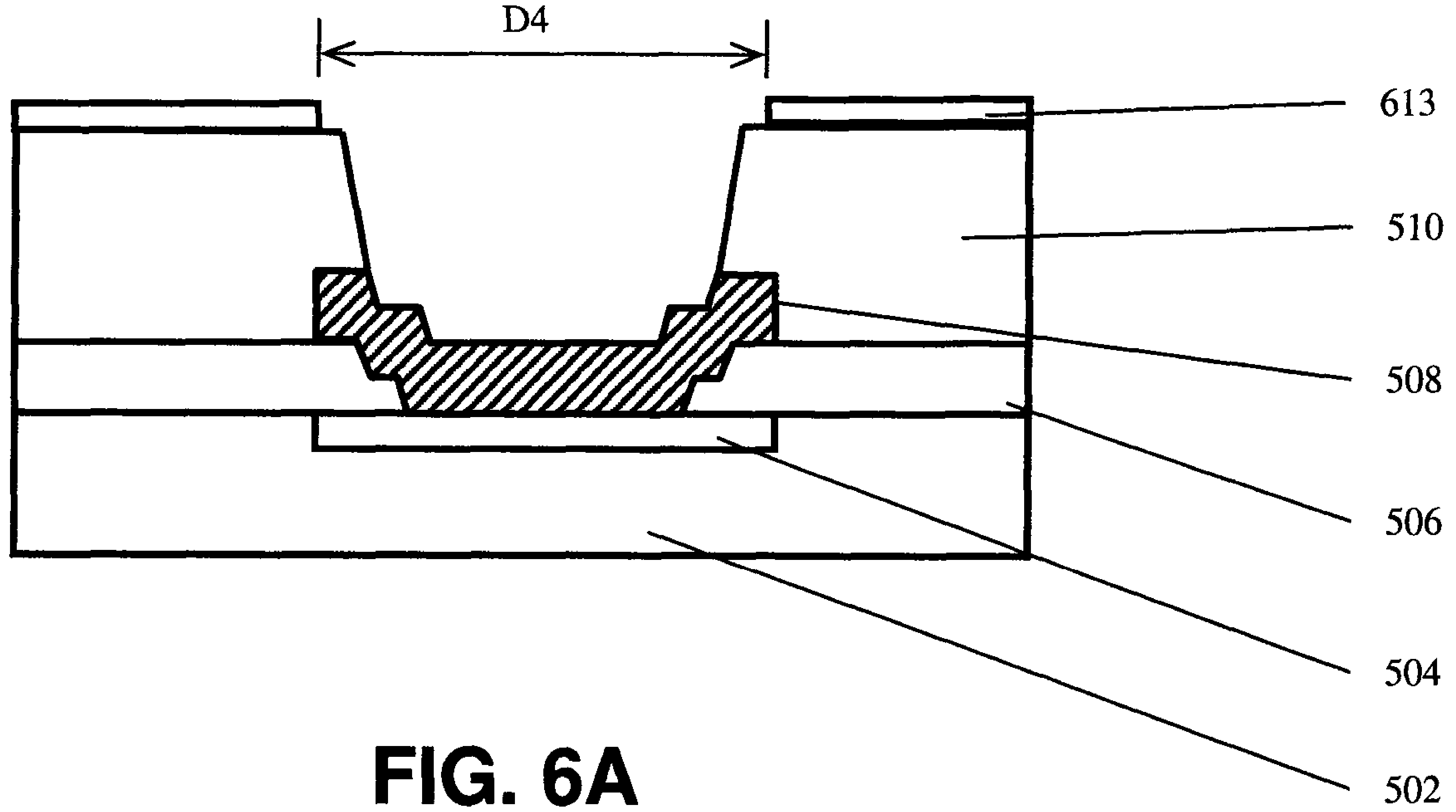
D4
613
510
508
506
504
502

FIG. 6A

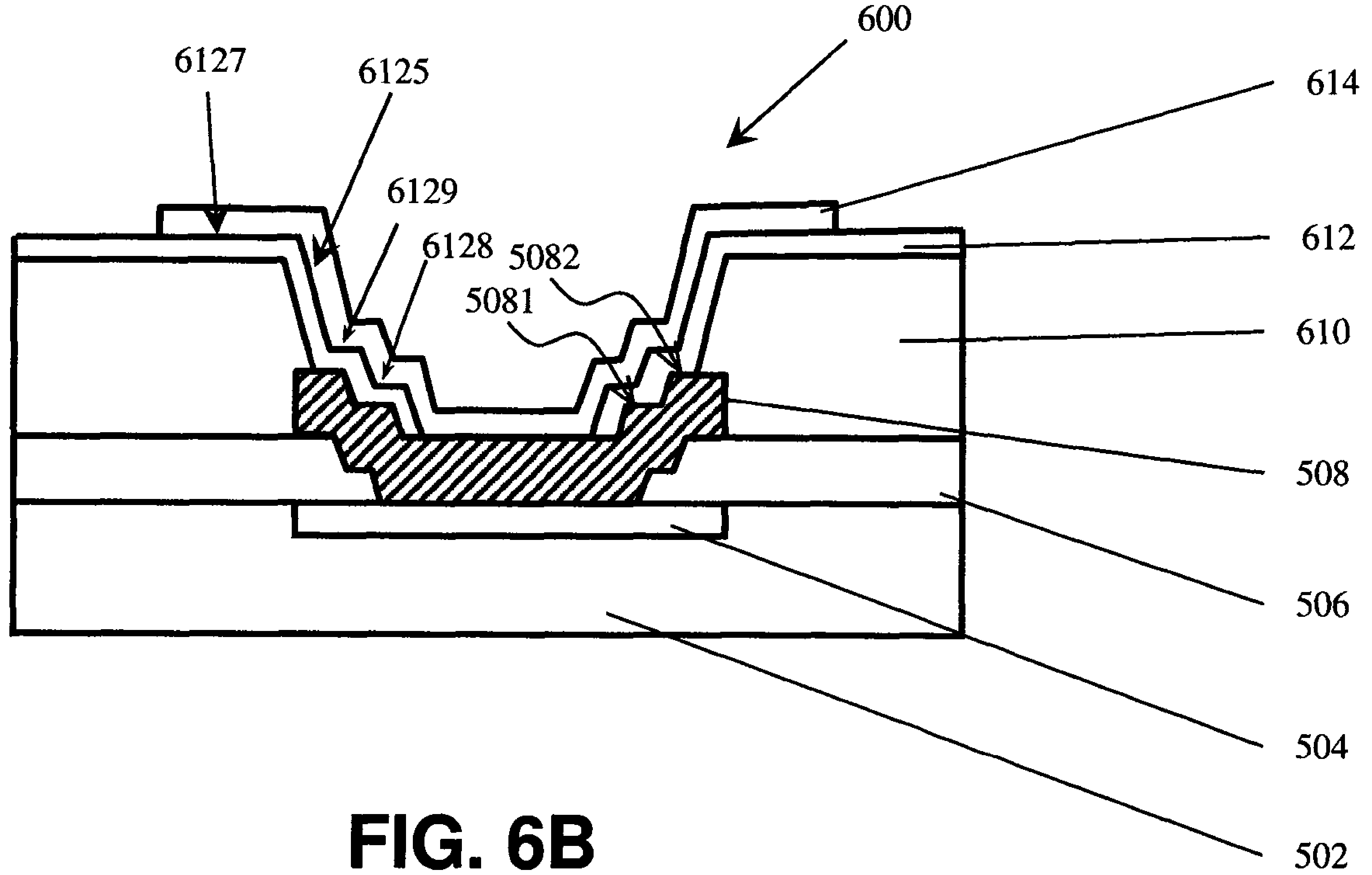
600
6127
6125
614
6129
6128
5082
5081
612
610
508
506
504
502

FIG. 6B

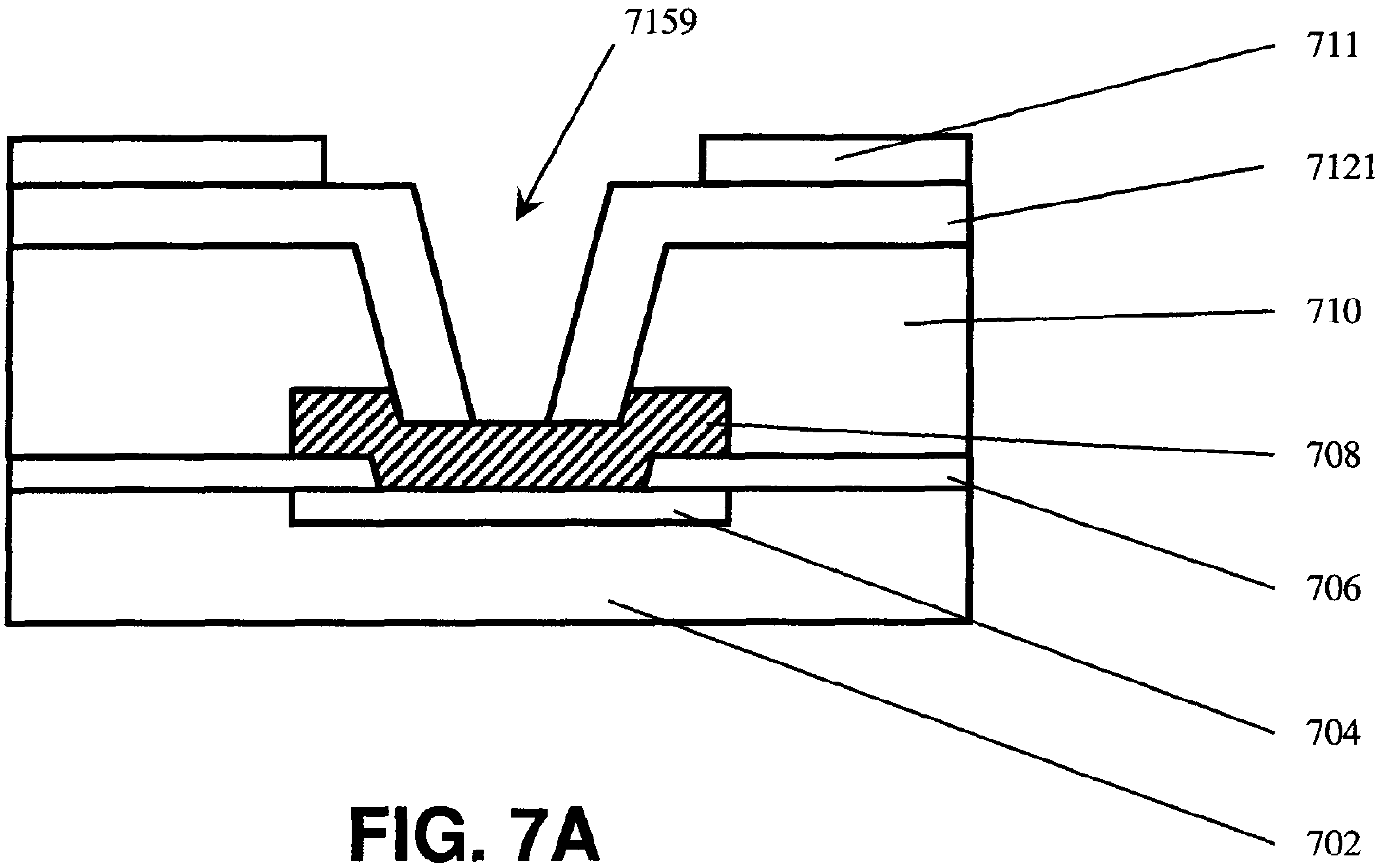
7159
711
7121
710
708
706
704
702

FIG. 7A

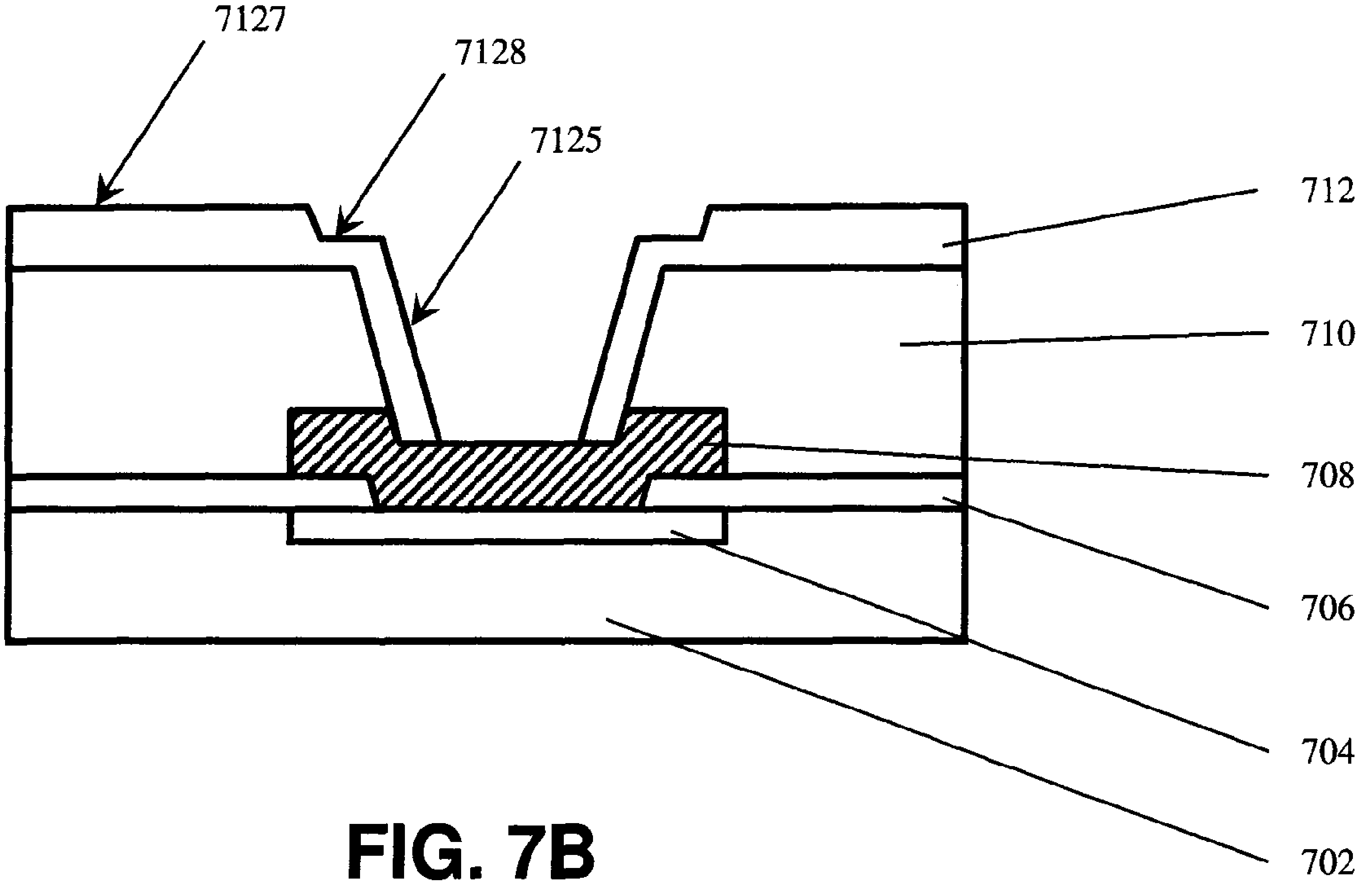
7127
7128
7125
712
710
708
706
704
702

FIG. 7B

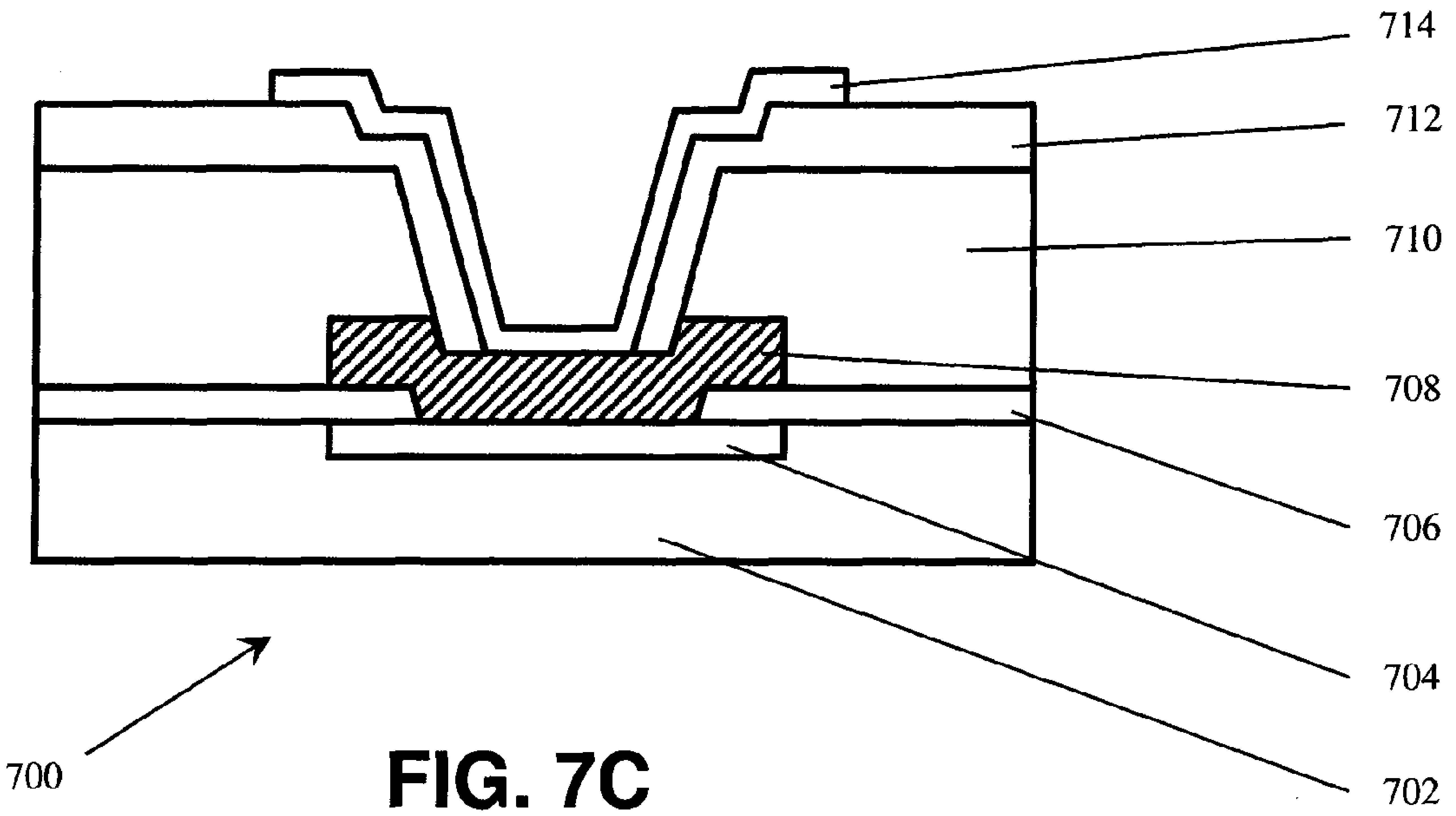

FIG. 7C

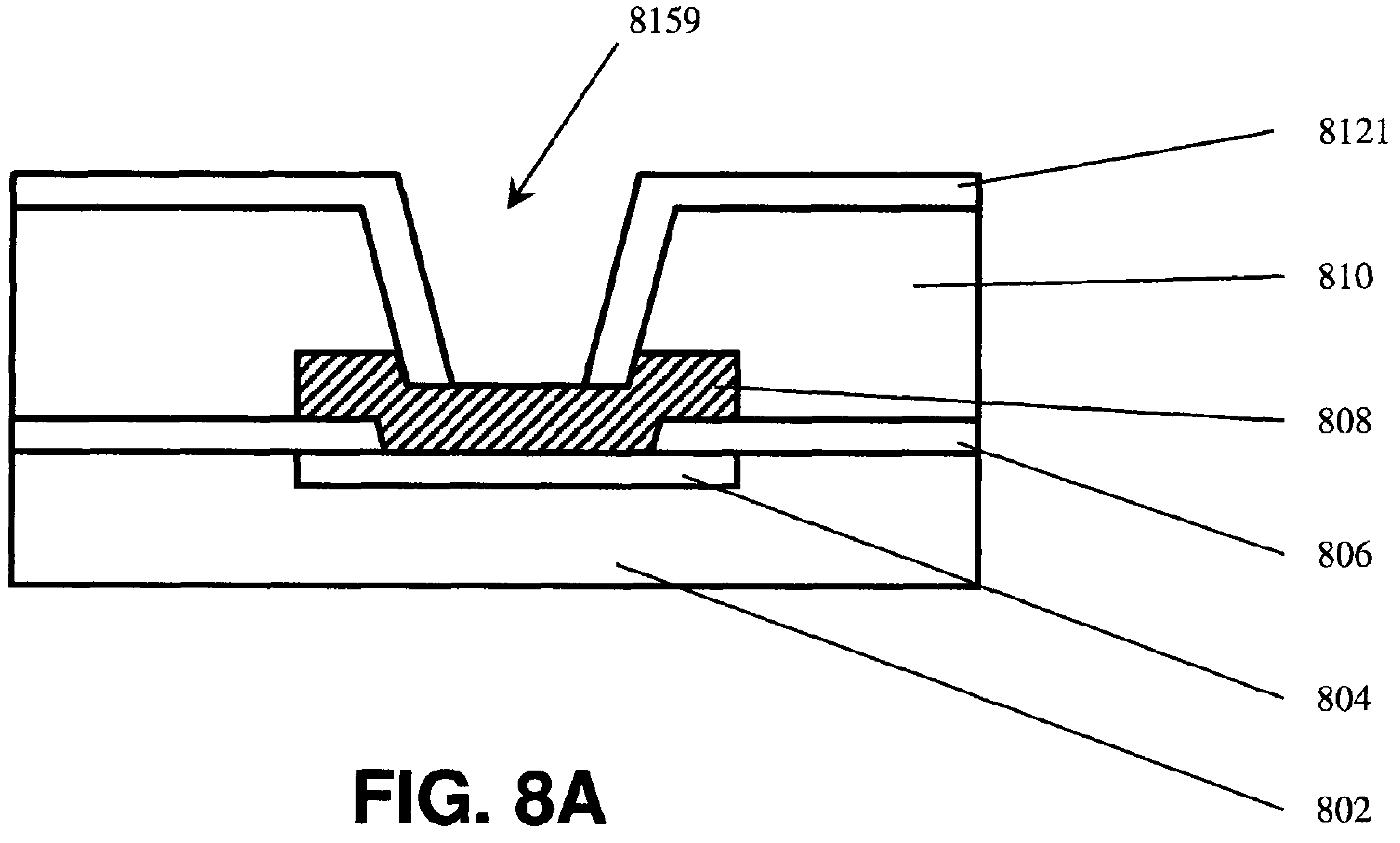

FIG. 8A

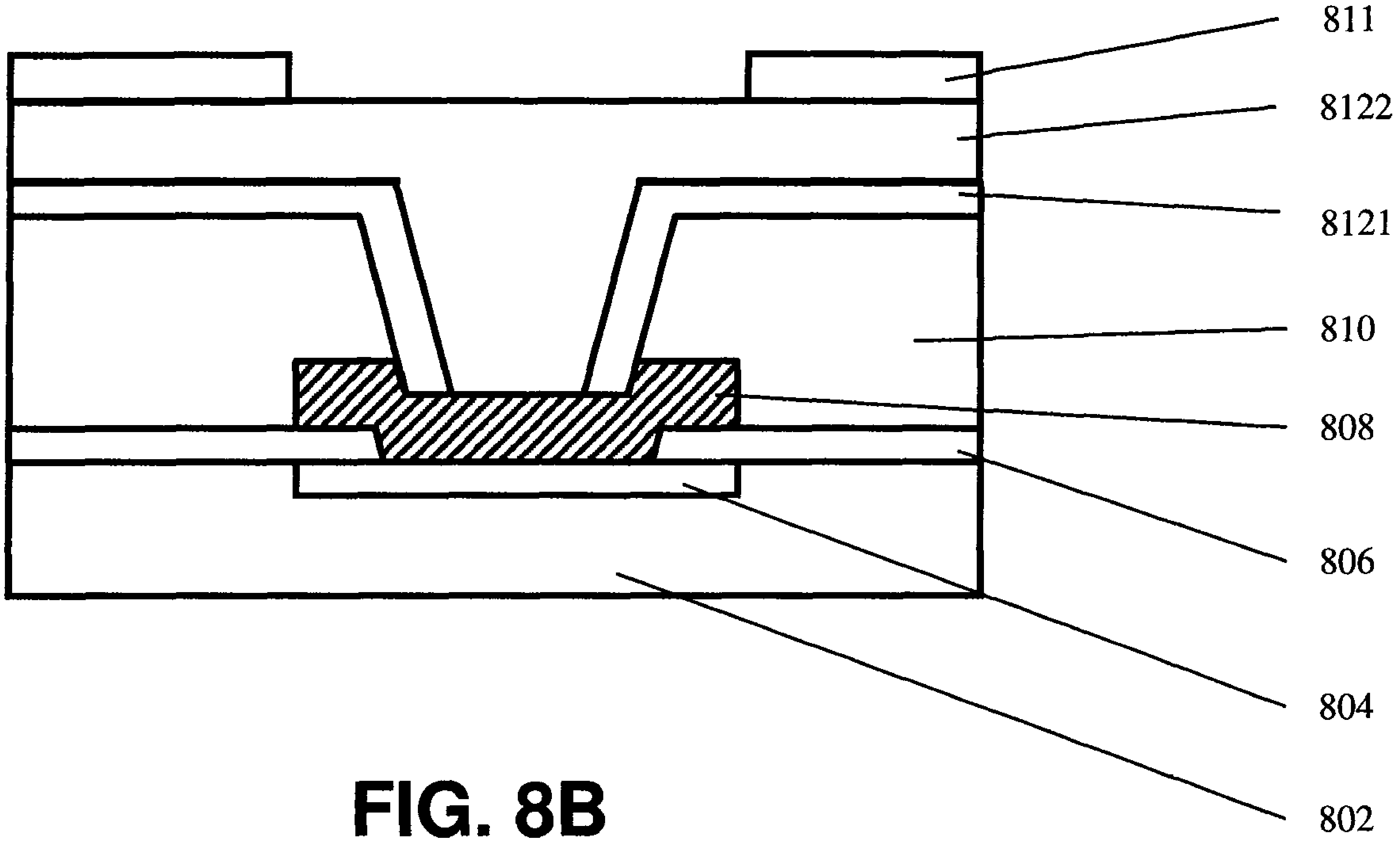
811
8122
8121
810
808
806
804
802

FIG. 8B

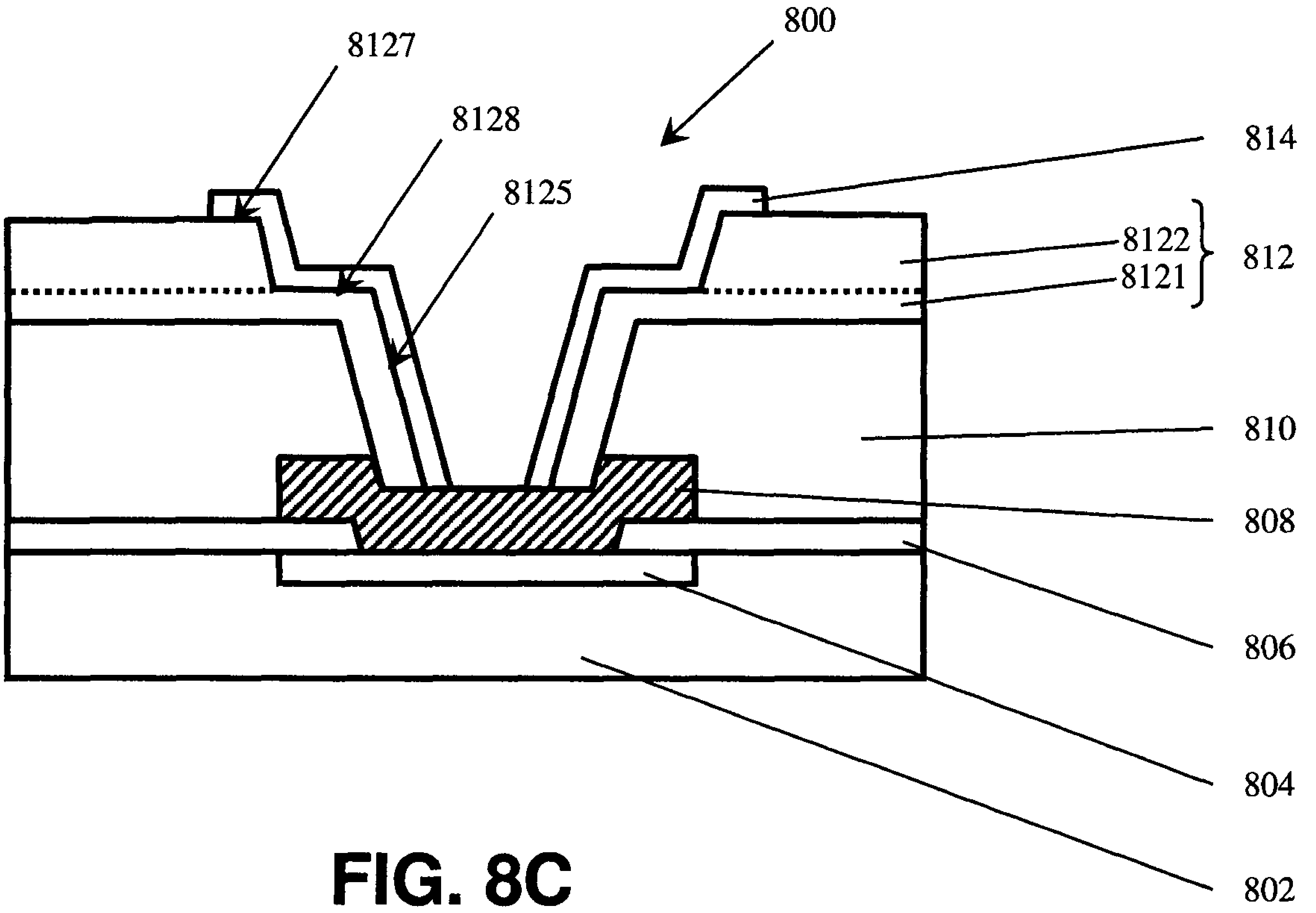
8127
800
8128
8125
814
8122
8121
812
810
808
806
804
802

FIG. 8C

STRESS BUFFER STRUCTURES IN A MOUNTING STRUCTURE OF A SEMICONDUCTOR DEVICE

PRIORITY CLAIM

The present application is a continuation of U.S. application Ser. No. 13/714,828, filed Dec. 14, 2012, now U.S. Pat. No. 8,906,798, issued Dec. 9, 2014, which is a divisional application of U.S. application Ser. No. 12/697,473 filed Feb. 1, 2010, now U.S. Pat. No. 8,354,750, issued Jan. 15, 2013, the disclosures of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

The present disclosure relates to stress buffer structures for a mounting structure of a semiconductor device.

BACKGROUND

Recently, there has been a trend in miniaturizing integrated circuits (ICs), requiring a high I/O (input/output) density which, in turn, requires small-size bonding pads. Such bonding pads are often formed on the active surface of a chip and define the places where the circuits of the chip are electrically connected to external devices. Bonding wires have become increasingly unpopular due to various potential problems, such as short circuits or inconsistent or inadequate bond strengths. Therefore, a flip chip technique has been introduced. According to this technique, solder bumps are formed on bonding pads of a chip, and the chip is mounted directly on a substrate by reflowing the solder bumps. The final product is often referred to as a ball grid array (BGA) or a flip chip ball grid array (FCBGA) chip or package.

To promote adhesion between the solder bump and the bonding pad, an under bump metallurgy or under bump metallization (UBM) structure is interposed between the solder bump and the bonding pad. UBM structures can also perform other functions, for example, as a barrier for preventing diffusion of the solder material into the bonding pad or even into the semiconductor material of the chip. A typical UBM structure includes several metal layers each performing a desired function.

Due to the concentration of multiple material layers of a UBM structure and a solder bump at and in the vicinity of each bonding pad, there is also a concentration of stress in this area. Such a stress, without preventive measure, may become sufficiently large to cause damage to inter-level dielectric (ILD) layers of the chip that are located immediately below or adjacent the bonding pad. Particularly sensitive to stress are low-k (low dielectric constant material) layers which are brittle and, in some applications, porous. Such low-k layers are easy to crack and/or delaminate under stress.

BRIEF DESCRIPTION OF THE DRAWINGS

One or more embodiments are illustrated by way of example, and not by limitation, in the figures of the accompanying drawings, wherein elements having the same reference numeral designations represent like elements throughout. The drawings are not to scale, unless otherwise disclosed.

FIG. **1** is a schematic, cross-sectional view of a solder bump structure in a semiconductor device.

FIGS. **2**A-**2**C are schematic, simplified cross-sectional views of several bonding structures for the solder bump structure.

FIGS. **3**A-**3**B are graphs comparing stress distributions and stress values, respectively, in the bonding structures of FIGS. **2**A-**2**C.

FIGS. **4**A-**4**H are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device according to some embodiments.

FIGS. **5**A-**5**D are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device according to further embodiments.

FIGS. **6**A-**6**B are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device according to yet further embodiments.

FIGS. **7**A-**7**C are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device according to still further embodiments.

FIGS. **8**A-**8**C are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device according to some other embodiments.

DETAILED DESCRIPTION

Throughout the description presented below, it will be understood that when a layer is referred to as being ‘on’ or ‘over’ another layer or substrate, it can be in direct contact with the other layer or substrate, or intervening layers may also be present therebetween.

FIG. **1** is a schematic, cross-sectional view of a solder bump structure **100** known to the inventors. Solder bump structure **100** is formed on an active surface **101** of a wafer or chip **102** of a semiconductor device, and includes a first passivation layer **106**, a bonding pad **108**, a second passivation layer **110**, a PI (polyimide) layer **112**, a UBM structure **114** and a solder bump **116** formed one on top another in the recited order. Chip **102** includes, under bonding pad **108**, a top-level metal **104** electrically connected to bonding pad **108**. The top-level metal **104** is a portion of an interconnection structure within chip **102**. The interconnection structure of chip **102** further includes, under and/or in the vicinity of top-level metal **104**, one or more dielectric layers (not shown) which, as discussed above, are often made of low-k or extreme low-k materials that are brittle and susceptible to cracks or delamination.

The inventors have found that solder bump structure **100** generally creates a high stress concentration at upper and lower corners **120**, **122** of UBM structure **114**. The stress distribution depends, among other things, on the inclination angle of a sidewall **1149** of UBM structure **114**. Specifically, the inventors have discovered that at a relatively acute inclination angle (e.g., 40° with respect to active surface **101**) of sidewall **1149**, stress is largely concentrated around lower corner **120**. As the inclination angle of sidewall **1149** increases toward 90°, the stress concentration shifts towards upper corner **122**. However, at any inclination angle, high stress is still transmitted to the dielectric layers of the interconnection structure underneath corners **120**, **122** and increases the possibility of cracks in or delamination of the dielectric layers.

FIG. **2**A is a simplified or partial view of solder bump structure **100** of FIG. **1**. FIGS. **2**B-**2**C are views similar to FIG. **2**A and show solder bump structures **240**, **250** in accordance with various embodiments.

Specifically, solder bump structure **240** of FIG. **2**B is formed on an active surface **201** of a semiconductor wafer or chip (not shown) of a semiconductor device. Solder bump structure **240** includes a bonding pad **208**, a stress buffer structure **212**, a UBM structure **214** and a solder bump **216** (partially shown) formed one on top another in the recited order. Under bonding pad **208**, the chip includes an interconnection structure comprising multiple conductive and dielectric layers alternatingly arranged one on top another. For the sake of simplicity, only a top-level conductive layer, e.g., a top metal layer, **204** of the interconnection structure is shown in the figure. The interconnection structure further includes, under and/or in the vicinity of top metal **204**, one or more dielectric layers (not shown) which, in some embodiments, are made of low-k or extreme low-k materials. Solder bump structure **240** defines a mounting structure for the chip when the chip is flipped over and placed on a carrier, such as a substrate or lead frame (not shown) and solder bump **216** is re-flown. In some embodiments, the chip comprises multiple bonding pads **208** for which multiple solder bump structures **240** are provided.

Stress buffer structure **212** defines a distinction from PI layer **112** of solder bump structure **100** in FIGS. **1** and **2**A. In particular, PI layer **112** has a sidewall **1125** that monotonously extends upward from bonding pad **108**, i.e., sidewall **1125** extends at a uniform slope from the bonding pad. As a result, UBM structure **114** formed on PI layer **112** and conforming in shape to PI layer **112** also has monotonously extending sidewall **1149**. Such solder bump structure **100**, as discussed above, is likely to cause stress concentration on the underlying layers, such as low-k or extremely low-k dielectric layers, of the chip.

To the contrary, stress buffer structure **212** of solder bump structure **240** in FIG. **2**B does not have a monotonously extending sidewall. Instead, sidewall **2125** of stress buffer structure **212** extends in a stepwise manner upwardly from bonding pad **208**. Sidewall **2125** includes at least two steps above the level of bonding pad **208**, namely lower step **2121** and upper step **2122** which have respective heights b and a as exemplarily depicted in FIG. **2**B. Since sidewall **2125** of stress buffer structure **212** is stepwise, UBM structure **214**, which is formed on stress buffer structure **212** and conforms in shape to stress buffer structure **212**, also has a stepwise sidewall **2149**. As discussed in detail herein below, the stepwise configuration of UBM structure **214** and stress buffer structure **212** results in a more uniform distribution of stress on the underlying layers, such as low-k or extremely low-k dielectric layers. The stepwise configuration further reduces the maximum and/or average values of stress compared to solder bump structure **100**.

Solder bump structure **250** in FIG. **2**C is similar to solder bump structure **240**, except for the height ratio between steps, such as lower step **2121** and upper step **2122**. The particular illustrated configuration in FIG. **2**B has an approximately 1:1 height ratio, i.e., the height b of lower step **2121** and the height of upper step **2122** are about the same. The particular illustrated configuration in FIG. **2**C has an approximately 2:1 height ratio, i.e., upper step **2122** is about twice as high as lower step **2121**.

Assuming that all characteristics (i.e., materials, thicknesses etc.) of solder bump structures **100**, **240** and **250** are the same, except for the particular shapes and the particular height ratios (applicable to FIGS. **2**B-**2**C) of PI layer **112**/stress buffer structure **212** and corresponding UBM structures, the results of performing a computer simulation of stress generation are shown in FIGS. **3**A-**3**B.

FIG. **3**A is a graph of stress distribution in the underlying low-k or extremely low-k dielectric (ELK) materials, e.g., under top metal layers **104**, **204**, in solder bump structures **100**, **240** and **250**. The stress distribution of solder bump structure **100** in FIG. **2**A is most uneven, having very high peaks (maximum stress values) at locations corresponding to lower corners **120** (FIG. **1**). The stress distribution of solder bump structure **240** in FIG. **2**B is more uniform than that of solder bump structure **100** in FIG. **2**A, having lower high peaks. The stress distribution of solder bump structure **250** in FIG. **2**C is even more uniform that that of solder bump structure **240** in FIG. **2**B, having even lower high peaks. As a result, the maximum stress values are reduced from solder bump structure **100** down to solder bump structure **240** and further down to solder bump structure **250**. Thus, high stress concentrations are less severe in solder bump structure **240** and solder bump structure **250** than in solder bump structure **100**.

The average stress values are also improved. FIG. **3**B is a graph showing average stress values in the underlying low-k or extremely low-k dielectric (ELK) materials, e.g., under top metal layers **104**, **204**, and in the overlying UBM structures, such as UBM structures **114**, **214**. As apparent from FIG. **3**B, average stress values, across the width of the UBM structure, in both the underlying dielectric materials and the UBM structures decrease from solder bump structure **100** to solder bump structure **240** and further to solder bump structure **250**. The average stress value in the underlying dielectric materials is reduced more than 25% (from 63.4 to 47.1) and the average stress value in the UBM structure is reduced for about 20% (from 183.3 to 147.1).

Thus, the stepwise configuration of the UBM structure and the stress buffer structure results in more uniform stress distribution and lower maximum/average stress values in both the underlying dielectric materials of the chip and in the UBM structure itself. In numerous unshown embodiments, by varying the number of steps (e.g., forming more than two steps) and/or the heights and/or height ratios among the steps of such stepwise configuration, stress values and distributions in the UBM structure as well as the underlying dielectric materials of the chip can be optimized as desired. Such stress optimization is performed either independently of or in combination with other adjustments, such as the thickness of the stress buffer structure (also referred to as "PI thickness" in some embodiments) and/or the size of the opening in the stress buffer structure (also referred to as "PI opening" in some embodiments) and/or the inclination angle of the sidewall of the opening.

Stress buffer structure **212** includes one or more material layers. For simplicity, only one layer of stress buffer structure **212** is shown in FIGS. **2**B-**2**C. Such layer is made of a stress buffer material and defines stepwise wall **2125** of stress buffer structure **212** and, hence, corresponding stepwise wall **2149** of UBM structure **214**. The stress buffer material in some embodiments is a polymer. The polymer in one or more embodiments is selected from the group consisting of polyimide, polybenzoxazole (PBO), epoxy-based polymers, phenol-based polymers, and benzocyclobutene (BCB).

In some embodiments, a passivation layer (not shown in FIGS. **2**B-**2**C) similar to second passivation layer **110** of solder bump structure **100** is provided under stress buffer structure **212** to adjust the height of stress buffer structure **212** without requiring a large amount of the stress buffer material. In further embodiments, multiple layers of one or more stress buffer materials are deposited on top the other to define stress buffer structure **212**, either entirely or in combination with a passivation layer.

FIGS. **4**A-**4**H are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device **400** (FIG. **4**H) according to some embodiments.

In FIG. **4**A, a semiconductor substrate **402** is provided. Semiconductor substrate **402** is, in some embodiments, a wafer. In further embodiments, semiconductor substrate **402** is a chip having internal circuitry and active surface **401**.

Semiconductor substrate **402** includes a top-level conductive layer, e.g., a top metal layer **404**. Semiconductor substrate **402** further includes, under and/or in the vicinity of top metal **404**, one or more dielectric layers (not shown) which are, in some embodiments, made of low-k or extremely low-k materials that are brittle and susceptible to cracks or delamination.

A first passivation layer **406** is formed on active surface **401** to partially cover top metal layer **404**. The part of top metal layer **404** that is not covered by first passivation layer **406** is exposed in a first opening also referred to herein as the first passivation opening. Passivation layer **406** in some embodiments comprises an oxide layer or a nitride layer, such as silicone oxide or silicon nitride. In further embodiments, first passivation layer **406** comprises polyimide. An exemplary process of forming first passivation layer **406** includes depositing (e.g., by chemical vapor deposition—CVD) a passivation material on active surface **401** and then etching away a portion of the passivation material to form the first passivation opening.

A conductive material is subsequently deposited in the first passivation opening, and on a top surface of first passivation layer **406** around the first passivation opening to form a bonding pad **408**. In some embodiments, bonding pad **408** is confined within the first passivation opening, without being deposited on the top surface of first passivation layer **406**. The conductive material of bonding pad **408** comprises Al or Cu and is deposited to be in electrical contact (e.g., via a conductive via) with the internal circuitry of semiconductor substrate or chip **402**.

A passivation material layer **4101** is deposited on bonding pad **408** and first passivation layer **406** as shown in FIG. **4**A. Passivation material layer **4101** in the particularly illustrated embodiment has a top surface conforming in shape to the underlying bonding pad **408**. In further embodiments, the top surface of passivation material layer **4101** is planarized prior to subsequent processing. Passivation material layer **4101** is made of the same as or similar material to first passivation layer **406**.

In FIG. **4**B, a mask **411** having an opening D1 is used to partially remove an exposed portion of passivation material layer **4101**. For example, mask **411** comprises a photoresist deposited and then photo-lithographically patterned on the top surface of passivation material layer **4101**. The removal of passivation material layer **4101** is performed by, e.g., a first etching process.

FIG. **4**C shows the result of the first etching process and after mask **411** is removed. Specifically, a second passivation opening **4159** is formed in passivation material layer **4101**. The once patterned passivation material layer **4101** will be referred to herein as passivation material layer **4102**. In some embodiments, as shown in FIG. **4**C, the etching of passivation material layer **4101** stops before bonding pad **408** is exposed. Consequently, a stepwise configuration with at least three steps will be obtained as disclosed herein below. In other embodiments, the etching of passivation material layer **4101** is performed until bonding pad **408** is exposed. As a result, a stepwise configuration with at least two steps will be obtained.

In FIG. **4**D, a further mask **413** having an opening D2 greater than D1 is used to further remove, e.g., by a second etching process, an exposed portion of passivation material layer **4102**. For example, mask **413** is formed similarly to mask **411**.

FIG. **4**E shows the result of the second etching process and after mask **413** is removed. Specifically, second passivation opening **4159** is enlarged and denoted as **4160**. The twice patterned passivation material layer **4101** has now become a second passivation layer **410**. As shown in FIG. **4**E, second passivation layer **410** has a stepwise wall **4107**. The second etching process of passivation material layer **4102** is performed until bonding pad **408** is exposed.

FIG. **4**E shows the result of the second etching process and after mask **413** is removed. Specifically, second passivation opening **4159** is enlarged and now denoted as **4160**. The twice patterned passivation material layer **4101** has now become a second passivation layer **410**. As shown in FIG. **4**E, second passivation layer **410** has a stepwise wall **4107**.

In FIG. **4**F, a stress buffer material layer **4121** is deposited, e.g., by spin-coating, on second passivation layer **410**, in second passivation opening **4160** and on the exposed portion of bonding pad **408**. A sidewall **4125** of stress buffer material layer **4121** has two upper steps conforming in shape to stepwise wall **4107** of second passivation layer **410**. Sidewall **4125** of stress buffer material layer **4121** further has a lower step conforming in shape to a raised portion **4083** of bonding pad **408**.

In FIG. **4**G, the portion of stress buffer material layer **4121** at the bottom of second passivation opening **4160** is removed to expose a portion of bonding pad **408**, using, for example, well-known patterning methods including photolithography and etching processes. The so formed and patterned stress buffer material layer **4121** has now become a stress buffer structure **412** having a stepwise configuration with three steps.

In FIG. **4**H, an UBM structure **414** is deposited on stress buffer structure **412**, conforming in shape to stress buffer structure **412** and in electrical contact with the exposed portion of bonding pad **408**. UBM structure **414** includes one or more layers of at least one metal selected from the group consisting of Cr, Ti, Ni, W, Pt, Cu, Pd, Au, Ag and alloys thereof. UBM structure **414** is formed by sequentially depositing, e.g., by CVD, plating or sputtering, the component layers on bonding pad **408**, and then etching away, e.g., by dry etching or wet etching, the unwanted portions. A solder bump **416** is formed on UBM structure **414** to complete semiconductor device **400**.

FIGS. **5**A-**5**D are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device **500** (FIG. **5**D) according to some embodiments.

In FIG. **5**A, a semiconductor substrate **502** similar to semiconductor substrate **402** is provided. Semiconductor substrate **502** includes a top-level conductive layer, e.g., a top metal layer **504** similar to top metal layer **404**. A first passivation layer **506**, a bonding pad **508** and a passivation material layer **5101** similar to first passivation layer **406**, bonding pad **408**, passivation material layer **4101**, respectively, are formed on semiconductor substrate **502** in manners substantially similar to those described with respect to FIG. **4**A.

A difference between FIGS. **5**A and **4**A is that in FIG. **5**A, first passivation layer **506** is patterned more than once, e.g., twice, whereas in FIG. **4**A, first passivation layer **406** is patterned once. As the result the first passivation opening in first passivation layer **506** has a stepwise sidewall as shown in FIG. **5**A. An exemplary process of forming the stepwise first passivation opening is similar to that described with respect to FIGS. **4**B-**4**E, e.g., by two etching processes with two differently sized masks. Other methods are, however, not excluded.

A further difference between FIGS. **5**A and **4**A is that bonding pad **508** formed on and conforming in shape to underlying first passivation layer **506** also has a stepwise configuration. Specifically, bonding pad **508** has a lower step **5081** and an upper step **5082** corresponding to a lower step **5061** and an upper step **5062** of first passivation layer **506**, respectively. In some embodiments (not shown), bonding pad **508** is confined within a boundary defined by upper step **5062** of first passivation layer **506**, and therefore has a configuration similar to that of FIG. **4**A.

In FIG. **5**B, a mask **511** similar to mask **411** and having an opening D**3** is used to remove an exposed portion of passivation material layer **5101**, in a manner similar to that described with respect to FIG. **4**B.

FIG. **5**C shows the result of the etching process of FIG. **5**B and after mask **511** is removed. Specifically, a second passivation opening **5159** is formed in the once patterned passivation material layer **5101** which has now become second passivation layer **510**. The etching of passivation material layer **5101** stops upon or after bonding pad **508** is exposed. A top surface of upper step **5082** of bonding pad **508** is buried in second passivation layer **510**, and therefore a stepwise configuration with at least two steps will be obtained as disclosed herein below.

In FIG. **5**D, a stress buffer material layer is deposited and patterned to define stress buffer structure **512** in manners similar to those described with respect to FIGS. **4**F-**4**G. A sidewall **5125** of stress buffer material layer **512** has an upper step **5127** corresponding to a top surface of second passivation layer **510**, and a lower step **5128** corresponding to lower step **5081** of bonding pad **508**.

An UBM structure **514** is deposited on stress buffer structure **512**, conforming in shape to stress buffer structure **512** and in electrical contact with the exposed middle portion of bonding pad **508** in manners similar to those described with respect to FIG. **4**H. A solder bump (not shown in FIG. **5**D) is formed on UBM structure **514** to complete semiconductor device **500**.

FIGS. **6**A-**6**B are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device **600** (FIG. **6**B) according to some embodiments.

FIG. **6**A is a continuation to the step of FIG. **5**C, in that a mask **613** having an opening D**4** greater than D**3** is used for further etching second passivation layer **510** to obtain stress buffer structure **612** (FIG. **6**B). Thus, the second passivation opening **5159** in FIG. **5**C is widened, and as a result, a top surface of upper step **5082** of bonding pad **508** is exposed, and defines a further step of the final stepwise configuration shown in FIG. **6**B.

Specifically, in FIG. **6**B, a sidewall **6125** of stress buffer material layer **612** has an upper step **6127** corresponding to a top surface of second passivation layer **610**, a lower step **6128** corresponding to lower step **5081** of bonding pad **508**, and a middle step **6129** corresponding to the top surface of upper step **5082** of bonding pad **508**.

An UBM structure **614** is deposited on stress buffer structure **612**, conforming in shape to stress buffer structure **612** and in electrical contact with the exposed middle portion of bonding pad **508** in manners disclosed herein. A solder bump (not shown in FIG. **6**B) is formed on UBM structure **614** to complete semiconductor device **600**.

In some embodiments, mask **613** is used instead of, rather than in combination with, mask **511** to etch passivation material layer **5101** as shown in FIG. **5**B, to obtain a semiconductor device similar to semiconductor device **600**.

FIGS. **7**A-**7**C are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device **700** (FIG. **7**C) according to some embodiments.

FIG. **7**A shows a state of the semiconductor device as being manufactured by several processes similar to those disclosed with respect to FIGS. **4**A-**4**C and **4**F-**4**H. Specifically, a semiconductor substrate **702** in FIG. **7**A is similar to semiconductor substrate **402**. Semiconductor substrate **702** includes a top-level conductive layer, e.g., a top metal layer **704** similar to top metal layer **404**. A first passivation layer **706**, a bonding pad **708** and a passivation material layer (not shown) similar to first passivation layer **406**, bonding pad **408**, passivation material layer **4101**, respectively, are formed on semiconductor substrate **702** in manners substantially similar to those described with respect to FIG. **4**A.

The passivation material layer is patterned with a mask similar to that described with respect to FIG. **4**B.

The patterning of the passivation material layer, unlike the process particularly shown in FIG. **4**C, is performed until the middle portion of bonding pad **708** is exposed, thereby obtaining a second passivation layer **710**.

A stress buffer material layer (not shown) is deposited on the patterned second passivation layer **710** as described with respect to FIG. **4**F, and patterned as described with respect to FIG. **4**G, thereby obtaining a patterned stress buffer material layer **7121** as illustrated in FIG. **7**A.

A mask **711** similar to mask **411** and having an opening (not numbered) wider than that of second passivation opening **7159** formed in second passivation layer **710** is used to remove a partial thickness of an exposed portion of patterned stress buffer material layer **7121** around second passivation opening **7159** to obtain a stress buffer structure **712** as shown in FIG. **7**B.

FIG. **7**B shows the result of the etching process of FIG. **7**A and after mask **711** is removed. Specifically, the partial thickness removal of patterned stress buffer material layer **7121** creates a stepwise wall **7125** for stress buffer structure **712**. In particular, sidewall **7125** of stress buffer material layer **712** has an upper step **7127** corresponding to a top surface of patterned stress buffer material layer **7121** before the second etching process, and a lower step **7128** corresponding to a top surface of the stress buffer material layer **7121** around second passivation opening **7159** after the second etching process. Thus, a stepwise configuration of two steps is obtained.

In FIG. **7**C, an UBM structure **714** is deposited on stress buffer structure **712**, conforming in shape to stress buffer structure **712** and in electrical contact with the exposed middle portion of bonding pad **708** in manners similar to those described with respect to FIG. **4**H. A solder bump (not shown in FIG. **7**C) is formed on UBM structure **714** to complete semiconductor device **700**.

FIGS. **8**A-**8**C are schematic cross-sectional views showing various steps of manufacturing a bonding structure for a semiconductor device **800** (FIG. **8**C) according to some embodiments.

FIG. **8**A is similar to FIG. **7**A, without mask **711**. Thus, a semiconductor substrate **802** in FIG. **8**A is similar to semiconductor substrate **702**. Semiconductor substrate **802** includes a top-level conductive layer, e.g., a top metal layer **804** similar to top metal layer **704**. A first passivation layer **806**, a bonding pad **808**, a second passivation layer **810** and a patterned stress buffer material layer **8121** similar to first passivation layer **706**, bonding pad **708**, second passivation layer **710** and patterned stress buffer material layer **7121**, respectively, are formed on semiconductor substrate **802** in manners disclosed herein. A second passivation opening **8159** similar to second passivation opening **7159** is also formed.

In FIG. **8**B, instead of immediately etching the structure shown in FIG. **8**A with a mask as discussed with respect to FIG. **7**A, a second stress buffer material layer **8122** is filled in second passivation opening **8159** and deposited to a desired thickness on patterned stress buffer material layer **8121**. A spin-coating process is used in some embodiments for forming such second stress buffer material layer **8122**. A mask **811** of a desired opening (not numbered) is then used to etch away the exposed portion of second stress buffer material layer **8122** in second passivation opening **8159** and on top of patterned stress buffer material layer **8121**. The etch selectivity of stress buffer materials of patterned stress buffer material layer **8121** and second stress buffer material layer **8122** is chosen such that the exposed portion of second stress buffer material layer **8122** is removed without significantly effecting the thickness of patterned stress buffer material layer **8121** within the opening of mask **811**.

FIG. **8**C shows the result of the etching process of FIG. **8**B and after mask **811** is removed. A stress buffer structure **812**, which is a combination of a remainder of second stress buffer material layer **8122** and patterned stress buffer material layer **8121**, is obtained with a stepwise wall **8125**. Sidewall **8125** of stress buffer material layer **812** has an upper step **8127** corresponding to a top surface of second stress buffer material layer **8122** and a lower step **8128** corresponding to a top surface of patterned stress buffer material layer **8121**. Thus, a stepwise configuration of two steps is obtained. The height ratio of the steps of the stepwise configuration can be adjusted by simply adjusting the thickness of second stress buffer material layer **8122** in relation to a depth of second passivation opening **8159** (FIG. **8**A).

An UBM structure **814** is deposited on stress buffer structure **812**, conforming in shape to stress buffer structure **812** and in electrical contact with the exposed middle portion of bonding pad **808** in manners similar to those described with respect to FIG. **4**H. A solder bump (not shown in FIG. **8**C) is formed on UBM structure **814** to complete semiconductor device **800**.

In some embodiments, a semiconductor device includes a bonding pad on a substrate. The semiconductor device further includes a passivation layer covering a peripheral portion of the bonding pad while exposing a middle portion of the bonding pad. Additionally, the semiconductor device includes a stress buffer layer over the passivation layer where the stress buffer layer exposes a portion of the bonding pad, and where a wall of the stress buffer layer extends, in steps, upwardly from the exposed portion of the bonding pad. Furthermore, the semiconductor device includes an under-bump metallurgy (UBM) layer over the stress buffer layer, where the UBM layer contacts a portion of the bonding pad.

In some embodiments, a semiconductor device includes a metal layer embedded in a substrate. The semiconductor device further includes a passivation layer over the metal layer where the passivation layer exposes a portion of the metal layer, and the passivation layer includes a stepped wall that extends upwardly from the exposed portion of the metal layer. Furthermore, the semiconductor device includes a bonding pad over the exposed portion of the metal layer. Additionally, the semiconductor device includes an under-bump metallurgy (UBM) layer over the bonding pad.

In some embodiments, a semiconductor device includes a bonding pad on a substrate. The semiconductor device further includes a stress buffer structure over the bonding pad where the stress buffer structure exposes a portion of the bonding pad and where the stress buffer structure comprises a stepped wall that extends upwardly from the exposed portion of the bonding pad. Additionally, the semiconductor device includes an under-bump metallurgy (UBM) layer over the bonding pad, where the UBM layer contacts a portion of the bonding pad.

The foregoing has outlined features of several embodiments so that those skilled in the art may better understand the detailed description that follows. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for modifying other processes and structures for carrying out one or more of the same or similar purposes and/or achieving one or more of the same or similar advantages of the embodiments disclosed herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor device, comprising:

a bonding pad on a substrate;

a passivation layer covering a peripheral portion of the bonding pad while exposing a middle portion of the bonding pad;

a stress buffer layer over the passivation layer, the stress buffer layer exposing a portion of the bonding pad, wherein a wall of the stress buffer layer extends, in steps, upwardly from the exposed portion of the bonding pad; and

an under-bump metallurgy (UBM) layer over the stress buffer layer, wherein the UBM layer contacts a portion of the bonding pad,

wherein the bonding pad comprises a stepwise configuration which at least partially defines a stepwise sidewall of the stress buffer layer.

2. The semiconductor device according to claim **1**, wherein the stress buffer polymer layer comprises polyimide, polybenzoxazole (PBO), epoxy-based polymers, phenol-based polymers, or benzocyclobutene (BCB).

3. The semiconductor device of claim **1**, wherein the wall of the stress buffer layer comprises an upper step and a lower step, wherein the upper step and the lower step have equal lengths.

4. The semiconductor device of claim **1**, wherein the wall of the stress buffer layer comprises an upper step and a lower step, wherein the upper step has a first length that is greater than a second length of the lower step.

5. The semiconductor device of claim **1**, further comprising a sidewall of the passivation layer conforming to the contours of the wall of the stress buffer layer.

6. The semiconductor device of claim **1**, further comprising the UBM layer conforming to the contours of the wall of the stress buffer layer.

7. A semiconductor device, comprising:

a bonding pad on a substrate;

a stress buffer structure over the bonding pad, the stress buffer structure exposing a portion of the bonding pad, wherein the stress buffer structure comprises a stepped wall that extends upwardly from the exposed portion of the bonding pad; and

an under-bump metallurgy (UBM) layer over the bonding pad, wherein the UBM layer contacts a portion of the bonding pad;

wherein the bonding pad comprises a stepwise configuration which at least partially defines a stepwise sidewall of the stress buffer layer.

8. The semiconductor device according to claim **7**, wherein the stress buffer polymer layer comprises polyimide, polybenzoxazole (PBO), epoxy-based polymers, phenol-based polymers, or benzocyclobutene (BCB).

9. The semiconductor device of claim **7**, further comprising a passivation layer surrounding sidewalls of the bonding pad.

10. The semiconductor device of claim **9**, wherein a sidewall of the passivation layer conforms to the contours of the stepped wall of the stress buffer structure.

11. The semiconductor device of claim **7**, wherein the UBM layer conforms to the contours of the stepped wall of the stress buffer layer.

12. The semiconductor device of claim **7**, further comprising a solder bump over the UBM layer.

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