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Watanabe

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(54) **VIDEO PROCESSING APPARATUS**

(71) Applicant: **Kabushiki Kaisha Toshiba**, Minato-ku, Tokyo (JP)

(72) Inventor: **Manabu Watanabe**, Kawasaki Kanagawa (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

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(51) **Int. Cl.**

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H04N 7/00	(2011.01)
H04N 5/067	(2006.01)
G09G 5/18	(2006.01)
G09G 5/00	(2006.01)
G06T 1/60	(2006.01)

(52) **U.S. Cl.**
CPC ***H04N 5/067*** (2013.01); ***G06T 1/60*** (2013.01); ***G09G 5/006*** (2013.01); ***G09G 5/18*** (2013.01)

(58) **Field of Classification Search**
CPC H04N 5/06; H04N 5/067; H04N 5/0675; H04N 5/10; H04N 5/08; H04N 5/12; H04N 7/0887; H04N 7/0882; H04N 7/0885; H04N 7/081; H04N 7/088; H04N 7/035
USPC 348/521, 524, 529–531, 464, 468, 461, 348/460, 476–479
IPC H04N 5/06,7/00
See application file for complete search history.

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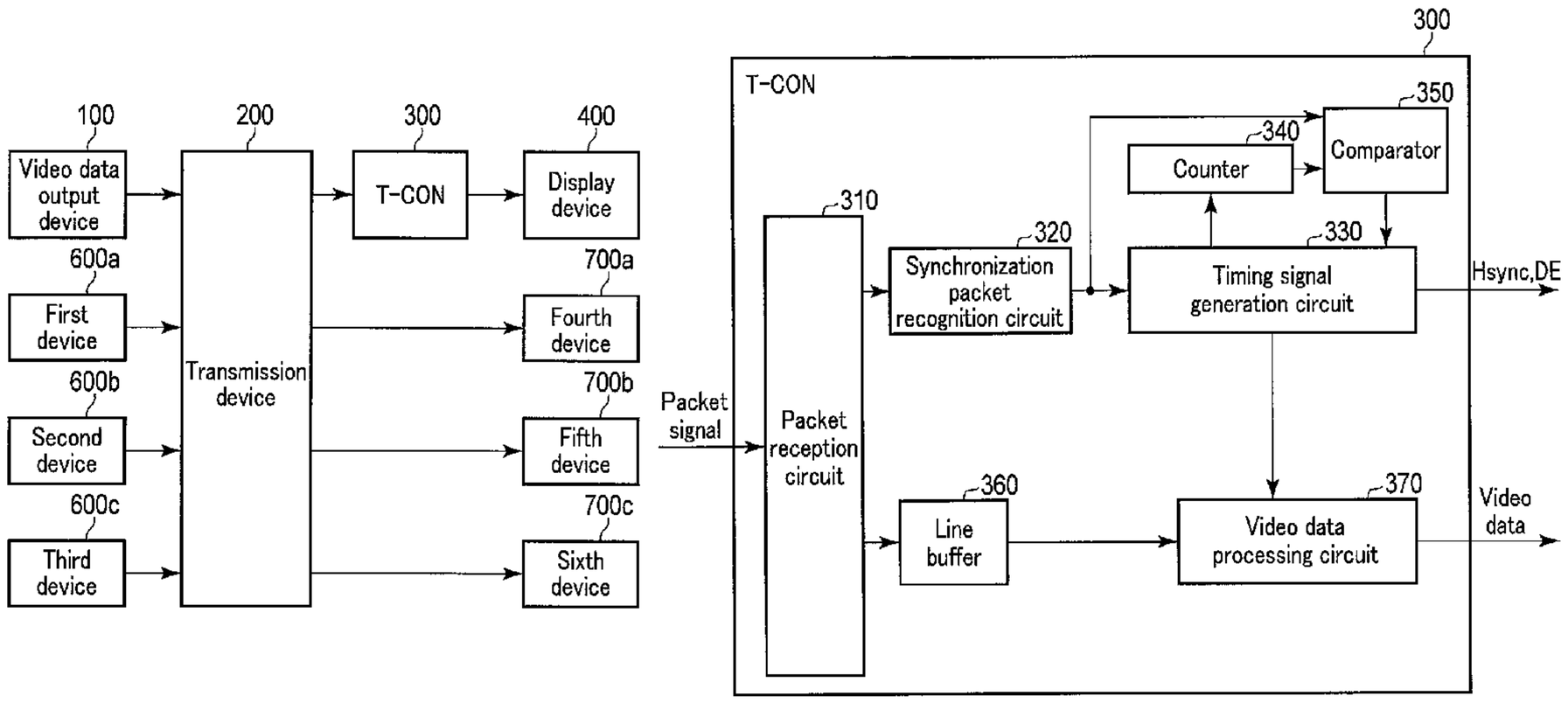
Primary Examiner — Sherrie Hsia
(74) *Attorney, Agent, or Firm* — White & Case LLP

(57) **ABSTRACT**

According to one embodiment, a video processing apparatus includes a video data output device which outputs a data packet signal obtained by packetizing a data enable signal and a synchronization packet signal obtained by packetizing a synchronization signal, a transmission device which transmits the data packet signal and the synchronization packet signal, the data packet signal being delayed by a first delay amount and the synchronization packet signal being delayed by a second delay amount, and a timing controller which generates the data enable signal and the synchronization signal so as to set a pulse of the synchronization signal within a blanking period of the data enable signal based on the data packet signal and the synchronization packet signal.

12 Claims, 8 Drawing Sheets



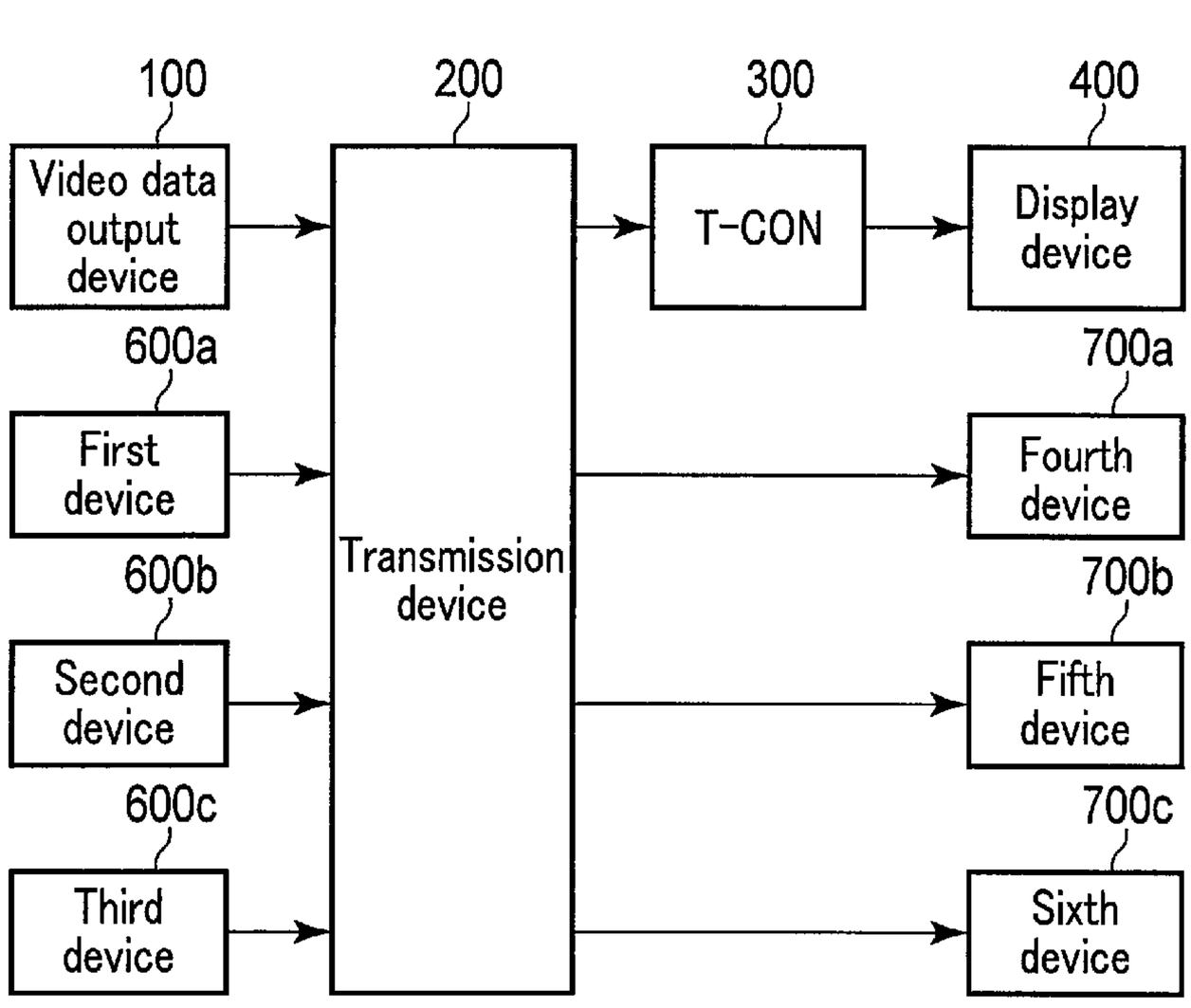

100
Video data output device
200
Transmission device
300
T-CON
400
Display device
600a
First device
600b
Second device
600c
Third device
700a
Fourth device
700b
Fifth device
700c
Sixth device

FIG. 1

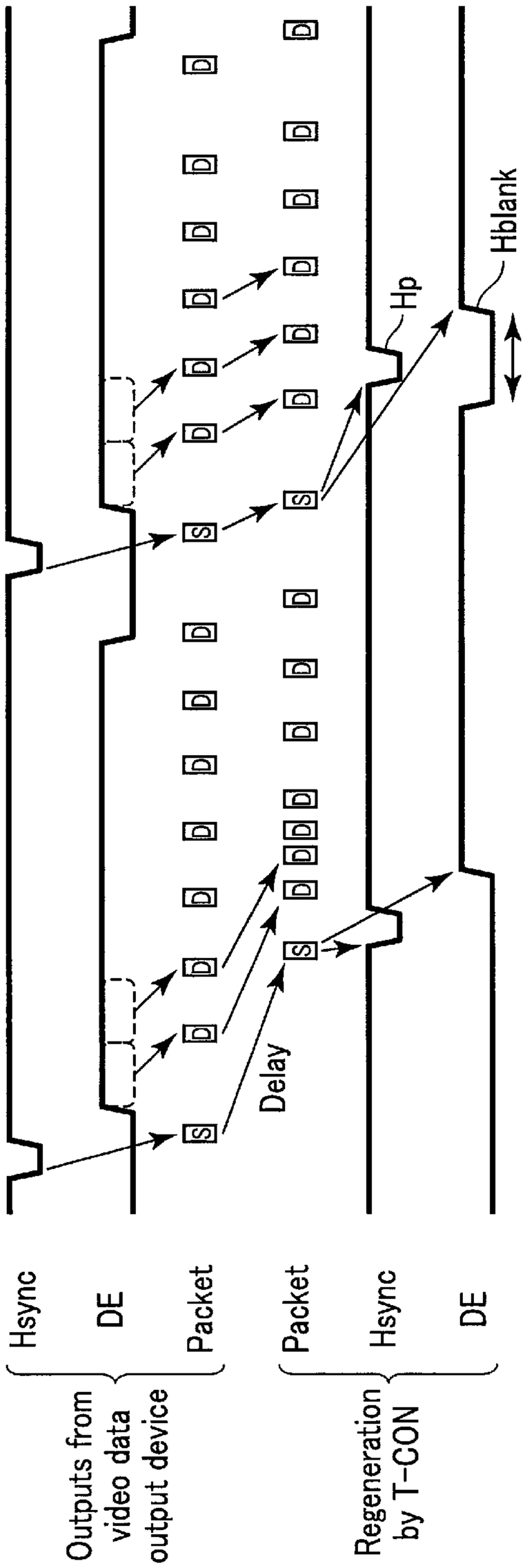

Hblank
Hp
Delay
Hsync
DE
Packet
Outputs from video data output device
Packet
Hsync
DE
Regeneration by T-CON

FIG. 2

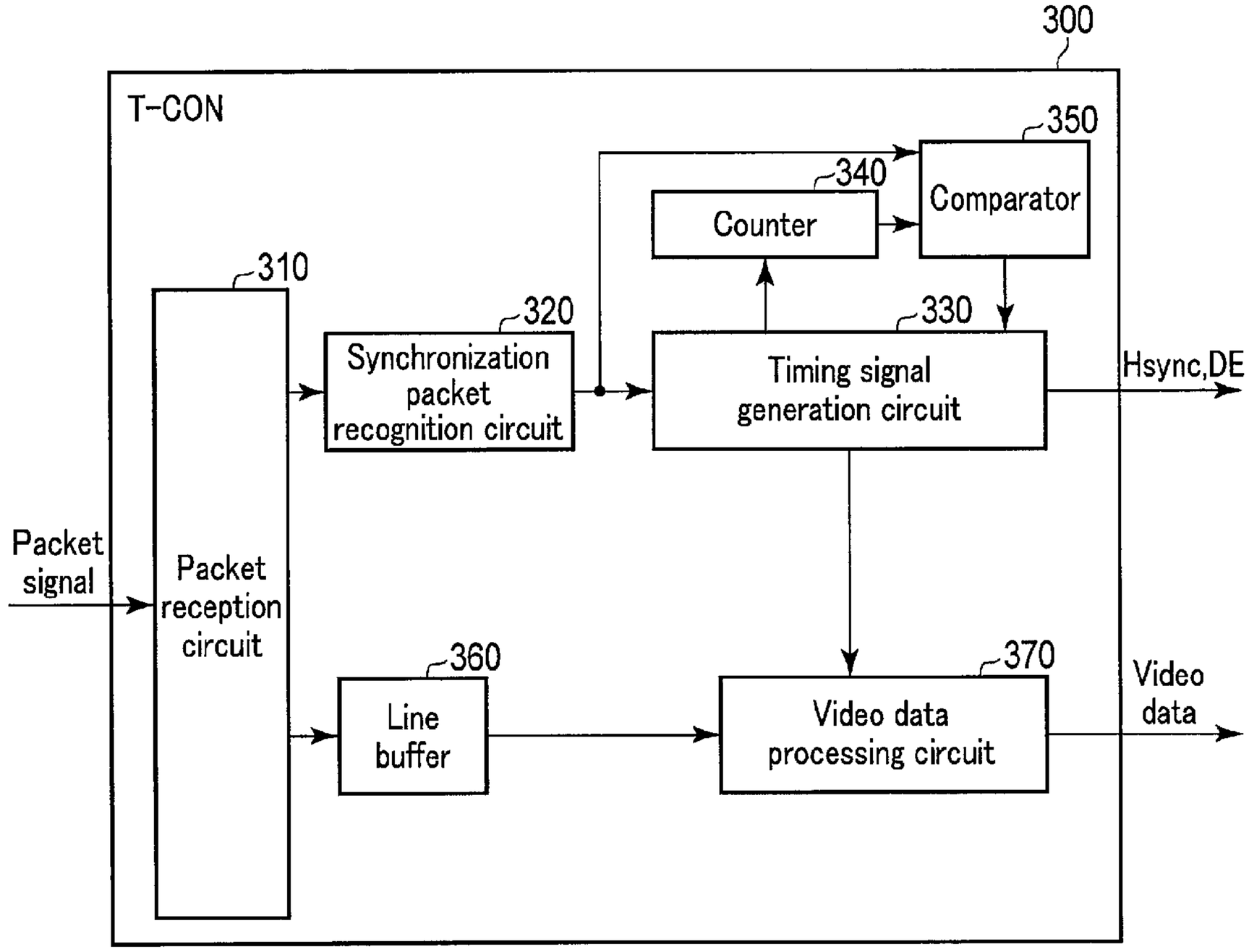

300
T-CON
350
Comparator
340
Counter
310
320
Synchronization packet recognition circuit
330
Timing signal generation circuit
Hsync,DE
Packet signal
Packet reception circuit
360
Line buffer
370
Video data processing circuit
Video data

FIG. 3

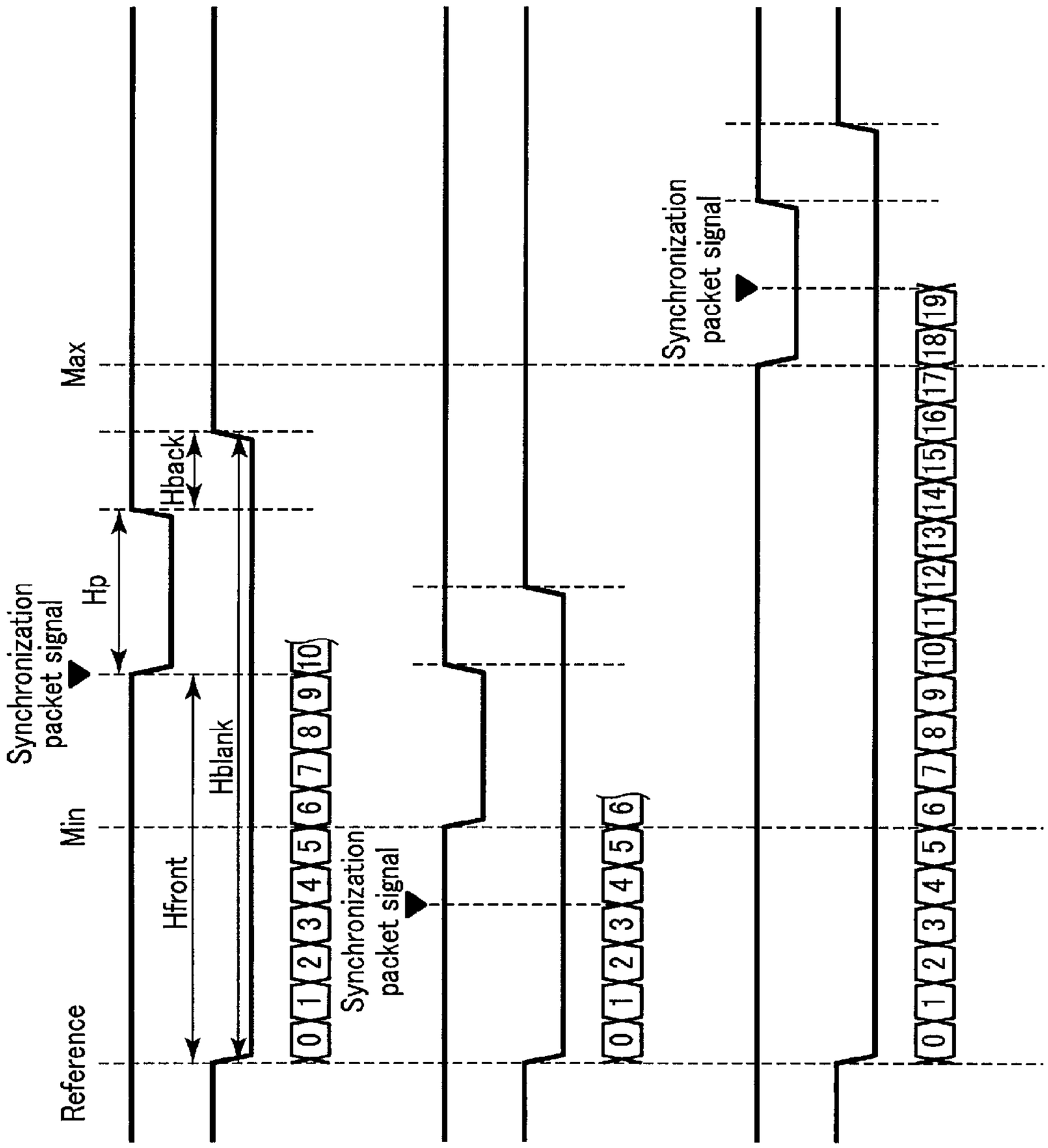

Max
Min
Reference
Hback
Hp
Hfront
Hblank
Synchronization packet signal
Synchronization packet signal
Synchronization packet signal
0 1 2 3 4 5 6 7 8 9 10
0 1 2 3 4 5 6
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
(a)
Synchronization packet signal is located between min and max
Hsync
DE
Counter
(b)
Synchronization packet signal is earlier than min
Hsync
DE
Counter
(c)
Synchronization packet signal is later than max
Hsync
DE
Counter

FIG. 4

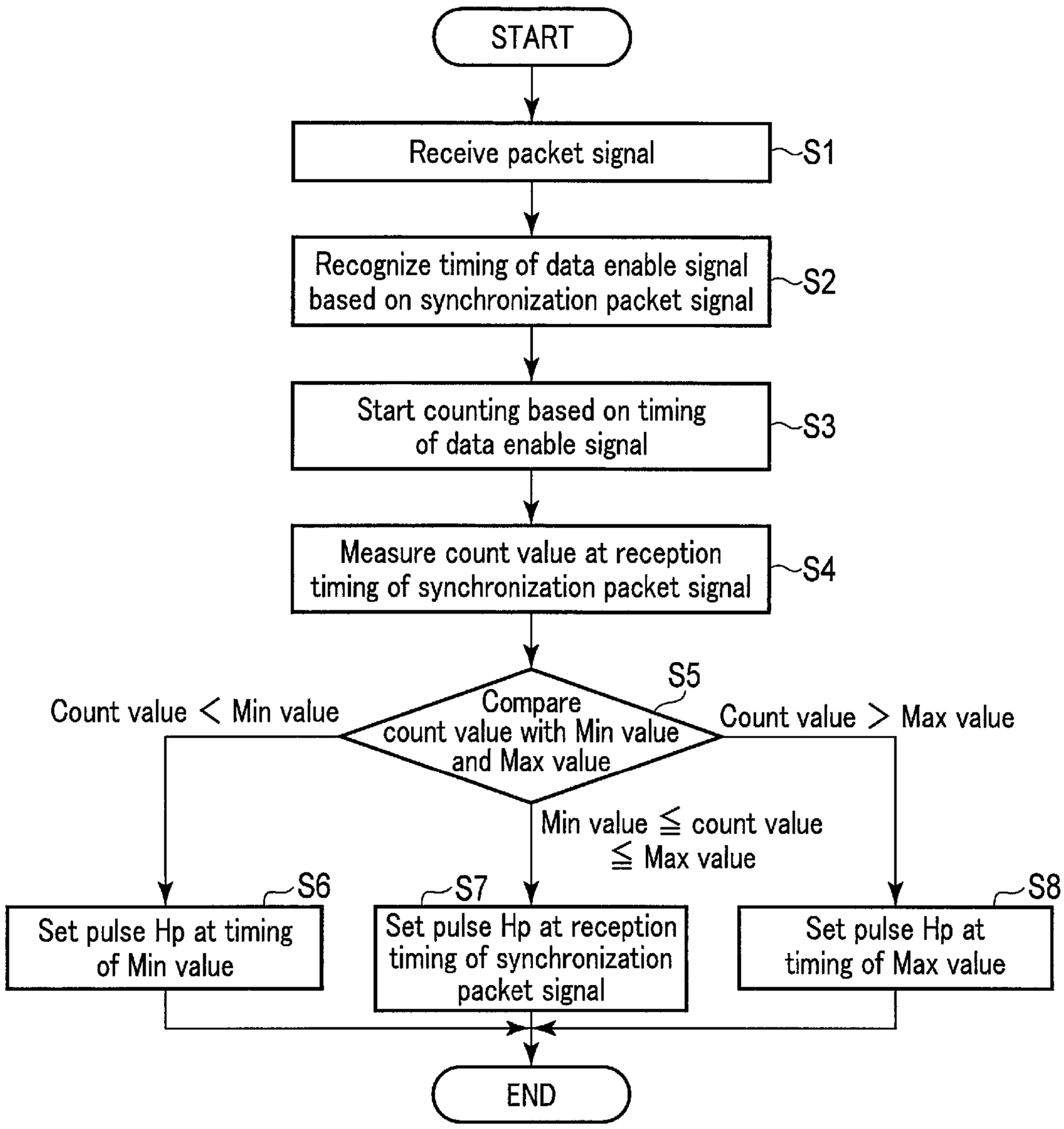

START
Receive packet signal
S1
Recognize timing of data enable signal based on synchronization packet signal
S2
Start counting based on timing of data enable signal
S3
Measure count value at reception timing of synchronization packet signal
S4
S5
Compare count value with Min value and Max value
Count value < Min value
Min value ≦ count value ≦ Max value
Count value > Max value
S6
Set pulse Hp at timing of Min value
S7
Set pulse Hp at reception timing of synchronization packet signal
S8
Set pulse Hp at timing of Max value
END

FIG. 5

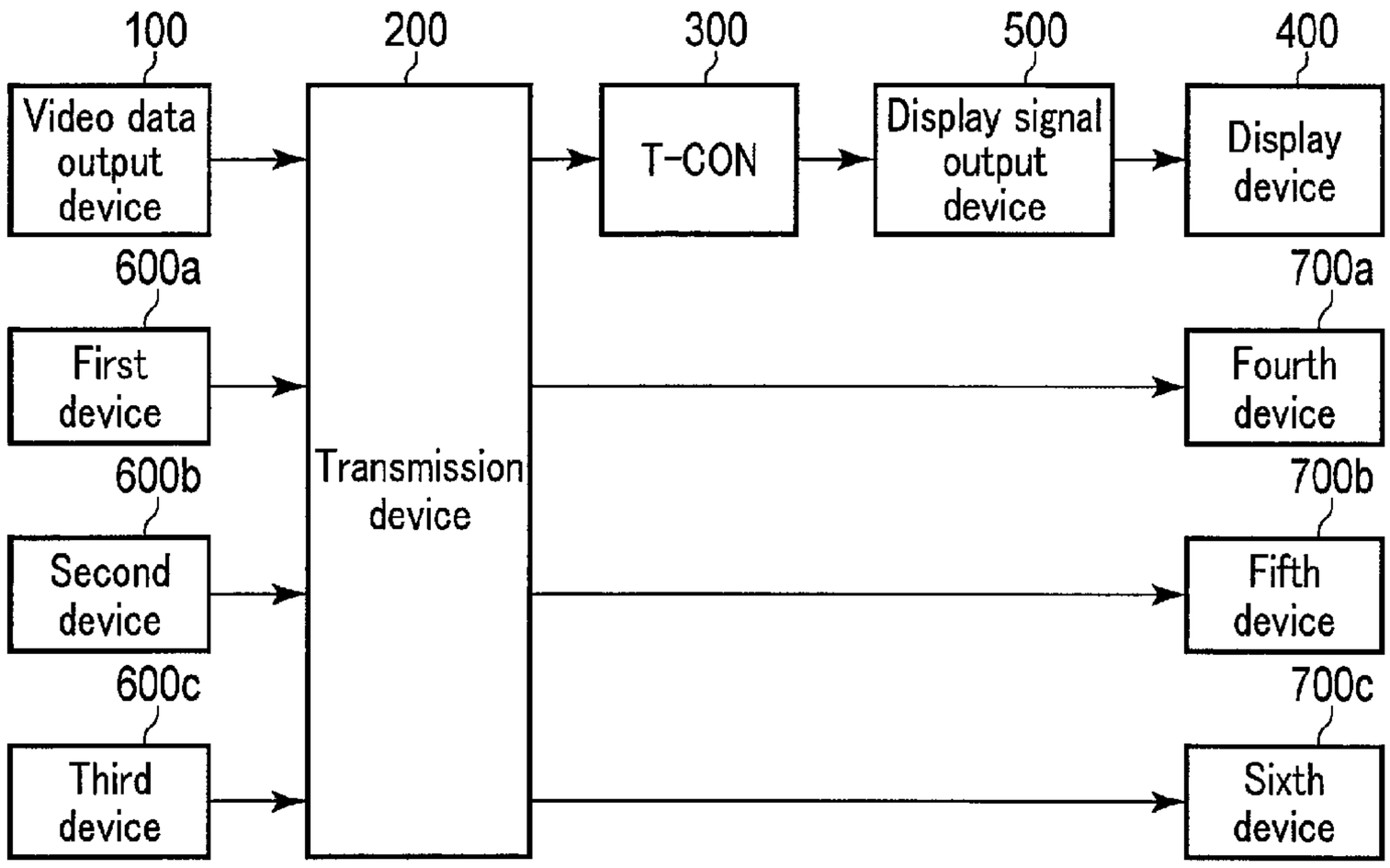

100
Video data output device
200
Transmission device
300
T-CON
500
Display signal output device
400
Display device
600a
First device
600b
Second device
600c
Third device
700a
Fourth device
700b
Fifth device
700c
Sixth device

FIG. 6

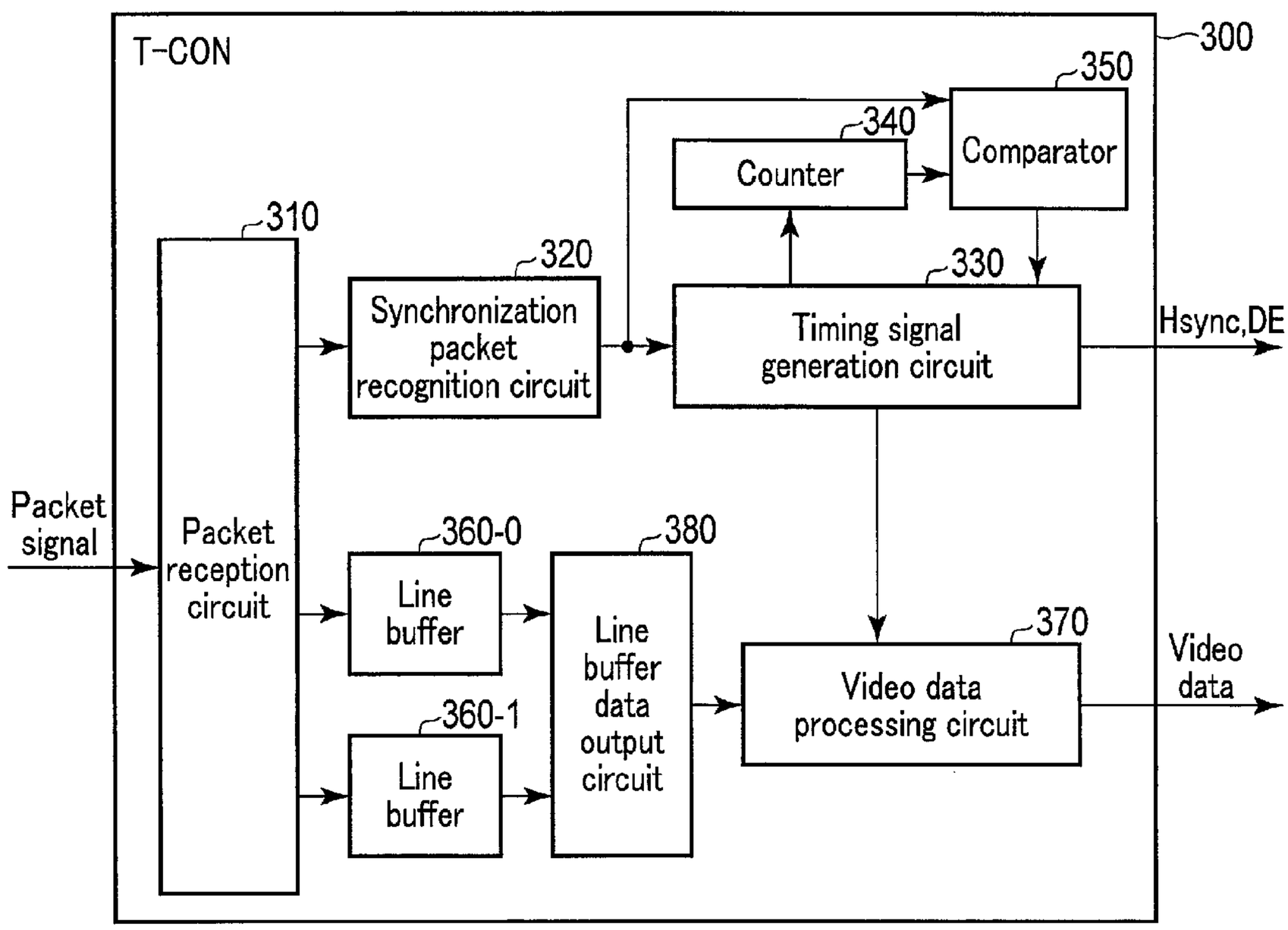

T-CON
300
350
Comparator
340
Counter
310
320
Synchronization packet recognition circuit
330
Timing signal generation circuit
Hsync,DE
Packet signal
Packet reception circuit
360-0
Line buffer
380
Line buffer data output circuit
370
Video data processing circuit
Video data
360-1
Line buffer

FIG. 7

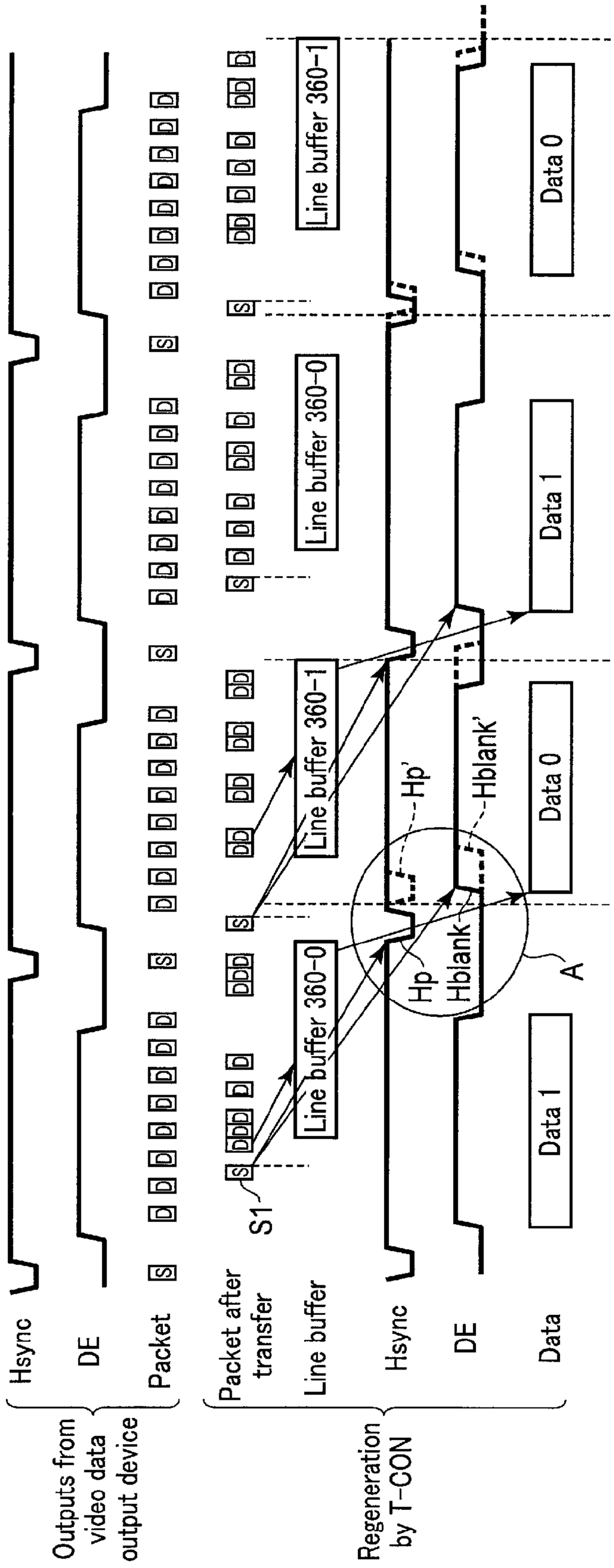

Outputs from video data output device
Hsync
DE
Packet
S
D
Regeneration by T-CON
Line buffer
Packet after transfer
S1
Line buffer 360-0
Line buffer 360-1
Hsync
DE
Data
Data 0
Data 1
Hp
Hblank
Hp'
Hblank'
A

FIG. 8

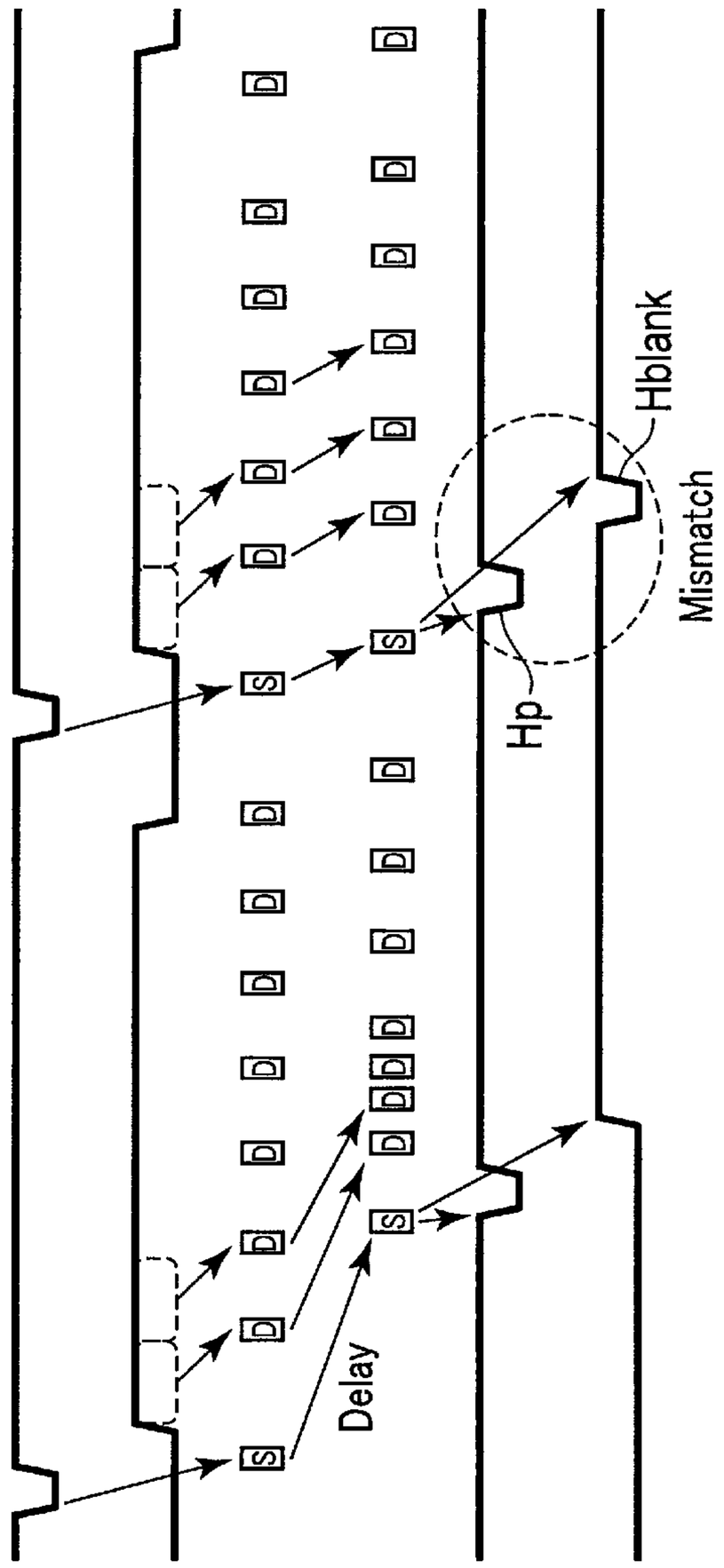

Hblank
Mismatch
Hp
Delay
Hsync
DE
Packet
Outputs from video data output device
Packet
Hsync
DE
Output from transmission device

FIG. 9

VIDEO PROCESSING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2014-197358, filed Sep. 26, 2014, the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a video processing apparatus.

BACKGROUND

In general, a video data output device directly transmits a packet signal based on video data to a display device. An I/F format conversion device or a video data processing device is sometimes arranged between the video data output device and the display device. In any case, a signal is transmitted to the display device at a stable timing complying with constraints of the display device.

Various packet signals are transmitted not only from a video data output device to a display device but also from other devices (hardware) different from the video data output device to other devices different from the display device. In this case, packet signals are transmitted via a common transmission device. The transmission device arbitrates between packet signals to determine from which device transmission is performed to which device.

At this time, packet signals are delayed by the transmission device by inconstant delay amounts (different delay amounts). For this reason, the packet signals based on video data from the video output device are transmitted to the display device upon being delayed by different delay amounts. There is therefore a possibility that video data may become a signal which does not meet the constraints of the display device (which is not accepted by the display device).

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a block diagram showing a video processing apparatus according to the first embodiment;

FIG. **2** is a timing chart showing output signals from a video data output device and regeneration signals by a timing controller according to the first embodiment;

FIG. **3** is a block diagram showing a timing controller according to the first embodiment;

FIG. **4** shows timing charts showing the details of regeneration signals by the timing controller according to the first embodiment;

FIG. **5** is a flowchart showing the operation of the timing controller according to the first embodiment;

FIG. **6** is a block diagram showing a modification of the video processing apparatus according to the first embodiment;

FIG. **7** is a block diagram showing a timing controller according to the second embodiment;

FIG. **8** is a timing chart showing output signals from a video data output device and regeneration signals by a timing controller according to the second embodiment; and

FIG. **9** is a timing chart showing output signals from a video data output device and output signals from a transmission device according to a comparative example.

DETAILED DESCRIPTION

In general, when a video data output device transmits a packet signal, video data and a synchronization signal are reproduced based on the packet signal. At this time, in order to meet the constraints of a display device, each pulse of the synchronization signal needs to be set in a corresponding blanking period of the video data. Blanking period is a period except for effective region of video data signal and L-level period of data enable signal.

As indicated by a comparative example in FIG. **9**, packet signals (synchronization packet signal S and video data packet signals D) from the video data output device are sometimes delayed by a transmission device by different delay amounts. In this case, a data enable signal DE and a synchronization signal Hsync are reproduced from the packet signals delayed by different delay amounts. Since these packet signals have different delay amounts, the data enable signal DE and the synchronization signal Hsync are generated at timings different from those of the original signals.

More specifically, the timing of a pulse Hp (L level) of the synchronization signal Hsync shifts from the timing of a blanking period Hblank (L level) of the data enable signal DE. As a result, the pulse Hp of the synchronization signal Hsync is located in an effective period (H level) of the data enable signal DE. This causes a mismatch in the relationship between the synchronization signal Hsync and the data enable signal DE. These signals therefore do not meet the constraints of the display device.

This embodiment is to solve the above problem by controlling the timing of the pulse Hp of the synchronization signal Hsync and the width of the blanking period Hblank of the data enable signal DE.

In general, according to one embodiment, a video processing apparatus includes a video data output device which outputs a data packet signal obtained by packetizing a data enable signal and a synchronization packet signal obtained by packetizing a synchronization signal, a transmission device which transmits the data packet signal and the synchronization packet signal, the data packet signal being delayed by a first delay amount and the synchronization packet signal being delayed by a second delay amount different from the first delay amount, and a timing controller which generates the data enable signal and the synchronization signal so as to set a pulse of the synchronization signal within a blanking period of the data enable signal based on the data packet signal and the synchronization packet signal.

Embodiments will be described below with reference to the accompanying drawing. Note that the same reference numerals throughout the drawing denote the same parts, and a repetitive description will be made as needed.

First Embodiment

A video processing apparatus according to the first embodiment will be described with reference to FIGS. **1**, **2**, **3**, **4**, **5**, and **6**. In the first embodiment, a timing controller (T-CON) **300** controls the timing of a pulse Hp of a synchronization signal Hsync and the width of a blanking period Hblank of a data enable signal DE. This makes it possible for the timing controller **300** to set the pulse Hp of the synchronization signal Hsync within the blanking period Hblank of the data enable signal DE. It is therefore possible to generate the synchronization signal Hsync and the data enable signal

DE which meet the constraints of a display device **400**. The first embodiment will be described in detail below.

Arrangement of First Embodiment

FIG. **1** is a block diagram showing the video processing apparatus according to the first embodiment. FIG. **2** is a timing chart showing output signals from a video data output device and regeneration signals by a timing controller according to the first embodiment.

The following description will exemplify a horizontal synchronization signal as a synchronization signal. However, a vertical synchronization signal may be the synchronization signal. In addition, the following description will exemplify a horizontal blanking period as a blanking period. However, a vertical blanking period may be the blanking period.

As shown in FIG. **1**, the video processing apparatus includes a video data output device **100**, a transmission device **200**, the timing controller **300**, the display device **400**, first to third devices **600***a* to **600***c*, and fourth to sixth devices **700***a* to **700***c*.

The video data output device **100** is, for example, an application processor. The video data output device **100** outputs packet signals obtained by packetizing the video data enable signal DE (to be simply referred to as the data enable signal DE hereinafter) and the synchronization signal Hsync. The timings of packet signals may or may not be constant.

As shown in FIG. **2**, a packet signal is constituted by a synchronization packet signal S and a data packet signal D. The synchronization packet signal S is a signal obtained by packetizing the pulse Hp of the synchronization signal Hsync. The data packet signal D is a signal obtained by packetizing an effective period (H-level period) of the data enable signal DE.

Note that a conversion device (not shown) may be arranged on the subsequent stage of the video data output device **100**. This conversion device may packetize the data enable signal DE and the synchronization signal Hsync.

As shown in FIG. **1**, the transmission device **200** outputs packet signals from the video data output device **100** to the timing controller **300** while delaying the signals by inconstant delay amounts (different delay amounts).

In addition, the transmission device **200** may arbitrate between various types of packet signals from a plurality of transmission sources (first to third devices **600***a* to **600***c*). For example, the transmission device **200** may select a packet signal from a plurality of transmission sources (first to third devices **600***a* to **600***c*) and determine one of a plurality of transmission destinations (fourth to sixth devices **700***a* to **700***c*) to which the signal is to be transmitted. At this time, various packet signals are output while being delayed by the transmission device **200** by different delay amounts.

The timing controller **300** receives the packet signals delayed by different delay amounts from the transmission device **200**, and converts the format of the signals into a format which allows the display device **400** to receive the signals. More specifically, the timing controller **300** generates (regenerates) and outputs the data enable signal DE and synchronization signal Hsync based on the packet signals delayed by the different delay amounts.

As shown in FIG. **2**, with regard to the data enable signal DE and the synchronization signal Hsync generated by the timing controller **300**, the pulse Hp of the synchronization signal Hsync is set within the blanking period Hblank of the data enable signal DE. The details of the timing controller **300** will be described later.

As shown in FIG. **1**, the display device **400** is, for example, an LCD (Liquid Crystal Display). The display device **400** displays a video based on the data enable signal DE and the synchronization signal Hsync generated by the timing controller **300**. The display device **400** has a constraint concerning a blanking period for an input signal. That is, in the display device **400**, the pulse Hp of the synchronization signal Hsync needs to fall within the blanking period Hblank of the data enable signal DE to display a video.

FIG. **3** is a block diagram showing a timing controller according to the first embodiment.

FIG. **4** shows timing charts showing the details of regeneration signals at the timing controller according to the first embodiment. More specifically, (a) in FIG. **4** is a timing chart showing a regeneration signal when the synchronization packet signal S is located between the Min value and the Max value. In FIG. **4**, (b) is a timing chart showing a regeneration signal when the synchronization packet signal S is earlier than the Min value. In FIG. **4**, (c) is a timing chart showing a regeneration signal when the synchronization packet signal S is later than the Max value. Note that the Min value and the Max value will be described later.

In the first embodiment, as indicated by (b) and (c) in FIG. **4**, when the synchronization packet signal S is earlier than the Min value or later than the Max value, the trailing edge timing of the pulse Hp of the synchronization signal Hsync is controlled as needed. The signals indicated by (a), (b), and (c) in FIG. **4** will be described in detail later.

As shown in FIG. **3**, the timing controller **300** includes a packet reception circuit **310**, a synchronization packet recognition circuit **320**, a timing signal generation circuit **330**, a counter **340**, a comparator **350**, a line buffer **360**, and a video data processing circuit **370**.

The packet reception circuit **310** separates a packet signal from the transmission device **200** into the synchronization signal S and the data packet signal D. The packet reception circuit **310** outputs the synchronization packet signal S to the synchronization packet recognition circuit **320**, and the data packet signal D to the line buffer **360**.

The synchronization packet recognition circuit **320** recognizes whether the synchronization packet signal S from the packet reception circuit **310** is a horizontal synchronization packet signal or a vertical synchronization packet signal. The synchronization packet recognition circuit **320** outputs the synchronization packet signal S to the timing signal generation circuit **330** and the comparator **350**.

The timing signal generation circuit **330** recognizes the timing of the data enable signal DE based on the synchronization packet signal S from the synchronization packet recognition circuit **320**. The timing of the data enable signal DE is recognized based on the synchronization packet signal S (first synchronization packet signal S) which is input before the synchronization packet signal S (second synchronization packet signal S) which will be counted is input. The timing signal generation circuit **330** outputs a control signal to the counter **340** based on the timing of the data enable signal DE. This control signal is a signal for notifying the trailing edge timing of the data enable signal DE.

In addition, the timing signal generation circuit **330** controls the timing of the pulse Hp and the width (time) of the blanking period Hblank in accordance with the control signal (trigger) based on a comparison result from the comparator **350**.

In this case, as indicated by (a), (b), and (c) in FIG. **4**, the blanking period Hblank includes the pulse Hp, a front porch Hfront, and a back porch Hback. The front porch Hfront indicates a period from a trailing edge of the data enable

signal DE to a trailing edge of the synchronization signal Hsync. The back porch Hback is a period from a leading edge of the synchronization signal Hsync and a leading edge of the data enable signal DE. Although the back porch Hback is constant, it need not be constant if the data enable signal DE is present.

The timing signal generation circuit **330** controls the timing of the pulse Hp with reference to the Min value or Max value of the blanking period Hblank.

The Min value of the blanking period Hblank indicates the termination time point in the minimum time of a period (front porch Hfront) from a trailing edge of the data enable signal DE and a trailing edge of the synchronization signal Hsync. The Max value of the blanking period Hblank indicates the termination time point in the maximum time of the front porch Hfront.

The Min value and Max value of the blanking period Hblank are set in advance based on the specifications of the display device **400**. More specifically, the Min value is set so as not to violate the constraints of the blanking period Hblank of the display device **400**. That is, the Min value is set so that the pulse Hp be to fall within the blanking period Hblank with a sufficient margin. In addition, the Min value and the Max value are set so as to suppress variations in the cycle (one horizontal cycle) of the synchronization signal Hsync. The Min value and the Max value are set by a setting register (not shown) in, for example, an application processor (video data output device).

If the input timing of the synchronization packet signal S is earlier than the Min value of the blanking period Hblank, the timing of the pulse Hp is forcibly set at the timing of the Min value. In contrast to this, if the input timing of the synchronization packet signal S is later than the Max value of the blanking period Hblank, the timing of the pulse Hp is forcibly set at the timing of the Max value.

In FIG. **4**, (a), (b), and (c) exemplify timing control on the pulse Hp when the Min value and Max value of the front porch Hfront are respectively "5" and "17".

As indicated by (a) in FIG. **4**, if the count value ("9") of the synchronization packet signal S is equal to or more the Min value and equal to or less than the Max value, the comparator **350** outputs a trigger at the input timing of the synchronization packet signal S. That is, the timing signal generation circuit **330** sets the pulse Hp of the synchronization signal Hsync at the input timing of the synchronization packet signal S.

As indicated by (b) in FIG. **4**, if the count value ("3") of the synchronization packet signal S is less the Min value, the comparator **350** outputs a trigger at the input timing of the Min value. That is, the timing signal generation circuit **330** sets the pulse Hp of the synchronization signal Hsync at the timing of the Min value.

As indicated by (c) in FIG. **4**, if the count value ("19") of the synchronization packet signal S is more than the Max value, the comparator **350** outputs a trigger at the timing of the Max value. That is, the timing signal generation circuit **330** sets the pulse Hp of the synchronization signal Hsync at the timing of the Max value without waiting for the synchronization packet signal S. In this case, the first synchronization packet signal S after this timing is discarded.

In this manner, the timing signal generation circuit **330** forcibly controls the timing of the pulse Hp with reference to the Min value or Max value of the blanking period Hblank when the synchronization packet signal S exceeds them. Along with the timing of the pulse Hp, the width of the front porch Hfront of the blanking period Hblank is determined. In addition, the width of the pulse Hp and the width of the back porch Hback are constant. Therefore, the width of the blanking period Hblank is determined along with the timing of the pulse Hp. In this manner, the timing signal generation circuit **330** generates the synchronization signal Hsync, with the timing of the pulse Hp being controlled, and the data enable signal DE, with the width of the blanking period Hblank being controlled.

As shown in FIG. **3**, the counter **340** starts counting based on a control signal from the timing signal generation circuit **330**. More specifically, as indicated by (a) and (b) in FIG. **4**, the counter **340** counts with reference to a trailing edge of the data enable signal DE. The counter **340** outputs the count to the comparator **350**.

As shown in FIG. **3**, the comparator **350** compares the count from the counter **340** with the reception timing of the synchronization packet signal S from the synchronization packet recognition circuit **320**. With this operation, the comparator **350** measures a count value at the reception timing of the synchronization packet signal S. This count value indicates the reception timing of the synchronization packet signal S with reference to a trailing edge of the data enable signal DE. The comparator **350** compares the count value at the reception timing of the synchronization packet signal S with the Min value and Max value of the blanking period Hblank (front porch Hfront). The comparator **350** outputs a control signal (trigger) corresponding to the comparison result to the timing signal generation circuit **330**.

As shown in FIG. **3**, the line buffer **360** temporarily stores the data packet signal D from the packet reception circuit **310** and outputs the packet to the video data processing circuit **370**.

The video data processing circuit **370** processes the data packet signal D from the line buffer **360** as video data. The video data processing circuit **370** outputs the video data based on the data enable signal DE whose timing is controlled by the timing signal generation circuit **330**.

Operation in First Embodiment

FIG. **5** is a flowchart showing the operation of the timing controller according to the first embodiment.

As shown in FIG. **5**, first of all, in step S**1**, the packet reception circuit **310** receives a packet signal.

In step S**2**, the timing signal generation circuit **330** recognizes the timing of the data enable signal DE based on the synchronization packet signal S.

In step S**3**, the counter **340** starts counting based on the timing of the data enable signal DE. More specifically, the counter **340** starts counting from the trailing edge timing of the data enable signal DE.

In step S**4**, the comparator **350** measures the count value of the reception timing of the synchronization packet signal S. This count value is obtained by comparing the count obtained by the counter **340** with the reception timing of the synchronization packet signal S.

In step S**5**, the comparator **350** compares the count value at the reception timing of the synchronization packet signal S with the Min value and Max value of the blanking period Hblank (front porch Hfront).

If it is determined in step S**5** that the count value is smaller than the Min value, the timing signal generation circuit **330** sets the pulse Hp at the timing of the Min value in step S**6**. If it is determined in step S**5** that the count value is equal to or more than the Min value and equal to or less than the Max value, the timing signal generation circuit **330** sets the pulse Hp at the input timing of the synchronization packet signal S in step S**7**. In addition, if it is determined in step S**5** that the

count value is larger than the Max value, the timing signal generation circuit **330** sets the pulse Hp at the timing of the Max value in step S**7**.

Effects in First Embodiment

According to the first embodiment described above, the timing controller **300** controls the timing of the pulse Hp of the synchronization signal Hsync and the width of the blanking period Hblank of the data enable signal DE. This enables the timing controller **300** to set the pulse Hp of the synchronization signal Hsync within the blanking period Hblank of the data enable signal DE. Therefore, it is possible to generate the synchronization signal Hsync and the data enable signal DE which meet the constraints of the display device **400**.

At this time, controlling the Min value of the blanking period Hblank makes it possible to generate the synchronization signal Hsync and the data enable signal DE which meet the constraints of the display device **400**. In addition, controlling also the Max value of the blanking period Hblank makes it possible to suppress variations in the cycle (one horizontal cycle) of the synchronization signal Hsync. This enables the display device **400** to perform stable display.

Modification of First Embodiment

FIG. **6** is a block diagram showing a modification of the video processing apparatus according to the first embodiment. The difference between the modification and the above embodiment will be mainly described.

As shown in FIG. **6**, the video processing apparatus includes a display signal output device **500**.

The display signal output device **500** converts output signals from the timing controller **300** into signals in various formats, and outputs the signals to the display device **400**. The display signal output device **500** converts an input signal into a signal in a format such as the DSI (Display Serial Interface), LVDS (Low Voltage Differential Signaling), or eDP (Embedded Display Port) format. This enables the video processing apparatus to cope with various signal formats.

Second Embodiment

A video processing apparatus according to the second embodiment will be described with reference to FIGS. **7** and **8**. According to the second embodiment, a timing controller **300** includes a first line buffer **360_0** and a second line buffer **360_1**. The data packet signals D are alternately stored in the first line buffer **360_0** and the second line buffer **360_1** in an arbitrary unit, and are alternately output. This can suppress the exhaustion of reception data at the time of data transfer. The second embodiment will be described in detail below.

Note that only differences between the second embodiment and the first embodiment will be mainly described while a description of parts similar to the first embodiment will be omitted.

Arrangement of Second Embodiment

FIG. **7** is a block diagram showing a timing controller according to the second embodiment. FIG. **8** is a timing chart showing output signals from a video data output device and regeneration signals at the timing controller according to the second embodiment.

As shown in FIG. **7**, the timing controller **300** includes the first line buffer **360_0**, the second line buffer **360_1**, and a line buffer data output circuit **380**.

The first line buffer **360_0** and the second line buffer **360_1** temporarily store data packet signals D from the packet reception circuit **310**, and output the signals to the line buffer data output circuit **380**. The line buffer data output circuit **380** alternately outputs data from the first line buffer **360_0** and the second line buffer **360_1**. The data packet signals D are alternately stored in the first line buffer **360_0** and the second line buffer **360_1** in an arbitrary unit, and are alternately output.

As shown in FIG. **8**, the first line buffer **360_0** and the second line buffer **360_1** store, for example, data corresponding to about one horizontal cycle and then output the data. In addition, while data **0** stored in the first line buffer **360_0** is output, data **1** is stored in the second line buffer **360_1**. While data **0** stored in the second line buffer **360_1** is output, new data **0** is stored in the first line buffer **360_0**.

In this case, (A) in FIG. **8** indicates a case in which the count value of a synchronization packet signal S**1** is larger than the Max value, and a pulse Hp of a synchronization signal Hsync is set at the timing of the Max value without waiting for the synchronization packet signal S**1**. That is, the pulse Hp is set at a timing earlier than that of a pulse Hp' which is the normal timing based on the synchronization packet signal S**1**. Along with this setting, the timing of the termination of a blanking period Hblank (a leading edge of a data enable signal DE) is earlier than that of the termination of a normal blanking period Hblank'.

According to the second embodiment, thereafter, data **0** in the first line buffer **360_0**, which has already been stored, is output at a leading edge timing of the blanking period Hblank. That is, this can suppress the exhaustion of reception data at the time of data transfer.

Although the two line buffers, namely the first line buffer **360_0** and the second line buffer **360_1** have been described above, three or more line buffers may be used.

Effects in Second Embodiment

In the first embodiment, if the count value of the synchronization packet signal S is larger than the Max value, the pulse Hp of the synchronization signal Hsync is set at the timing of the Max value without waiting for the synchronization packet signal S ((c) in FIG. **4**). Along with this setting, the back porch Hback is set as a constant value. That is, the data enable signal DE may rise before the synchronization packet signal S after the pulse Hp and the subsequent data packet signal D are received. This causes a problem in data transfer (exhaustion of reception data) because there is no data which can be received.

In contrast to this, according to the second embodiment, the timing controller **300** includes the first line buffer **360_0** and the second line buffer **360_1**. The data packet signals D are alternately stored in the first line buffer **360_0** and the second line buffer **360_1** and are alternately output. More specifically, while data **0** stored in the first line buffer **360_0** is output, data **1** is stored in the second line buffer **360_1**. Subsequently, while data **1** stored in the second line buffer **360_1** is output, new data **0** is stored in the first line buffer **360_0**. That is, data on the next line is stored in the line buffer in advance. This can suppress exhaustion of reception data at the time of data transfer.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the

embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A video processing apparatus comprising:

a video data output device which outputs a data packet signal obtained by packetizing a data enable signal and a synchronization packet signal obtained by packetizing a synchronization signal;

a transmission device which transmits the data packet signal and the synchronization packet signal, the data packet signal being delayed by a first delay amount and the synchronization packet signal being delayed by a second delay amount different from the first delay amount;

a timing controller which generates the data enable signal and the synchronization signal so as to set a pulse of the synchronization signal within a blanking period of the data enable signal based on the data packet signal and the synchronization packet signal; and

a display device which displays a video based on the data enable signal and the synchronization signal generated by the timing controller.

2. The apparatus of claim **1**, wherein the timing controller comprises:

a counter which starts to count based on the data enable signal;

a comparator which compares a count value of an input of the synchronization packet signal obtained by the counter with a count value corresponding to a Min value and a count value corresponding to a Max value in the blanking period; and

a timing signal generation circuit which generates the data enable signal and the synchronization signal so as to set a pulse of the synchronization signal within a blanking period of the data enable signal in accordance with a comparison result obtained by the comparator.

3. The apparatus of claim **2**, wherein the timing signal generation circuit sets a pulse of the synchronization signal at a reception timing of the synchronization packet signal when the count value of an input of the synchronization packet signal is not less than the count value corresponding to the Min value and not more than the count value corresponding to the Max value,

sets a pulse of the synchronization signal at a timing of the count value corresponding to the Min value when the count value of the input of the synchronization packet signal is smaller than the count value corresponding to the Min value, and

sets a pulse of the synchronization signal at a timing of the count value corresponding to the Max value when the count value of the input of the synchronization packet signal is larger than the count value corresponding to the Max value.

4. The apparatus of claim **3**, wherein when the count value of the input of the synchronization packet signal is larger than the count value corresponding to the Max value, the synchronization packet signal is discarded.

5. The apparatus of claim **2**, wherein the counter starts counting with reference to a trailing edge of the data enable signal.

6. The apparatus of claim **1**, wherein the synchronization signal comprises a horizontal synchronization signal, and the blanking period comprises a horizontal blanking period.

7. The apparatus of claim **1**, wherein the synchronization signal comprises a vertical synchronization signal, and the blanking period comprises a vertical blanking period.

8. The apparatus of claim **1**, wherein the timing controller further comprises a first line buffer and a second line buffer configured to alternately store the data packet signals from the video data output device and alternately output the data packet signals.

9. The apparatus of claim **8**, wherein while the first line buffer outputs a first data packet signal of the data packet signals, the second line buffer stores a second data packet signal of the data packet signals different from the first data packet signal.

10. The apparatus of claim **1**, wherein the video data output device comprises an application processor.

11. The apparatus of claim **1**, wherein the transmission device selects and receives a packet signal from any one of a plurality of transmission source devices, selects any one of a plurality of transmission destination devices, and transmits the packet signal.

12. The apparatus of claim **1**, further comprising a display signal output device configured to convert formats of the data enable signal and the synchronization signal from the timing controller and output the data enable signal and the synchronization signal to the display device.

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