US009270506B2

(12) **United States Patent**
Hollis

(10) **Patent No.: US 9,270,506 B2**
(45) **Date of Patent: Feb. 23, 2016**

(54) **METHODS FOR BYPASSING FAULTY CONNECTIONS**

(71) Applicant: **MICRON TECHNOLOGY, INC.**, Boise, ID (US)

(72) Inventor: **Timothy M. Hollis**, Poway, CA (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/308,122**

(22) Filed: **Jun. 18, 2014**

(65) **Prior Publication Data**

US 2014/0301499 A1 Oct. 9, 2014

Related U.S. Application Data

(62) Division of application No. 13/588,728, filed on Aug. 17, 2012, now Pat. No. 8,792,247, which is a division of application No. 12/323,241, filed on Nov. 25, 2008, now Pat. No. 8,259,461.

(51) **Int. Cl.**

H04L 25/49	(2006.01)
H04L 1/22	(2006.01)
G11C 5/02	(2006.01)
H01L 21/66	(2006.01)
H01L 25/065	(2006.01)
H04L 25/02	(2006.01)
H04L 27/02	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H04L 25/4917*** (2013.01); ***G11C 5/02*** (2013.01); ***H01L 22/22*** (2013.01); ***H01L 25/0657*** (2013.01); ***H04L 1/22*** (2013.01); ***H04L 25/0264*** (2013.01); *H01L 23/481* (2013.01); *H01L 2225/06541* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC G06F 11/1402; H01L 25/0657; H01L 2225/06527; G11C 7/1051; G11C 7/18; H03K 19/0002; H04L 25/0272; H04L 25/4917

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,949,242	A	4/1976	Hirasawa et al.
4,038,564	A	7/1977	Hakata
4,205,203	A	5/1980	Mehta et al.

(Continued)

OTHER PUBLICATIONS

A. W. Topol et al., "Three-dimensional integrated circuits", Jul./Sep. 2006, IBM J. Res. & Dev., vol. 50, No. 4/5, pp. 491-506.*

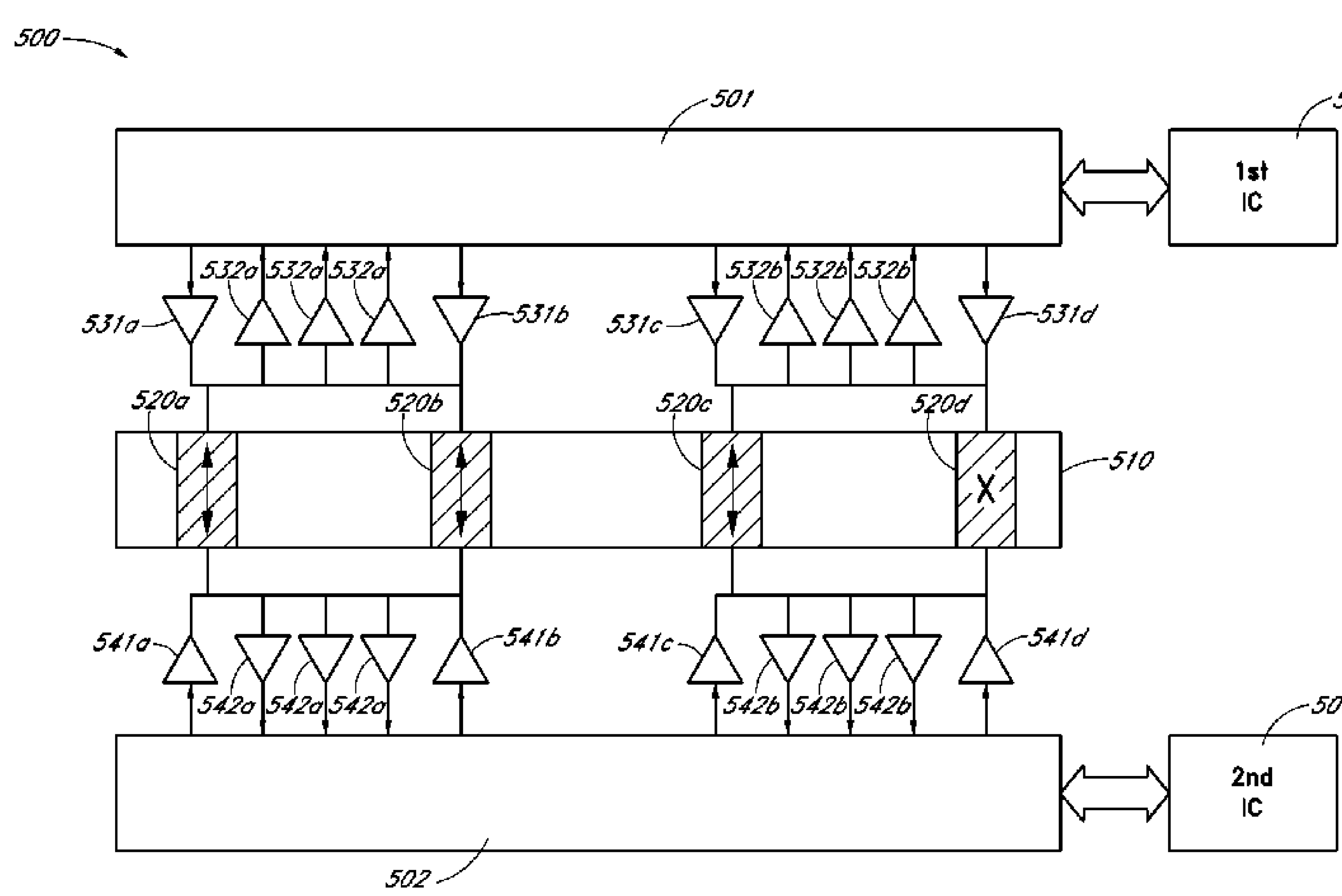
(Continued)

Primary Examiner — Chieh M Fan
Assistant Examiner — Michelle M Koeth
(74) *Attorney, Agent, or Firm* — Dorsey & Whitney LLP

(57) **ABSTRACT**

Apparatus are disclosed, such as those involving a 3-D integrated circuit. One such apparatus includes a first die including a plurality of vertical connectors formed therethrough. The apparatus also includes a first circuit configured to encode multiple data bits into a multi-bit symbol, and provide the multi-bit symbol to two or more of the vertical connectors. The apparatus further includes a second circuit configured to receive the multi-bit symbol from at least one of the two or more vertical connectors, and decode the multi-bit symbol into the multiple data bits. The apparatus provides enhanced repairability with no or less redundant vertical connectors, thus avoiding the need for "on the fly" or field repair of defective vertical connectors.

16 Claims, 10 Drawing Sheets



(51) **Int. Cl.**

G06F 11/20	(2006.01)
H01L 23/48	(2006.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,408,135	A	10/1983	Yuyama et al.	
5,048,022	A	9/1991	Bissett et al.	
5,056,015	A	10/1991	Baldwin et al.	
5,266,833	A	11/1993	Capps	
5,327,426	A	7/1994	Dolin et al.	
5,382,847	A	1/1995	Yasuda	
5,428,754	A	6/1995	Baldwin	
5,502,333	A *	3/1996	Bertin et al.	257/685
5,745,003	A	4/1998	Wakimoto et al.	
5,991,163	A *	11/1999	Marconi et al.	361/788
6,097,519	A	8/2000	Ford et al.	
6,133,626	A	10/2000	Hawke et al.	
6,137,849	A	10/2000	Humphrey	
6,140,841	A	10/2000	Suh	
6,292,014	B1	9/2001	Hedberg	
6,339,622	B1	1/2002	Kim	
6,438,178	B1	8/2002	Lysdal et al.	
6,486,549	B1	11/2002	Chiang	
6,646,472	B1	11/2003	Trivedi et al.	
6,772,351	B1	8/2004	Werner et al.	
6,794,899	B2	9/2004	Little et al.	
6,861,737	B1	3/2005	Jeong et al.	
7,053,655	B2	5/2006	Brox	
7,072,415	B2	7/2006	Zerbe et al.	
7,113,417	B2	9/2006	Pochmuller	
7,206,876	B2	4/2007	Jang	
7,349,488	B1 *	3/2008	Margolese et al.	375/272
7,729,151	B2	6/2010	Tsern et al.	
8,026,740	B2	9/2011	Hollis	
8,259,461	B2	9/2012	Hollis	
8,792,247	B2	7/2014	Hollis	
2003/0047798	A1	3/2003	Halahan	
2003/0095606	A1	5/2003	Horowitz et al.	
2004/0114854	A1	6/2004	Ouchi	
2005/0051903	A1	3/2005	Ellsberry et al.	
2005/0088314	A1	4/2005	O'Toole et al.	
2005/0098868	A1	5/2005	Chang et al.	
2005/0108459	A1	5/2005	Pochmuller	
2005/0170600	A1	8/2005	Fukuzo	
2006/0019484	A1	1/2006	Chen et al.	
2006/0071316	A1	4/2006	Garth	
2007/0070669	A1	3/2007	Tsern	
2007/0153618	A1	7/2007	Fujito et al.	
2007/0194426	A1	8/2007	Hsu	
2008/0029870	A1	2/2008	Chen et al.	
2008/0036050	A1	2/2008	Lin et al.	
2008/0036082	A1	2/2008	Eun	
2008/0048832	A1	2/2008	O'Toole et al.	
2008/0082878	A1	4/2008	Check et al.	
2008/0143379	A1	6/2008	Norman	
2008/0157318	A1	7/2008	Chow et al.	
2008/0260075	A1 *	10/2008	Waters et al.	375/341
2009/0102037	A1	4/2009	Kim	
2009/0161402	A1	6/2009	Oh et al.	
2009/0168855	A1	7/2009	Balamurugan et al.	

OTHER PUBLICATIONS

A. W. Topoi et al., "Three-dimensional integrated circuits", Jul./Sep. 2006, IBM J. Res. & Dev., vol. 50, No. 4/5, pp. 491-506.*

U.S. Appl. No. 12/053,265, filed Mar. 21, 2008.

Farzan et al., "A CMOS 10-Gb/s power-efficient 4-PAM transmitter," *IEEE Journal of Solid-State Circuits*, vol. 39, No. 3, pp. 529-532 (Mar. 2004).

Farjad-Rad et al., "An equalization scheme for 10Gb/s 4-PAM signaling over long cables," *Center for Integrated System, Stanford University, Mixed Signal Conference*, Jul. 1997, Cancun, Mexico, 4 pages.

Farjad-Rad et al., "A 0.4μm CMOS 10-Gb/s 4-PAM pre-emphasis serial link transmitter," *IEEE VLSI Symposium* 1998, 2 pages.

Zerbe et al.,"1.6 Gb/s/pin 4-PAM signaling and circuits for a multi-drop bus," *Symposium on VLSI Circuits Digest of Technical Papers*, vol. 10, No. 2, pp. 128-131 (2000).

Zerbe et al., "Equalization and Clock Recovery for a 2.5-10Gb/s 2-PAM/4-PAM/ backplane transceiver cell," *IEEE International Solid-State Circuits Conference*, ISSCC 2003 / Session 4 / Clock Recovery and Backplane transceivers / Paper 4.6 (2003).

* cited by examiner

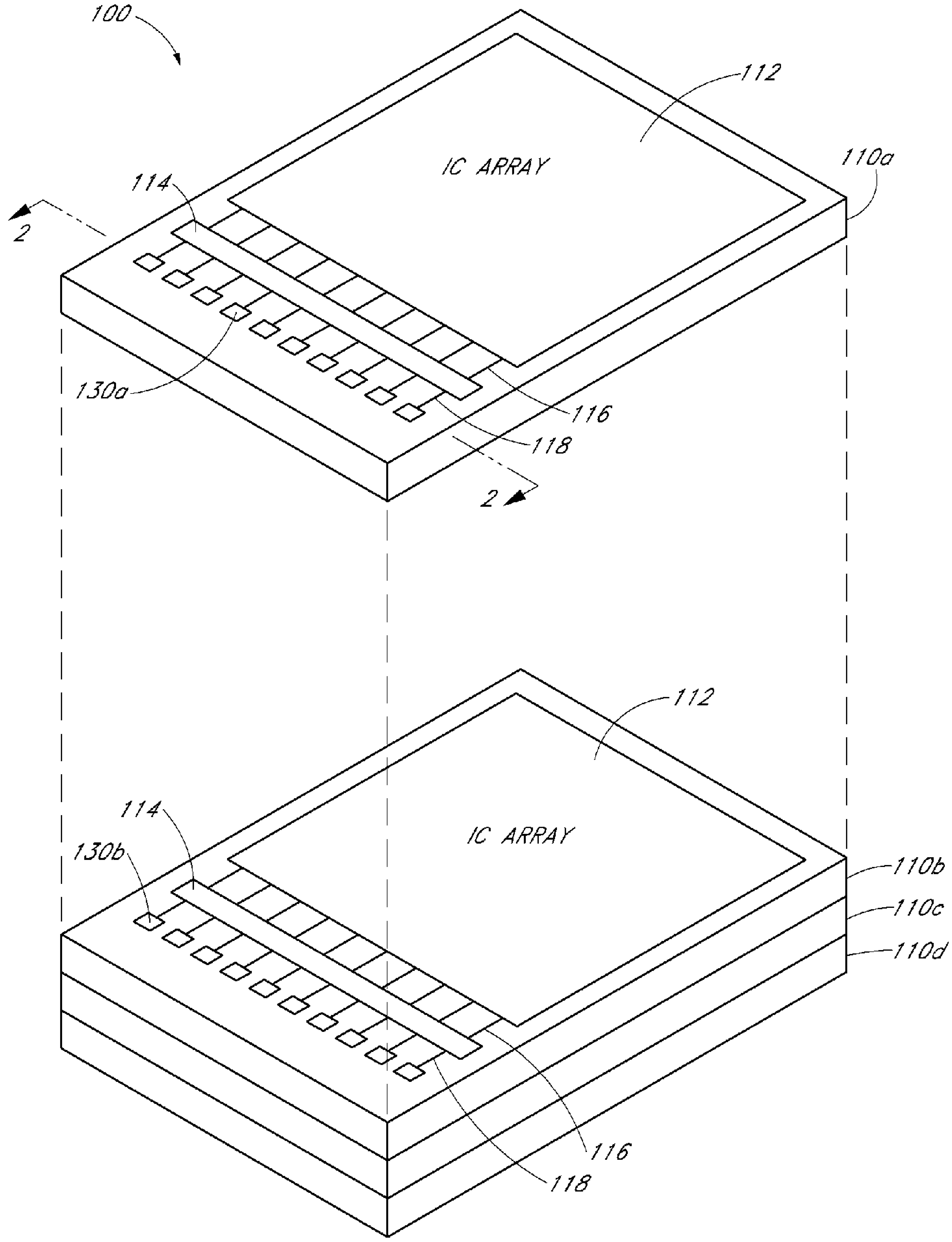


FIG. 1
(PRIOR ART)

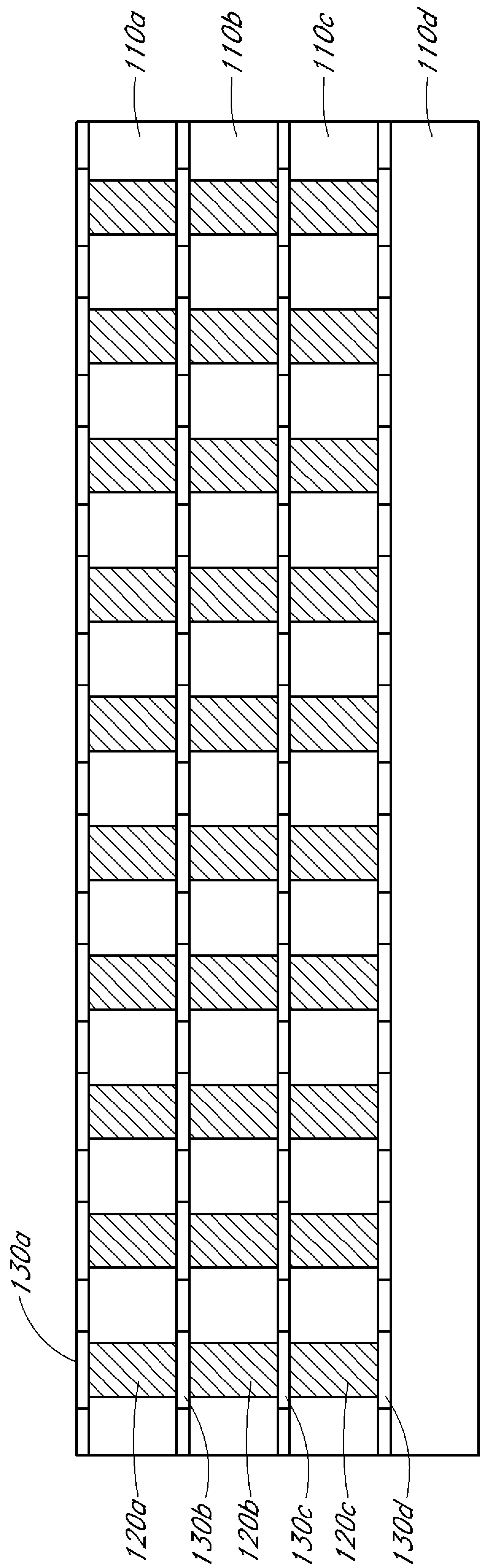


FIG. 2
(PRIOR ART)

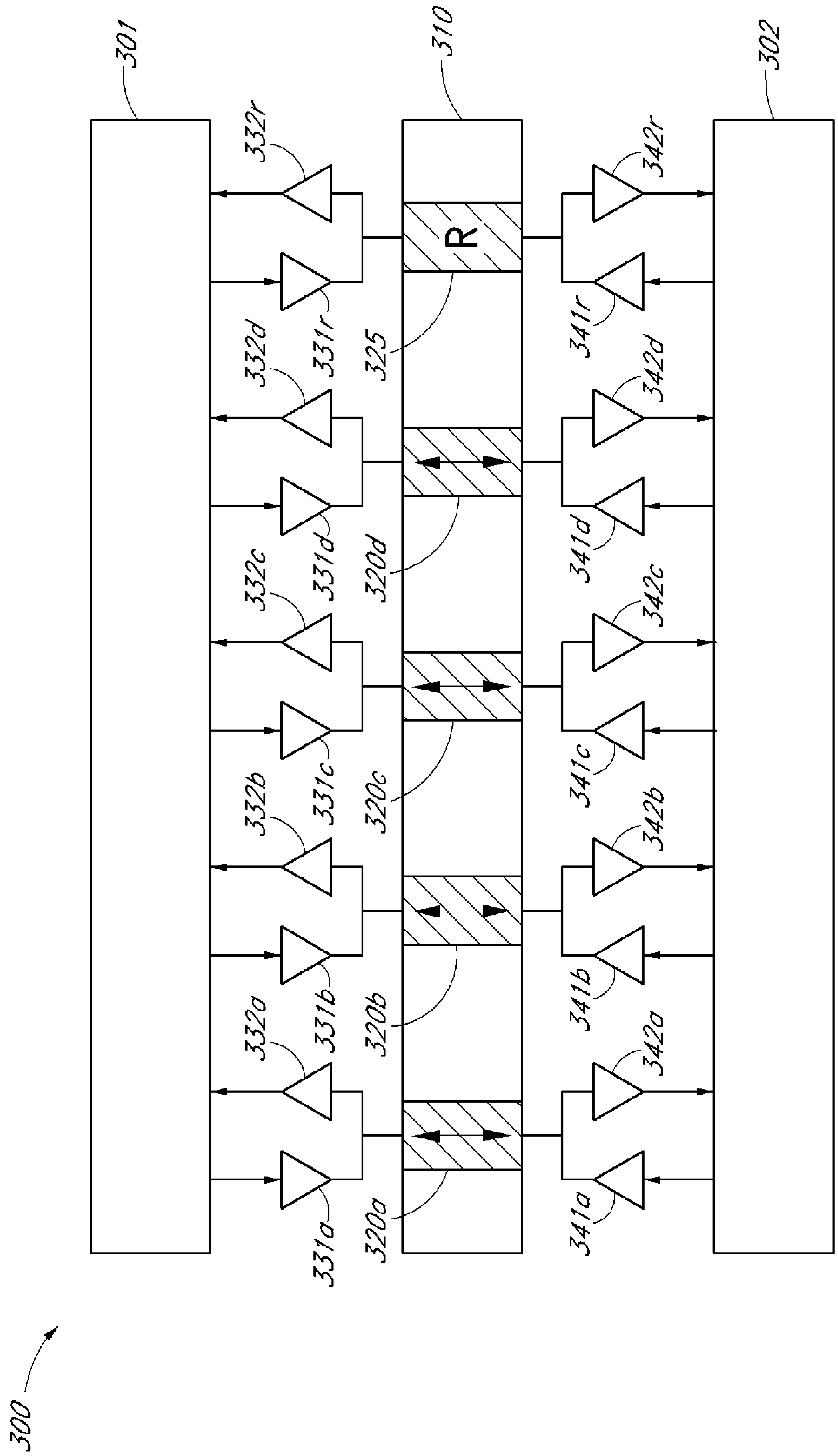


FIG. 3A
(PRIOR ART)

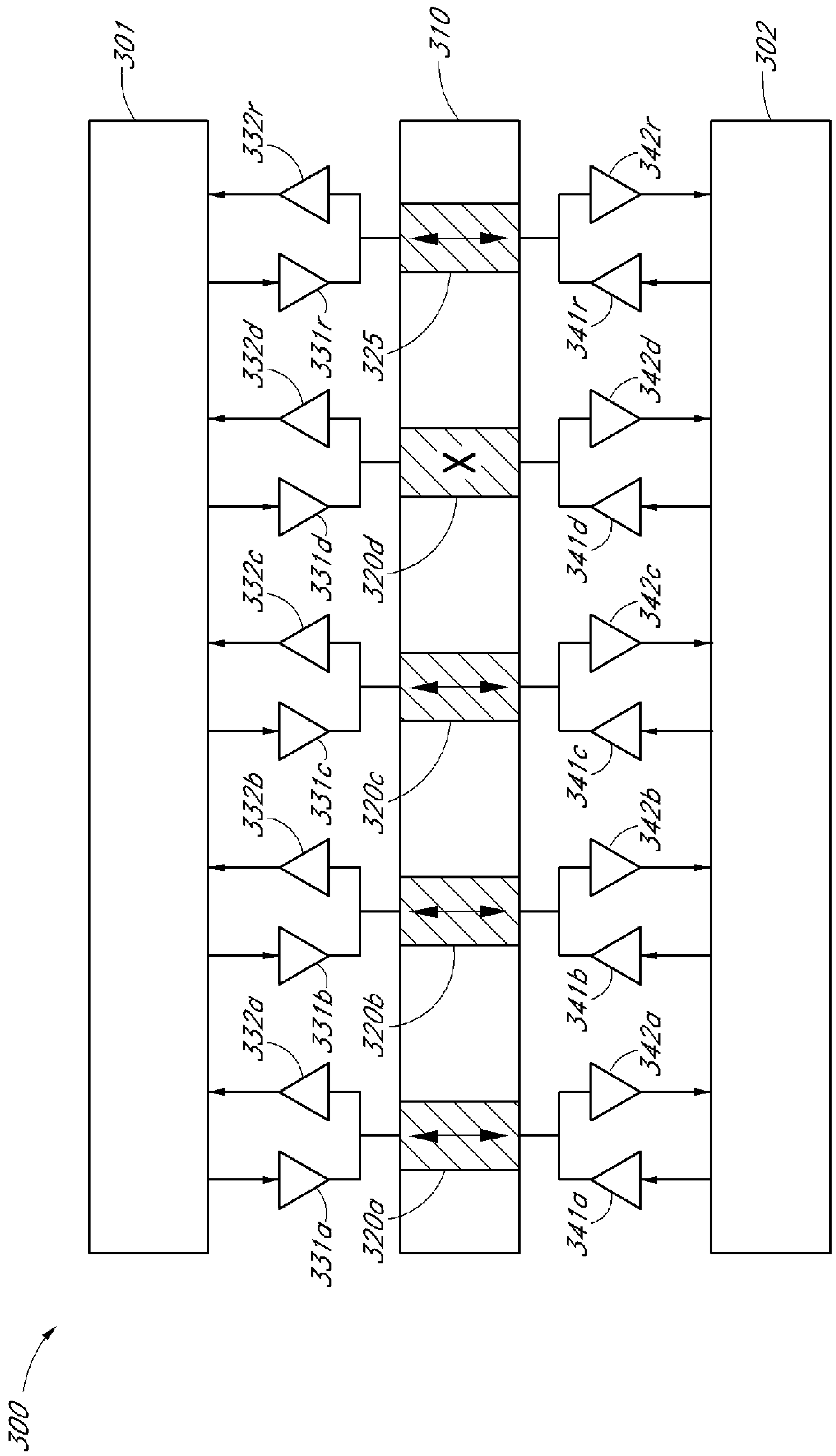


FIG. 3B
(PRIOR ART)

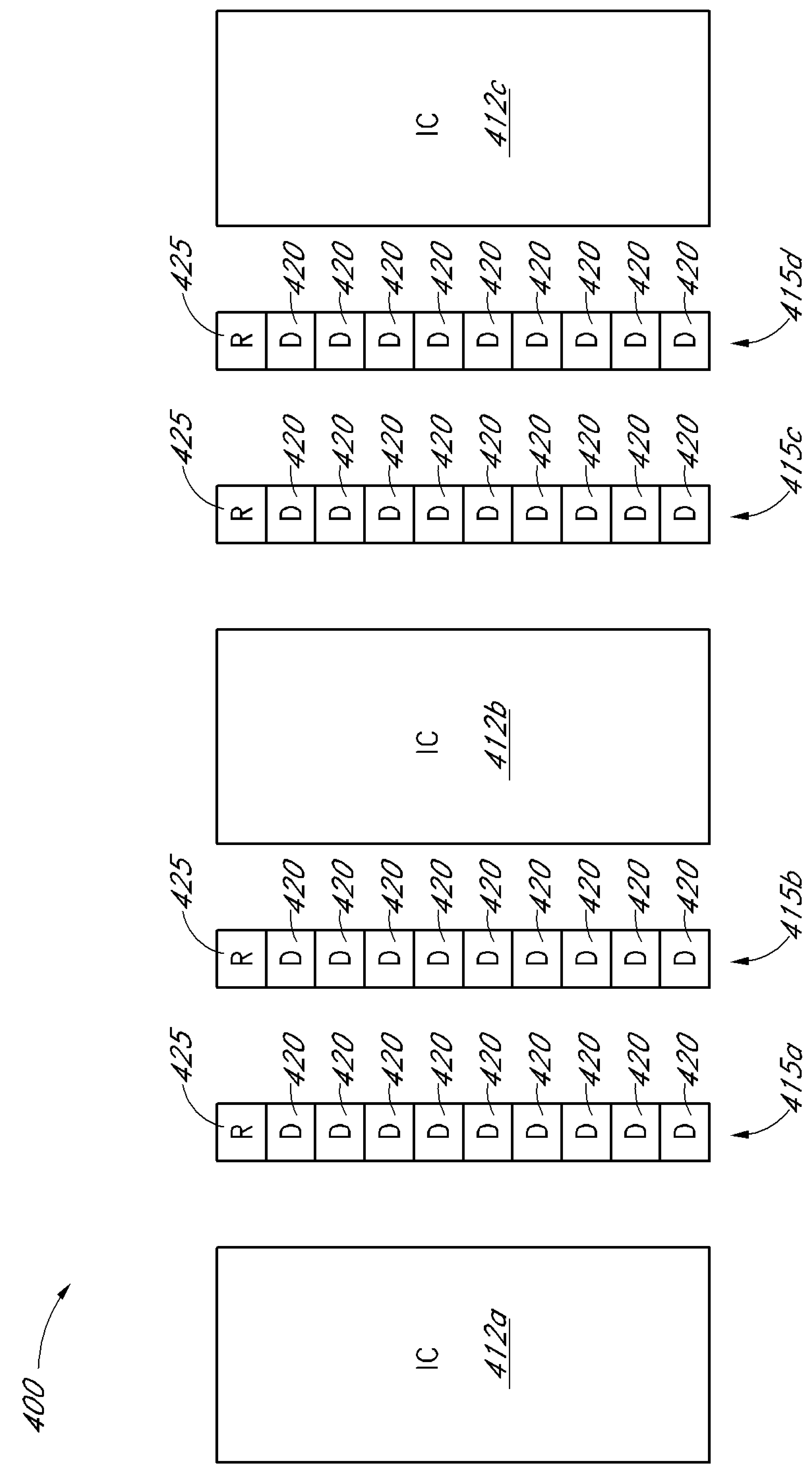
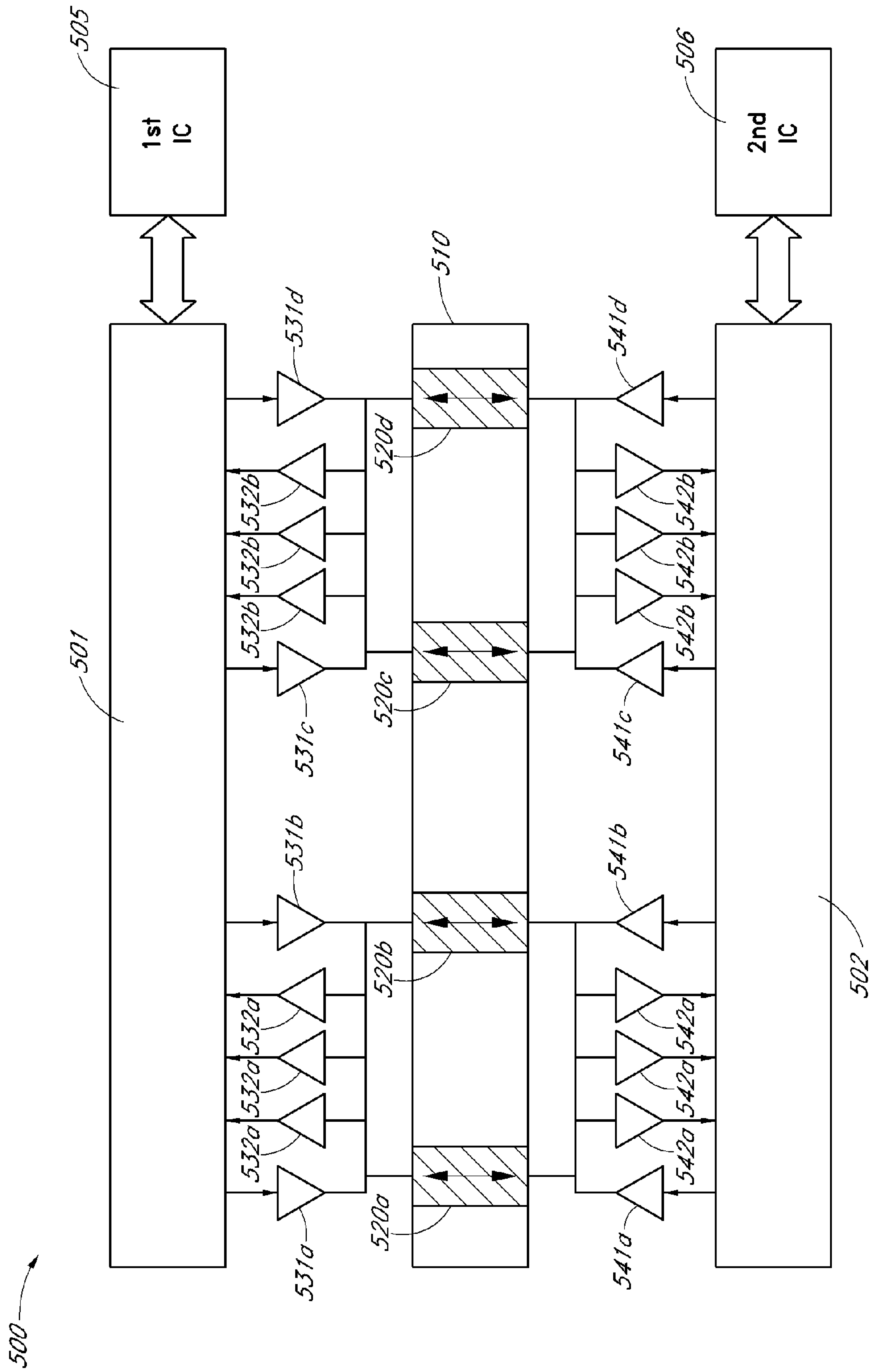


FIG. 4
(PRIOR ART)



505
1st IC
506
2nd IC
510
501
502
531a
531b
531c
531d
532a
532b
520a
520b
520c
520d
541a
541b
541c
541d
542a
542b
500

FIG. 5A

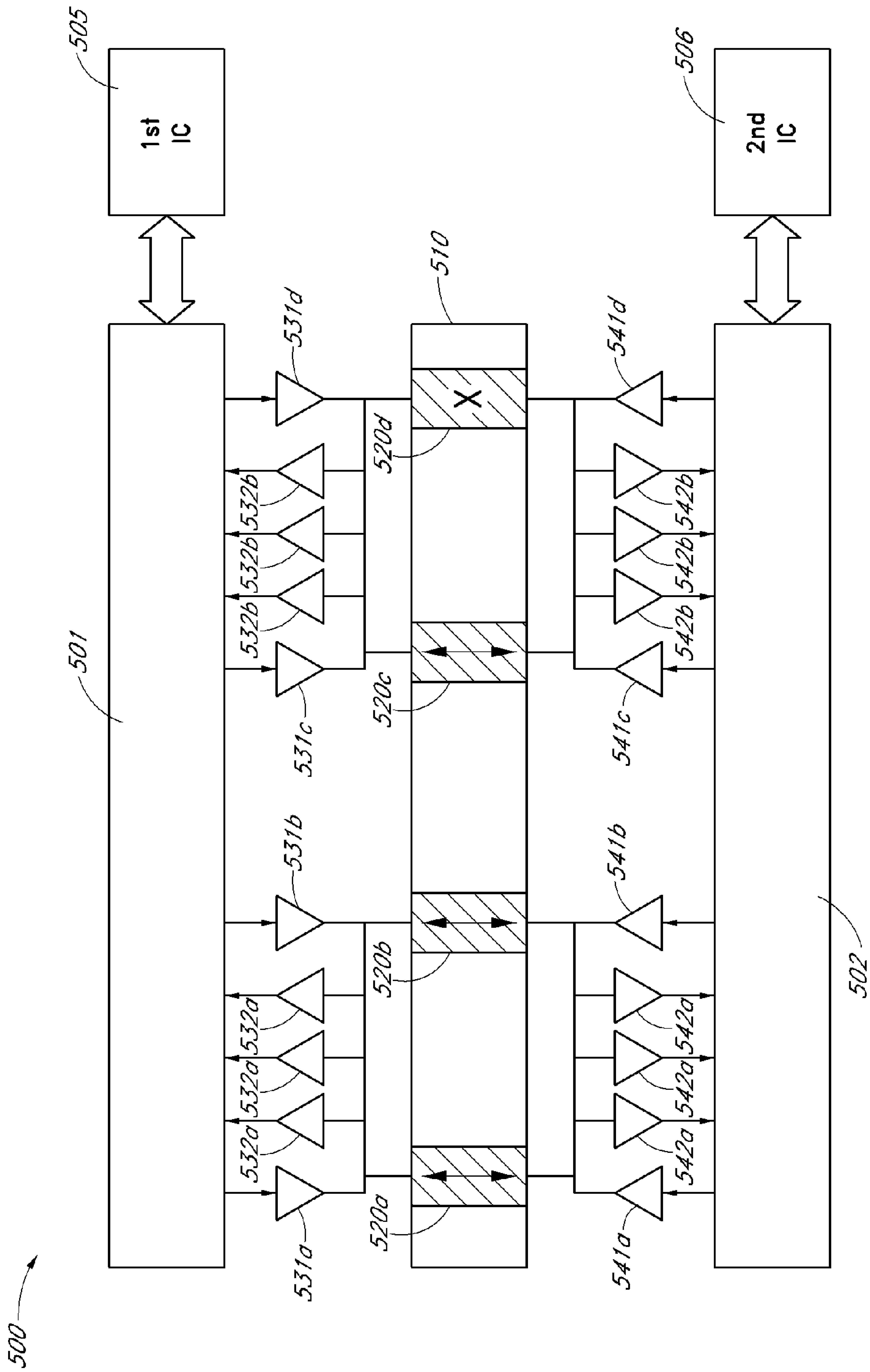

505
1st IC
506
2nd IC
510
531d
541d
X
520d
532b
532b
532b
542b
542b
542b
501
520c
531c
541c
531b
541b
520b
532a
532a
532a
542a
542a
542a
502
520a
531a
541a
500

FIG. 5B

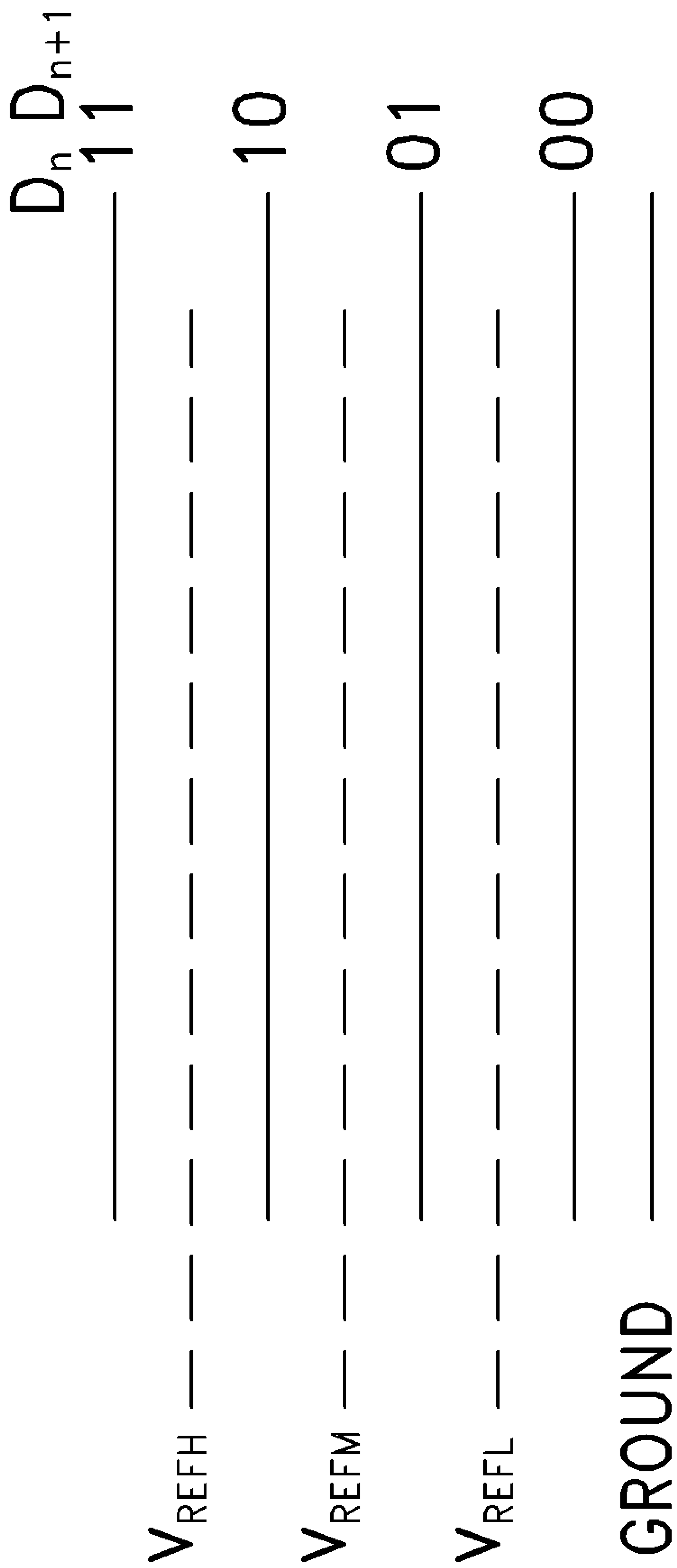


FIG. 6A

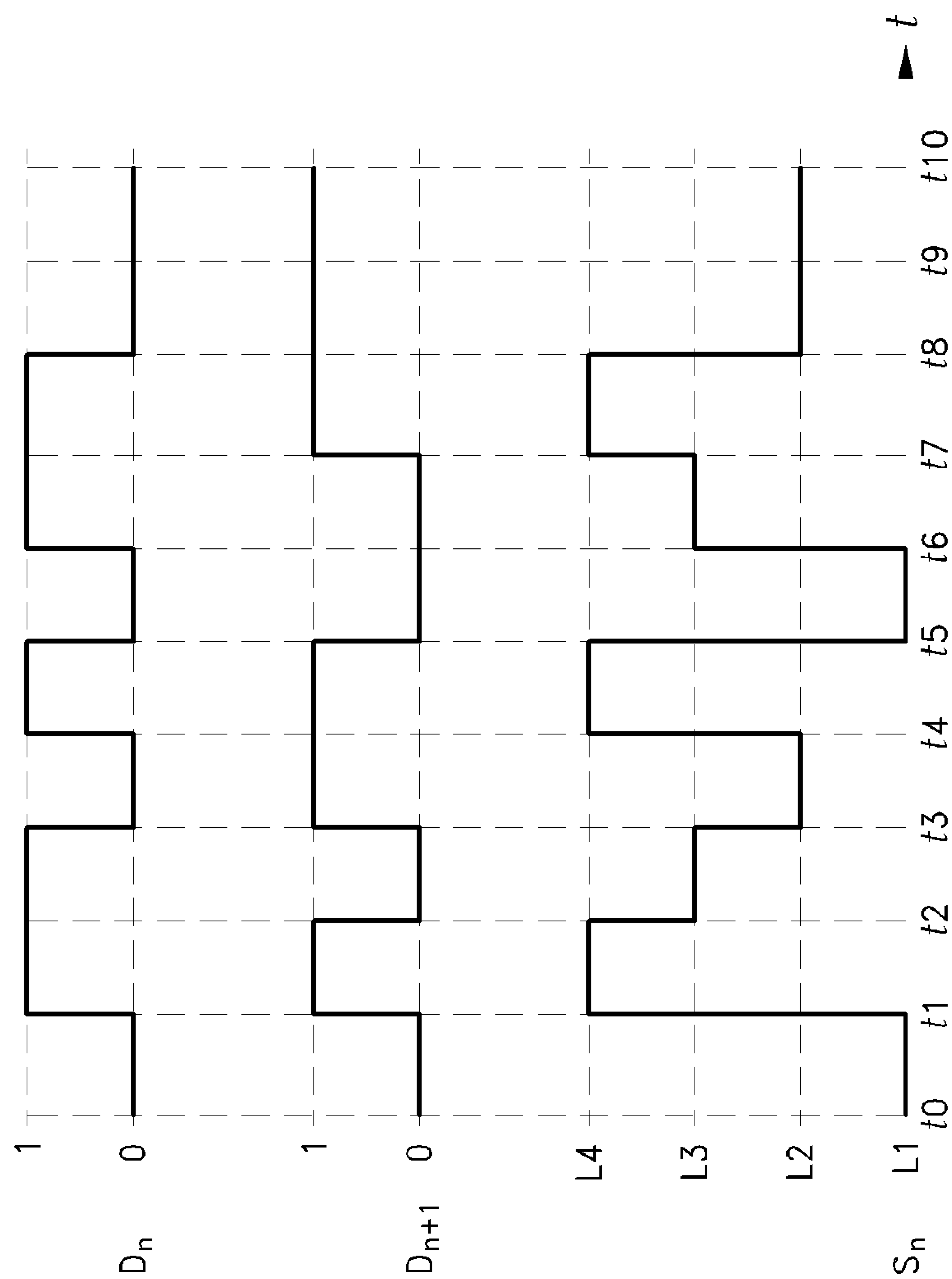


FIG. 6B

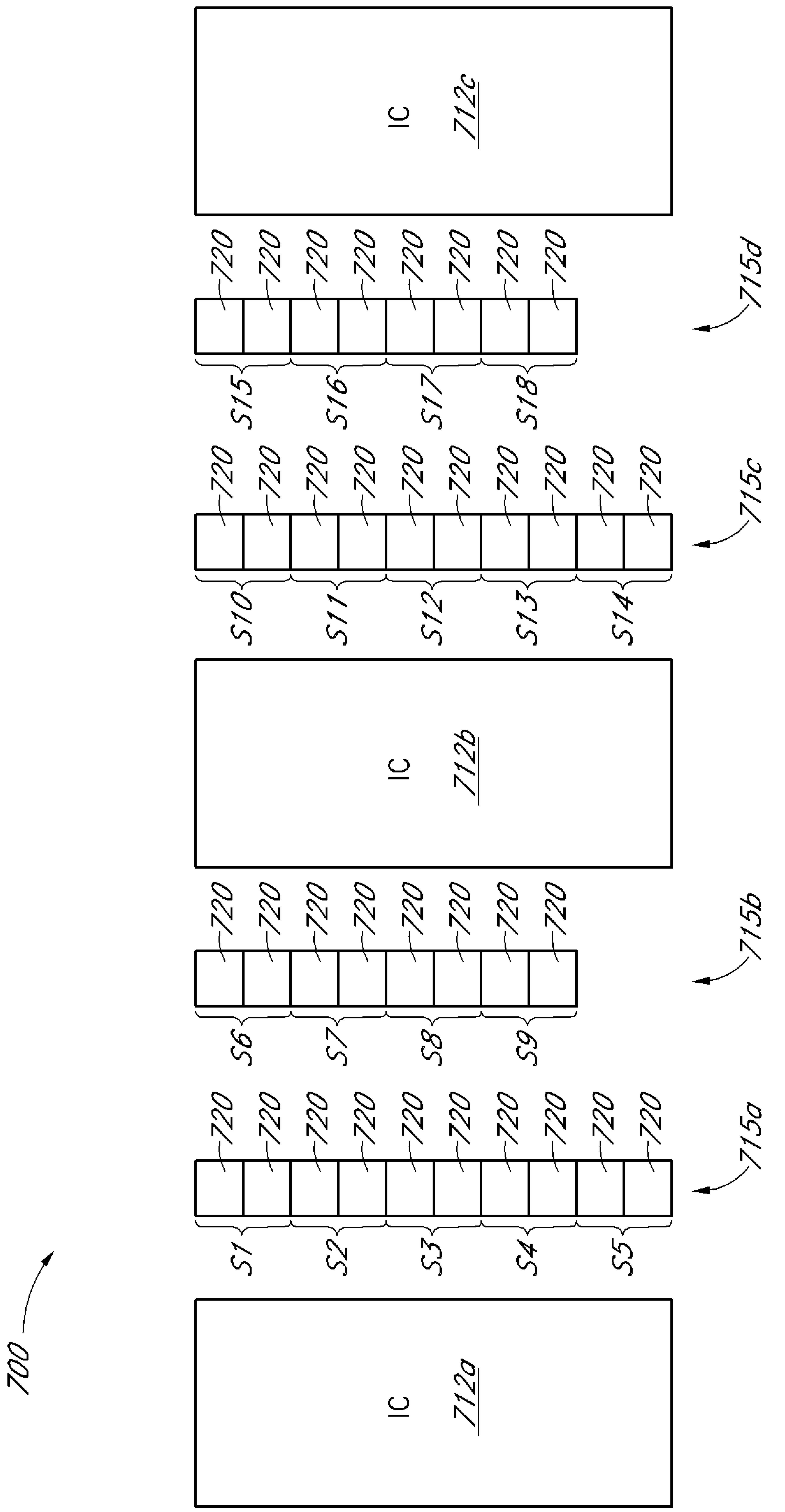

700
IC
712a
IC
712b
IC
712c
715a
715b
715c
715d
720
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18

FIG. 7

METHODS FOR BYPASSING FAULTY CONNECTIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 13/588,728, filed Aug. 17, 2012, titled "APPARATUS FOR BYPASSING FAULTY CONNECTIONS," which is a divisional of U.S. patent application Ser. No. 12/323,241, filed Nov. 25, 2008, titled "APPARATUS FOR BYPASSING FAULTY CONNECTIONS," issued as U.S. Pat. No. 8,259,461 on Sep. 4, 2012, the disclosures of each of which are hereby incorporated by reference in their entireties herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

Embodiments of the invention relate to integrated circuits, and more particularly, in one or more embodiments, to 3-D integrated circuits.

2. Description of the Related Art

Integrated circuits (ICs) may include many devices and circuit members that are formed on a single semiconductor wafer or die. The current trends in IC technology are towards faster and more complicated circuits. However, as more complex ICs are manufactured, various speed-related problems become more challenging. This is especially true when ICs having different functions are used to create electronic systems, for example, computing systems including processor and memory ICs, where different ICs are electrically connected by a network of global interconnects. As global interconnects become longer and more numerous in electronic systems, RC delay and power consumption, as well as low system performance, become limiting factors.

One proposed solution to these problems is three-dimensional (3-D) integration or packaging technology. 3-D integration refers to the vertical stacking of multiple die, packaged die, wafers, or chips including ICs within a package. In recent 3-D integration technology, multiple die or wafers are electrically connected using vertical connectors or 3-D conductive structures. Vertical connectors extend through one or more of the die and are aligned when the die are stacked to provide electrical communication among the ICs in the stack. Such vertical connectors are often formed of a conductive material, such as copper. 3-D integration typically results in a reduction of the packaged IC's footprint as well as a reduction in power consumption, and a simultaneous increase in performance.

Referring to FIGS. **1** and **2**, a conventional 3-D IC device will be described below. The illustrated 3-D IC device **100** includes first to fourth die **110***a*-**110***d* stacked over one another. The first die **110***a* is the uppermost die, and the fourth die **110***d* is the lowermost die. The second and third die **110***b*, **110***c* are interposed between the first and fourth die **110***a*, **110***d*. In other examples, a 3-D IC device can include a greater or fewer number of die than the device of FIG. **1**.

Each of the first to fourth die **110***a*-**110***d* includes an IC array **112**, a transceiver **114**, first interconnect lines **116**, second interconnect lines **118** and landing pads **130***a*-**130***d*. Each of the die **110***a*-**110***c*, except for the lowermost die (the fourth die **110***d* in the illustrated example), also includes vertical connectors **120***a*-**120***c* (FIG. **2**). In the context of this document, such vertical connectors may also be referred to as "3-D interconnects" or "3-D conductive structures." In an example where the die are formed of silicon, such vertical connectors may be referred to as "through-silicon vias" (TSVs).

The IC array **112** may include one or more integrated circuits, including, but not limited to, one or more memories (for example, volatile and/or non-volatile memories) and one or more processors. The first interconnect lines **116** provide data paths between the IC array **112** and the transceiver **114** on a respective one of the die **110***a*-**110***d*. The second interconnect lines **118** provide data paths between the transceiver **114** and the landing pads **130***a*-**130***d* of a respective one of the die **110***a*-**110***d*.

The vertical connectors **120***a*-**120***c* provide electrical paths between the landing pads **130***a*-**130***d* of two die **110***a*-**110***d* that are stacked immediately next to each other, thereby completing parts of data paths between the IC arrays **112** on the two die. In certain cases, the vertical connectors **120***a*-**120***c* of two or more die **110***a*-**110***d* that are stacked over one another are aligned in series, and can together provide serial data paths among the two or more die.

Referring to FIGS. **3**A and **3**B, a conventional scheme for data transfer between two ICs on different die via vertical connectors will be described below. The illustrated portion of a 3-D IC device **300** includes a die **310**, a first re-routing logic circuit **301**, a second re-routing logic circuit **302**, transmission drivers **331***a*-**331***d*, **341***a*-**341***d*, **331***r*, **341***r*, and comparators **332***a*-**332***d*, **342***a*-**342***d*, **332***r*, **342***r*.

The die **310** includes first to fourth nominal vertical connectors **320***a*-**320***d* and a repair vertical connector **325**. The repair vertical connector **325** may also be referred to as "redundant vertical connector" in the context of this document. In other examples, a die may include a greater or fewer number of nominal and/or repair vertical connectors than the die **310** of FIG. **3**A.

The first and second re-routing logic circuits **301**, **302** are configured to route data signals between the two ICs on the different die. One of the two ICs may be on the die **310**, and the other IC may be on a die immediately below the die **310**. The transmission drivers **331***a*-**331***d*, **341***a*-**341***d*, **331***r*, **341***r* are configured to buffer the data signals for transfer through the vertical connectors **320***a*-**320***d*, **325**. The comparators **332***a*-**332***d*, **342***a*-**342***d*, **332***r*, **342***r* are configured to detect the levels of the data signals that have been transferred through the vertical connectors **320***a*-**320***d*, **325**.

When there is no defect in the nominal vertical connectors **320***a*-**320***d*, the first and second re-routing logic circuits **301**, **302** can route data signals between the ICs on the different die, using the nominal vertical connectors **320***a*-**320***d*, as shown in FIG. **3**A. Statistically, however, it is improbable that 100% of the vertical connectors are functional, following the stress of fabrication and testing.

Thus, 3-D IC devices are typically tested during fabrication to determine if there are any defective vertical connectors. For example, if any one (for example, the fourth vertical connector **320***d*, as shown in FIG. **3**B) of the nominal vertical connectors **320***a*-**320***d* is found to be defective during the fabrication/testing of the 3-D IC device, the first and second re-routing logic circuits **301**, **302** are configured to replace the defective vertical connector **320***d* with the repair vertical connector **325**. Thus, data signals are routed via the repair vertical connector **325** and the remaining non-defective nominal vertical connectors (for example, the first to third vertical connector **320***a*-**320***c*, as shown in FIG. **3**B).

FIG. **4** illustrates the layout of a conventional 3-D IC device **400** employing the scheme described above in connection with FIGS. **3**A and **3**B. The illustrated portion of the 3-D IC device **400** includes IC arrays **412***a*-**412***c* on a die, and first to fourth columns **415***a*-**415***d* of vertical connectors **420**, **425**.

Each of the first to fourth columns **415***a*-**415***d* includes nominal vertical connectors **420** and a repair vertical connector **425**. In the illustrated example, each of the first to fourth columns **415***a*-**415***d* includes nine (9) nominal vertical connectors **420** and one (1) repair vertical connector **425**. Any one of the nine nominal vertical connectors **420** in a column **415***a*-**415***d* may be replaced with the repair vertical connector **425** in the column, when it is found to be defective.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments will be better understood from the Detailed Description of Embodiments and from the appended drawings, which are meant to illustrate and not to limit the embodiments, and wherein:

FIG. **1** is a schematic perspective view of a conventional 3-D integrated circuit device;

FIG. **2** is a cross-section of the device of FIG. **1**, taken along the line **2-2**;

FIG. **3**A is a block diagram illustrating the operation of a conventional 3-D integrated circuit device that transfers data via vertical connectors when there is no defective vertical connector;

FIG. **3**B is a block diagram illustrating the operation of the device of FIG. **3**A when one of the nominal vertical connectors is repaired with a repair vertical connector;

FIG. **4** is a schematic top plan view illustrating the layout of a die in a conventional 3-D integrated circuit device;

FIG. **5**A is a block diagram illustrating the operation of one embodiment of a 3-D integrated circuit device that transfers data via vertical connectors when there is no defective vertical connector;

FIG. **5**B is a block diagram illustrating the operation of the device of FIG. **5**A when one of the vertical connectors is defective;

FIG. **6**A is a graph illustrating a multi-level signaling scheme for use in the device of FIGS. **5**A and **5**B according to one embodiment;

FIG. **6**B is a timing diagram illustrating a multi-level signaling scheme for use in the device of FIGS. **5**A and **5**B according to one embodiment; and

FIG. **7** is a schematic top plan view illustrating one embodiment of the layout of a die in a 3-D integrated circuit device.

DETAILED DESCRIPTION OF EMBODIMENTS

In a 3-D IC device including vertical connectors for data transfer, malfunction of any of the vertical connectors may render at least some portion of the device inaccessible. In the conventional 3-D IC devices described above in connection with FIGS. **3** and **4**, a first group of vertical connectors includes a number of nominal vertical connectors and a single repair vertical connector. A defective nominal vertical connector in the group may be replaced with the repair vertical connector in the same group. When two or more nominal vertical connectors in the first group are defective, one or more repair vertical connectors in other groups of vertical connectors may be used to replace the defective nominal vertical connectors in the first group.

In certain instances, however, if the number of defective nominal vertical connectors in a die exceeds the number of available repair vertical connectors in the die, at least some of the defective nominal vertical connectors cannot be repaired. In practice, however, it is difficult to predict how many repair vertical connectors are needed to avoid such problems and how repair vertical connectors may most efficiently be configured. The addition of a large number of redundant vertical connectors may consume a large die area and increase signal routing congestion.

Furthermore, the replacement of a defective vertical connector with a remotely-located repair vertical connector may complicate the re-routing of data signals by the re-routing circuits. In addition, there can be a skewed delay due to data transfer through the repair vertical connectors, which may reduce timing margins. Another disadvantage of the conventional scheme of FIGS. **3** and **4** is that it does not allow for the "on the fly" or "in the field" reconfiguration during the operation of the 3-D IC device without detection of defective vertical connectors in real time.

Therefore, there is a need for a scheme that can efficiently provide the repair of a defective vertical connector without including a large number of repair vertical connectors while reducing the complication of re-routing. There is also a need for the "on the fly" repair of defective vertical connectors during the operation of the 3-D IC device.

In one embodiment, a 3-D integrated circuit device includes two or more die stacked over one another. Each of the die may include one or more integrated circuits (ICs) formed therein. The device also includes a plurality of vertical connectors formed through at least one of the die. The vertical connectors are configured to form at least part of the data paths between two of the ICs that are on two different ones of the die.

The device further includes a first encoding/decoding circuit to encode multiple independent data digits from one of the two ICs into a single multi-level signal. As used herein, multi-level means more than two levels. The device transfers the same multi-level signal through two or more of the vertical connectors. The device also includes a second encoding/decoding circuit to decode the multi-level signal transferred through the vertical connectors into the original multiple data digits. The decoded multiple data digits are provided to the other of the two ICs.

Even if one or more, but not all, of the two or more vertical connectors (through which the same multi-level signal is transferred) are defective, the second encoding/decoding circuit can recover the original multiple data bits using the multi-level signal from non-defective ones of the two or more vertical connectors, thus repairing or bypassing the defective vertical connectors in effect without any signal rerouting.

Referring to FIGS. **5**A and **5**B, a scheme for data transfer between two ICs on different die via vertical connectors in a 3-D IC device according to one embodiment will be described below. The illustrated portion of the 3-D IC device **500** includes a die **510**, a first IC **505**, a second IC **506**, a first encoding/decoding circuit **501**, a second encoding/decoding circuit **502**, transmission drivers **531***a*-**531***d*, **541***a*-**541***d*, and first to fourth sets of comparators **532***a*, **532***b*, **542***a*, **542***b*.

The illustrated die **510** includes first to fourth nominal vertical connectors **520***a*-**520***d*, and does not need to include a repair vertical connector. In some embodiments, the die **510** may include at least one repair vertical connector. In other embodiments, a die may include more or fewer nominal vertical connectors than the illustrated die **510**.

The first IC **505** may be located on the die **510**, and the second IC **506** may be located on a second die (not shown) immediately below the die **510**. In some embodiments, the first IC **505** may be located on a third die (not shown) above the die **510**. In other embodiments, the second IC **506** may be located on a fourth die (not shown) below the second die.

The first encoding/decoding circuits **501** may be located on the die **510** or on the third die (not shown) above the die **510**.

When transferring data from the first IC **505** to the second IC **506**, the first encoding/decoding circuit **501** may encode data digits from the first IC **505** into multi-level signals. When transferring data from the second IC **506** to the first IC **505**, the first encoding/decoding circuit **501** may decode multi-level signals from the vertical connectors **520***a*-**520***d* into the original data digits, and provide them to the first IC **505**.

The second encoding/decoding circuits **502** may be located on the second die (not shown) immediately underlying the die **510** or on the fourth die (not shown) below the second die. When transferring data from the second IC **506** to the first IC **505**, the second encoding/decoding circuit **502** may encode data digits from the second IC **506** into multi-level signals. When transferring data from the first IC **505** to the second IC **506**, the second encoding/decoding circuit **502** may decode multi-level signals from the vertical connectors **520***a*-**520***d* into the original data digits, and provide them to the second IC **506**.

The transmission drivers **531***a*-**531***d*, **541***a*-**541***d* serve to buffer data signals for transfer through the vertical connectors **520***a*-**520***d*. A skilled artisan will appreciate that any suitable types of drivers can be adapted for use as the transmission drivers **531***a*-**531***d*, **541***a*-**541***d*.

The first to fourth sets of comparators **532***a*, **532***b*, **542***a*, **542***b* serve to detect the levels of the data signals that have been transferred through the vertical connectors **520***a*-**520***d*. The number of comparators in each set can vary, depending on how many levels the multi-level signals have.

In the illustrated embodiment, when, for example, transferring data from the first IC **505** to the second IC **506**, the first encoding/decoding circuit **501** (which is on the transmitting side) encodes every two parallel data bits into a four (4) level signal, as shown in FIG. **6**A. In FIG. **6**A, the four signal levels represent two independent data bits b_0 b_1. The highest voltage level over a high reference voltage V_{REFH} may represent the bits "**11**." The second highest voltage level between the high reference voltage V_{REFH} and a middle reference voltage V_{REFM} (which is lower than V_{REFH}) may represent the bits "**10**." The third highest voltage level between the middle reference voltage and a low reference voltage V_{REFL} (which is lower than V_{REFM}) may represent the bits "**01**." The lowest voltage level lower than V_{REFL} may represent the bits "**00**." Such an encoding scheme may be referred to as 4-level pulse amplitude modulation (or 4-PAM). Other encoding schemes can alternatively be used and will be readily determined by one of ordinary skill in the art.

FIG. **6**B illustrates an example of how two data bits are converted into a digit of a single four-level signal. For example, a first data signal D_n and a second data signal D_{n+1} have bits "**0**" and "**0**," respectively, between t**0** and t**1**. These two bits are converted into a 4-level signal S_n having the lowest signal level L**1**. The first data signal D_n and the second data signal D_{n+1} have bits "**1**" and "**1**," respectively, between t**1** and t**2**. These two bits change the 4-level signal S_n to have the highest signal level L**4**. The first data signal D_n and the second data signal D_{n+1} have bits "**1**" and "**0**," respectively, between t**2** and t**3**. These two bits change the 4-level signal S_n to have the second highest signal level L**3**. The first data signal D_n and the second data signal D_{n+1} have bits "**0**" and "**1**," respectively, between t**3** and t**4**. These two bits change the 4-level signal S_n to have the second lowest signal level L**2**. The 4-level signal is transmitted at every clock edge by transferring an appropriate one of the four voltage levels.

Referring back to FIG. **5**A, the first encoding/decoding circuit **501** encodes every two data bits into a digit of a single 4-level signal. Any suitable encoding circuit may be used for such encoding. A difference between the 4-PAM encoding described here and 4-PAM encoding often used in communication systems is that typically the two data bits which are encoded into a single multi-level symbol are located sequentially (serially) in the data stream, whereas in the proposed embodiment the two encoded data bits would be concurrent (parallel), or located within the same cycle of a neighboring data stream. The 4-level signal is provided to a pair of transmission drivers, for example, two transmission drivers **531***a* and **531***b*, or two transmission drivers **531***c* and **531***d* on the transmitting side in the illustrated embodiment. The pair of transmission drivers provide the same 4-level signal to a pair of vertical connectors, for example, first and second vertical connectors **520***a*, **520***b*, or the third and fourth vertical connectors **520***c*, **520***d* in the illustrated embodiment.

The 4-level signal propagates through the pair of vertical connectors, and is detected by the third or fourth set **542***a*, **542***b* of comparators on the receiving side. The third or fourth set **542***a*, **542***b* of comparators combine with the second encoding/decoding circuit **502** to capture and decode or translate the level of the 4-level signal into the appropriate original data bits on the receiving side (e.g., the second IC **506**).

In the illustrated embodiments where 4-PAM is used for data transfer, every data bits are encoded into a 4-level signal for data transfer through a pair of vertical connectors. In other embodiments, other multi-level pulse amplitude modulation (M-PAM) can be used for data transfer via the vertical connectors. The number of signal levels is indicated by a number before the acronym "PAM." For example, a PAM signaling scheme using eight signal levels is represented by 8-PAM.

In such other embodiments, the number of comparators for detecting such a multi-level signal and the number of vertical connectors through which the same multi-level signal is transferred can vary, depending on how many signal levels the multi-level signal has. In one embodiment where an **8**-PAM signaling scheme is used for data transfer, the same 8-PAM signal may be transferred through three different vertical connectors. In such an embodiment, 7 comparators may be used for leveling the decoding of the 8-PAM signal. A skilled artisan will appreciate that other suitable signaling schemes can be used for such data transfer, including Quadrature-Phase-Shift-Keying (Q-PSK), in which the two original data bits are encoded into one of four symbols comprising a single signal level and a corresponding signal phase shift. Such an embodiment would simply require the appropriate encoding/decoding, and transmitting/receiving circuits, all of which are well known to those skilled in the art of digital communication. For consistency, the remainder of the Detailed Description of Embodiments will continue to focus on multi-level signal representations, though it is understood that at a more general level, the invention would function with any multi-bit signal representation, as just described. It is also pointed out here that when signals are encoded in this manner (multiple bits into a single cycle), the resulting multi-bit cycle is commonly referred to as a symbol or multi-bit symbol. For generality, this terminology will be employed in the accompanying claims.

When there is no defect in the vertical connectors **520***a*-**520***d*, data transfer via the vertical connectors **520***a*-**520***d* is carried out as described above in connection with FIG. **5**A. Even if any one (for example, the fourth vertical connector **520***d*, as shown in FIG. **5**B) of the vertical connectors **520***a*-**520***d* is found to be defective during the fabrication of the 3-D integrated circuit device **500** or if it malfunctions during the normal operation, data transfer can be carried out without error. In such an instance, typically, no signal is transferred through the defective or malfunctioning vertical connector. However, the other vertical connector(s) paired (or grouped) with the defective vertical connector provide(s) a data path for a multi-level signal. The encoding/decoding circuit on the receiving side can decode the multi-level signal back into the original data bits, in effect repairing or bypassing the defective vertical connector.

Referring to FIG. **7**, one embodiment of the layout of a 3-D IC device **700** will be described below. The 3-D IC device **700** employs the scheme described above in connection with FIGS. **5**A and **5**B. The illustrated portion of the 3-D IC device **700** includes IC arrays **712***a*-**712***c* on a die, and first to fourth columns **715***a*-**715***d* of vertical connectors **720**.

In the illustrated embodiment, each of the first to fourth columns **715***a*-**715***d* may include a plurality of nominal vertical connectors **720**, but no designated repair vertical connector **720**. Each of the first and third columns **715***a*, **715***c* includes ten (10) vertical connectors **720**. Each of the second and fourth columns **715***b*, **715***d* includes eight (8) vertical connectors **720**. A skilled artisan will, however, appreciate that the number of vertical connectors in the columns **715***a*-**715***d* can vary widely, depending on the design of the IC device **700**.

In the illustrated embodiment, 4-level signals are used for data transfer through the vertical connectors. In the illustrated embodiment, in each of the columns **715***a*-**715***d*, every two adjacent vertical connectors **720** are paired with each other. Each pair S**1**-S**18** of vertical connectors provides two separate data paths for the same 4-level signal. Thus, when one of the paired vertical connectors S**1**-S**18** is defective, the other non-defective vertical connector can still provide a data path for the 4-level signal, thereby allowing the encoding/decoding circuit on the receiving side to recover the original two data bits.

In alternative embodiments, any two of the vertical connectors (not limited to adjacent two vertical connectors) may be grouped together for providing data paths for the same 4-level signal. In alternative embodiments, other multi-bit signaling schemes may be used for data transfer. For example, rather than representing the parallel data bits with a multi-level symbol, multiple parallel data bits may be represented with symbols comprising both signal level and phase, as discussed previously. In such embodiments, a different number of vertical connectors may be grouped together for providing data paths for the same multi-bit signal. Thus, rather than representing two parallel data bits with four signal levels (4-PAM) or four signal phase shifts (Q-PSK), three parallel data bits to be transmitted across three connectors may be represented with eight signal levels (8-PAM) or two signal levels and four phase shifts (8-PSK).

In certain embodiments, a 3-D integrated circuit device may use the scheme described above in connection with FIGS. **5**A, **5**B, **6**A, **6**B, and **7**, and yet include one or more repair vertical connectors. Such repair vertical connectors may be used when all of a pair or a group of vertical connectors for transferring the same multi-level signal are defective.

The schemes in the embodiments described above in connection with FIGS. **5**A, **5**B, **6**A, **6**B, and **7** use zero or fewer redundant repair vertical connectors because a nominal vertical connector can effectively provide the repair or bypass of a defective nominal vertical connector paired or grouped with it. Thus, area on a die for such repair vertical connectors can be saved or reduced.

In certain embodiments, such spaces can be used for any other components of the IC device. In one embodiment, vertical connectors for power transfer and FatCap (alternatively, referred to as "CFAT") may be provided on the die in place of such repair vertical connectors. The term "FatCap" refers to decoupling capacitance placed between power supplies to dampen noise. FatCaps typically occupy a relatively large space.

Because each pair of vertical connectors has effectively one repair vertical connector in the schemes described above, the schemes provide more repairability with no or less extra designated repair vertical connectors than the conventional scheme of FIGS. **3**A and **3**B. In addition, the schemes can avoid complex re-routing circuitry as described above in connection with FIGS. **3**A and **3**B. This minimizes delay skews due to re-routing. Furthermore, the schemes allow "field" repair, that is, any defective vertical connectors grouped with functional connectors are effectively bypassed and therefore require no on the fly repair during the operation of the IC device.

3-D IC devices employing the above described schemes can be implemented into various electronic devices. Examples of the electronic devices can include, but are not limited to, consumer electronic products, parts of the consumer electronic products, electronic test equipments, etc. Examples of the electronic devices can also include memory chips, memory modules, circuits of optical networks or other communication networks, and disk driver circuits. The consumer electronic products can include, but are not limited to, a mobile phone, a telephone, a television, a computer monitor, a computer, a hand-held computer, a personal digital assistant (PDA), a microwave, a refrigerator, a stereo system, a cassette recorder or player, a DVD player, a CD player, a VCR, an MP3 player, a radio, a camcorder, a camera, a digital camera, a portable memory chip, a washer, a dryer, a washer/dryer, a copier, a facsimile machine, a scanner, a multi functional peripheral device, a wrist watch, a clock, etc. Further, the electronic device can include unfinished products.

In one embodiment, an apparatus includes: a first die; a second die encapsulated within a same package as the first die; a first data path for a multi-bit symbol configured to carry data between the first and second die; and a second data path configured to carry the same multi-bit symbol for redundancy.

In another embodiment, an integrated circuit device includes two or more die stacked over one another. Each of the die includes an IC formed therein. The device also includes a plurality of vertical connectors on at least one of the die. The vertical connectors are configured to couple data paths between at least two of the ICs of different die. The device further includes an encoding/decoding circuit configured to transfer an identical multi-bit symbol through a set of two or more of the vertical connectors, wherein the identical multi-bit symbols have more than two voltage levels.

In yet another embodiment, a method of transferring data in a 3-D integrated circuit device includes: encoding two or more data bits into a multi-bit symbol representing the two or more data bits; transferring, for redundancy of communication, the same multi-bit symbol through two or more vertical connectors formed through a die of the 3-D integrated circuit device; and decoding the digit of the transferred multi-bit symbol into the two or more data bits.

In yet another embodiment, a method of transferring data between integrated circuit devices, includes: encoding two or more data bits into a multi-bit symbol representing the two or more data bits; transferring, for redundancy of communication, the same multi-bit symbol across two or more IC connectors; and decoding the transferred multi-bit symbol into the two or more data bits.

Although this invention has been described in terms of certain embodiments, other embodiments that are apparent to those of ordinary skill in the art, including embodiments that do not provide all of the features and advantages set forth herein, are also within the scope of this invention. Moreover, the various embodiments described above can be combined to provide further embodiments. In addition, certain features shown in the context of one embodiment can be incorporated into other embodiments as well. Accordingly, the scope of the present invention is defined only by reference to the appended claims.

I claim:

1. A method of transferring data in a three-dimensional (3-D) integrated circuit device, the method comprising:

encoding two or more data bits into a multi-bit symbol representing the two or more data bits, wherein encoding the two or more data bits comprises encoding the two or more data bits into a multi-level pulse amplitude modulation (PAM) signal, wherein the multi-level PAM signal comprises an 8-PAM signal;

transferring, for redundancy of communication, the same multi-bit symbol through two or more of a plurality of vertical connectors formed through a die of the 3-D integrated circuit device, wherein transferring the multi-bit symbol comprises transferring the 8-PAM signal via four of the plurality of vertical connectors; and

decoding the transferred multi-bit symbol into the two or more data bits.

2. The method of claim **1**, wherein transferring comprises transferring the multi-bit symbol redundantly by way of through-silicon vias.

3. The method of claim **1**, wherein decoding comprises detecting a signal level of the multi-bit symbol.

4. The method of claim **1**, further comprising:

providing the two or more data bits from a first integrated circuit on or above the die before encoding the two or more data bits; and

providing the two or more data bits decoded from the multi-bit symbol to a second integrated circuit below the die after decoding the multi-bit symbol.

5. A method of transferring data in a three-dimensional (3-D) integrated circuit device, the method comprising:

encoding two or more data bits into a multi-bit symbol representing the two or more data bits;

transferring, for redundancy of communication, the same multi-bit symbol through two or more of a plurality of vertical connectors formed through a die of the 3-D integrated circuit device;

decoding the transferred multi-bit symbol into the two or more data bits;

providing the two or more data bits from a first integrated circuit on or above the die before encoding the two or more data bits; and

providing the two or more data bits decoded from the multi-bit symbol to a second integrated circuit below the die after decoding the multi-bit symbol.

6. The method of claim **5**, wherein encoding the two or more data bits comprises encoding the two or more data bits into a multi-level pulse amplitude modulation (PAM) signal.

7. The method of claim **6**, wherein the multi-level PAM signal comprises a 4-PAM signal, and wherein transferring the multi-bit symbol comprises transferring the 4-PAM signal via two of the plurality of vertical connectors.

8. The method of claim **5**, further comprising transferring a second multi-bit symbol from the second integrated circuit to the first integrated circuit.

9. The method of claim **5**, further comprising buffering the multi-bit symbol before transferring the multi-bit symbol.

10. The method of claim **5**, wherein transferring the multi-bit symbol comprises transferring the multi-bit symbol through only non-defective ones of the two or more of the plurality of vertical connectors when any of the two or more vertical connectors is defective.

11. The method of claim **5**, wherein decoding comprises detecting a signal level of the multi-bit symbol from among more than two signal levels.

12. The method of claim **5**, wherein the die is a silicon die, and wherein transferring comprises transferring the same multi-bit symbol through two or more through-silicon vias formed through the die.

13. The method of claim **5**, wherein encoding is performed on a first die and decoding is performed on a second die, and wherein the first die and the second die are stacked on one another.

14. The method of claim **13**, wherein the first die and the second die are encapsulated within the same package.

15. The method of claim **13**, further comprising transferring a second multi-bit symbol redundantly through the two or more vertical connectors from the second die to the first die.

16. The method of claim **5**, further comprising, after transferring, detecting a signal level of the multi-bit symbol using comparators.

* * * * *