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Liu et al.

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(54) **FORMATION OF NICKEL SILICON AND NICKEL GERMANIUM STRUCTURE AT STAGGERED TIMES**

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(22) Filed: **Dec. 18, 2013**

(65) **Prior Publication Data**

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(51) **Int. Cl.**

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H01L 29/78	(2006.01)
H01L 29/16	(2006.01)
H01L 27/092	(2006.01)
H01L 21/8238	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/16*** (2013.01); ***H01L 21/8238*** (2013.01); ***H01L 27/092*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 21/823807; H01L 21/823842; H01L 21/823814; H01L 29/7843; H01L 29/7833
USPC 438/231, 199; 257/369
See application file for complete search history.

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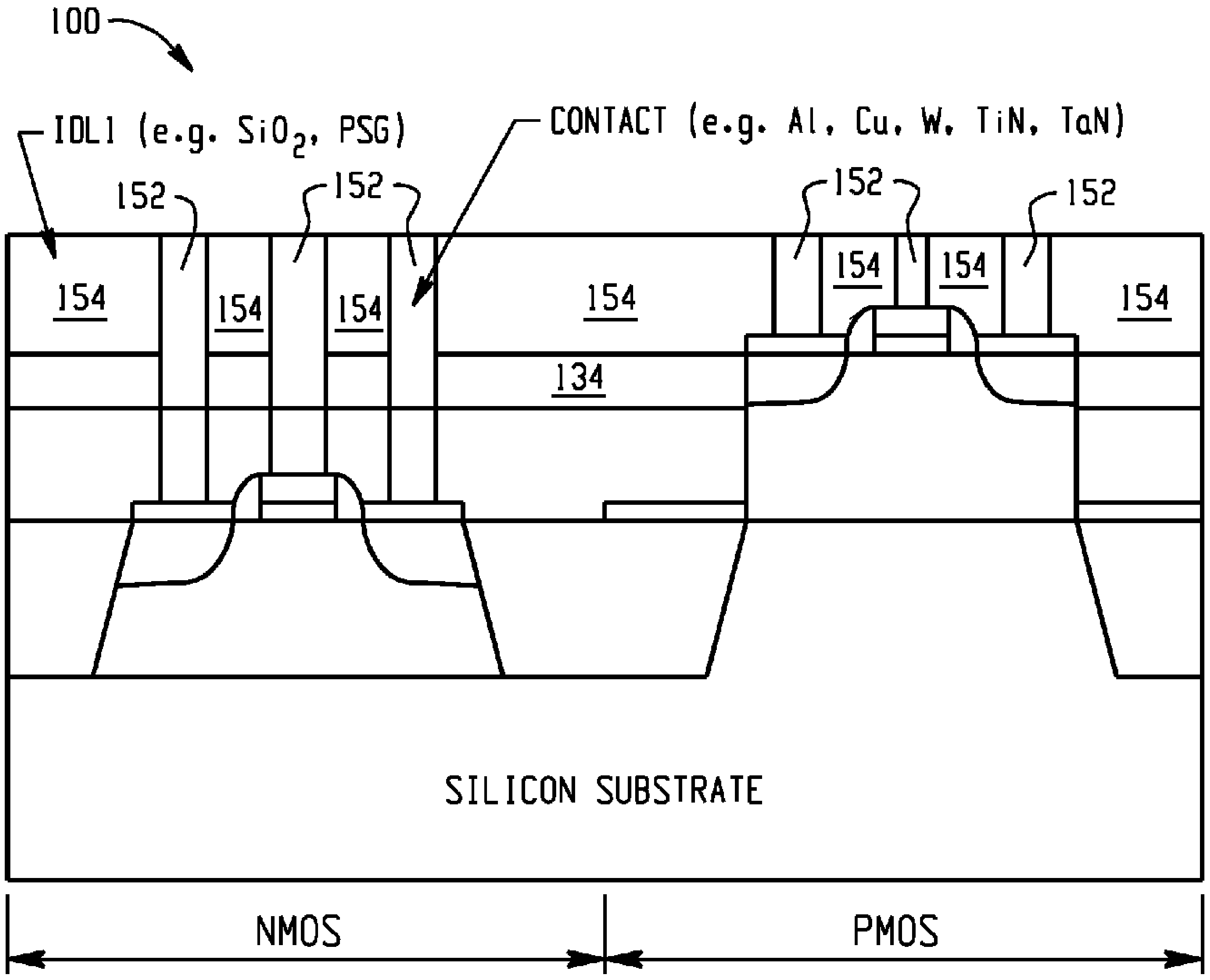
(57) **ABSTRACT**

Systems and methods are provided for generating a semiconductor device on a single semiconductor substrate. A single semiconductor substrate is generated that includes a Silicon material portion and a Germanium material portion. A first set of source/drain contacts is formed from a first metal on the Silicon material portion. The first set of source/drain contacts is annealed with the Silicon material portion at a first temperature. A second set of source/drain contacts is formed from a second metal on the Germanium material portion after heating the semiconductor substrate to the first temperature, and the second set of source/drain contacts is annealed with the Germanium material portion at a second temperature, where the second temperature is less than the first temperature.

20 Claims, 7 Drawing Sheets



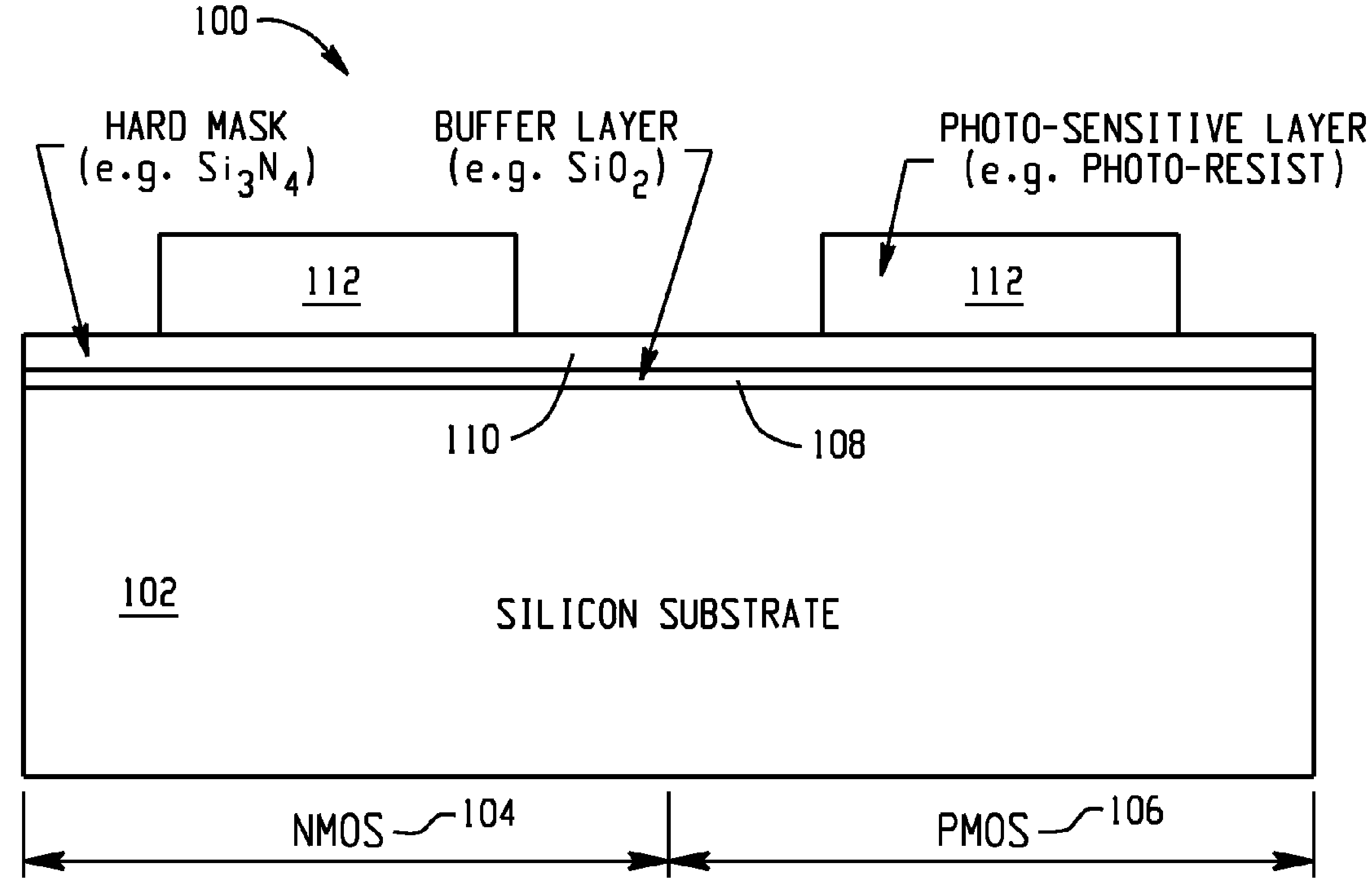

100
HARD MASK
(e.g. Si_3N_4)
BUFFER LAYER
(e.g. SiO_2)
PHOTO-SENSITIVE LAYER
(e.g. PHOTO-RESIST)
112
112
110
108
102
SILICON SUBSTRATE
NMOS 104
PMOS 106

Fig. 1

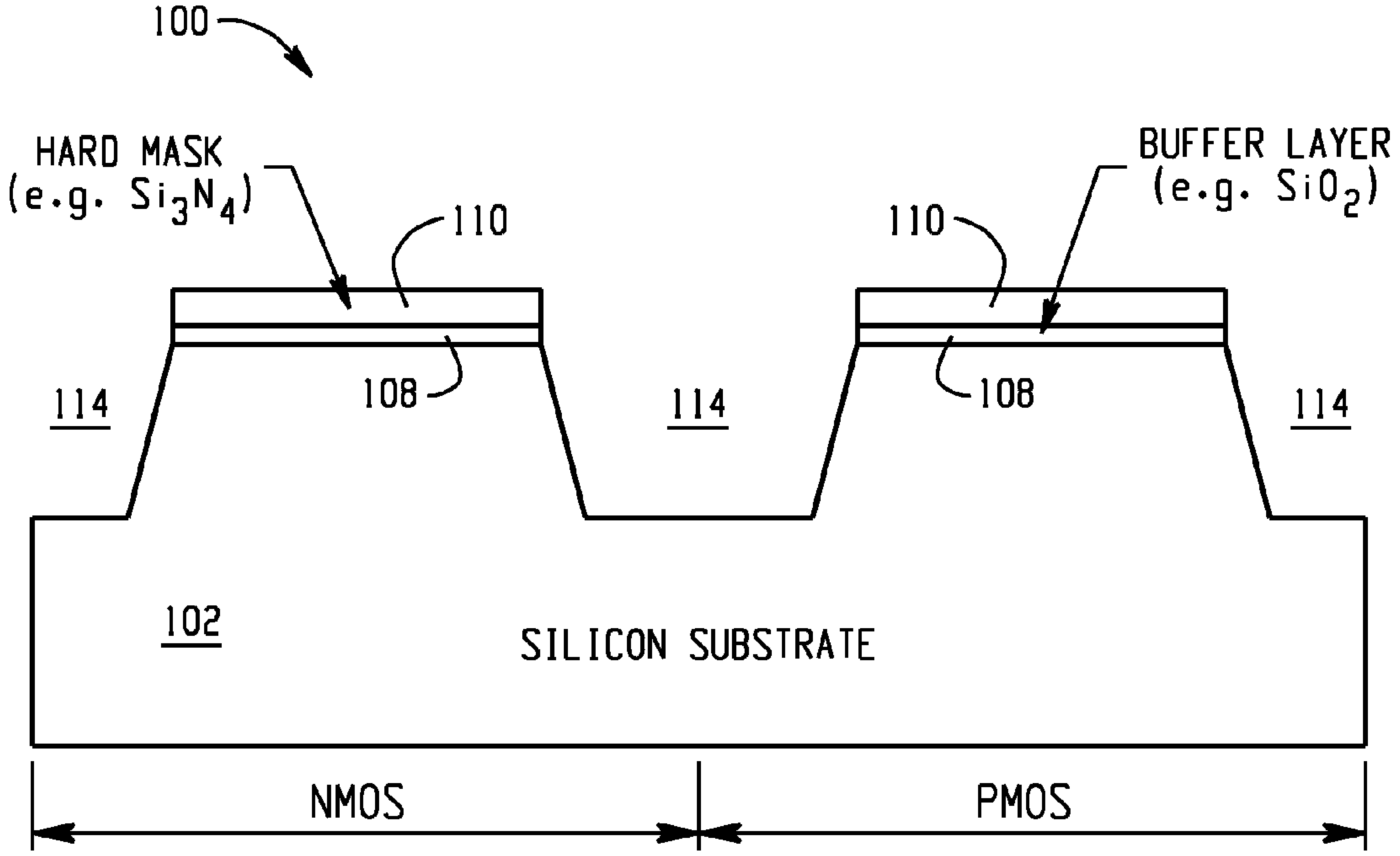

100
HARD MASK
(e.g. Si_3N_4)
BUFFER LAYER
(e.g. SiO_2)
110
110
108
108
114
114
114
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 2

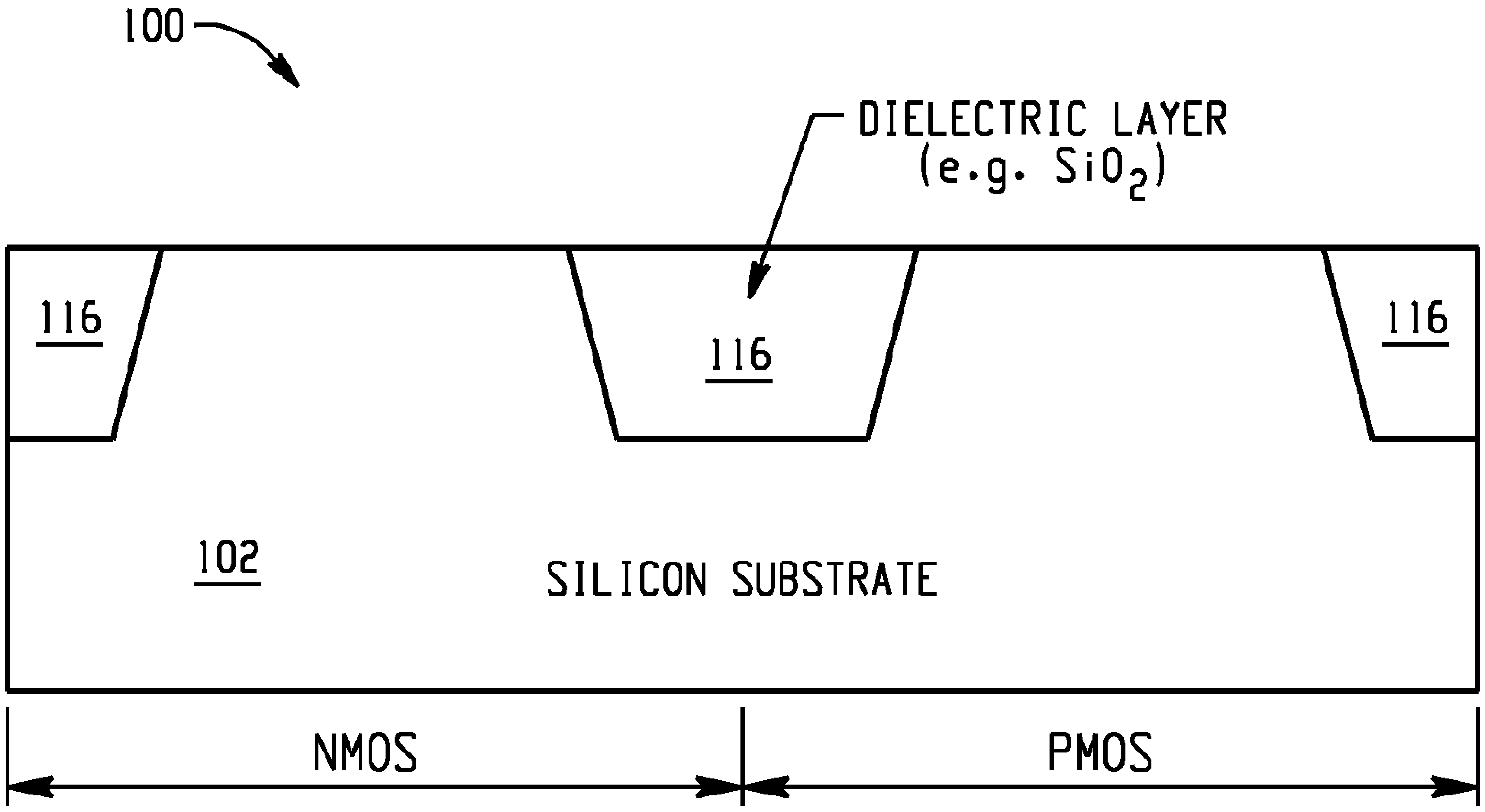

100
DIELECTRIC LAYER (e.g. SiO_2)
116
116
116
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 3

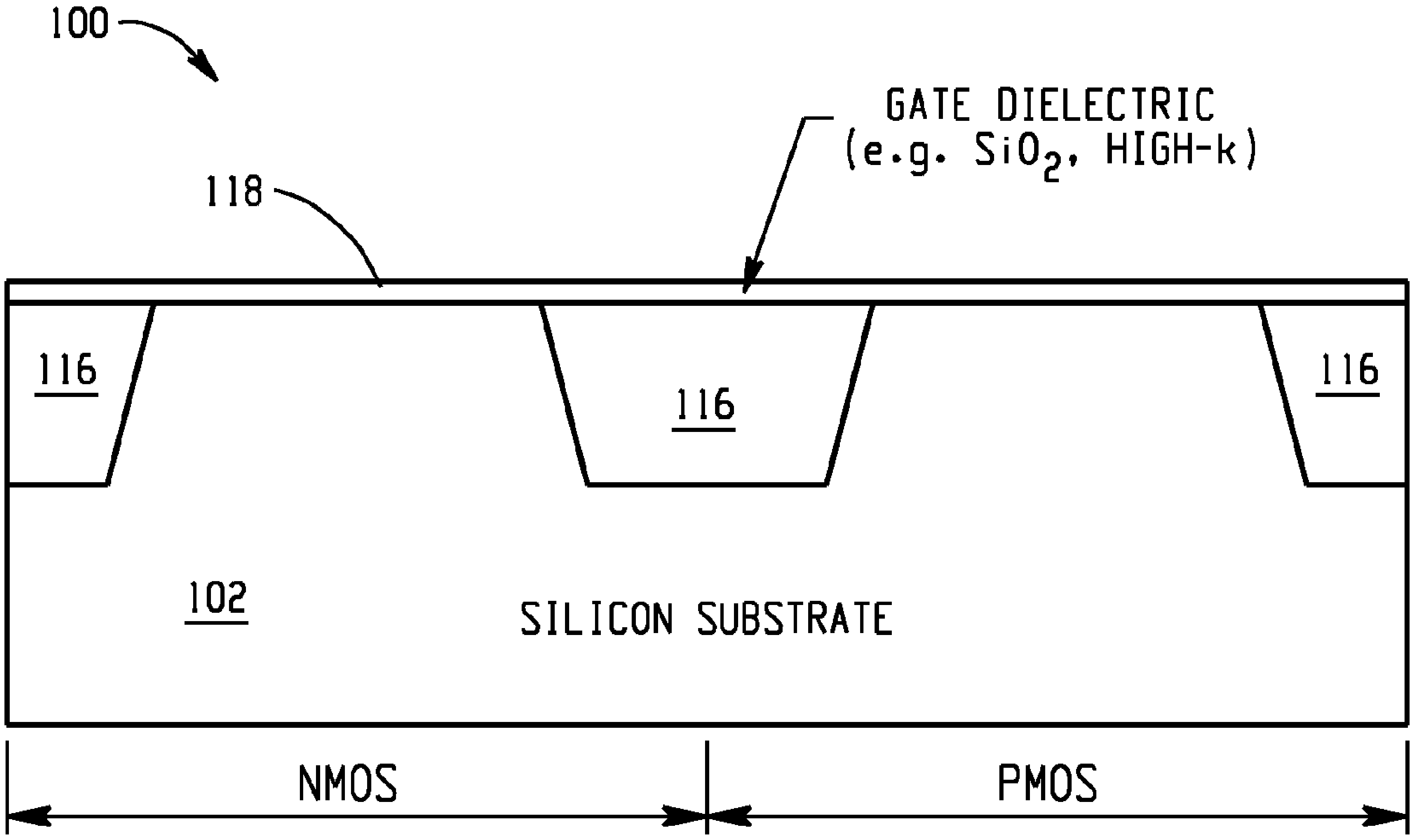

100
GATE DIELECTRIC (e.g. SiO_2, HIGH-k)
118
116
116
116
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 4

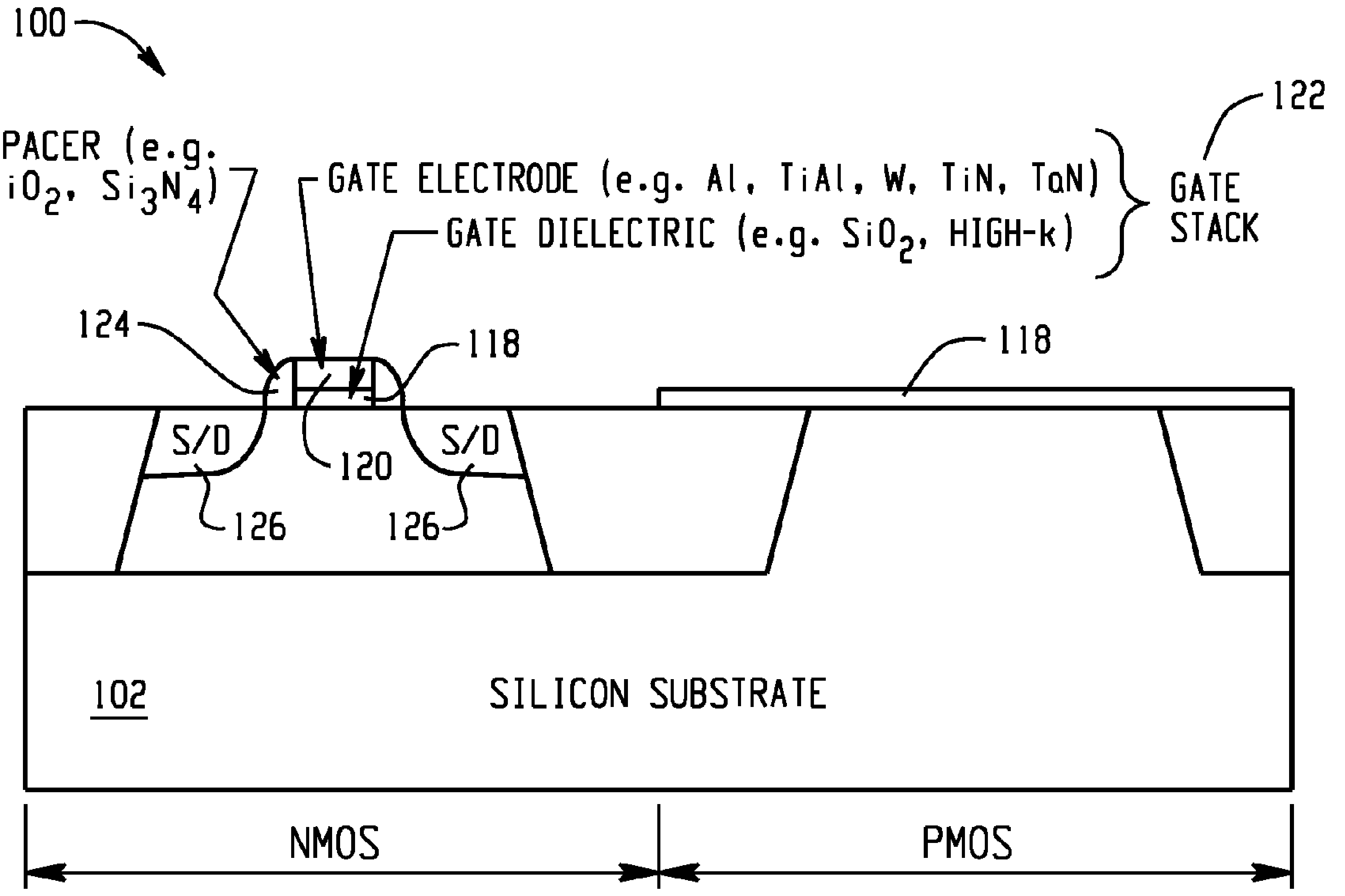

100
SPACER (e.g. SiO_2, Si_3N_4)
GATE ELECTRODE (e.g. Al, TiAl, W, TiN, TaN)
GATE DIELECTRIC (e.g. SiO_2, HIGH-k)
GATE STACK
122
124
118
118
S/D
S/D
120
126
126
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 5

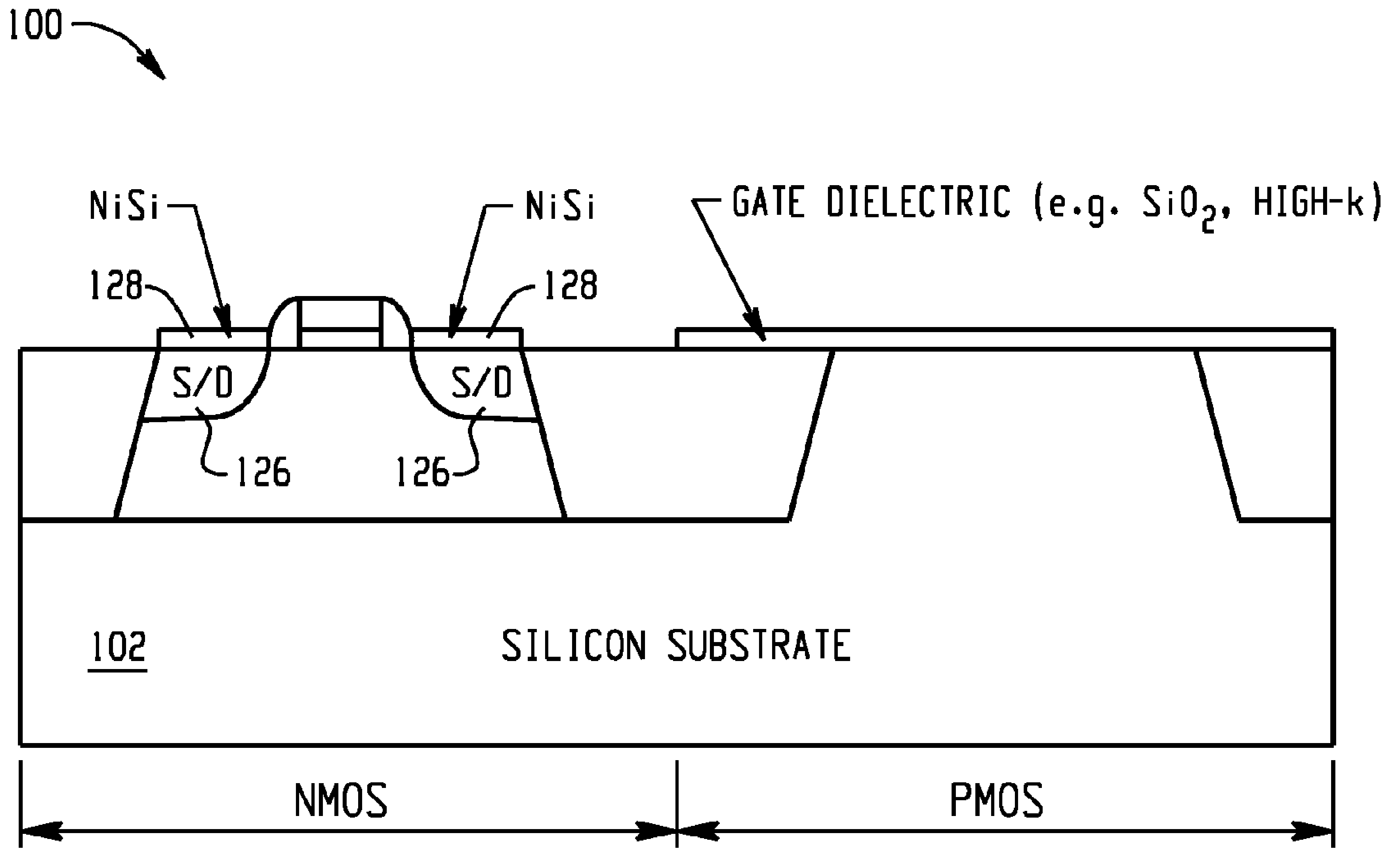

100
NiSi
NiSi
GATE DIELECTRIC (e.g. SiO_2, HIGH-k)
128
128
S/D
S/D
126
126
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 6

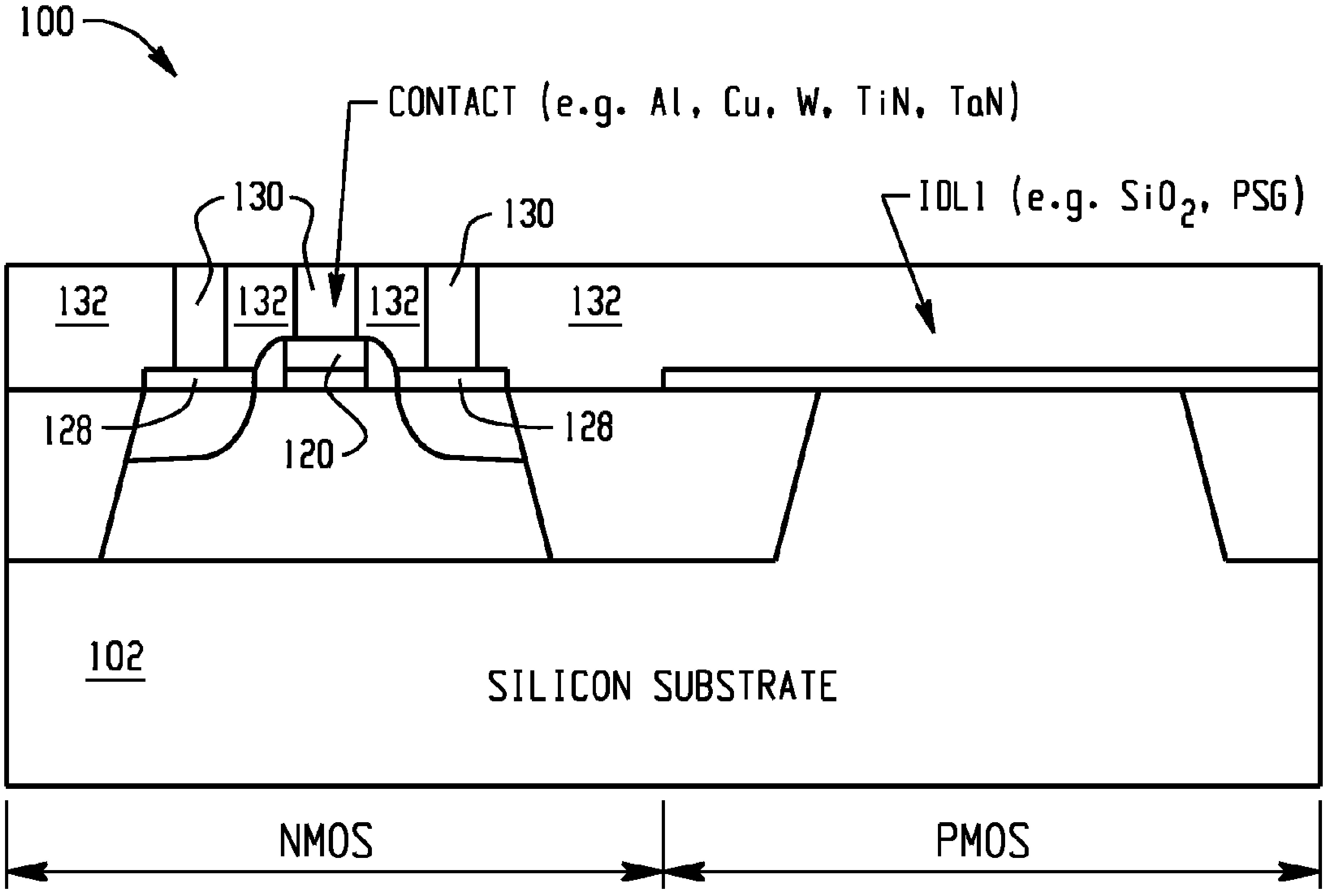

100
CONTACT (e.g. Al, Cu, W, TiN, TaN)
130
130
IDL1 (e.g. SiO$_2$, PSG)
132
132
132
132
128
120
128
102
SILICON SUBSTRATE
NMOS
PMOS

Fig. 7

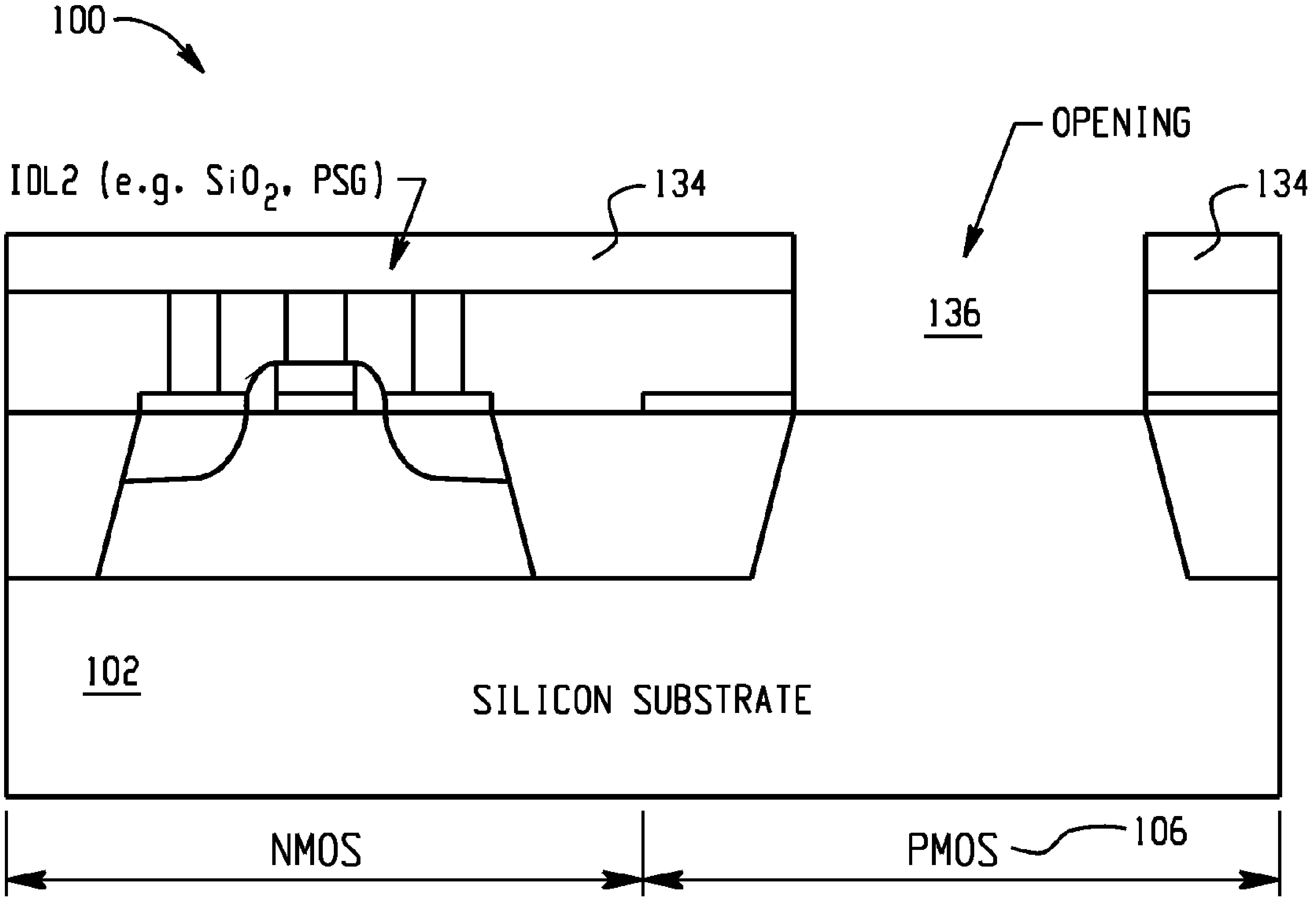

100
OPENING
IDL2 (e.g. SiO$_2$, PSG)
134
134
136
102
SILICON SUBSTRATE
NMOS
PMOS
106

Fig. 8

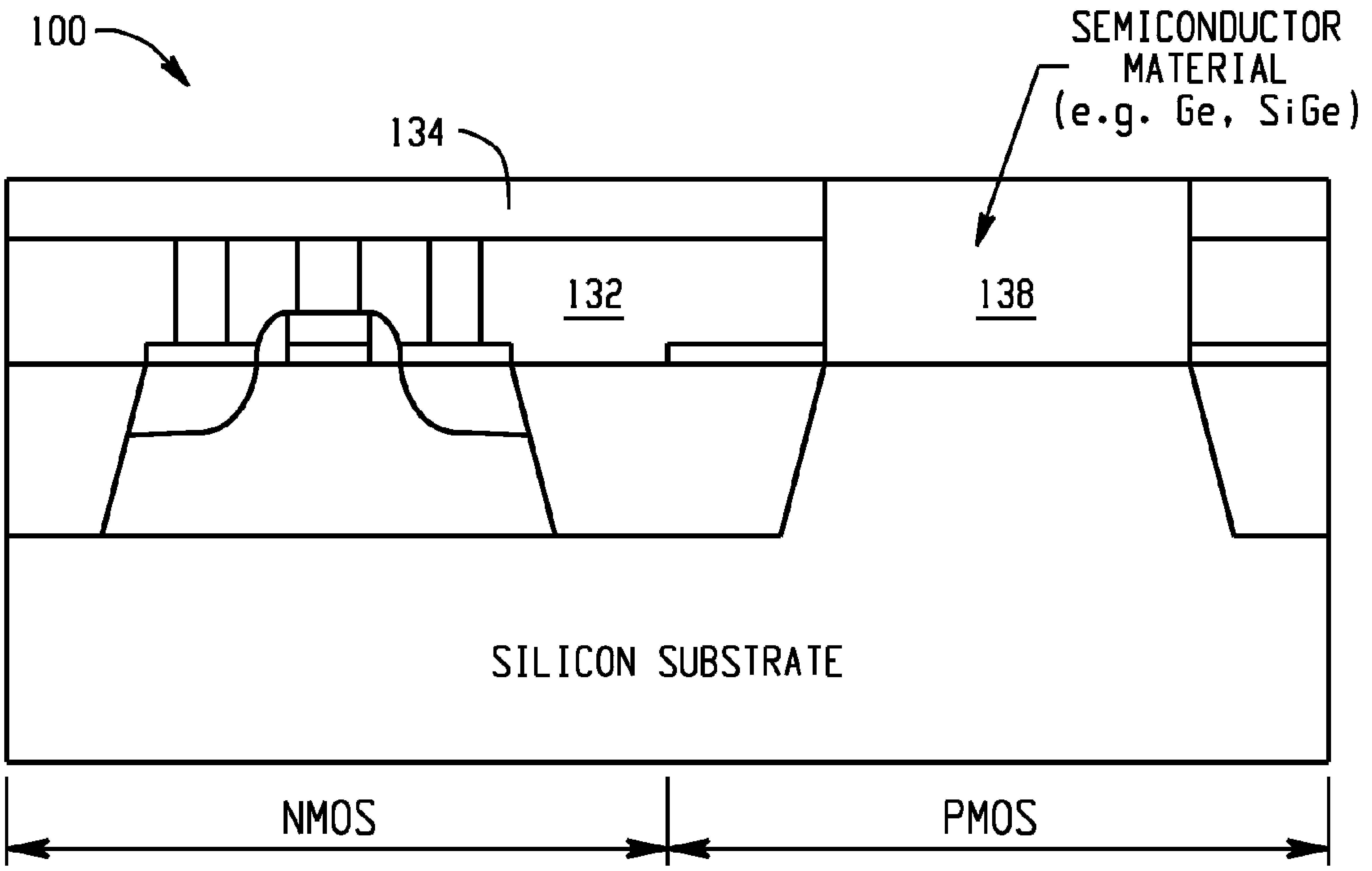

100
SEMICONDUCTOR
MATERIAL
(e.g. Ge, SiGe)
134
132
138
SILICON SUBSTRATE
NMOS
PMOS

Fig. 9

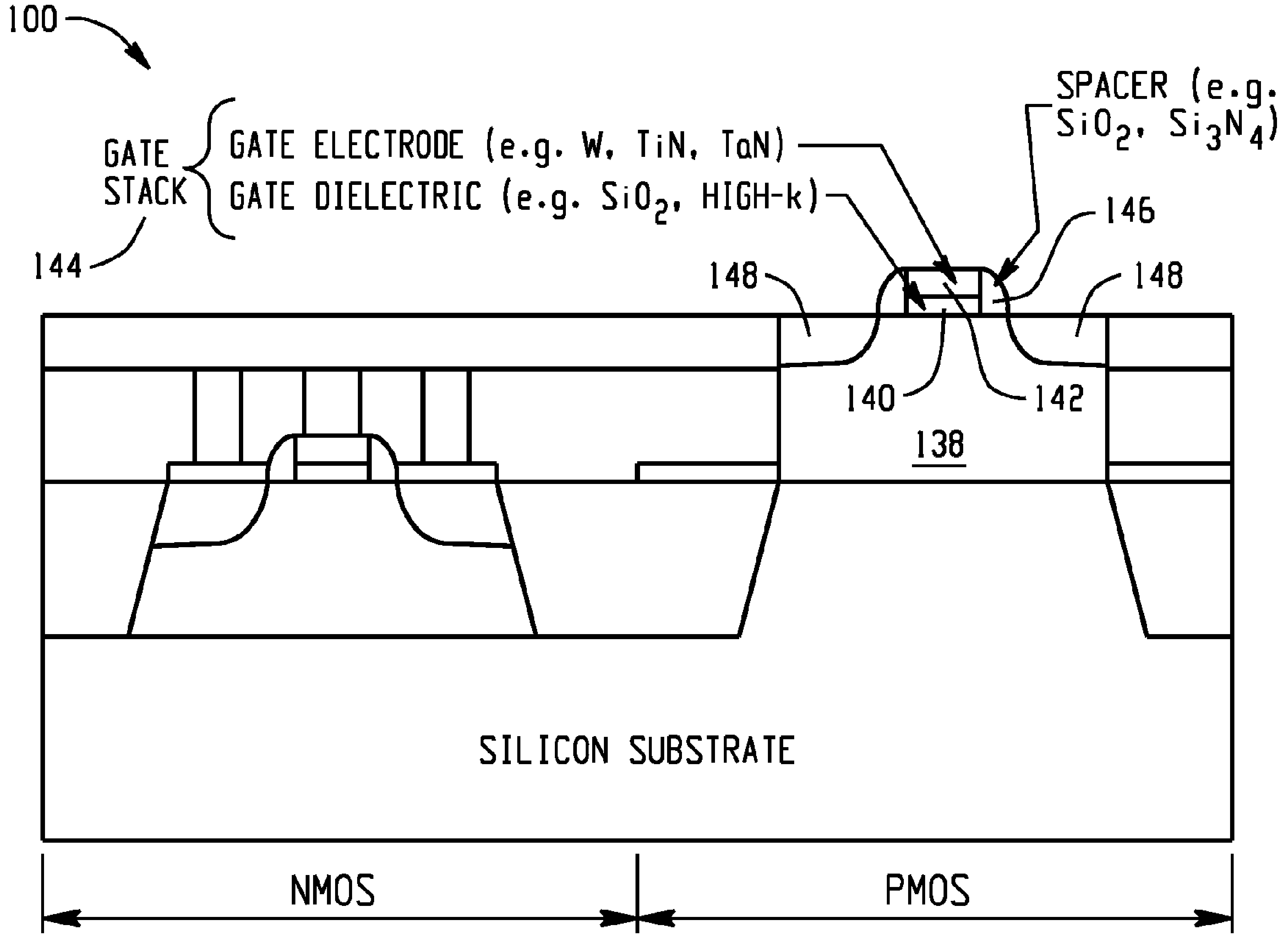

100
SPACER (e.g.
SiO_2, Si_3N_4)
GATE STACK
GATE ELECTRODE (e.g. W, TiN, TaN)
GATE DIELECTRIC (e.g. SiO_2, HIGH-k)
144
146
148
148
140
142
138
SILICON SUBSTRATE
NMOS
PMOS

Fig. 10

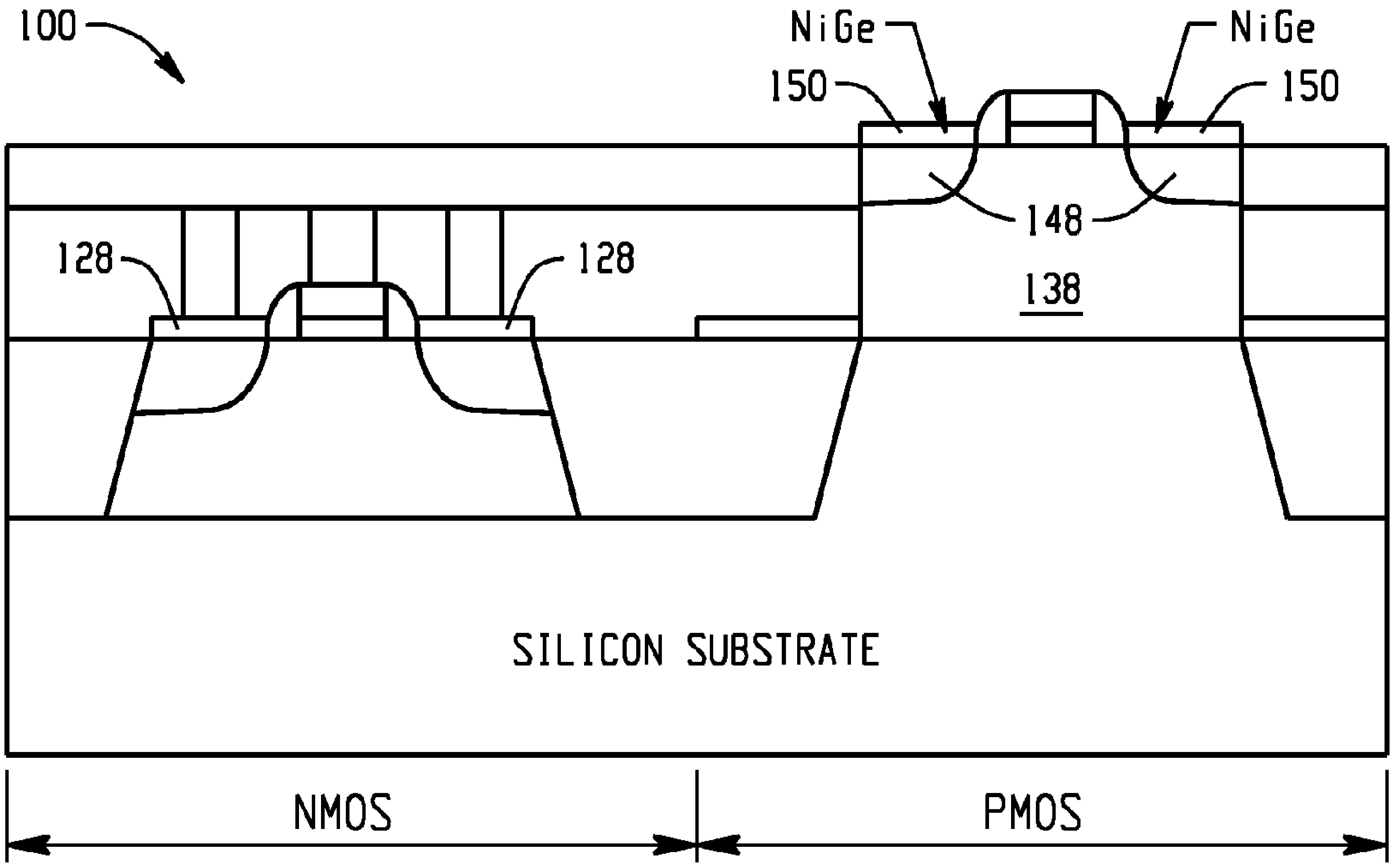

100
NiGe
NiGe
150
150
148
128
128
138
SILICON SUBSTRATE
NMOS
PMOS

Fig. 11

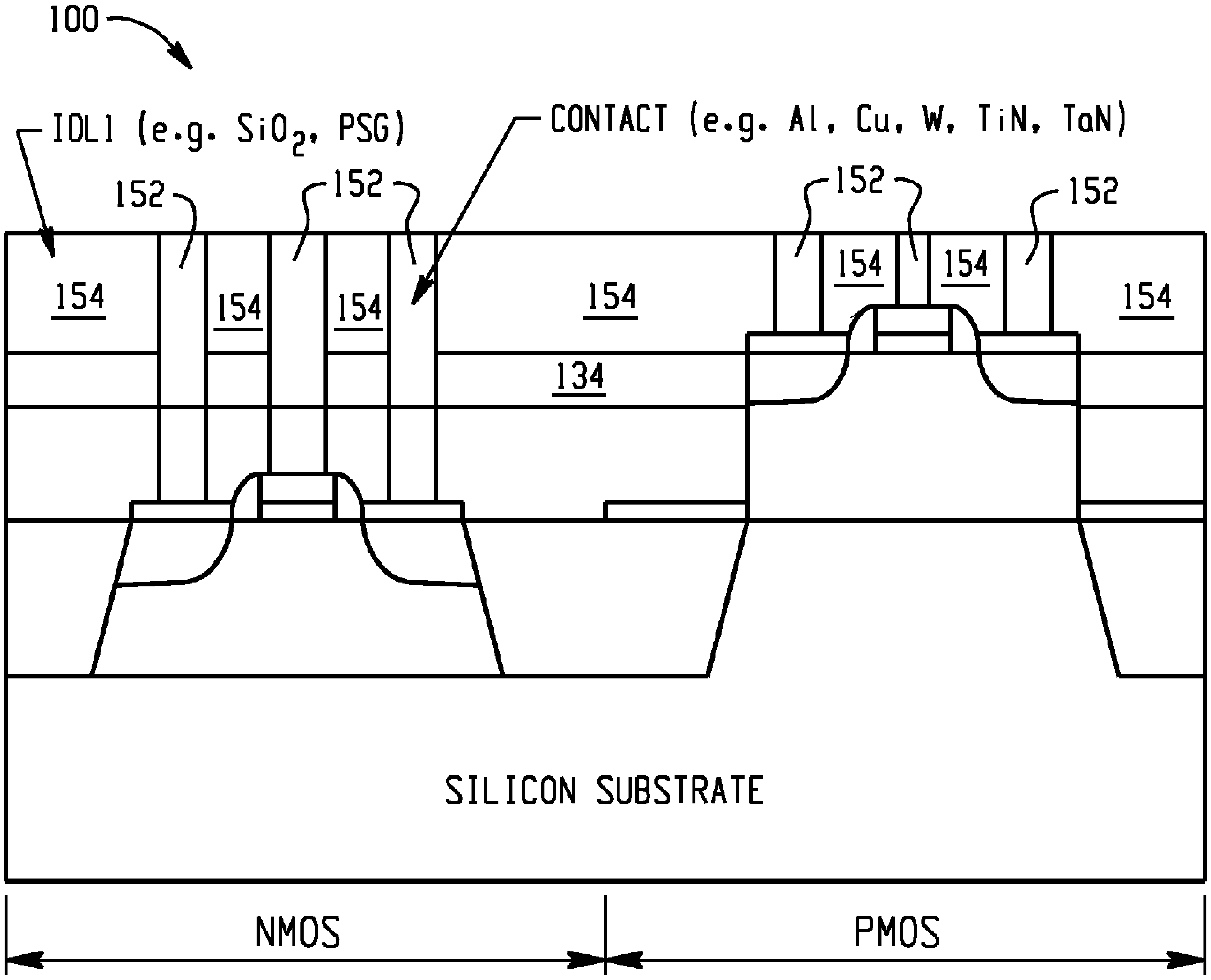

100
IDL1 (e.g. SiO_2, PSG)
CONTACT (e.g. Al, Cu, W, TiN, TaN)
152
152
152
152
154
154
154
154
154
154
154
134
SILICON SUBSTRATE
NMOS
PMOS

Fig. 12

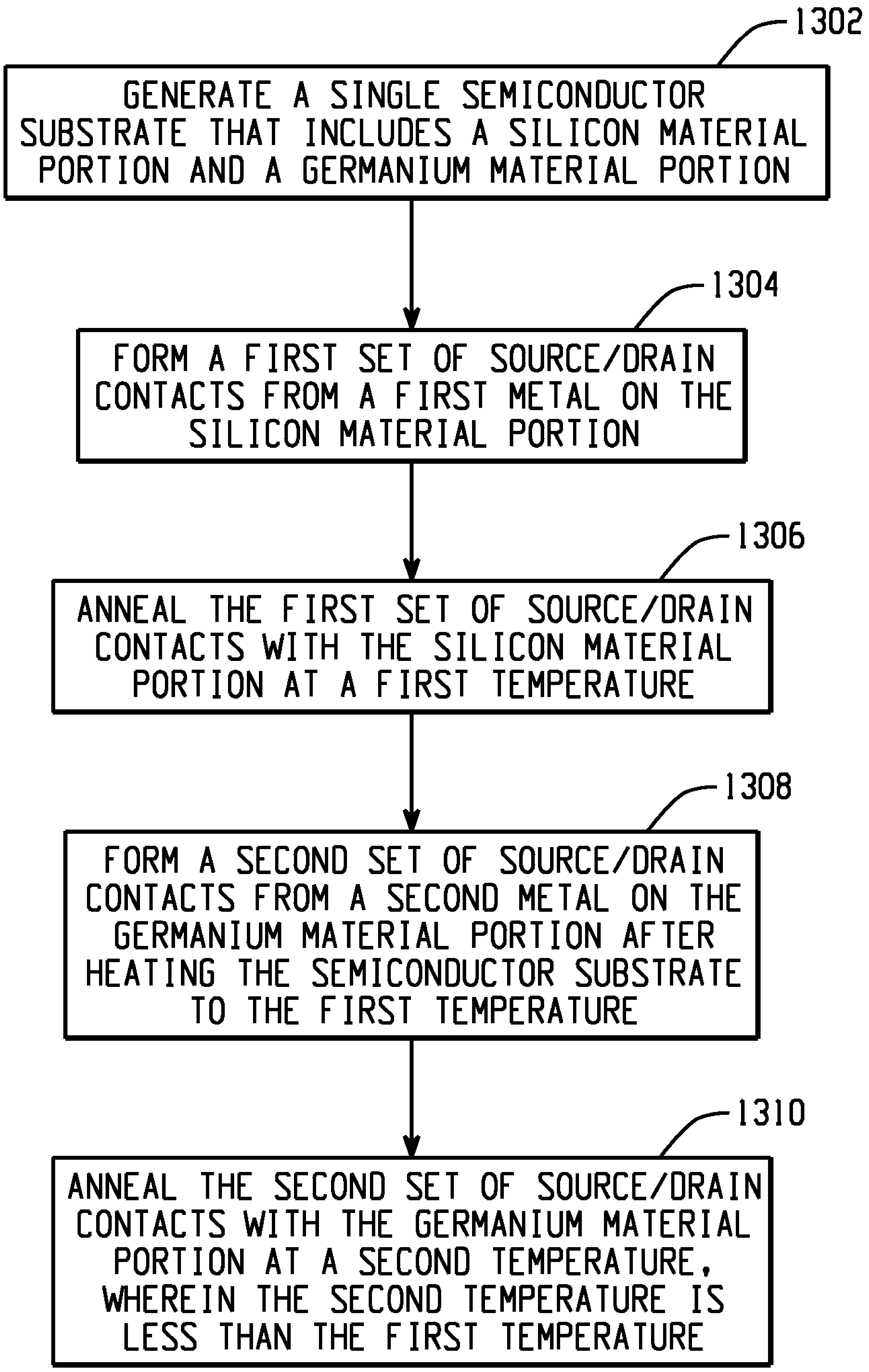

1302
GENERATE A SINGLE SEMICONDUCTOR SUBSTRATE THAT INCLUDES A SILICON MATERIAL PORTION AND A GERMANIUM MATERIAL PORTION
1304
FORM A FIRST SET OF SOURCE/DRAIN CONTACTS FROM A FIRST METAL ON THE SILICON MATERIAL PORTION
1306
ANNEAL THE FIRST SET OF SOURCE/DRAIN CONTACTS WITH THE SILICON MATERIAL PORTION AT A FIRST TEMPERATURE
1308
FORM A SECOND SET OF SOURCE/DRAIN CONTACTS FROM A SECOND METAL ON THE GERMANIUM MATERIAL PORTION AFTER HEATING THE SEMICONDUCTOR SUBSTRATE TO THE FIRST TEMPERATURE
1310
ANNEAL THE SECOND SET OF SOURCE/DRAIN CONTACTS WITH THE GERMANIUM MATERIAL PORTION AT A SECOND TEMPERATURE, WHEREIN THE SECOND TEMPERATURE IS LESS THAN THE FIRST TEMPERATURE

Fig. 13

FORMATION OF NICKEL SILICON AND NICKEL GERMANIUM STRUCTURE AT STAGGERED TIMES

FIELD

The technology described in this disclosure relates generally to semiconductor device fabrication and more particularly to multi-layer structures.

BACKGROUND

Non-planar transistor structures provide a means to achieve high device performance in a small footprint. The fabrication of such structures is often limited by the material properties of the substances used to create those structures. Performing component formulations in particular orders can increase the menu of available semiconductor configurations that can be achieved by avoiding certain component formulation conflicts.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram depicting a patterning of a photo-sensitive layer onto a single semiconductor substrate.

FIG. **2** depicts the semiconductor device after a material removing procedure and stripping of the photo-sensitive layer.

FIG. **3** depicts the semiconductor device after incorporation of a dielectric layer.

FIG. **4** depicts the semiconductor device after incorporation of a gate dielectric material.

FIG. **5** depicts formation of a gate on the NMOS portion of the semiconductor device.

FIG. **6** depicts formation of Nickel Silicide on the source/drain regions of the NMOS transistor.

FIG. **7** depicts the formation of an inter-layer dielectric above the NMOS transistor layers.

FIG. **8** depicts formation of an opening for fabrication of the PMOS transistor components.

FIG. **9** depicts incorporation of an additional semiconductor material.

FIG. **10** depicts formation of a gate stack of the PMOS transistor.

FIG. **11** depicts formation of Nickel Germanide on the source/drain regions of the PMOS transistor.

FIG. **12** depicts incorporation of a capping interlayer dielectric.

FIG. **13** is a flow diagram depicting a method of generating a semiconductor device on a single semiconductor substrate.

DETAILED DESCRIPTION

When planning a semiconductor fabrication process, certain material properties limit the ability to form different structures. For example, certain semiconductor structure fabrication processes require that the semiconductor structure be exposed to particular temperature levels (e.g., annealing processes between different materials require differing formation temperatures). While some structures require high temperature, other structures could potentially be damaged by exposure to those high temperatures. Strategic ordering of component fabrication avoids certain component formulation conflicts and expands the set of semiconductor configurations available.

The following figures describe an example where a semiconductor device **100** that includes an NMOS transistor **104**, having Nickel Silicide source/drain contacts **126**, and a PMOS transistor **106**, having Nickel Germanide source/drain contacts **150**, is formed on a single semiconductor substrate **102** (shown in FIGS. **1**-**12**). The following process enables these structures to be formed, despite the formation temperature of Nickel Germanide for the PMOS **106** transistor being much lower (250-300° C.) than the formation temperature of Nickel Silicide for the NMOS transistor **104** (400-600° C.).

FIG. **1** is a diagram depicting a patterning of a photo-sensitive layer onto a single semiconductor substrate. A Silicon substrate **102** is divided into regions **104**, **106** for forming an NMOS transistor **104** and a PMOS transistor **106**, respectively. A buffer layer (e.g., SiO_2) **108** and a hard mask (e.g. Si_3N_4) **110** are formed on the Silicon substrate **102**, with a photo-sensitive layer (e.g., Photo-resist) **112** being placed over portions of the regions **104**, **106** to preserve underlying layers during a material removing procedure (e.g., wet etching, dry etching).

FIG. **2** depicts the semiconductor device **100** after the material removing procedure and stripping of the photo-sensitive layer **112**. The material removing procedure eliminated certain portions of the Silicon substrate **102**, the buffer layer **108**, and the hard mask **110** that were not protected by the photo-sensitive layer **112** that has now been stripped from the semiconductor device **100**. The material removing procedure creates certain recessed regions **114** within the Silicon substrate **102**.

FIG. **3** depicts the semiconductor device **100** after incorporation of a dielectric layer. Following the material removing procedure, the recessed regions of the Silicon substrate **102** are filled with a dielectric material **116**, such as SiO_2. The hard mask **110** and buffer layer **108** are removed (e.g., via chemical-mechanical polishing/planarization (CMP) process), leaving the Silicon substrate **102** having associated recessed regions containing dielectric material **116**.

FIG. **4** depicts the semiconductor device **100** after incorporation of a gate dielectric material. Following filling the recessed regions **114** of the Silicon substrate **102** with dielectric material **116**, a gate dielectric material **118** is formed on top of the silicon substrate **102** and the dielectric material **116**. The gate dielectric material **118** is formed from SiO_2 or a high-k material, such as HfO_2.

FIG. **5** depicts formation of a gate on the NMOS portion **104** of the semiconductor device **100**. A portion of the gate dielectric **118** is removed from the NMOS portion **104** of the semiconductor device **100**, leaving a smaller gate dielectric portion **118** at the left, raised portion of the silicon substrate **102**. A gate electrode (e.g., Al, TiAl, W, TiN, TaN) **120** is deposited on the remaining NMOS side gate dielectric **118** to form a gate stack **122**. The gate stack **122** is surrounded by a spacer material **124** (e.g., SiO_2, Si_3N_4). The areas of the NMOS raised Silicon substrate portions formed by an implantation process to the immediate left and right of the gate stack **122** are designated as source/drain regions **126** of the NMOS transistor **104**.

FIG. **6** depicts formation of Nickel Silicide on the source/drain regions of the NMOS transistor **104**. In one embodiment, the Nickel Silicide contacts **128** on the source/drain regions **126** are formed in stages. In that example, a metal layer of Nickel is formed on the source/drain regions **126** of the Silicon substrate **102** to form a first set of source/drain contacts **128**. The first set of source/drain contacts **128** is annealed with the Silicon material of the source/drain regions **126** at a first temperature (e.g., 400-600° C.) to form Nickel Silicide. Unreacted Nickel is then removed, leaving the Nickel Silicide source/drain contacts **128**.

FIGS. **7-12** depict formation of components of a PMOS transistor **106** on the PMOS region **106** of the single semiconductor substrate **102** at a differing level of the semiconductor device **100** from the NMOS transistor **104**. In other embodiments of the disclosure, the NMOS and PMOS transistors **104**, **106** are formed on the same or nearby layers of the semiconductor device **100**.

FIG. **7** depicts the formation of an inter-layer dielectric above the NMOS transistor layers. A plurality of contact extensions (e.g., Al, Cu, W, TiN, TaN) **130** are fabricated on the source/drain contacts **128** and the gate electrode **120** to enable connection to those contacts **128** and electrode **120** from higher layers of the semiconductor device **100**. An inter-layer dielectric (ILD1) **132** is formed on top of the other components from a material such as SiO_2 or PSG.

FIG. **8** depicts formation of an opening for fabrication of the PMOS transistor components. In FIG. **8**, a second inter-layer dielectric (ILD**2**) **134** is formed from a material such as SiO_2 or PSG. Further, an opening **136** is formed (e.g., via wet or dry etching) in the PMOS region **106** of the semiconductor device **100**, such as to a depth of the Silicon substrate **102**.

FIG. **9** depicts incorporation of an additional semiconductor material. In FIG. **9**, the opening formed in ILD**1** **132** and ILD**2** **134** in FIG. **8** is filled with a semiconductor material **138**, such as a Germanium containing material (e.g., Ge, SiGe). The top of the semiconductor material **138**, in one embodiment, is further treated with a chemical-mechanical polishing/planarization (CMP) process.

FIG. **10** depicts formation of a gate stack of the PMOS transistor **106**. A gate dielectric (e.g. SiO_2 or other High-k material) **140** is formed on the Germanium containing material **138**, and a gate electrode (e.g. W, TiN, TaN) **142** is further formed thereon to generate a gate stack **144**. The gate stack **144** is surrounded by a spacer material (e.g., SiO_2, Si_3N_4) **146**, and the regions of the Germanium containing material by an implantation process to the left and right of the spacer surrounded gate stack **144** are designated as source/drain regions **148** of the PMOS transistor.

FIG. **11** depicts formation of Nickel Germanide on the source/drain regions of the PMOS transistor **106**. In one embodiment, the Nickel Germanide contacts **150** on the source/drain regions **148** are formed in stages. In that example, a metal layer of Nickel is formed on the source/drain regions **148** of the Germanium containing material **138** to form a second set of source/drain contacts **150** (the NMOS source drain contacts **128** being the first set). The second set of source/drain contacts **150** is annealed with the Germanium material of the source/drain regions **148** at a second temperature (e.g., 250-300° C.) to form Nickel Germanide. Unreacted Nickel is then removed, leaving the Nickel Germanide source/drain contacts **150**. Then, the substrate **102** is annealed at a third temperature (e.g., 600-750° C.) to form a low-resistance Nickel silicide and a low-resistance Nickel Germanide.

The second temperature (e.g., 250-300° C.) used in the annealing process to form the Nickel Germanide is less than the first temperature (e.g., 400-600° C.) used to form the Nickel Silicide at **128**. By performing the operation in the described order, the Nickel Germanide contacts **150** are never subjected to the first temperature used in the annealing process for the Nickel Silicide contacts at **128**, where the Nickel Germanide contacts **150** could be damaged by exposure to such contacts.

FIG. **12** depicts incorporation of a capping interlayer dielectric. Contacts (e.g., Al, Cu, W, TiN, TaN) **152** for each of the source/drain regions and the gates of the respective NMOS and PMOS transistors are extended through the second inter-layer dielectric **134**, where necessary and beyond. An additional third inter-layer dielectric (ILD**3**) **154**, formed from a dielectric such as SiO_2 or PSG, is formed around the contacts **152** to generate a uniform, single substrate semiconductor device.

FIG. **13** is a flow diagram depicting a method of generating a semiconductor device on a single semiconductor substrate. At **1302**, a single semiconductor substrate is generated that includes a Silicon material portion and a Germanium material portion. At **1304**, a first set of source/drain contacts is formed from a first metal on the Silicon material portion. At **1306**, the first set of source/drain contacts is annealed with the Silicon material portion at a first temperature. At **1308**, a second set of source/drain contacts is formed from a second metal on the Germanium material portion after heating the semiconductor substrate to the first temperature, and at **1310**, the second set of source/drain contacts is annealed with the Germanium material portion at a second temperature, where the second temperature is less than the first temperature.

This written description uses examples to disclose the disclosure, include the best mode, and also to enable a person skilled in the art to make and use the disclosure. The patentable scope of the disclosure may include other examples that occur to those skilled in the art. For example, certain systems and methods include additional steps to form interconnections and for passivation.

As another example, in a method of generating a semiconductor device on a single semiconductor substrate, a single semiconductor substrate is generated that includes a Silicon material portion and a Germanium material portion. A first set of source/drain contacts is formed from a first metal on the Silicon material portion. The first set of source/drain contacts is annealed with the Silicon material portion at a first temperature. A second set of source/drain contacts is formed from a second metal on the Germanium material portion after heating the semiconductor substrate to the first temperature, and the second set of source/drain contacts is annealed with the Germanium material portion at a second temperature, where the second temperature is less than the first temperature.

As a further example, a semiconductor device formed on a single semiconductor substrate includes a single semiconductor substrate that includes a Silicon material portion and a Germanium material portion. A first set of source/drain contacts is formed from a first metal on the Silicon material portion, where the first set of source/drain contacts is annealed with the Silicon material portion at a first temperature. A second set of source/drain contacts is formed from a second metal on the Germanium material portion, where the second set of source/drain contacts is formed after the semiconductor substrate was heated to the first temperature, wherein the second set of source/drain contacts is annealed with the Germanium material portion at a second temperature that is less than the first temperature.

One skilled in the relevant art will recognize that the various embodiments may be practiced without one or more of the specific details, or with other replacement and/or additional methods, materials, or components. Well-known structures, materials, or operations may not be shown or described in detail to avoid obscuring aspects of various embodiments of the disclosure. Various embodiments shown in the figures are illustrative example representations and are not necessarily drawn to scale. Particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments. Various additional layers and/or structures may be included and/or described features may be omitted in other embodiments. Various operations may be described as multiple discrete operations in turn, in a manner that is most helpful in understanding the disclosure. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Operations described herein may be performed in a different order, in series or in parallel, than the described embodiment. Various additional operations may be performed and/or described. Operations may be omitted in additional embodiments.

This written description and the following claims may include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position may refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and may still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) may not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the figures.

What is claimed is:

1. A method of generating a semiconductor device on a single semiconductor substrate, comprising:

providing a substrate having a silicon material portion;

forming a first set of source/drain contacts from a first metal on a substrate surface that includes the Silicon material portion;

annealing the first metal with the Silicon material portion at a first temperature to form the first set of source/drain contacts;

subsequent to forming the first set of source/drain contacts, disposing a germanium material portion on the substrate surface on which the first set of source/drain contacts are formed proximate the silicon material portion;

forming a second set of source/drain contacts from a second metal on the Germanium material portion; and

annealing the second metal with the Germanium material portion at a second temperature to form the second set of source/drain contacts, wherein the second temperature is less than the first temperature.

2. The method of claim **1**, wherein the first metal and the second metal are of the same type.

3. The method of claim **2**, wherein the first metal and the second metal both include Nickel.

4. The method of claim **1**, wherein the first temperature is in a range of 400-600° C.

5. The method of claim **1**, wherein the second temperature is in a range of 250-300° C.

6. The method of claim **1**, wherein the second set of source/drain contacts is formed at a higher level of the single semiconductor substrate than the first set of source/drain contacts is formed.

7. The method of claim **1**, wherein the second set of source/drain contacts is formed at a same level of the single semiconductor substrate than the first set of source/drain contacts is formed.

8. The method of claim **1**, wherein the Silicon material portion is part of a Silicon substrate, and wherein the Germanium material portion of formed on top of the Silicon substrate.

9. The method of claim **1**, wherein the first set of source/drain contacts on the Silicon material portion are components of an NMOS transistor, wherein the second set of source/drain contacts on the Germanium portion are components of an PMOS transistor.

10. The method of claim **1**, further comprising removing an unreacted portion of the first metal or the second metal.

11. The method of claim **1**, further comprising forming a dielectric layer and a gate electrode on each of the Silicon material portion and the Germanium material portion to form two transistors on the single semiconductor substrate.

12. A semiconductor device formed on a single semiconductor substrate, comprising;

a semiconductor substrate that includes a silicon material portion defining a first level surface,

a first set of source/drain contacts including a first metal formed on the first level surface in the silicon material portion;

a germanium material portion disposed proximate the silicon material portion on the first level surface, the germanium material portion defines a second level surface higher than the first level surface;

an inter-layer dielectric layer disposed adjacent to the germanium material portion and covering the first set of source/drain contacts in the silicon material portion, wherein a height of the inter-layer dielectric layer is substantially leveled with that of the second level surface; and

a second set of source/drain contacts including a second metal formed on the second level surface in the germanium material portion.

13. The device of claim **12**, wherein the first metal and the second metal are of the same type.

14. The device of claim **13**, wherein the first metal and the second metal both include Nickel.

15. The device of claim **12**, wherein the first set of source/drain contacts are formed by annealing the first metal with the silicon material portion at a first temperature in a range of about 400 to about 600° C.

16. The device of claim **12**, wherein the second set of source/drain contacts are formed by annealing the second metal with the germanium material portion at a second temperature in a range of about 250 to about 300° C.

17. The device of claim **12**, wherein the Silicon material portion is part of a Silicon substrate, and wherein the Germanium material portion of formed on top of the Silicon substrate.

18. The device of claim **12**, wherein the first set of source/drain contacts on the Silicon material portion are components of an NMOS transistor, wherein the second set of source/drain contacts on the Germanium portion are components of an PMOS transistor.

19. A method for generating a semiconductor device, comprising:

providing a substrate of a first semiconductor material having a first device region and a second device region defined thereon, the substrate defining a first level surface;

forming a first set of contacts on the first level surface in the first device region;

disposing a first dielectric layer on the first level surface in the first device region to cover the first set of contacts, the first dielectric layer defining a height;

disposing a second semiconductor material layer on the first level surface in the second device region adjacent to the first dielectric layer, the second semiconductor material layer defining a second level surface; wherein the height of the first dielectric layer is no higher than the second level surface; and

disposing a second set of contacts on the second level surface in the second device region.

20. The method of claim **19**, wherein

the forming of the first set of contacts includes disposing a first metal on the first level surface in the first device region, and annealing the first metal at a first temperature;

the forming of the second set of contacts includes disposing a second metal on the second level surface in the second device region, and annealing the second metal at a second temperature after the formation of the first set of contacts;

the second temperature is less than the first temperature.

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